

# 74ALVCH16373

2.5 V/3.3 V 16-bit D-type transparent latch; 3-state

Rev. 7 — 30 January 2019

Product data sheet

## 1. General description

The 74ALVCH16373 is 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.

Incorporates bus hold data inputs which eliminate the need for external pull-up or pull-down resistors to hold unused inputs.

One latch enable (LE) input and one output enable ( $\overline{OE}$ ) are provided per 8-bit section.

The 74ALVCH16373 consists of 2 sections of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the nDn inputs enter the latches. In this condition the latches are transparent, therefore a latch output will change each time its corresponding D-input changes.

When LE is LOW, the latches store the information that was present at the nDn inputs at a set-up time preceding the LOW-to-HIGH transition of LE. When  $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

## 2. Features and benefits

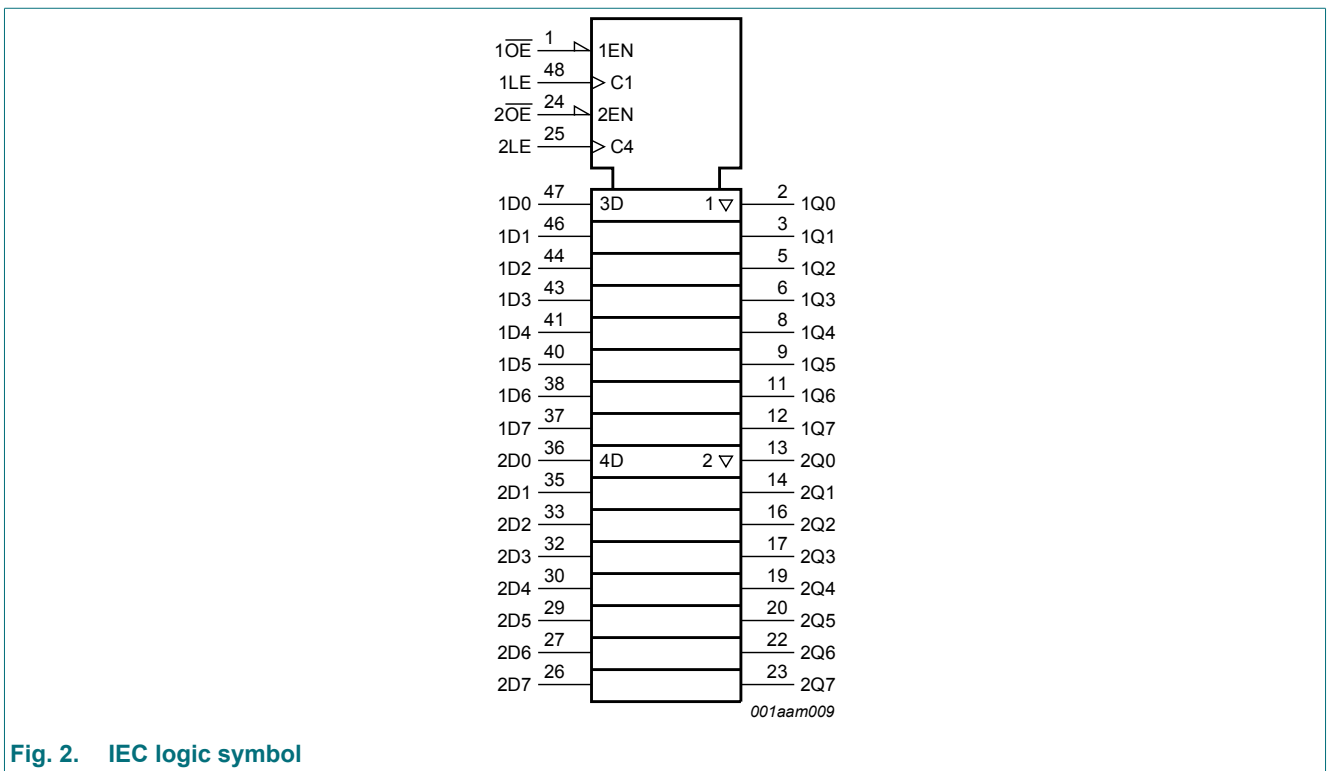
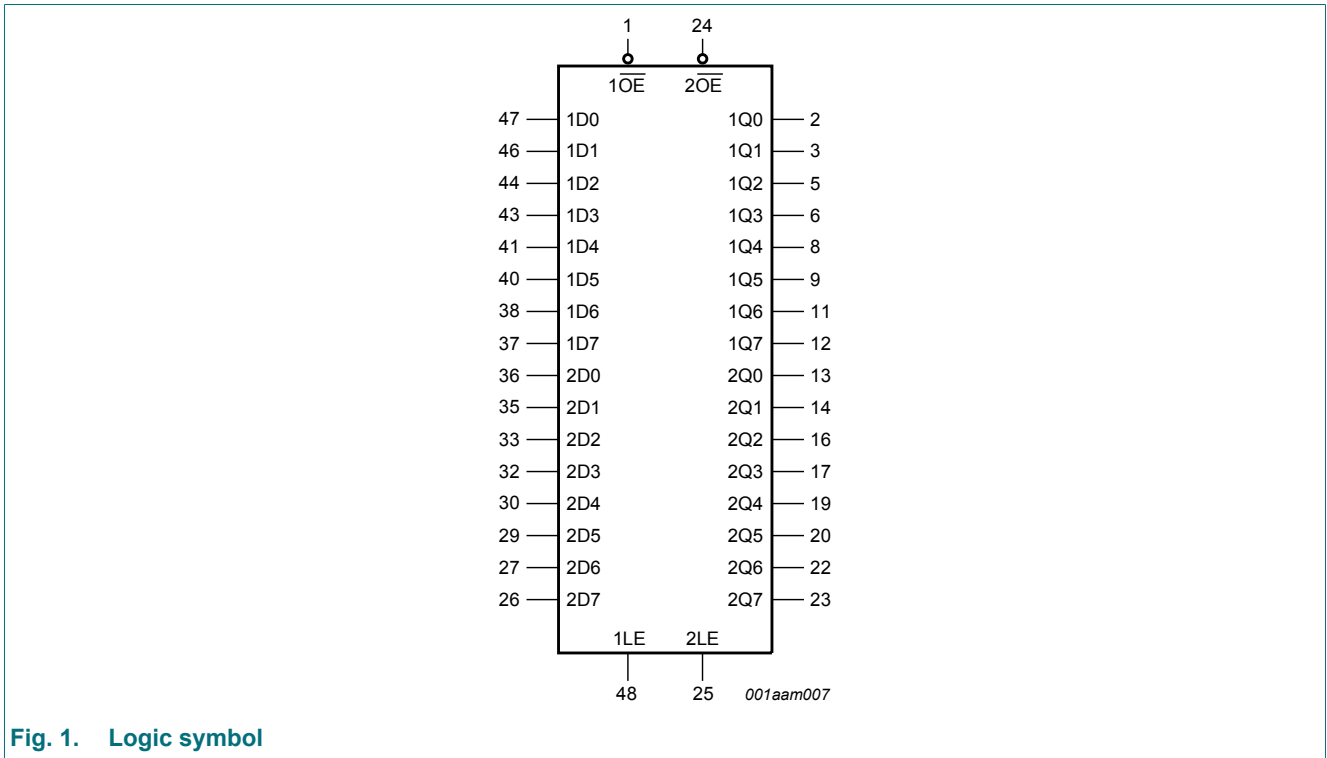
- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Current drive  $\pm 24$  mA at  $V_{CC} = 3.0$  V

## 3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVCH16373DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

### 4. Functional diagram



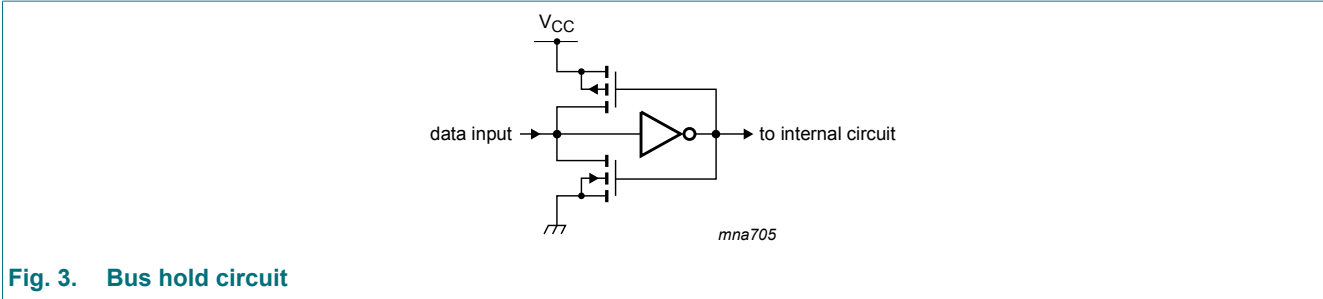


Fig. 3. Bus hold circuit

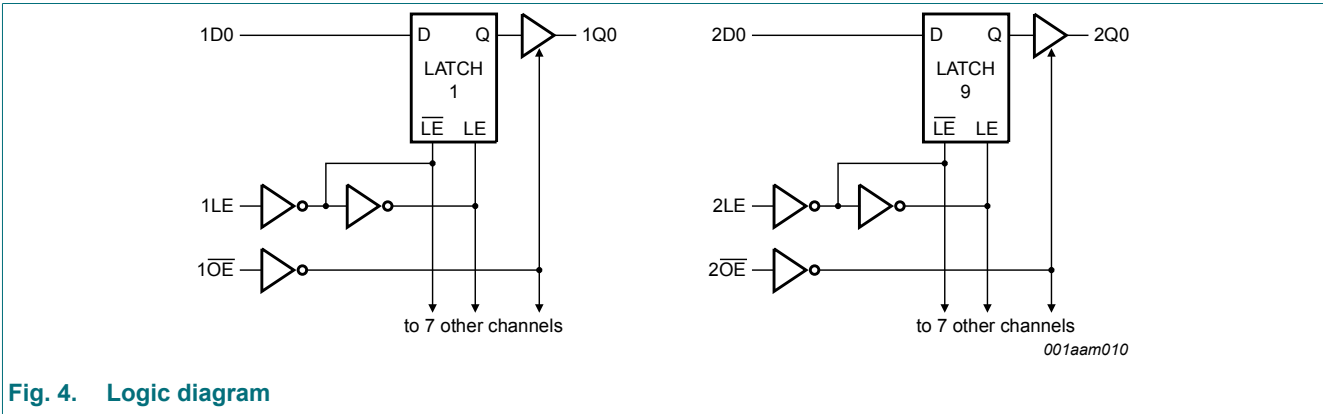


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning

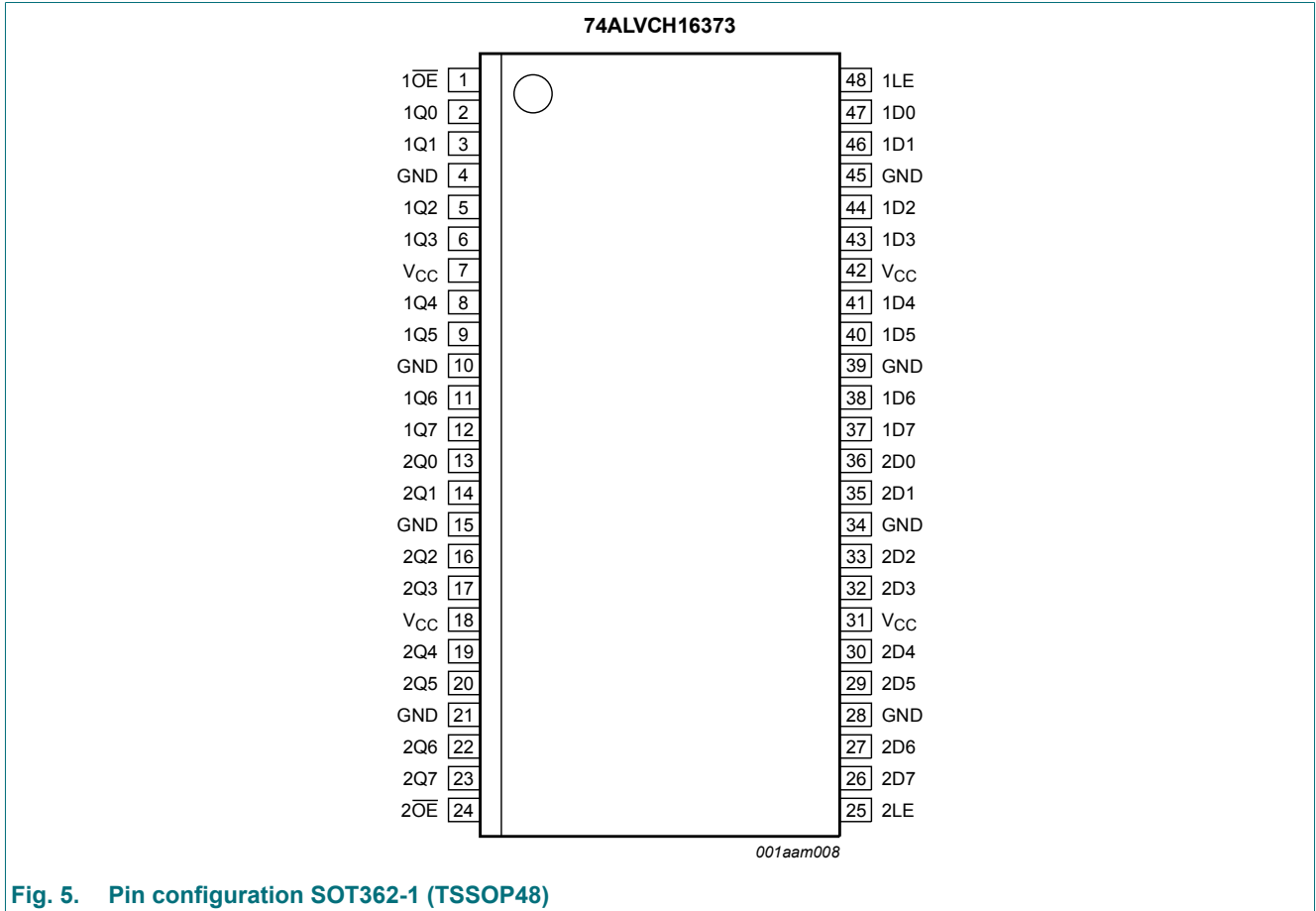


Fig. 5. Pin configuration SOT362-1 (TSSOP48)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 24	output enable input (active LOW)
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	positive supply voltage
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data inputs
1LE, 2LE	48, 25	latch enable input (active HIGH)

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition;  
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition;  
Z = high-impedance OFF-state.

Inputs			Internal latches	Outputs nQn	Operating mode
nOE	nLE	nDn			
L	H	L	L	L	enable and read register (transparent mode)
L	H	H	H	H	
L	L	l	L	L	latch and read register (hold mode)
L	L	h	H	H	
H	L	l	L	Z	latch register and disable outputs
H	L	h	H	Z	

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage	control inputs [1]	-0.5	+4.6	V
		data inputs [1]	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
V <sub>O</sub>	output voltage	[1]	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C [2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage	maximum speed performance				
		C <sub>L</sub> = 30 pF	2.3	-	2.7	V
		C <sub>L</sub> = 50 pF	3.0	-	3.6	V
		low voltage applications	1.2	-	3.6	V
V <sub>I</sub>	input voltage	data inputs	0	-	V <sub>CC</sub>	V
		control inputs	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.3 V to 3.0 V	0	-	20	ns/V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 1.8 V	0.7V <sub>CC</sub>	0.9	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0	V
		V <sub>CC</sub> = 1.8 V	-	0.9	0.2V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.8 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> - 0.4	V <sub>CC</sub> - 0.1	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.17	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.8 V to 3.6 V	-	0	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 1.8 V	-	0.09	0.30	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.20	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.40	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 2.3 V	-	0.23	0.60	V
I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V		

## 2.5 V/3.3 V 16-bit D-type transparent latch; 3-state

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$I_I$	input leakage current	$V_{CC} = 1.8\text{ V to }3.6\text{ V}$				
		control input; $V_I = 5.5\text{ V or GND}$	-	0.1	5	$\mu\text{A}$
		data input; $V_I = V_{CC}\text{ or GND}$	-	0.1	5	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}\text{ or }V_{IL}; V_O = V_{CC}\text{ or GND}$				
		$V_{CC} = 1.8\text{ V to }2.7\text{ V}$	-	0.1	5	$\mu\text{A}$
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	0.1	10	$\mu\text{A}$
$I_{LIZ}$	OFF-state input leakage current	$V_I = V_{CC}\text{ or GND}$				
		$V_{CC} = 1.8\text{ V to }2.7\text{ V}$	-	0.1	10	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$	-	0.1	15	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A};$				
		$V_{CC} = 1.8\text{ V to }2.7\text{ V}$	-	0.2	40	$\mu\text{A}$
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	0.2	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 0.6\text{ V}; I_O = 0\text{ A}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$				
		per control input	-	5	500	$\mu\text{A}$
		per data I/O input	-	150	750	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_{CC} = 2.3\text{ V}; V_I = 0.7\text{ V}$ [2]	45	-	-	$\mu\text{A}$
		$V_{CC} = 3.0\text{ V}; V_I = 0.8\text{ V}$ [2]	75	150	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 2.3\text{ V}; V_I = 1.7\text{ V}$ [2]	-45	-	-	$\mu\text{A}$
		$V_{CC} = 3.0\text{ V}; V_I = 2.0\text{ V}$ [2]	-75	-175	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 2.7\text{ V}$ [2]	300	-	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ [2]	450	-	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 2.7\text{ V}$ [2]	-300	-	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ [2]	-450	-	-	$\mu\text{A}$
$C_I$	input capacitance		-	5.0	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ }^\circ\text{C}$ .

[2] Valid for data inputs of bus hold parts only.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

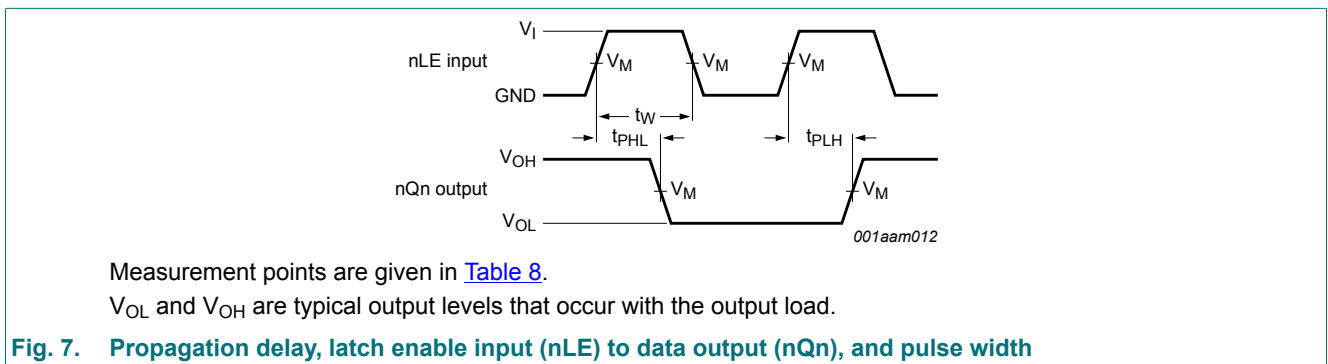
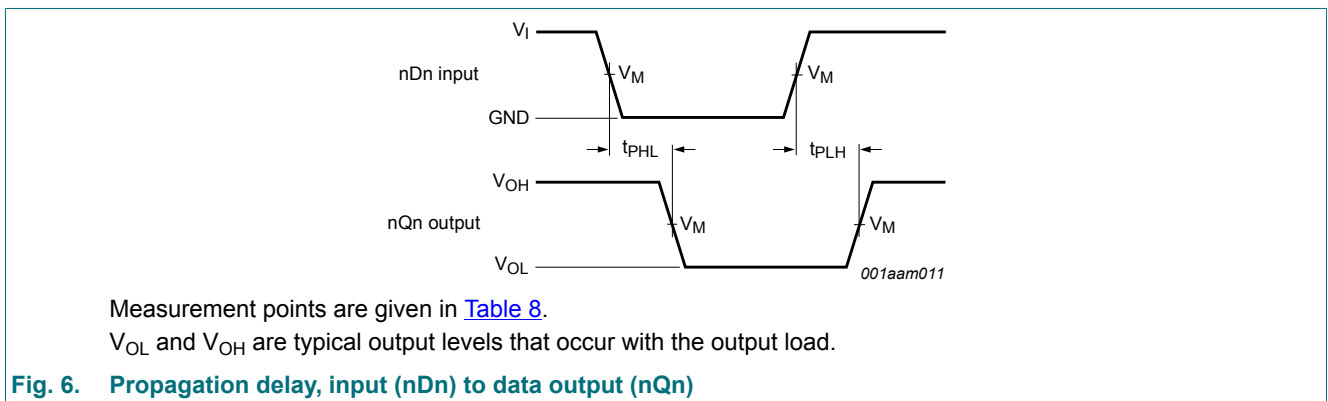
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit	
$T_{amb} = -40\text{ °C to }+85\text{ °C}$							
$t_{pd}$	propagation delay	nDn to nQn; see Fig. 6 [2]					
		$V_{CC} = 1.2\text{ V}$	-	8.8	-	ns	
		$V_{CC} = 1.8\text{ V}$	1.5	3.2	5.7	ns	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ [3]	1.0	2.1	3.9	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	2.3	3.7	ns	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [4]	1.0	2.1	3.3	ns	
		nLE to nQn; see Fig. 7 [2]					
		$V_{CC} = 1.2\text{ V}$	-	7.4	-	ns	
		$V_{CC} = 1.8\text{ V}$	1.5	3.4	5.9	ns	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ [3]	1.0	2.2	3.9	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	2.2	3.5	ns	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [4]	1.0	2.2	3.2	ns	
$t_{en}$	enable time	nOE to nQn; see Fig. 8 [5]					
		$V_{CC} = 1.2\text{ V}$	-	8.9	-	ns	
		$V_{CC} = 1.8\text{ V}$	1.5	4.0	7.3	ns	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ [3]	1.0	2.6	5.2	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	2.9	4.9	ns	
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [4]	1.0	2.3	4.2	ns			
$t_{dis}$	disable time	nOE to nQn; see Fig. 8 [6]					
		$V_{CC} = 1.2\text{ V}$	-	8.9	-	ns	
		$V_{CC} = 1.8\text{ V}$	1.5	3.2	5.6	ns	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ [3]	1.0	2.2	4.1	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	3.1	4.7	ns	
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [4]	1.0	2.8	4.1	ns			
$t_{w}$	pulse width	nLE HIGH; see Fig. 7					
		$V_{CC} = 1.8\text{ V}$	3.5	1.0	-	ns	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ [3]	3.0	1.0	-	ns	
		$V_{CC} = 2.7\text{ V}$	3.0	1.0	-	ns	
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [4]	2.5	1.0	-	ns			
$t_{su}$	set-up time	nDn to nLE; see Fig. 9					
		$V_{CC} = 1.8\text{ V}$	1.0	-0.1	-	ns	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ [3]	1.0	-0.1	-	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	-0.1	-	ns	
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [4]	1.0	0.0	-	ns			

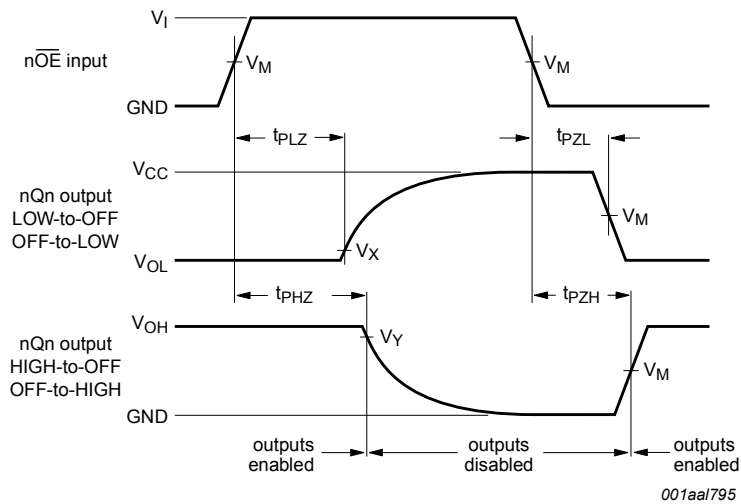


Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t <sub>h</sub>	hold time	nDn to nLE; see Fig. 9				
		V <sub>CC</sub> = 1.8 V	1.2	0.1	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	1.5	0.2	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	0.4	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	1.2	0.2	-	ns
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> [7]				
		outputs enabled	-	16	-	pF
		outputs disabled	-	10	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] Typical values are measured at V<sub>CC</sub> = 2.5 V.
- [4] Typical values are measured at V<sub>CC</sub> = 3.3 V.
- [5] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.
- [6] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [7] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in Volts;  
 N = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

### 10.1. Waveforms and test circuit

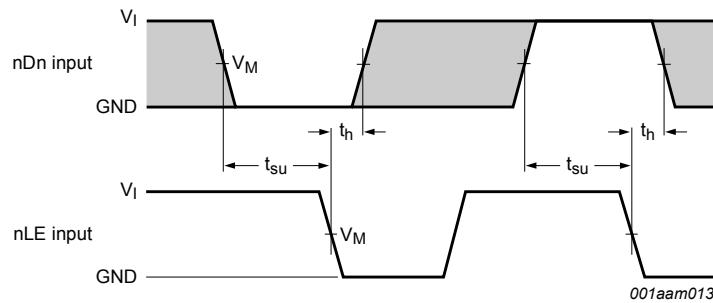




Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

**Fig. 8. 3-state enable and disable times**



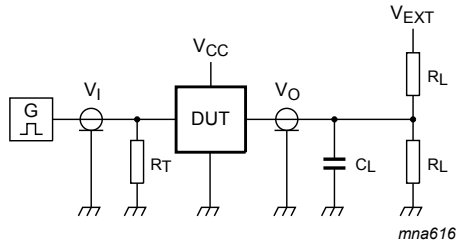
Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 9. Data setup and hold times for input (nDn) to input (nLE)**

**Table 8. Measurement points**

Supply voltage	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
2.3 V to 2.7 V and < 2.3 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 10. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
2.3 V to 2.7 V and < 2.3 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

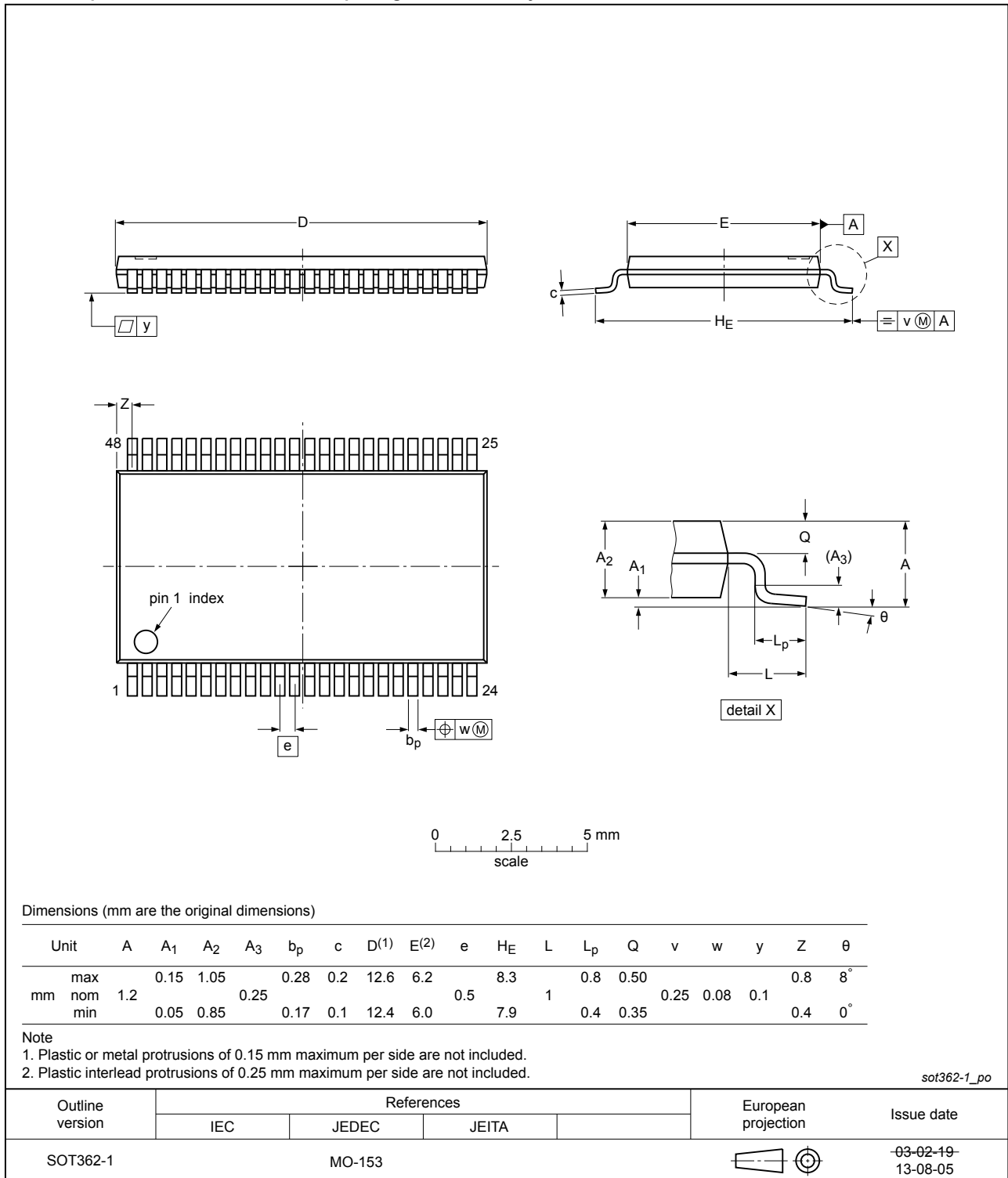


Fig. 11. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16373 v.7	20190130	Product data sheet	-	74ALVCH16373 v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74ALVCH16373DL (SOT370-1) removed.</li> <li>Package outline drawing <a href="#">SOT362-1</a> (TSSOP48) updated.</li> </ul>			
74ALVCH16373 v.6	20120710	Product data sheet	-	74ALVCH16373 v.5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 8</a> corrected (errata).</li> </ul>			
74ALVCH16373 v.5	20111117	Product data sheet	-	74ALVCH16373 v.4
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74ALVCH16373 v.4	20100531	Product data sheet	-	74ALVCH16373 v.3
74ALVCH16373 v.3	19990920	Product specification	-	74ALVCH16373 v.2
74ALVCH16373 v.2	19980629	Product specification	-	74ALVCH16373 v.1
74ALVCH16373 v.1	19970321	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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