



BUK6D43-60E

60 V, N-channel Trench MOSFET

13 December 2017

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Extended temperature range $T_j = 175^\circ\text{C}$
- Side wettable flanks for optical solder inspection
- Small and leadless ultra thin SMD plastic package: $2 \times 2 \times 0.65 \text{ mm}$
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

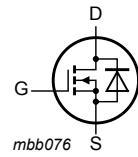
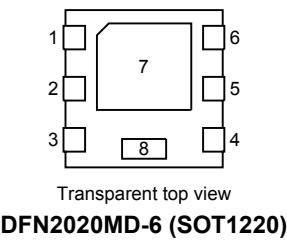
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10 \text{ V}; T_{sp} = 25^\circ\text{C}$	-	-	13	A
P_{tot}	total power dissipation	$T_{sp} = 25^\circ\text{C}$	-	-	15	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25^\circ\text{C}$		-	32	43
						$\text{m}\Omega$

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain		
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		



6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6D43-60E	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6D43-60E	4A

8. Limiting values

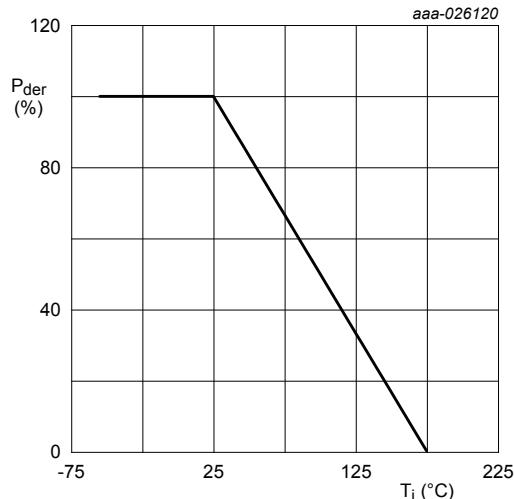
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25^\circ\text{C}$		-	13	A
		$V_{GS} = 10\text{ V}; T_{sp} = 100^\circ\text{C}$		-	8.2	A
		$V_{GS} = 10\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-	5	A
I_{DM}	peak drain current	$T_{sp} = 25^\circ\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	52	A
P_{tot}	total power dissipation	$T_{sp} = 25^\circ\text{C}$		-	15	W
		$T_{amb} = 25^\circ\text{C}$	[1]	-	2.3	W
T_j	junction temperature			-55	175	$^\circ\text{C}$
T_{amb}	ambient temperature			-55	175	$^\circ\text{C}$
T_{stg}	storage temperature			-65	175	$^\circ\text{C}$
Source-drain diode						
I_S	source current	$T_{sp} = 25^\circ\text{C}$		-	13	A
		$T_{amb} = 25^\circ\text{C}$	[1]	-	2.3	A
I_{SM}	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}; T_{sp} = 25^\circ\text{C}$		-	52	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	500	V
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25^\circ\text{C}; I_D = 0.75\text{ A}$; DUT in avalanche (unclamped)		-	24	mJ

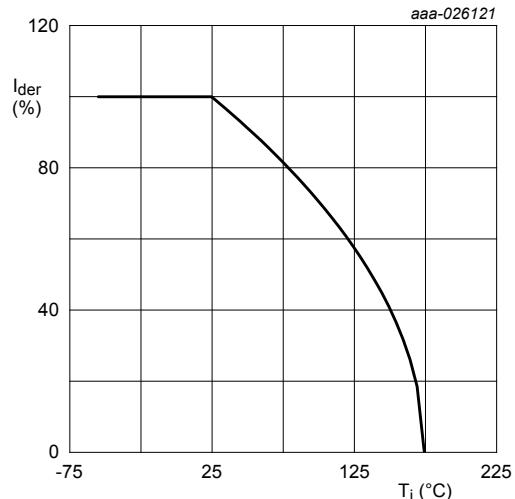
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

[2] Measured between all pins.



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \text{ \%}$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_D(25^\circ\text{C})} \times 100 \text{ \%}$$

Fig. 2. Normalized continuous drain current as a function of junction temperature

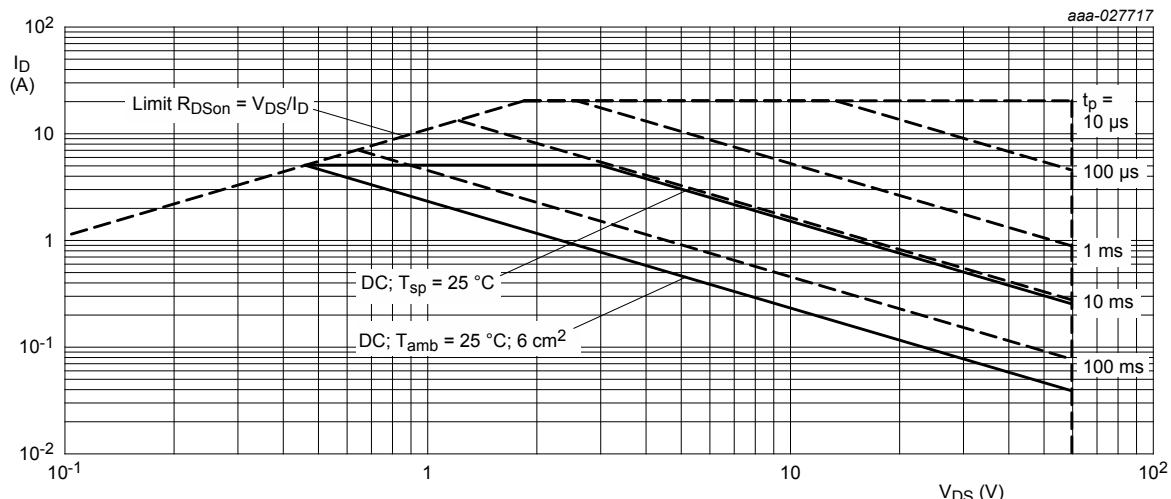


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	57	66	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	6	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

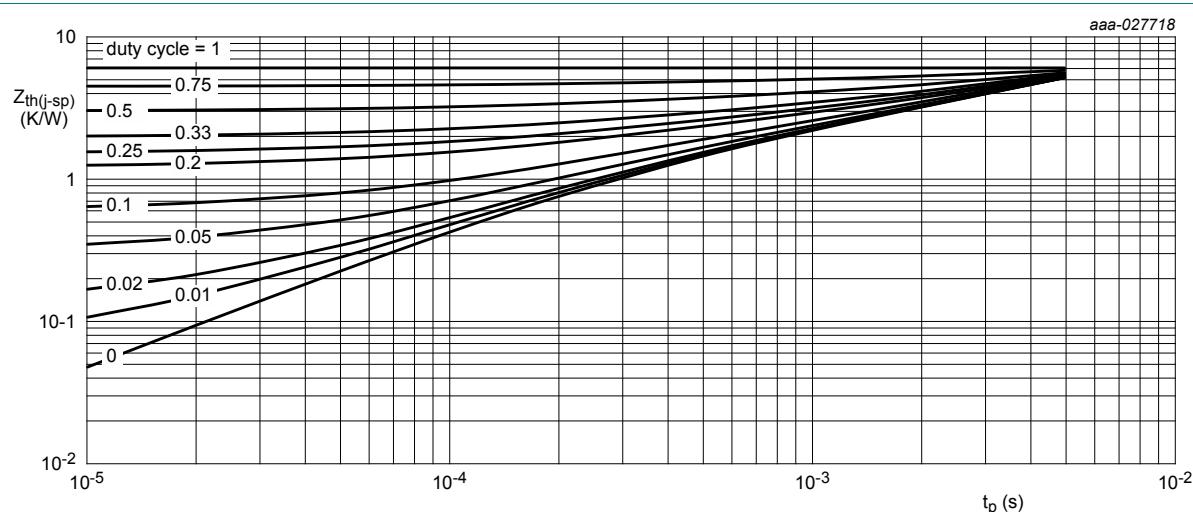


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values

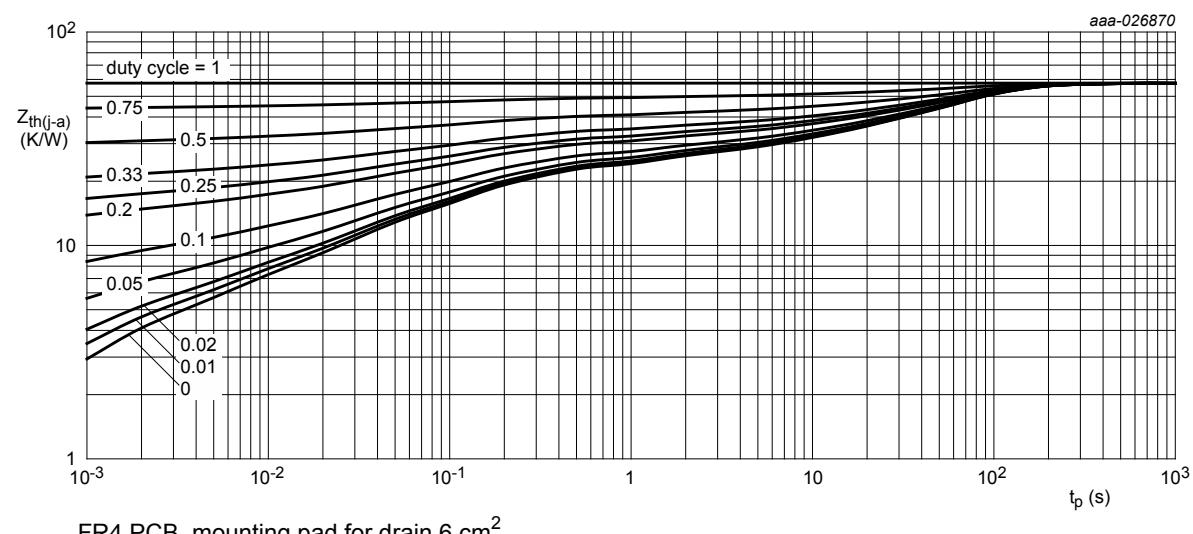
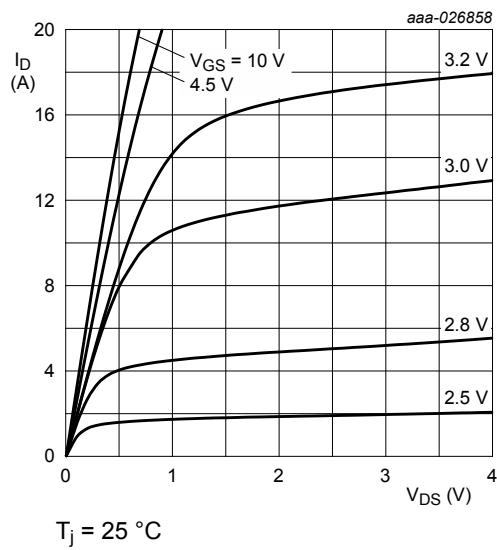


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

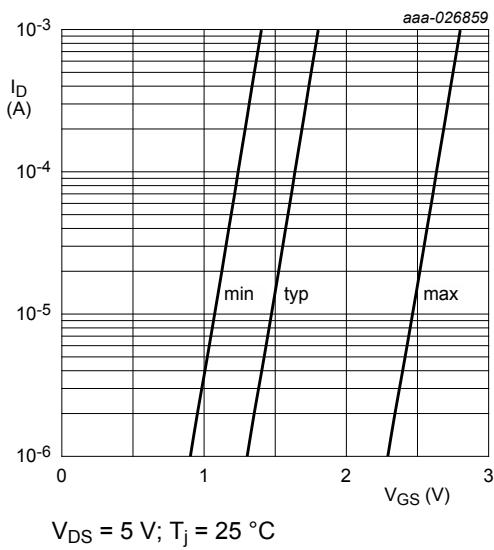
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		60	-	-	V
V_{GSTh}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS}=V_{GS}; T_j = 25^\circ C$		1.3	1.7	2.7	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	1	μA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175^\circ C$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 5 A; T_j = 25^\circ C$		-	32	43	$m\Omega$
		$V_{GS} = 10 V; I_D = 5 A; T_j = 175^\circ C$		-	69	93	$m\Omega$
		$V_{GS} = 4.5 V; I_D = 4.5 A; T_j = 25^\circ C$		-	38	53	$m\Omega$
g_{fs}	forward transconductance	$V_{DS} = 5 V; I_D = 5 A; T_j = 25^\circ C$		-	5	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$		-	3.5	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 6 A; V_{GS} = 10 V; T_j = 25^\circ C$		-	10	18	nC
Q_{GS}	gate-source charge			-	1.7	-	nC
Q_{GD}	gate-drain charge			-	2.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25^\circ C$		-	590	-	pF
C_{oss}	output capacitance			-	60	-	pF
C_{rss}	reverse transfer capacitance			-	34	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; I_D = 6 A; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	3	-	ns
t_r	rise time			-	5	-	ns
$t_{d(off)}$	turn-off delay time			-	11	-	ns
t_f	fall time			-	4	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 2.3 A; V_{GS} = 0 V; T_j = 25^\circ C$		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 2.3 A; dI_S/dt = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25^\circ C$		-	15.5	-	ns
Q_r	recovered charge			-	8.3	-	nC



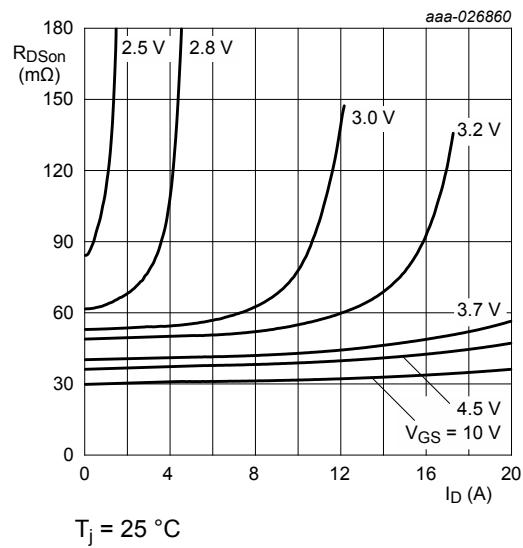
$T_j = 25^\circ\text{C}$

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



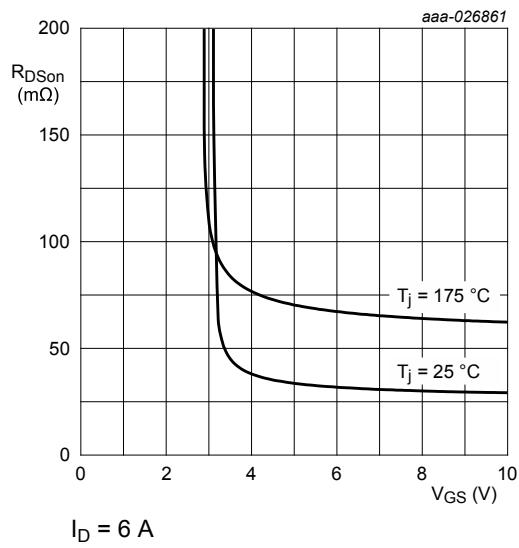
$V_{DS} = 5\text{ V}; T_j = 25^\circ\text{C}$

Fig. 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}$

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



$I_D = 6\text{ A}$

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

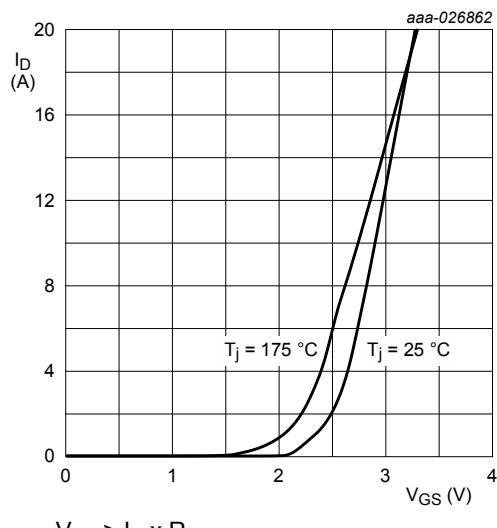


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

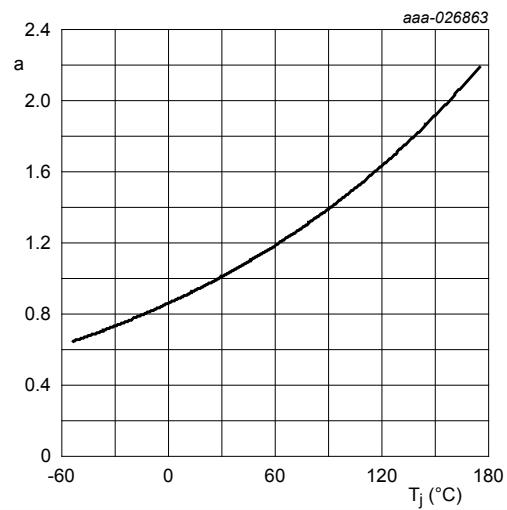


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

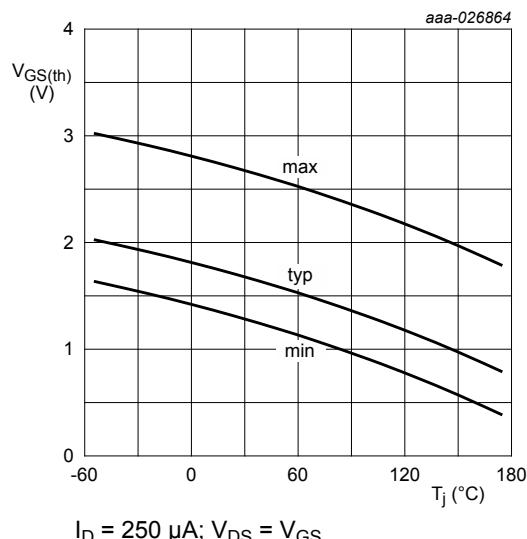


Fig. 12. Gate-source threshold voltage as a function of junction temperature

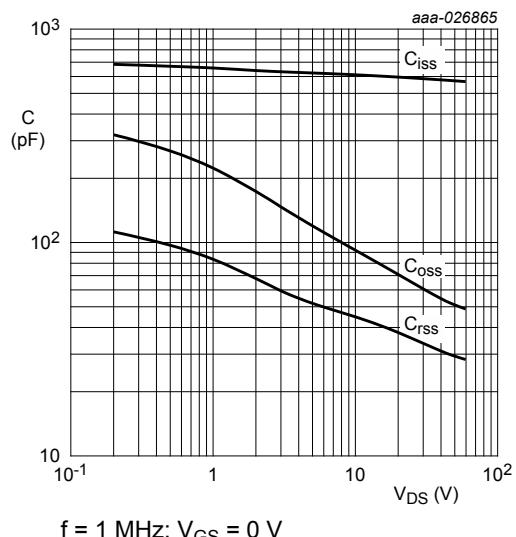
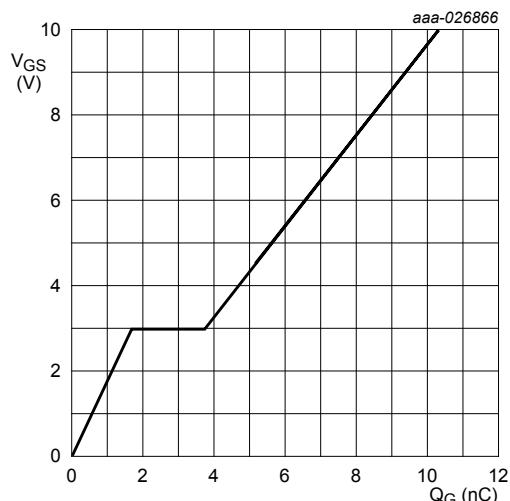


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 30$ V; $I_D = 6$ A; $T_{amb} = 25$ °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

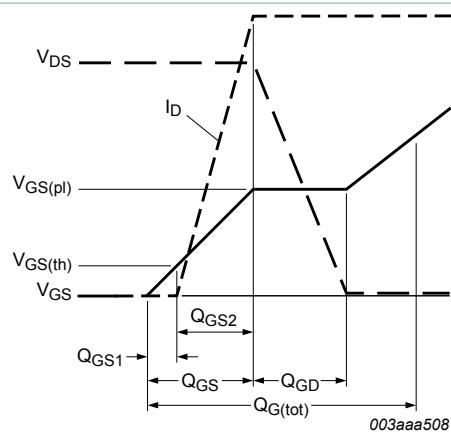
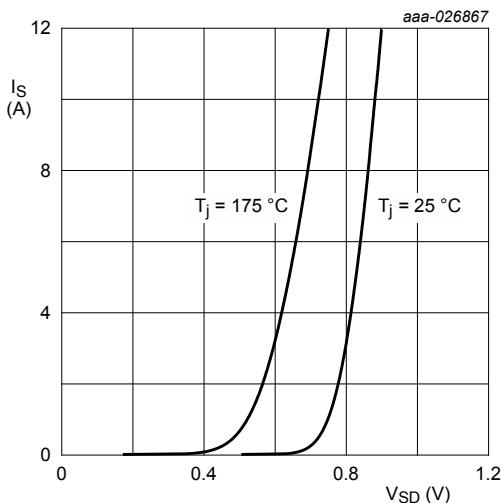


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

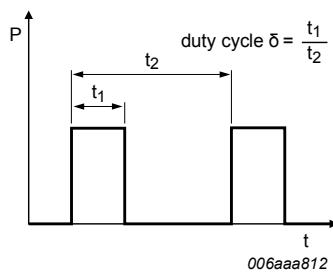


Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1220

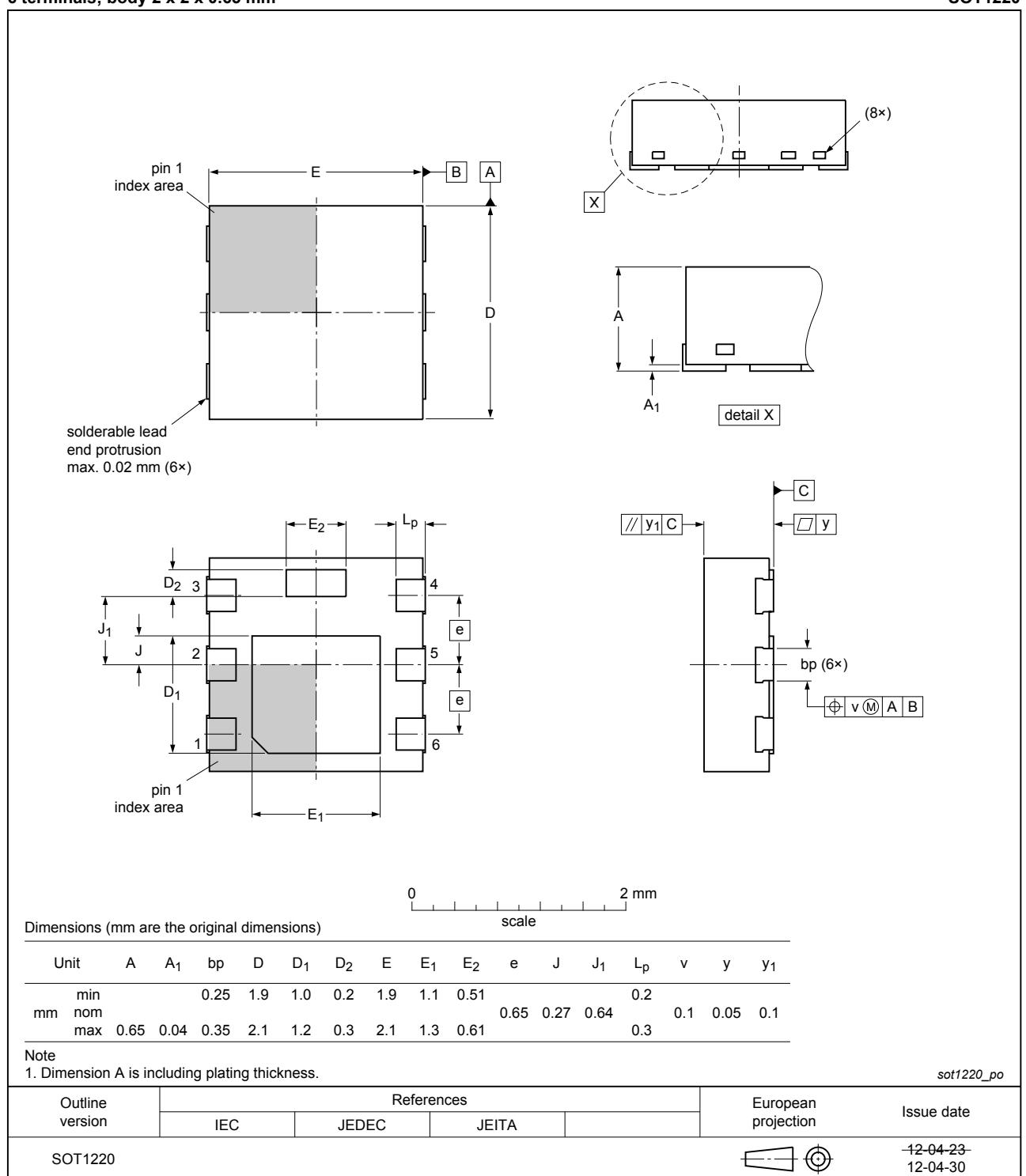
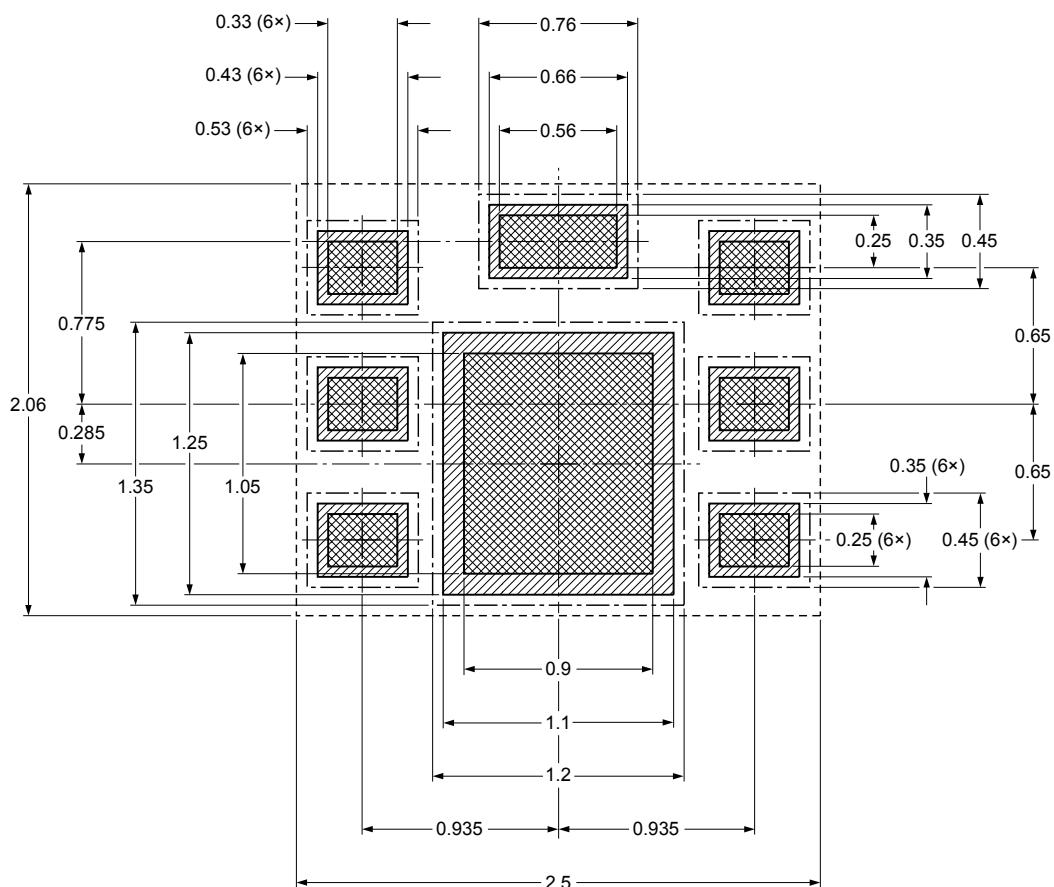


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

Footprint information for reflow soldering of DFN2020MD-6 package

SOT1220



solder land



solder land plus solder paste



solder paste deposit



solder resist

--- occupied area

Dimensions in mm

sot1220_fr

Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6D43-60E v.1	20171213	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 13 December 2017



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