

PI6C49S1510A

High Performance Differential Fanout Buffer

Features

- 10 differential outputs with 2 banks
- User configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- LVC MOS reference output up to 200MHz
- Up to 1.5GHz output frequency for differential outputs
- Ultra low additive phase jitter: < 0.02 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range); < 0.01 ps (typ) (differential 156.25MHz, 10kHz to 1MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. < 0.9ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFN-48 package

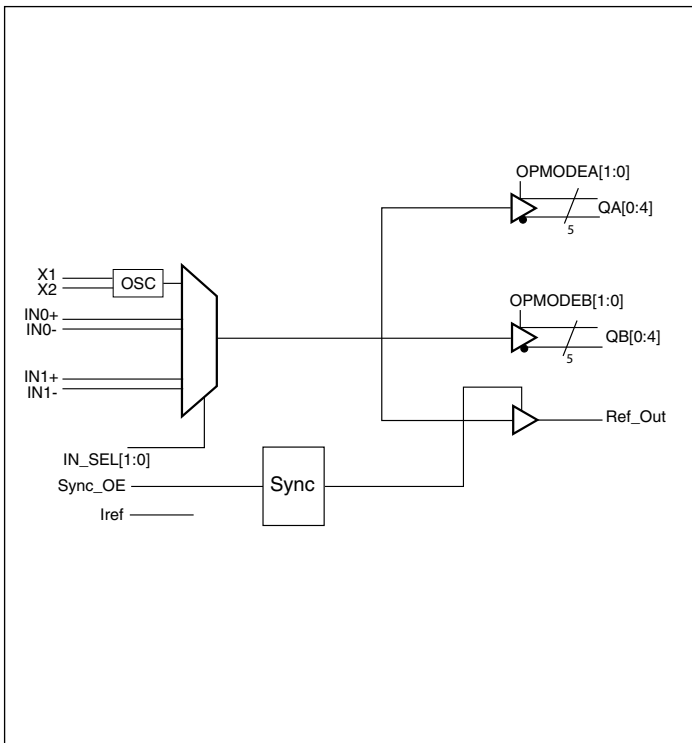
Description

The PI6C49S1510A is a high performance fanout buffer device which supports up to 1.5GHz frequency. It also integrates a unique feature with user configurable output signaling standards on per bank basis which provide great flexibilities to users. The device also uses Pericom's proprietary input detection technique to make sure illegal input conditions will be detected and reflected by output states. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

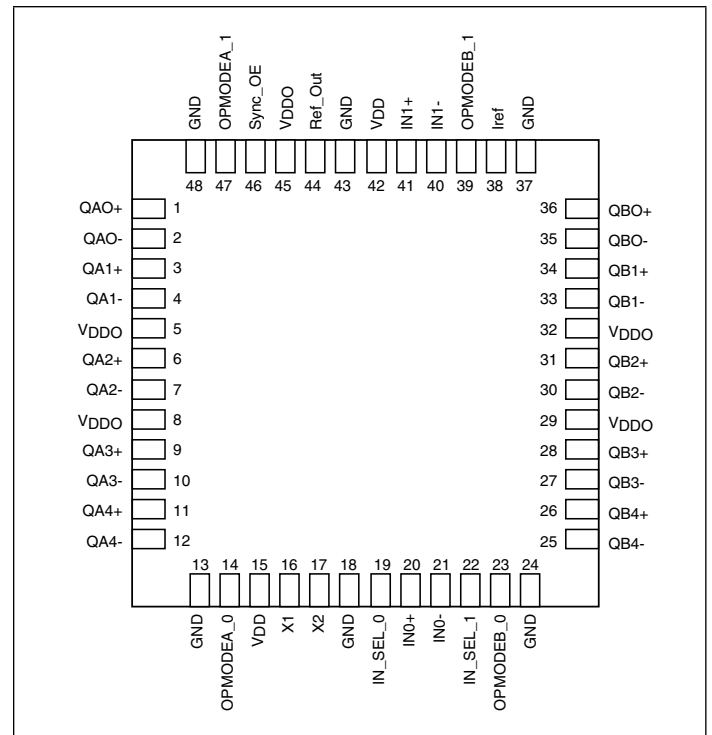
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (48-TQFN)



Pin Description

Pin #	Pin Name	Type		Description
1,2	QA0+ QA0-	Output		Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
3,4	QA1+ QA1-	Output		Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
5,8,29,32,45	VDDO	Power		Power supply pins for IO
6,7	QA2+ QA2-	Output		Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
9,10	QA3+ QA3-	Output		Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
11,12	QA4+ QA4-	Output		Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
13,18,24,37,43,48	GND	Power		Power supply ground
14,47	OPMODEA	Input	Pulldown	Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels
15,42	V _{DD}	Power		Power supply pins
16	X1	Input		XTAL input, can also be used as single ended input pin
17	X2	Output		XTAL output. If X1 is used as a single ended input pin, X2 is to be left open
19,22	IN_SEL	Input	Pulldown	Input clock select. See Table 1 for function. LVCMOS/LVTTL interface levels.
20	IN0+	Input	Pulldown	Reference input 0
21	IN0-	Input	Pull-up/ Pulldown	Inverted reference input 0, internal bias to V _{DD} /2
23,39	OPMODEB	Input	Pulldown	Output mode select for Bank B. See Table 2 for functions, LVCMOS/LVTTL interface levels
26,25	QB4+ QB4-	Output		Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
28,27	QB3+ QB3-	Output		Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
31,30	QB2+ QB2-	Output		Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
34,33	QB1+ QB1-	Output		Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.

Pinout Description Cont.

Pin #	Pin Name	Type		Description
36,35	QB0+	Output		Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB0-			
38	Iref	Output		A fixed precision resistor (475ohm) from this pin to ground provides a reference current for HCSL mode. If LVPECL or LVDS mode chosen, pin can be left open
40	IN1-	Input	Pull-up/ Pulldown	Inverted reference input, internal bias to $V_{DD}/2$
41	IN1+	Input	Pulldown	Reference input 1
44	Ref_Out	Output		Reference output, CMOS
46	Sync_OE	Input	Pulldown	Synchronous output enable for Ref_Out, see Table 3 for functions

Function Table

Table 1: Input select function

IN_SEL [1]	IN_SEL [0]	Function
0	0	IN0 is the selected reference input
0	1	IN1 is the selected reference input
1	X	XTAL is the selected input

Table 2: Output Mode select function

OPMODEA/B [1]	OPMODEA/B [0]	Output Bank A / Bank B Mode
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Table 3: Reference output enable function

Sync_OE	Ref_Out
0	Hi-Z
1	Output enabled

Table 4: Illegal input level function

Input illegal status	Output status
Input open	Logic Low
Input both high	Logic Low
Input both low	Logic Low

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....	-55 to +150°C
Supply Voltage to Ground Potential (V_{DD}, V_{DDO})...	-0.5 to +4.6V
Inputs (Referenced to GND)	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Latch up	200mA
ESD Protection (Input)	2000 V min (HBM)
Junction Temperature	125 °C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375		3.465	V
V_{DDO}	Output Supply Voltage		2.375		3.465	V
I_{DD}	Core Power Supply Current			90	120	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded		150	190	
		All LVDS outputs loaded		110	130	
		All HCSL outputs unloaded		80	120	
T_A	Ambient Operating Temperature ¹		-40		85	°C
T_B	PCB Operating Temperature ¹		-40		105	°C

Note 1: Either T_A or T_B used as operating condition

DC Electrical Specifications - Differential Inputs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
C_{IN}	Input capacitance			3		PF
V_{IH}	Input high voltage				$V_{DD}+0.3$	V
V_{IL}	Input low voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK		0.15		$V_{DD}-0.85$	V
V_{CM}	Common mode input voltage		GND + 0.5		$V_{DD}-0.85$	V
ISO_{MUX}	MUX isolation			-89		dBc

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I _{IH}	Input High current	Input = V _{DD}			150	uA
I _{IL}	Input Low current	Input = GND	-150			uA
V _{IH}	Input high voltage	V _{DD} =3.3V	2.0		V _{DD} +0.3	V
V _{IL}	Input low voltage	V _{DD} =3.3V	-0.3		0.8	V
V _{IH}	Input high voltage	V _{DD} =2.5V	1.7		V _{DD} +0.3	V
V _{IL}	Input low voltage	V _{DD} =2.5V	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V _{OH}	Output High voltage		V _{DDO} -1.4		V _{DDO} -0.9	V
V _{OL}	Output Low voltage		V _{DDO} -2.2		V _{DDO} -1.7	V

DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V _{OH}	Output High voltage			1.43		V
V _{OL}	Output Low voltage			1.0		V
V _{ocm}	Output commode voltage			1.25		V
DV _{ocm}	Change in V _{ocm} between completely output states				50	mV
R _o	Output impedance		85		140	Ω

DC Electrical Specifications – HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V _{OH}	Output High voltage		520		900	mV
V _{OL}	Output Low voltage		-150		150	mV

DC Electrical Specifications – LVCMOS Output

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V _{OH}	Output High voltage	V _{DDO} =3.3V +/-5%, I _{OH} = 8mA	2.3			V
		V _{DDO} =2.5V +/- 5%, I _{OH} = 8mA	1.5			V
V _{OL}	Output Low voltage	V _{DDO} =3.3V +/-5%, I _{OL} = -8mA			0.5	V
		V _{DDO} =2.5V +/- 5%, I _{OL} = -8mA			0.4	V
V _{OH}	Output High voltage	V _{DDO} =3.3V +/-5%, I _{OH} = 24mA	2.1			V
		V _{DDO} =2.5V +/- 5%, I _{OH} = 16mA	1.5			V
V _{OL}	Output Low voltage	V _{DDO} =3.3V +/-5%, I _{OL} = -24mA			1	V
		V _{DDO} =2.5V +/- 5%, I _{OL} = -16mA			0.8	V
R _{IUT}	Output Impedance	V _{DDO} = 3.3V ± 5%		17		Ω
		V _{DDO} = 2.5V ± 5%		22		Ω

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units	
F _{OUT}	Clock output frequency	LVPECL, LVDS			1500	MHz	
		HCSL			250		
T _r	Output rise time	From 20% to 80%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	300		700	
T _f	Output fall time	From 80% to 20%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	300		700	
T _{ODC}	Output duty cycle	Frequency<650MHz, V _{ID} ≥ 400mV	LVPECL, HCSL (<250MHz)	48		52	%
			LVDS	47		53	
		Frequency<1GHz, V _{ID} ≥ 400mV	LVPECL	45		55	
			LVDS	45		55	
Frequency<1.5GHz, V _{ID} ≥ 400mV	LVDS	40		60			
	Frequency<1.5GHz, V _{ID} ≥ 400mV	LVPECL	40		60		
V _{PP}	Output swing Single-ended	LVPECL outputs @ <1GHz	500		1100	mV	
		LVPECL outputs @ >1GHz	400		1000		
		LVDS outputs @ <1GHz	250		600		
		LVDS outputs @ >1GHz	250		550		

AC Electrical Specifications – Differential Outputs Cont.

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
T _j	Buffer additive jitter RMS	156.25MHz, 12kHz to 20MHz		0.02		ps
		156.25MHz, 10kHz to 1MHz		0.01		ps
V _{CROSS}	Absolute crossing voltage	HCSL		460		mV
DV _{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T _{SK}	Output Skew	10 outputs devices, outputs in same tank, with same load, at DUT.		15	40	ps
T _{PD}	Propagation Delay	LVPECL, LVDS @ 3.3V, 100MHz		570		ps
		HCSL @ 3.3V, 100MHz		900		ps
T _{OD}	Valid to HiZ				80	ns
T _{OE}	HiZ to valid				80	ns
T _{P2P Skew}	Part to Part Skew ¹			80	120	ps

AC Electrical Specifications – CMOS

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F _{OUT}	Ref_Out frequency	XTAL input	10		50	MHz
		Reference input			200	MHz
T _j	Buffer additive jitter RMS	XTAL input		0.3		ps
		Reference input		0.03		ps
t _r /t _f	Rise time, Fall time	C _L = 10pF		1.5		ns
T _{ODC}	Output duty cycle	C _L = 10pF	45		55	%
t _{PD}	Propagation delay	3.3V, 25MHz		2200		ps
t _S	Setup time		300			ps
t _{SOD}	Clock edge to output disable	Ref_Out	2		4	cycles
t _{SOE}	Clock edge to output enable	Ref_Out	2		4	cycles

Notes:

1. This parameter is guaranteed by design

Crystal Characteristics

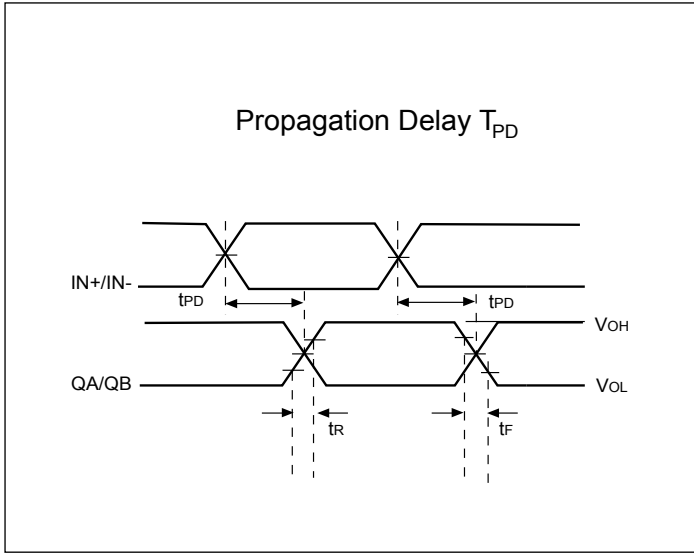
Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation	Fundamental			
Frequency Range	10		50	MHz
Equivalent Series Resistance (ESR)			70	Ω
Shunt Capacitance			7	pF
Load Capacitance	10		18	pF
Drive Level			500	μ W

Recommended Crystals

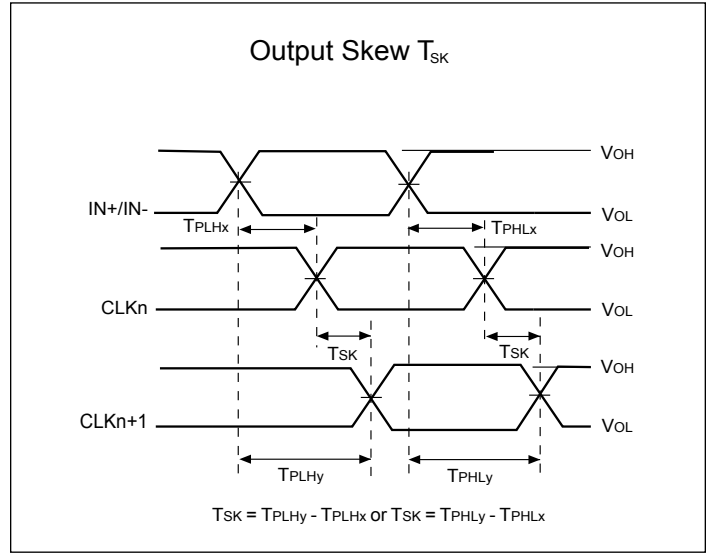
Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf
- b) FY2500091, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf
- c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

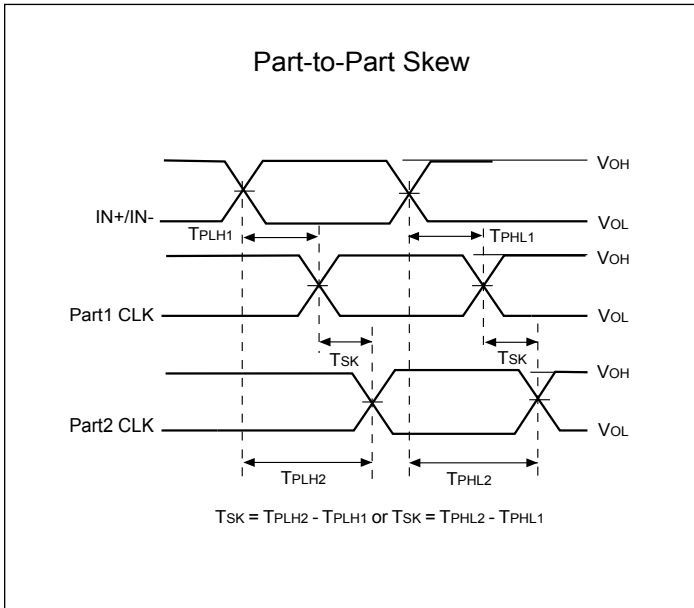
Propagation Delay



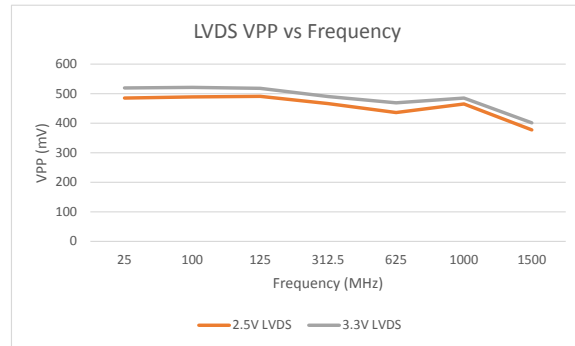
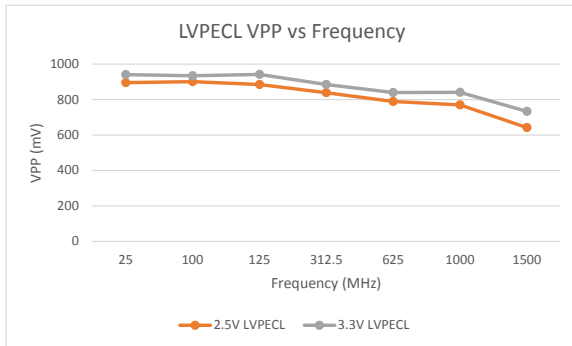
Output Skew



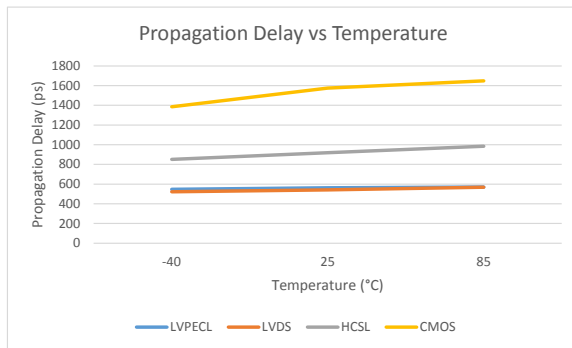
Part to Part Skew



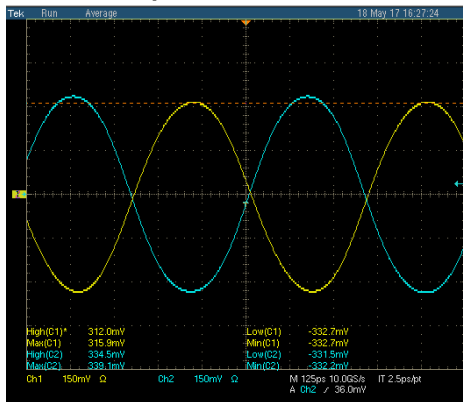
LVPECL/ LVDS Output Swing vs. Frequency



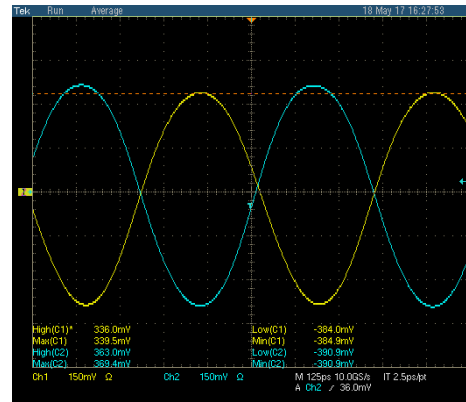
Propagation Delay vs Temperature



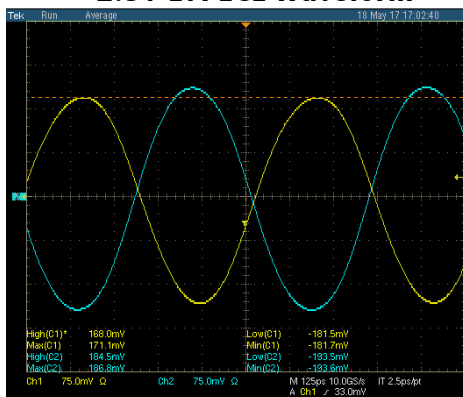
1.5GHz LVPECL/ LVDS Waveform



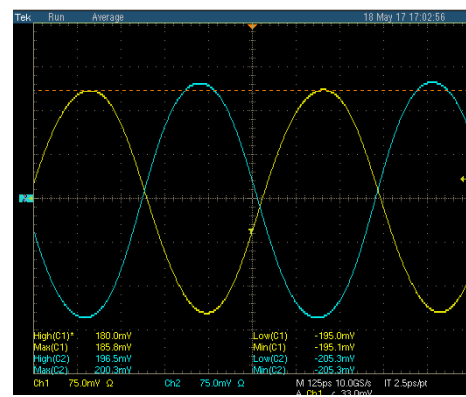
2.5V LVPECL Waveform



3.3V LVPECL Waveform



2.5V LVDS Waveform

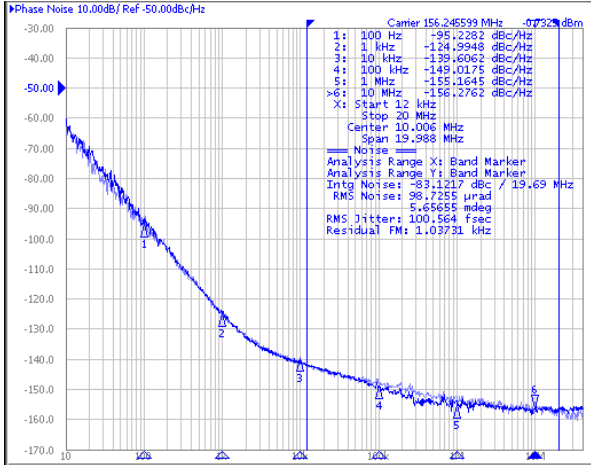


3.3V LVDS Waveform

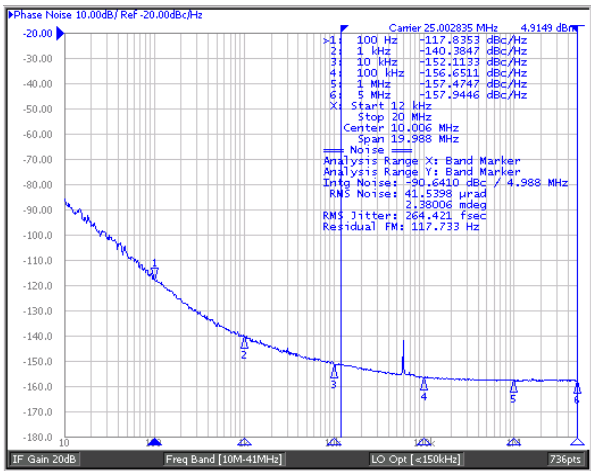
Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

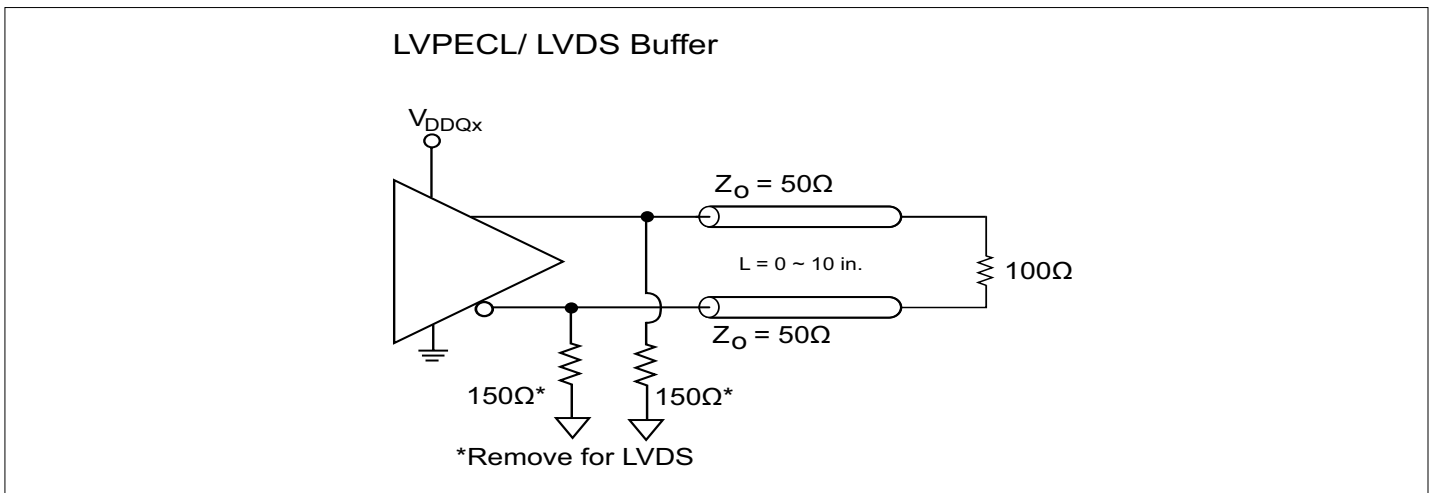
Additive jitter is calculated at 156.25MHz~27fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



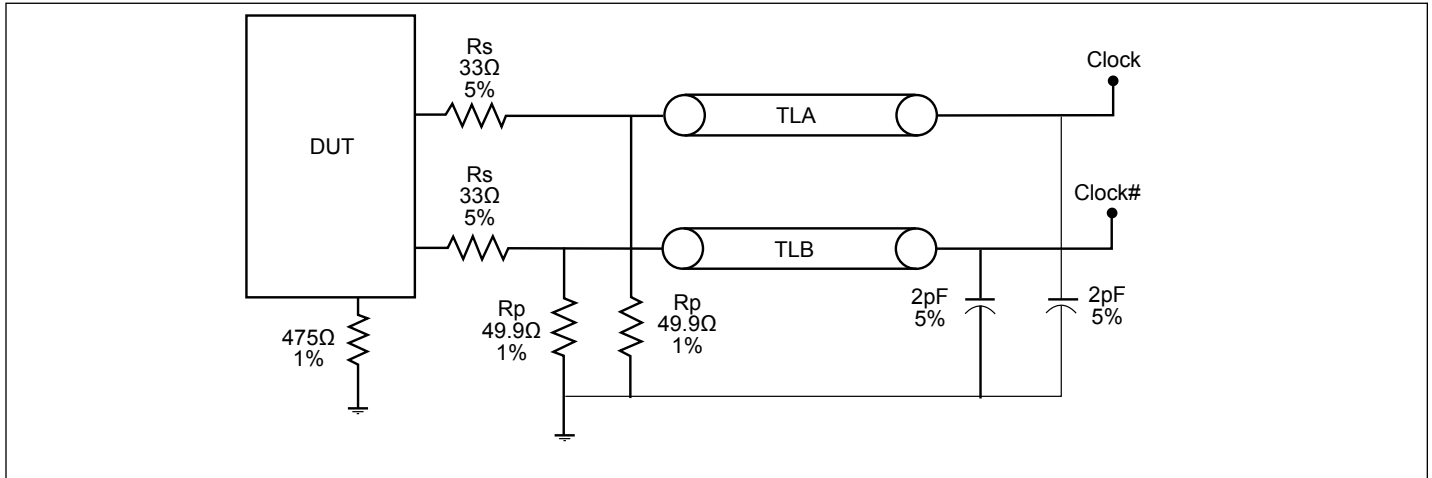
Total phase jitter with 25MHz XTAL ~ 264fs RMS (12kHz ~20MHz)



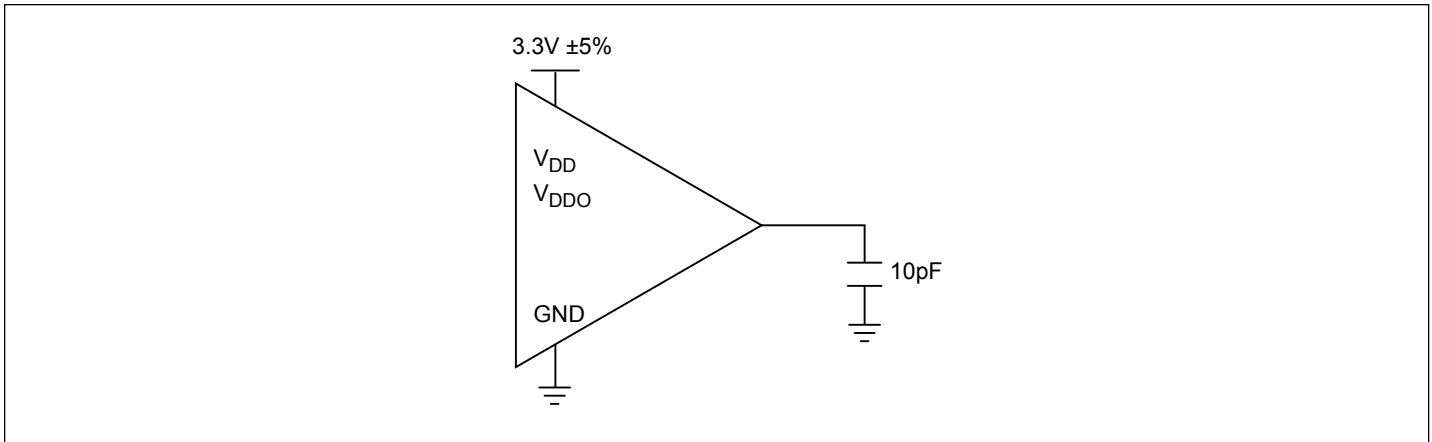
Configuration Test Load Board Termination for LVPECL/ LVDS Outputs



Configuration Test Load Board Termination for HCSL Outputs



Configuration Test Load Board Termination for LVCMOS Outputs



Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R1/R2 = 0.609$.

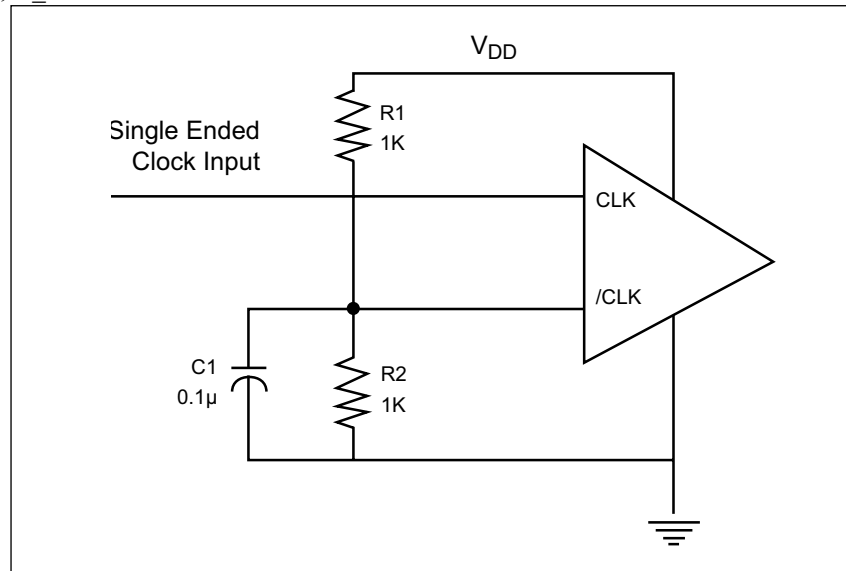
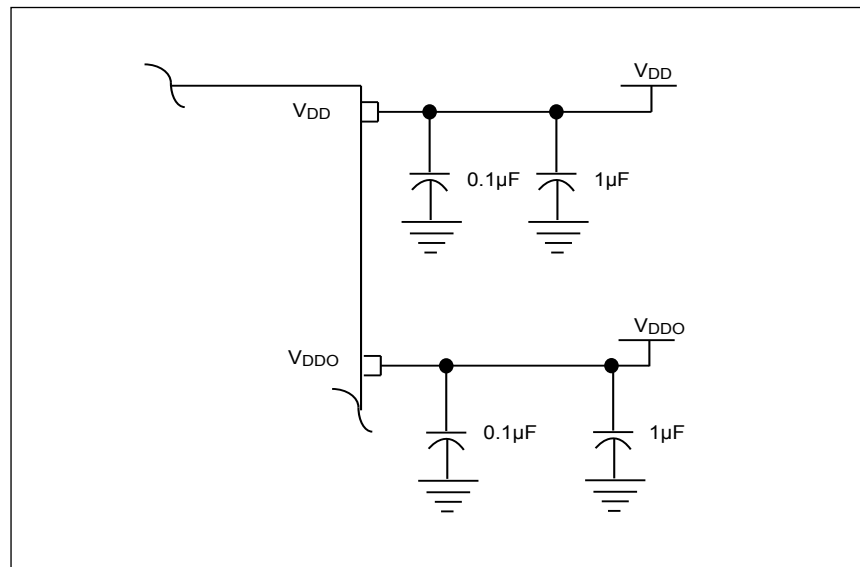


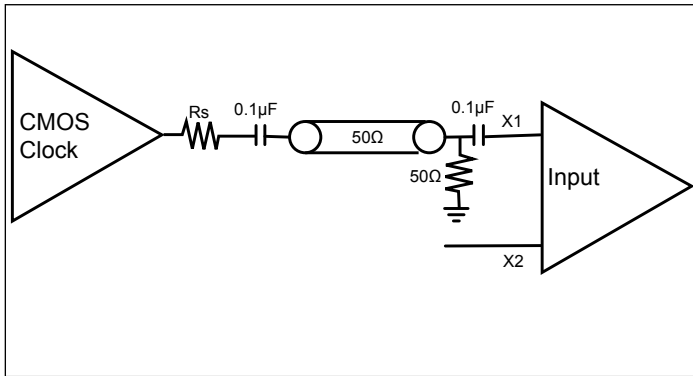
Figure 1. Single-ended input to Differential input device

Power Supply Filtering Techniques

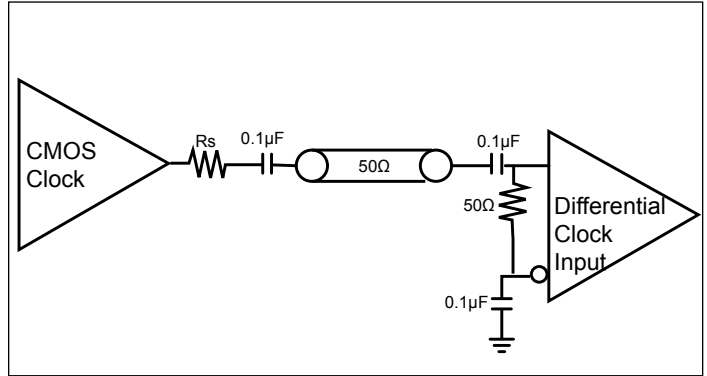
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF and 1µF bypass capacitors should be used for each pin.



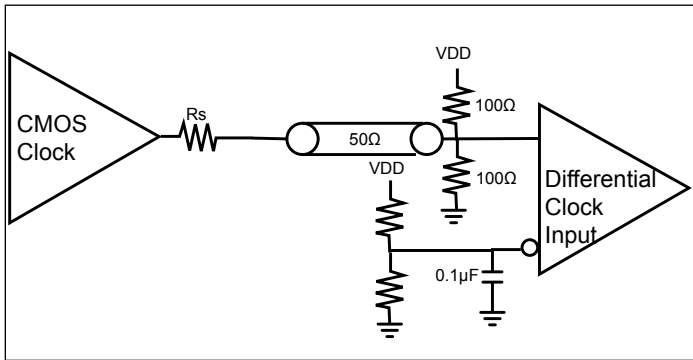
Driving X1 with a Single Ended Input



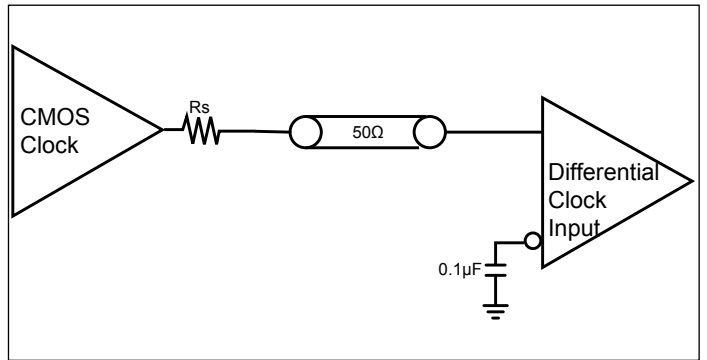
Single Ended Input, AC couple



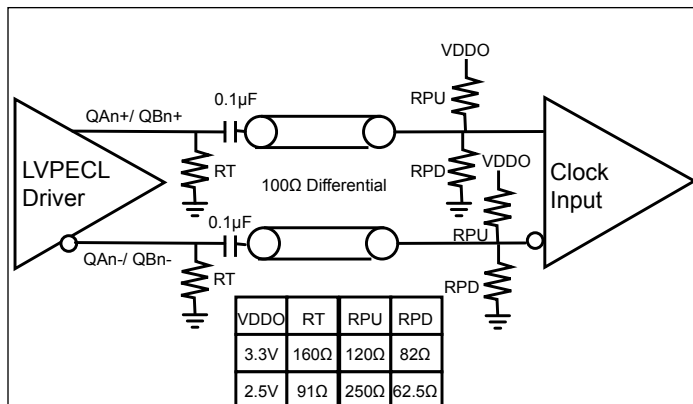
Single Ended Input, DC couple



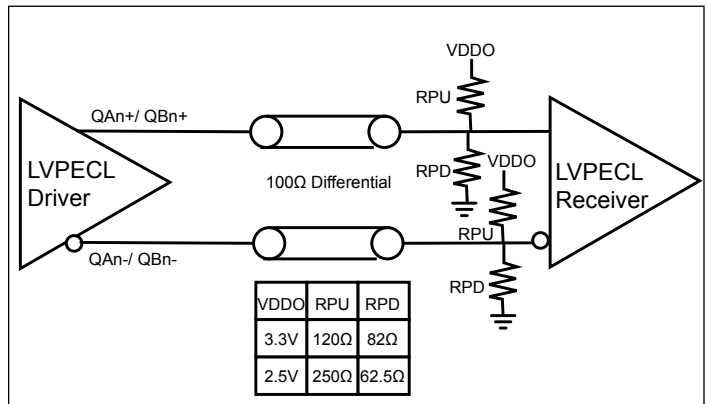
Single Ended Input, DC couple



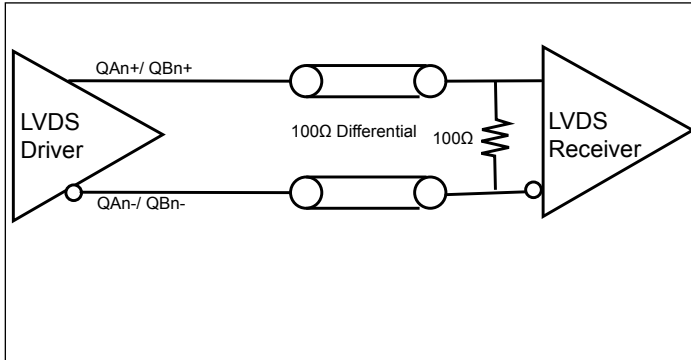
LVPECL, AC Couple, Thevenin Equivalent



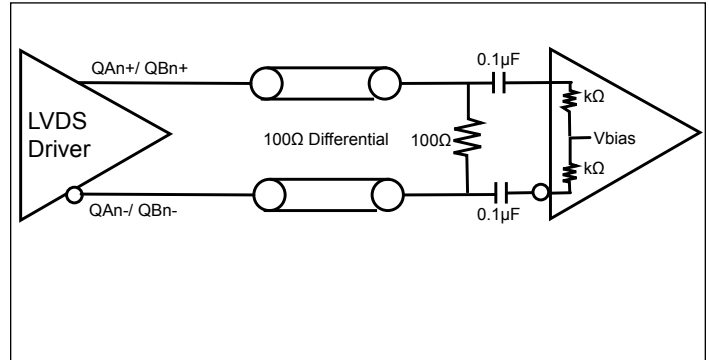
LVPECL, DC Couple, Thevenin Equivalent



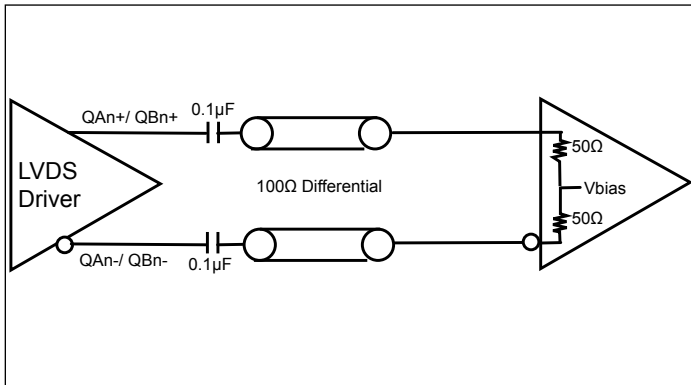
LVDS DC Couple



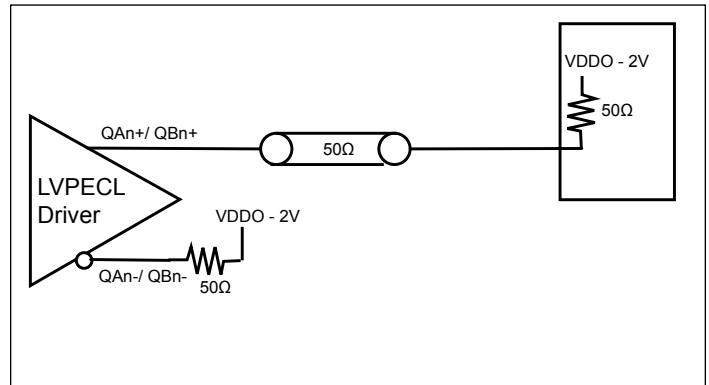
LVDS AC Couple at Load



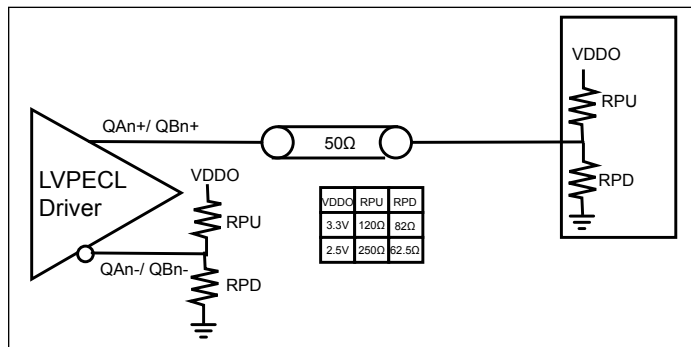
LVDS AC Couple with Internal Termination



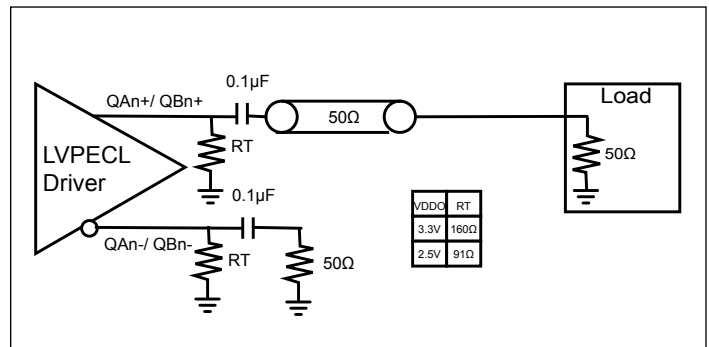
Single Ended LVPECL, DC Couple



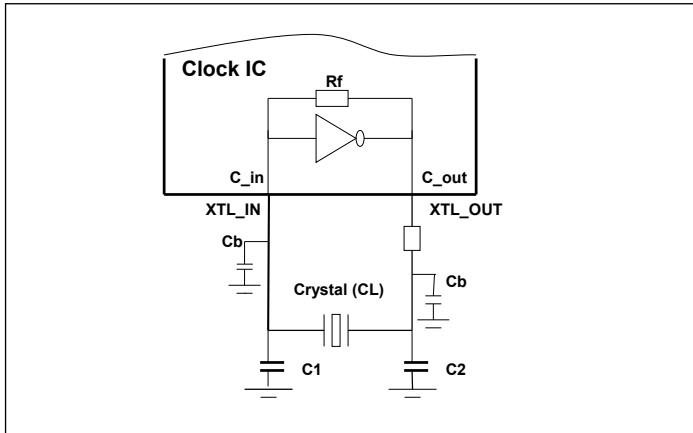
Single Ended LVPECL, DC Couple, Thevenin Equivalent



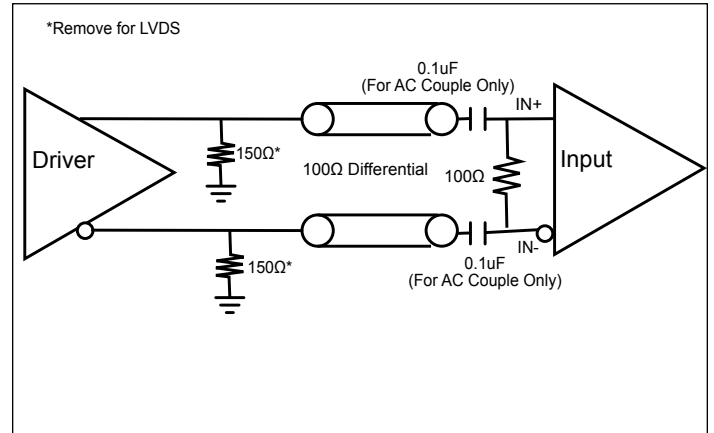
Single Ended LVPECL, AC Couple, Thevenin Equivalent



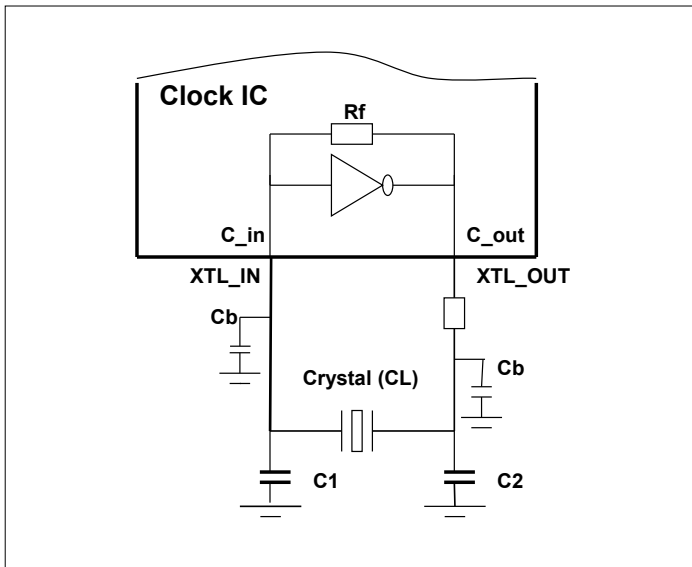
Clock IC Crystal Input Guide



LVPECL/ LVDS AC and DC input



Clock IC Crystal loading cap. design guide



CL = crystal spec. loading cap.

C_{in/out} = (3~5pF) of IC pin cap.

C_b = PCB trace (2~4pF)

C_{1,C2} = load cap. of design

R_d = 50 to 100ohm drive level limit

Design guide: $C_1=C_2=2 * CL - (C_b + C_{in/out})$ to meet target +/-ppm < 20 ppm

Example1: Select CL=18 pF crystal, $C_1=C_2=2*(18pF) - (4pF+5pF)=27pF$, check datasheet too

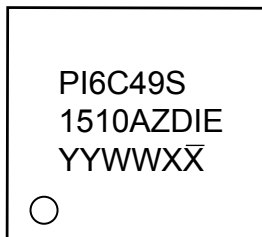
Example2: For higher frequency crystal (=>20MHz), can use formula $C_1=C_2=2*(CL-6)$, can do fine tune of C₁, C₂ for more accurate ppm if necessary

Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	23.65 °C/W
Θ_{JC}	Junction-to-case thermal resistance		9.10 °C/W

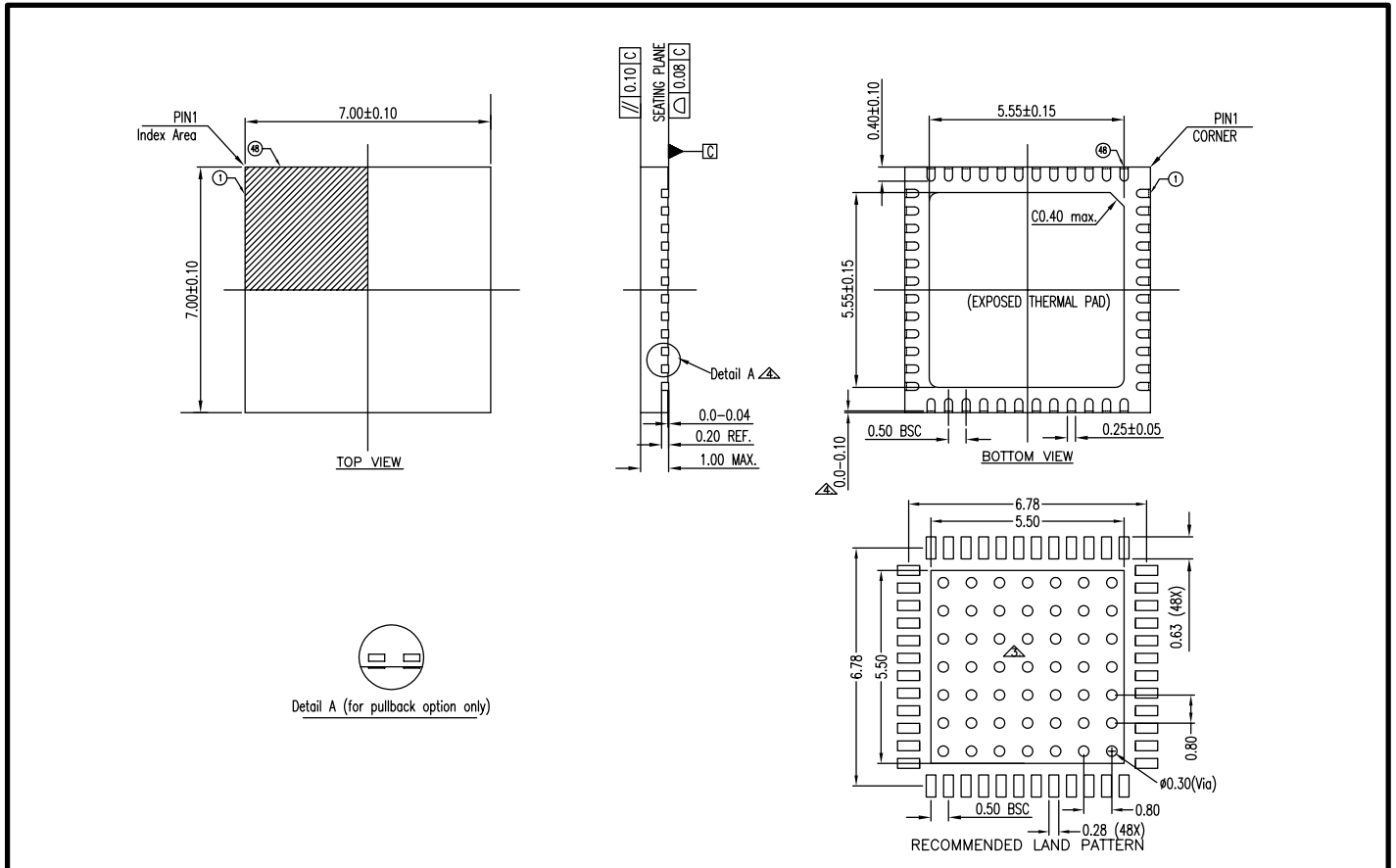
Part Marking

ZD Package



YY : Year
WW : Workweek
1st X : Assembly Site Code
2nd X : Wafer Site Code

Packaging Mechanical: 48-TQFN (ZD)



- NOTE :
1. All dimensions are in mm. Angles in degree.
 2. Refer JEDEC MO-220
 3. Thermal Pad Soldering Area
 4. Depending on the method of lead termination at the edge of the package, pull back maybe present.
 5. Recommended Land Pattern is for reference only.

DIODES INCORPORATED	PERICOM A PRODUCT LINE OF DIODES INCORPORATED ENABLING SERIAL CONNECTIVITY	DATE: 07/26/16
DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN)		
PACKAGE CODE: ZD (ZD48)		
DOCUMENT CONTROL #: PD-2045		REVISION: F

16-0151

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C49S1510AZDIEX	ZD	48-Contact, Very Thin Quad Flat No-Lead (TQFN)	-40 °C to 85 °C

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See <http://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А