World Modem™ Secure

Features

- Self-contained 300 – 2400 baud modem family
- V.21, V.22, V.23, Bell 103, Bell 212A Error Correction
- Compliant with global regulatory standards
- 3V and 5V power supply models
- Serial host interface
- Internal UART with HW/SW flow control
- Supports standard alarm protocols
- Caller ID detection and decode
- Phone Line Snoop and Tamper Detection
- Pin Compatible with all Copeland Communications modem products.
- Socket Modem™ compatible
- Low power consumption – 20mA
- Low Power Standby Mode – 100uA
- Small footprint – 1.045" X 2.54"

Applications

- Global Embedded applications
- Point-of-sale terminals
- Set-top boxes
- Vending & gaming machines
- Security Systems
- Remote monitoring & control
- Remote telemetry and SCADA
- OEM applications
- Bridge for other CCI products

Description

The CC-2401K2 World modem™ Secure is a compact integrated 2400 baud modem with World Modem™ compatibility. The modem features a transformer-less DAA meeting global telephone system requirements, no electro-mechanical components and flexible DSP data pump. The modem is user-configurable to meet virtually all global telecom requirements. The modem supports serial host communications via flexible internal UART. The modem conforms to the industry standard World Modem™ mechanical and interface specifications. Because of its built-in features and flexibility, many applications and OEM products can be created using the World Modem™ Secure. The World Modem™ Secure is an ideal modem for world-wide embedded applications due to its flexibility, global compliance, small size, low power consumption and upgradeability. Copeland Communications World modems are software and plug compatible with many other Copeland Communications Socket products. In addition, the CC-2401K2 features include fast connect times for electronics point-of-sale applications and alarm protocols for security systems.

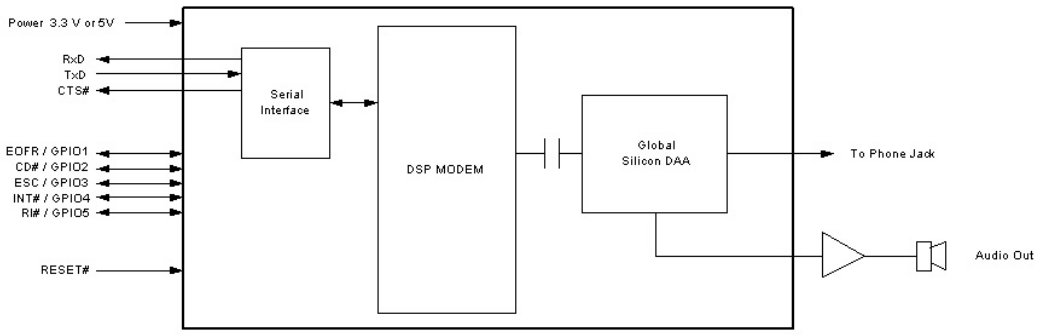
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Table of Contents

Features 1
Applications 1
Description 1
Block Diagram 3
Serial Interface 4
Mechanical Outline 5
Features 6
Functional Description 8
Host Interface 9
Line Interface 9
Command / Data Mode 10
Flow Control 10
Power Save Modes 10
Global Operation 11
Parallel Phone Detection 11
On-Hook Intrusion Detection 11
Off-Hook Intrusion Detection 12
Interrupt Detection 13
Loop Current Detection 13
Loss of Carrier Detection 13
Overcurrent Detection 13
Caller ID Monitor/Bellcore Caller ID 13
UK Caller ID 13
V.23 Operation / V.23 Reversing 13
V.42 HDLC Operation 15
Fast Connect 16
AT Command Set 17
Command Line Execution 17
AT Command Set Description 19
Alarm Industry AT Commands 21
Modem Result Codes and Call Progress 23
Automatic Call Progress Detection 24
Manual Call Progress Detection 25
Low Level DSP Control 28
DSP registers 28
Call Progress Filters 31
CE DECLARATION OF CONFORMITY 66
Revision Information 68
Contact Information 69
Warranty 69
Legal 69

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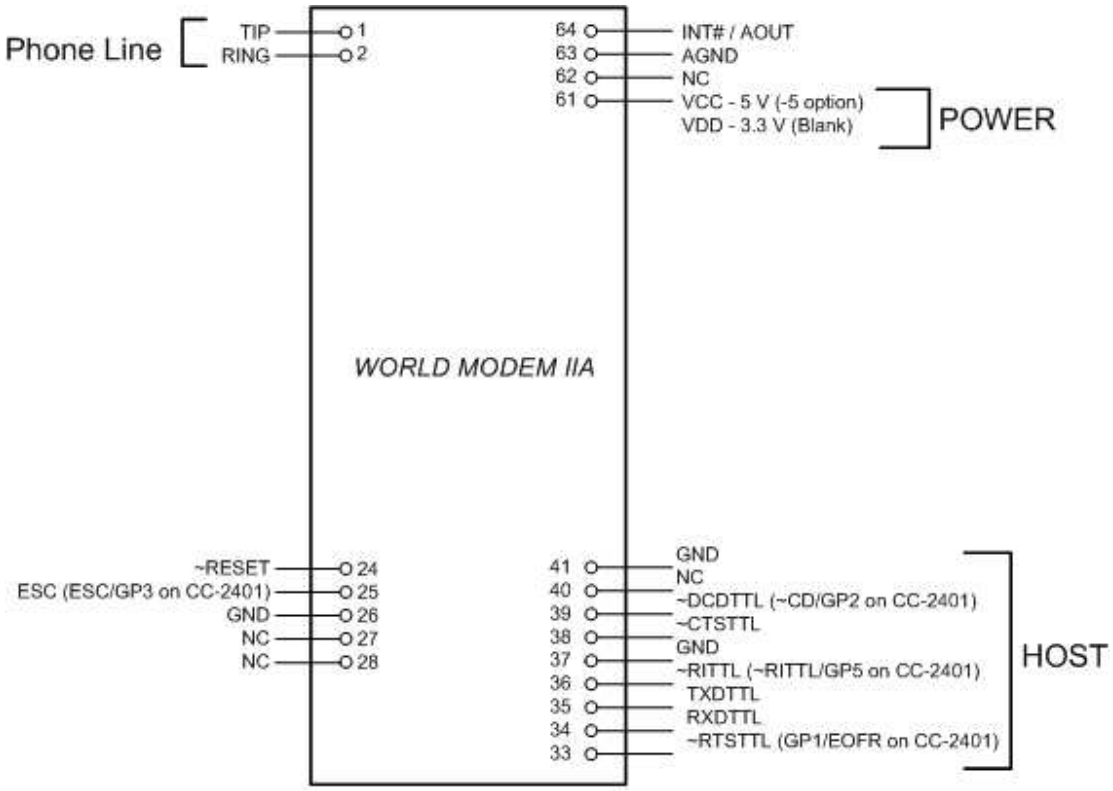
Block Diagram



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Serial Interface

The pin out of the serial modem is shown in the figure below.



Note: Signals on pins 24, 25, 33-40 are TTL.

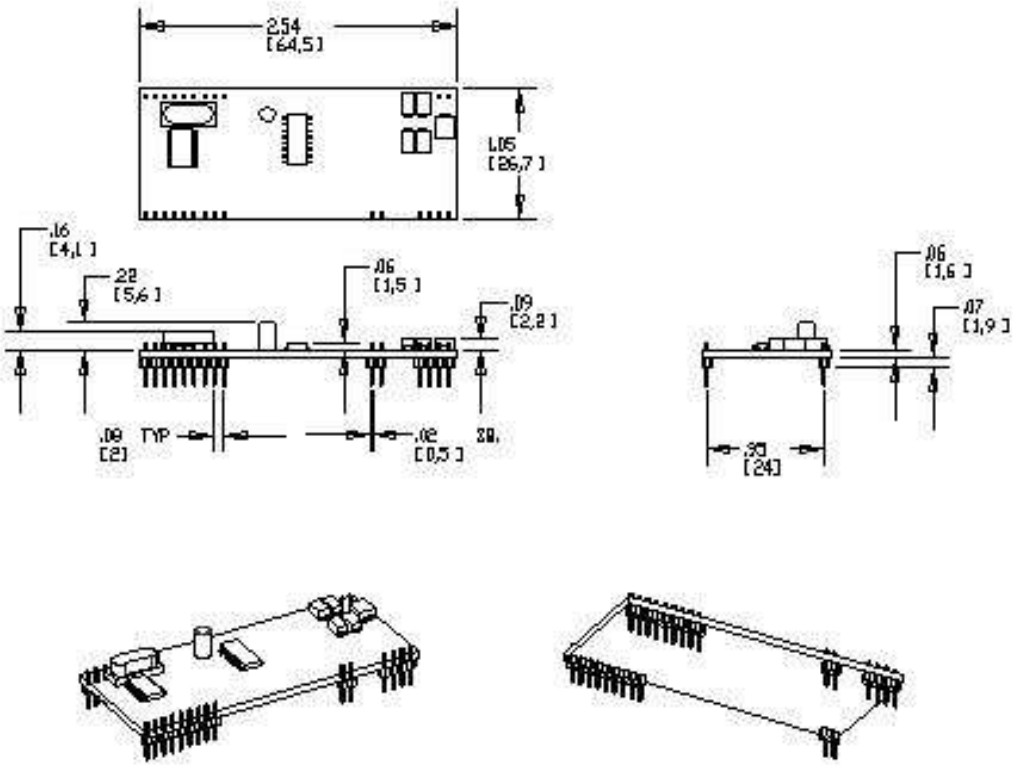
Serial Host Interface

The host interface control and data signals are 3.3 volts and are 5 volt tolerant. The World modem II modems can be directly connected into 3.3 or 5 volt systems. On 5V models (CC-2401K2-xx5), connect pin 61 to 5V. On 3.3V models, connect Pin 61 to +3.3V.

WARNING: DO NOT CONNECT PIN 61 TO 5V ON 3.3 VOLT MODELS.

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Mechanical Outline



Mechanical

The modem module is on an 0.062 thick FR-4 PC board. The module has two rows of 2mm pins located 24mm on center. The module is designed to plug into 2 mm sockets with the same 24 mm spacing.

Due to the low mass of the board, no retention is required aside from the sockets. A large tie-wrap may be used to insure retention in high shock or vibration environments, if desired.

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Detailed Specifications

Item	Specification
Data Rate	
2400 bps 1200 bps 300 bps	V.22, V.23, Bell 212A V.22, V.23, Bell 212A V.21, Bell 103
Data Format	
Bit format	Selectable 8,9, bits per character
Compatibility	V.23, V.22bis, V.21, Bell 212A & Bell 103
Control	AT command set
Host Interface	
Serial	TTL - 8, 9 bit asynchronous data @ 2400-307200 bps rate
Flow Control	CTS, DCD, RI
Features	
Caller ID	Bellcore (US) & ETSI (European)
PCM/CODEC	
Parallel Phone Detection	On-hook and off-hook detection
International Operation	Via programmable control registers
Dialing	DTMF & pulse
Power Requirements Voltage Current	 3.3 V Nominal 3.0V Minimum 3.6V Maximum 25 mA Operating Maximum 100 µA Standby Maximum
Environmental	
Temp Range	Commercial 0C-70C (contact factory for extended temperature options)
Compliance	FCC part 15 FCC part 68 EN55022 EN55024 EN61000 TBR-21

Asynchronous Serial Interface

The Asynchronous Serial Interface is a complete UART consisting of Receive and Transmit signals as well as CTS, DCD and RI control signals.

The UART is programmable to support a number of baud rates and data formats. Supported data rates and formats are:

Data Bits: 8
Stop Bits: 1
Baud Rates: 300, 1200, 2400 (default), 9600, 19200, 38400, 115200, 307200

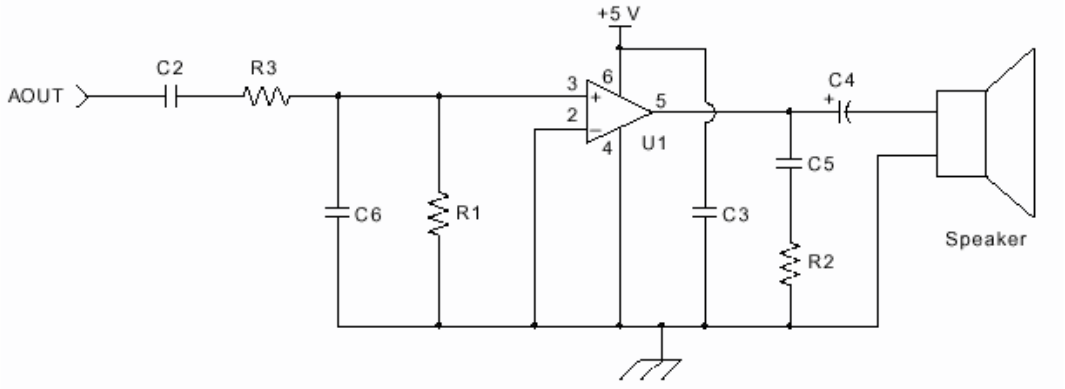
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Status
In addition to flow control, the modem provides two hardware status signals. These signals are multiplexed and may be used as general purpose IO signals:

DCD
RI

Reset – A hardware reset is provided to reset the modem controller on power-up or to force the modem back to its default settings. This active low signal has an on-board pull up. Leave this pin unconnected if hardware reset is not needed.

Audio Output
The World Modem II modules support an analog (audio) output. This analog signal can be used for call progress monitoring. This signal is multiplexed with the INT# signal.



Optional Call Progress Monitor

Suggested Component Values

Symbol	Value
C2, C3, C5	0.1 µF, 16 V, ±20%
C4	100 µF, 16 V, Elec. ±20%
C6	820 pF, 16 V, ±20%
R1	10 kΩ, 1/10 W, ±5%
R2	10 Ω, 1/10 W, ±5%
R3	47 kΩ, 1/1 W, ±5%
U1	LM386

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Functional Description

The CC-2401K2 is a complete modem with integrated DAA that provides a programmable line interface meeting all global telephone line requirements. The modem accepts simple AT commands and provides connect rates up to 2400 baud, full-duplex. The modem supports V.42 hardware support through HDLC framing. To minimize handshake times, the CC-2401K2 can implement a V.22-based fast connect. V.23 reversing protocol and standard alarm formats including SIA are also supported.

The World Modem II family of products is ideal for embedded applications due to its small form factor, low power consumption and global compliance. The CC-2401K2 contains everything necessary to connect to the Public Switched Telephone Network (PTSN). All that is needed is a connector to the local phone line. No external filtering or fusing are required.

The CC-2401K2 is designed for rapid design into existing modem applications. The modem interfaces directly to a microcontroller's UART. The CC-EVAL kit comes with full schematics to help design and a fully functional board to connect to a PC serial port for rapid testing and evaluation.

The modem can be fully programmed to meet international telephone line interface requirements with full compliance to FCC, TBR21, JATE and other country-specific PTT specifications. The CC-2401 is designed to meet worldwide requirements for out-of-band energy, billing-tone immunity, high voltage surges, and safety requirements.

Configuration	Modulation	Carrier Frequency (Hz)	Data Rate (bps)	Standard Compliance
V.21	FSK	1080/1750	300	Full
V.22*	DPSK	1200/2400	1200	Full
V.22bis*	QAM	1200/2400	2400	No retrain
V.23	FSK	1300/2100	1200/75	Full; plus reversing (Europe)
V.23	FSK	1300/1700	600/75	
Bell 103	FSK	1170/2125	300	Full
Bell 212A	DPSK	1200/2400	1200	Full
Security	DTMF	-	40	Full
SIA-Pulse	Pulse	-	Low	Full
SIA Format	FSK	1170/2125	300 half-duplex	300 bps only

* **NOTE:** The CC-2401 only adjusts its DCE rate from 2400 bps to 1200 bps if it is connecting to a V.22-only (1200 bps only modem. Because the V.22bis specification does not outline a fallback procedure, the host should implement a fallback mechanism consisting of hanging up and connecting at a lower baud rate. Retraining to accommodate changes in line conditions that occur during a call must be implemented by terminating the call and redialing.

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Host Interface

The host interface is serial TTL. The default host speed of 2400 baud and 8N1 format (8 data bits, no parity bit and 1 stop bit). The defaults can be changes after initialization by using standard AT commands. A true RS-232 interface is available on the World modem Evaluation Board.

To change the serial baud rate, the command ATSE0=xxx where xxx is (a carriage return must follow every command for it to be effected):

DTE Rate (bps)	SE0[2:0] (SD)
300	000
1200	001
2400	010
9600	011
19200	100
38400	101
115200	110
307200	111

As soon as the command is issued, the host must change its baud rate to match the World Modem II's new data rate.

Line Interface

The CC-2401 can be configured to any of the Bell and CCITT operation modes listed in table <SC>. In V.22bis, the modem connects at 1200 bps if the other modem is configured for V.22. The CC-2401 also supports S1A and other protocols for the security industry. Contact the factory for other modem configurations.

Protocol	Register S07 Value
V.22bis	0x06
V.22	0x02
V.21	0x03
Bell 212A	0x00
Bell 103	0x01
V.23 (1200 tx, 75 rx)	0x14
V.23 (75 tx, 1200 rx)	0x24
V.23 (600 tx, 75 rx)	0x10
V.23 (75 tx, 600 rx)	0x20

The CC-2401 does not continuously check for stop bits on the incoming digital data. If the TXD pin is not high, the RXD pin may echo meaningless characters to the host. This requires the UART to flush its receiver FIFO upon initialization.

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Command / Data Mode

On Reset, the CC-2401 is in command mode. In this mode, the modem accepts AT commands. Type “ATDT#” (tone dial) to initiate a call once the modem has been initialized. Use ATDP for pulse lines. Every command must be followed by a carriage return. Once a connection is established, the modem responds with “c, “d”, or “v” and enter data mode. Once in this mode, the modem will not respond to AT style commands. There are three ways to return to command mode:

- Use the ESC pin. To enable the ESC pin feature, set SE2[5:4) = 11. A positive edge on this pin will return the modem to command mode. To reenter data mode, type “ATO”.
- Use 9-bit data mode. If 9-bit data format with escape is configured a 1 detected on bit 9 returns the modem to command mode. To enable this feature, set SE0[3] (ND) = 1 and S15[0] (NBE) = 1. Again, use “ATO” to return to data mode.
- Use “+++”. The escape sequence is a sequence of three escape characters that are set in S-register S0F (“+” character is the default escape). If this sequence is seen and the modem detects no activity on the line before or after, the modem will return to command mode.

No matter the escape method, when carrier is lost, the modem will return to command mode and reports “N”.

Flow Control

Flow control is only needed if the DTE and DCE rate are not the same. If the DTE rate is set higher than the line (DCE), flow control is required to prevent data loss to the transmitter.

To control data flow, the CTS pin is used. When CTS is asserted, the CC-2401 is ready to accept a character. While CTS is negated, no data should be sent to the modem on TXD. To simplify flow control, the CC-2401 has an integrated ten character transmit FIFO and allows for two different CTS reporting methods. By default, the CTS pin is negated as soon as a start bit is detected on the TXD pin and remains negated until the modem is ready to accept another character. Setting SFC7[7]=1 (CTSM), CTS is negated when the FIFO is 70% full and is reasserted when the FIFO is 30% full.

Power Save Modes

The CC-2401 has three low power modes:

- DSP Power down. The DSP processor can be powered down by setting SEB[3](PDDE) = 1. In this mode, the serial interface still functions and the modem detects ringing and intrusion. No modem modes or tone detection features function.
- Wake on Ring. Issuing ATz command causes the modem into a low power mode where both the controller and DSP are powered down. Only an incoming ring, a low TXD signal, or a total reset will power up the modem again. Return from wake-on-ring triggers the INT pin if S09[6] (WOR) = 1.
- Total Power down. SF1[5] = 1 and SF1[6] = 1 places the modem into total powerdown mode. All logic, including the crystal, is powered down.

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Global Operation

The CC-2401 provides a programmable line interface to meet international telephone line requirements. The following table provides the register settings required to meet various country PTT standards.

Register	**SF5**				**SF6**		
Country	**OHS**	**ILIM**	**RZ**	**RT**	**MINI[1:0]**	**DCV[1:0]**	**ACT[3:0]**
Australia	10	0	0	0	00	00	0011
Brazil[1]	00	0	0	0	00	00	0000
TBR21[2]	00	1	0	0	11	11	0011
Czech Republic	00	0	0	0	11	11	0011
FCC[3]	00	0	0	0	11	11	0000
Latvia	00	1	0	0	11	11	0011
Malaysia[4]	00	0	0	0	00	00	0000
New Zealand	00	0	0	0	11	11	0100
Nigeria	00	11	0	0	11	11	0011
Philippines	00	0	0	0	00	00	0000
Poland, Slovenia	00	0	1	1	11	11	0000
South Africa	10	0	1	0	11	11	0000
South Korea	00	00	1	0	11	11	0000

Notes:

1. The following countries require the same settings as Brazil: Armenia, China, Egypt, Georgia, Japan, Jordan, Kazakhstan, Kyrgyzstan, Malaysia, Moldova, Oman, Pakistan, Qatar, Russia, Syria, Taiwan, Thailand, Ukraine.
2. The following countries require the same settings as TBR21: Austria, Bahrain, Belgium, Bulgaria, Croatia, Cyprus, Denmark, Estonia, European Union, Finland, France, Germany, Greece, Guadeloupe, Iceland, Ireland, Israel, Italy, Lebanon, Liechtenstein, Luxembourg, Malta, Martinique, Morocco, Netherlands, Norway, Polynesia (French), Portugal, Reunion, Spain, Sweden, Switzerland, Turkey, and the United Kingdom.
3. The following countries require the same settings as FCC: Argentina, Brunei, Canada, Chile, Columbia, Dubai, Equador, El Salvador, Guam, Hong Kong, Hungary, India, Indonesia, Kuwait, Macao, Mexico, Peru, Puerto Rico, Romania, Saudi Arabia, Singapore, Slovakia, Tunisia, UAE, USA, Venezuela, Yemen.
4. Supported for loop current ≥ 20mA.

Parallel Phone Detection

The CC-2401 can detect when another telephone, modem or other device that is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle the interruption when the modem is using the phone line.

On-Hook Intrusion Detection

When the CC-2401 is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect when another device is using a shared telephone line, the host can use the modem to monitor the TIP-RING dc voltage with the LVS[7:0] bits (SDB). This register has a resolution of 1V per bit with an accuracy of about ±10%. Bits 0 through 6 of the 8 bit signed 2's complement number indicate the line voltage value. Bit 7 indicates the polarity of TIP and RING.

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When all devices on the phone line are on-hook, there is no loop current through TIP and RING. Therefore, the voltage is at maximum. On most telephone lines, this is a minimum of 40V. When a device goes off-hook the TIP-RING voltage drops. On most telephone lines, this off-hook voltage is a maximum of 20V.

If the host checks the voltage via LVS before initiating a call (or going off-hook for any reason), the modem can be used to determine if another device is using the telephone line. One way to do this is to verify the voltage in LVS is above a fixed threshold, such as 30V.

Off-Hook Intrusion Detection

Once a call has begun and the modem is in data mode, the serial port is used for modem data making it difficult for the host to monitor registers. Therefore, when the modem is off-hook, an algorithm is implemented to automatically monitor the TIP-RING loop current via the LCS register (SF3). Because the TIP-RING voltage drops significantly when off-hook, TIP-RING current is a better indicator of another device using the phone line. The LCS[7:0] bits have a resolution of 1.1mA per bit. An LCS register value of 0x00 indicates less than the required loop current is present, and a value of 0xff indicates excessive current draw (> 120mA if ILIM = 0 or > 60mA if ILIM = 1). The user can read these bits directly through the LCS register. Upon detecting an intrusion, an "I" result code is sent to the host if it is in the call negotiation stage or command mode. Otherwise, the modem can be programmed to generate an interrupt to notify the host of the intrusion.

The off-hook intrusion algorithm monitors the value of LCS (SF3) at a sample rate determined by the DGSR (SDF, bits 6:0) register (40 ms units). The algorithm compares each LCS sample to the reference value in the ACL register (S12). If LCS is lower than ACL by an amount greater than DCL (S11, bits 4:0), the algorithm waits for another LCS sample, and if the next LCS sample is also lower than ACL by an amount greater than DCL, an interrupt occurs. This helps the modem avoid a false parallel phone detection (PPD) interrupt due to glitches on the phone line. The ACL is continually updated with the value of LCS as outlined below. The algorithm can be outlined as follows:

```
IF      LCS(t) = LCS(t – 40 ms x DGSR)
        and
        LCS(t) – ACL > DCL
THEN
        ACL = LCS(t)
IF      (ACL – LCS[t – 40 ms x DGSR]) > DCL)
        and
        (ACL – LCS[t]) > DCL)
THEN    an intrusion interrupt is sent to the host.
```

The off-hook intrusion algorithm does not begin to operate immediately after going off-hook. This avoids accidental interrupts occurring as a result of transients resulting from the modem itself going from on-hook to off-hook. The time delay between the modem going off-hook and the start of the intrusion algorithm is about 1 second. This can be adjusted using the IST register (S82, bits 7:4).

The off-hook intrusion algorithm may also be disabled for a period of time after dialing begins via the IB register (S82, bits 2:1). This avoids triggering an interrupt due to pulse dialing, open-switch intervals or line transients from central office switching. Intrusion can be disabled from the start of dialing to the end of dialing (IB = Dib), from the start of dialing to the timeout of the IS (S29, bits 7:0) by setting IB = 11. The off-hook intrusion algorithm is only suspended (not disabled) during this IB interval and sustains through the end of the interval triggers a PPD interrupt.

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Interrupt Detection

The interrupt pin (pin 64) can be programmed to alert the host of loss-of-carrier, loss-of-phone-line voltage/current, parallel phone detection, and other interrupts listed in the interrupt status mask (S08). After the host receives an interrupt via the INT# pin, the host should issue the AT:I command. This command causes a read-clear of the WOR, PPD, NLD, RI, OCD, and REV bits of the S09 register and raises (deactivates) the INT# pin. All the interrupt status bits in the register S09 remain high after being set until cleared by the AT:I command.

Loop Current Detection

The CC-2401 can monitor the loss of loop current. This feature can be enabled by setting S08[4] (NLDM) = 1. This feature is disabled by default. If the loop current is too low for normal DAA operation, S09[4] (NLD) is set. During this event, if the NLR result code is enabled by setting S62[1](NLR) = 1, the "I" result code is sent. Once the loop current returns to a normal current state, the "L" result code is sent. The INT# pin is also asserted if enabled.

Loss of Carrier Detection

The CC-2401 has two methods of implementing a loss of carrier function. If GPIO4 is programmed as INT# and if S08[7](CDM)=1, INT# asserts in data mode when a loss of carrier is detected. The carrier detect function may also be implemented on GPIO2 by setting SE2[3:2] (GPIO2) = 01 and SOC[7](CDE) = 1.

Overcurrent Detection

The CC-2401 begins monitoring for an overcurrent condition at a programmable time set by S32 (OCDT) after going off-hook (default = 20ms). If an overcurrent condition is detected, the CC-2401 sets S09[1] interrupt status. As long as GPIO4 is programmed as INT and the overcurrent mask bit is enabled by setting S08[1](OCDM) = 1, INT asserts during an overcurrent situation. The host may then check S09[1] (OCD) via the AT:I command to confirm that an overcurrent condition occurred.

Caller ID Monitor/Bellcore Caller ID

The CC-2401 continuously monitors the phone line for the caller ID mark signals. This can be useful in systems that require detection of caller ID data before the ring signal, voice mail indicator signals and Type II caller ID monitor support. To force the CC-2401 into caller ID monitor mode, set SOC[6:5] (CIDM) = 11.

NOTE: CIDM should be disabled before going off-hook.

UK Caller ID

The CC-2401 starts searching for the Idle State Tone Alert Signal. When this signal has been detected, the modem transmits an "a" to the host. After the Idle State Tone Alert Signal is completed, the modem applies the wetting pulse for the required 15 ms by quickly going off-hook and on-hook. From this point on, the algorithm is identical to that of Bellcore in that it searches for the channel seizure signal and the marks before echoing an "m" and then reports the decoded caller ID data.

V.23 Operation / V.23 Reversing

The CC-2401 supports full V.23 operation including the V.23 reversing procedure. V.23 operation is enabled by setting S07 (MF1) = $xx10xx00_b$ of $xx01xx00_b$. If S07[5] (V23R) = 1, the CC-2401

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receives data at 75 bps and receives data at 600 or 1200 bps. If S07[4] (V23T) = 1, the CC-2401 Receives data at 75 bps and transmits data at 600 or 1200 bps. S07[2] (BAUD) is the 1200 or 600 bps indicator. BAUD = 1_b enables the 1200/600 V.23 channel to run at 1200 bps, while BAUD = 0_b enables 600 bps operation.

When a V.23 connection is established, the modem responds with a "c" if the connection is made with the modem transmitting at 1200/600 bps and receiving at 75 bps. The modem responds with a "v" character if a V.23 connection is established with the modem transmitting at 75 bps and receiving at 1200/600 bps.

The CC-2401 supports V.23 turnaround procedure, allowing a modem that is transmitting at 75 bps to initiate a "turnaround" procedure so it can begin transmitting data at 1200/600 bps and receiving data at 75 bps. The modem is defined as being in V.23 master mode if it is transmitting at 75 bps and as being in slave mode if it is transmitting at 1200/600 bps.

Modem in Master Mode

To perform a direct turnaround once a modem connection is established, the master host goes into online command mode by sending an escape command (Escape pin activation, TIES, or ninth bit escape) to the master modem.

NOTE: The host can initiate a turnaround only if the CC-2401 is the master.

The host then sends the ATRO command to the CC-2401 to initiate a V.23 turnaround and return to online data mode.

The CC-2401 then changes its carrier frequency from 390 Hz to 1300 Hz) and wait to detect a 390 Hz carrier for 440 ms. If the modem detects more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it echoes the "c" response. If the modem does not detect more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it hangs up and echoes the "N" (no carrier) character as a response.

Modem in Slave Mode

Enable Slave mode by configuring GPIO4 and INT# (SE2[7:6][GPIO4] = 11). The CC-2401 performs a reverse turnaround when it detects a carrier drop longer than 20 ms. The CC-2401 then reverses and waits to detect a 1300 Hz carrier for 400 ms. If the CC-2401 detects more than 40 ms of a 1300 Hz carrier in a time window of 400 ms, it sets the S09[7] bit and the next character echoed by the CC-2401 is a "v".

If the CC-2401 doe not detect more than 40 ms of the 1300 Hz carrier in a time window of 400 ms, it reverses again and waits to detect a 390 Hz carrier for 440 ms. Then if the CC-2401 detects more than 40 ms of a 390 Hz carrier in a time window of 220 ms, it sets the S09[7] bit, and the CC-2401 echoes a "c".

At this point, if the CC-2401 does not detect more than 40 ms of the 390 Hz carrier in a time window of 440 ms, it hangs up, sets the S09[7] bit, and the CC-2401 echoes a "N" (no carrier).

Successful completion of a turnaround procedure in master or slave mode automatically updates S07[4](V23T) and S07[5] (V23R) to indicate the new status of the V.23 connection.

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To avoid using the INT# pin, the host may also be notified of the INT# condition using the 9-bit data mode. Setting S15[0] (NBE) = 1 and S0C[3] (9BF) = 0_b configures the ninth bit on the CC-2401 TXD path to function exactly as the INT# pin has been described.

V.42 HDLC Operation

The CC-2401 supports V.42 through hardware HDLC framing in all modem data modes. Frame packing and unpacking including opening and closing flag generation and detection, CRC computation and checking, zero insertion and deletion, and modem data transmission and reception are all performed by the CC-2401. V.42 error correction and V.42bis data compression must be performed by the host.

The digital link interface in this mode uses the same UART interface (8-bit data mode and 9-bit data formats) as in the asynchronous modes, and the ninth data bit may be used as an escape by setting S15[0](NBE) = 1. When using HDLC in 9-bit data mode, if the ninth bit is not used as an escape, it is ignored.

To use the HDLC feature on the CC-2401, the host must enable HDLC operation by setting S13[1](HDEN) = 1. The host may initiate the call or answer the call using either the "ATDT#", the "ATA" command or the auto answer mode. Auto answer mode is implemented by setting register S00 (NR) to a non-zero value. When the call is connected, a "c", "d" or a "v" result is echoed to the host controller. The host may now send and receive data across the UART using either the 8 or 9 bit data formats with flow control.

Once in this state, the CC-2401 begins framing data into the HDLC format. On the transmit side, if no data is available from the host, the HDLC flag pattern is sent repeatedly. When data is available, the CC-2401 computes the CRC code throughout the frame, and the data is sent with the HDLC zero-bit insertion algorithm.

HDLC flow control operates in a similar manner to normal asynchronous flow control across the UART. To operate flow control using the CTS pin to indicate when the CC-2401 is ready to accept a character, a DTE rate higher than the line rate should be selected. The method of transmitting HDLC frames is as follows:

1. After the call is connected, the host should begin sending the frame data to the CC-2401 using the CTS# flow control to ensure data synchronicity.
2. When the frame is complete, the host should simply stop sending data to the CC-2401. Since the CC-2401 does not yet recognize the end of frame, it expects an extra byte and asserts CTS. If CTS is used to cause a host interrupt, this final interrupt should be ignored by the host.
3. When the CC-2401 is ready to send the next byte, if it has not yet received any data from the host, it recognizes this as an end of frame, raises CTS, calculates the final CRC code, transmits the code and begins transmitting stop flags.
4. After transmitting the first stop flag, the CC-2401 lowers CTS indicating that it is ready to receive the next frame from the host. At this point, the process begins again at step 1.

The method for receiving HDLC frames follows:

1. After the call is connected, the CC-2401 searches for flag data. Once the first non flag word is detected, the CRC is continuously computed and the data is sent across the UART to the host after removing the HDLC zero-bit insertion. The DTE rate of the host must be at least as high as that of data transmission. HDLC mode only works with 8 bit data words; the ninth bit is used only for escape on TXD and end of frame received (EOFR) on RXD.
2. When the CC-2401 detects the stop flag, it sends the last data word in the frame as well as the two CRC bytes and determine if the CRC checksum matches. Thus, the last two bytes are not frame data but are the CRC bytes, which can be discarded by the host. If the checksum

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matches, the CC-2401 sends “G” (good). If the checksum does not match, the CC-2401 sends “e” (error). In addition, if the CC-2401 detects an abort (seven or more contiguous ones), it sends an “A”. When the “G”, “e”, or “A” (referred to as a frame result word) is sent, the CC-2401 raises the EOFR (end of frame receive) pin. The GPIO1 pin must be configured as EOFR by setting SE4[3](GPE) = 1. In addition to using the EOFR pin to indicate that the byte is a frame result word, if in 9 bit data mode, (set S15[0] (NBE) = 1), the ninth bit is raised if the byte is a frame result word. To program this mode, set S0C[3] (9BF) = 1 and SE0[3] (ND) = 1.

3. When the next frame of data is detected, EOFR is lowered and the process repeats with step 1.

When receiving HDLC frames, the host begins receiving data asynchronously from the CC-2401. When each byte is received, the host should check the EOFR pin (or the ninth data bit). If the EOFR pin (or ninth data bit) is low, the data is valid frame data. If the EOFR pin (or ninth bit) is high, the data is a frame result word.

Fast Connect

In modem applications that require fast connection times, it is possible to reduce the length of the handshake. Additional modem handshaking control can be adjusted through the registers shown in the following table. These registers are most useful if the user has control of both the originating and answering modems. When the fast connect settings are used, there may be unintended data received initially. The host must tolerate these bytes.

Register	Name	Function	Units	Default	Fast Connect
S1E	TATL	Transmit Answer Tone Length	1 s	0x03	00
S1F	ATTD	Answer Ton to Transmit Delay	5/3 ms	0x2D	00
S20	UNL	Unscrambled Ones Length-V.22	5/3 ms	0x5D	00
S21	TSOD	Transmit Scrambled Ones Delay – V.22	53.3 ms	0x09	00
S22	TSOL	Transmit Scrambled Ones Length – V.22	5/3 ms	0xA2	00
S23	VDDL	V.22/22b Data Delay Low	5/3 ms	0xCB	00
S24	VDDH	V.22/22b Data Delay High	(256) 5/3 ms	0x08	00
S34	TASL	Answer Tone Length (only used in S1E[TATL] = 0x00)	5/3 ms	0x5A	F0
S35	RSOL	Receive V.22 Scrambled Ones Length	5/3 ms	0xA2	00

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AT Command Set

The CC-2401 provides several vital functions including AT command parsing, DAA control, connect sequence control, DCE protocol control, intrusion detection, parallel phone off-hook detection, escape control, caller ID control and formatting, ring detect, DTMF control, call progress monitoring, and HDLC framing. The controller uses AT (Attention) commands and S-Registers to configure and control the modem.

The modem has two modes of operation: Command mode and data mode. The CC-2401 is asynchronous in both modes. At power up, after a reset, before a connection to another modem is made, after a connection is dropped (hang up or lost) and during an escape sequence out of data mode (ESC pin, "+++" or other break), the modem is in command mode.

The CC-2401 supports a subset of the typical modem AT command set since it is intended for use with a dedicated microcontroller instead of general terminal applications. AT commands begin with the letters "AT" and are followed directly (no space) by the command. All commands are case sensitive. All AT commands must be entered in upper case including AT. The exceptions are w, r, m, q and z (wakeup on ring).

AT commands can be divided into two groups: Control commands and configuration commands. Control commands, such as ATD, cause the modem to perform an action. The value of this type of command is changed at a particular time to perform a particular action.

Configuration commands change modem characteristics until they are modified or reversed by a subsequent configuration command or the modem is reset. Modem configuration status can be determined with the use of "ATSR?" (followed by a carriage return), where "R" is the two character hexadecimal address of an S-register.

A command line is defined as a string of characters starting with "AT" and ending with an end of line character <CR> (13 decimal). Command lines may contain several commands one after the other. If there are no characters between "AT" and <CR>, the modem responds with a "O" after the carriage return.

Command Line Execution

The characters in a command line are executed one at a time. Unexpected command characters are ignored, but unexpected data characters may be interpreted incorrectly.

After the modem has executed a command line, the result code corresponding to the last command executed is returned to the terminal or host. To echo command line characters, set the CC-2401 to echo mode using the E1 command. All numeric arguments, including the address and value of an S-register, are in hexadecimal format and two digits must always be entered.

<CR> End Of Line Character

This character is typed to end a command line. The value of the <CR> character is 13 decimal (the ASCII carriage return character). When the modem detects the carriage return, it executes the commands in the command line.

Note: Commands that do not require a response are executed immediately and do not need a <CR>.

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Command	Function
A	Answer line immediately with modem
DT#	Tone dial number
DP#	Pulse dial number
E	Local echo on/off
H0	Go on hook (hang up)
H1	Go off hook
I	Chip revision
:I	Interrupt read and clear
M	Speaker control options
O	Return online
RO	V.23 reverse
S	Read/write S-Registers
w##	Write S-Register in binary
r#	Read S-Register in binary
m#	Monitor S-Register in binary
q#	Read S-Register in binary
V0	Result code with no carriage return
V1	Result code with added carriage returns
Z	Software reset
z	Wakeup on ring

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AT Command Set Description

A Answer

The "A" command makes the modem go off hook and respond to an incoming call. This command is to be executed after the CC-2401 has indicated a ring has occurred. The modem indicates an incoming ring by sending an "R" to the UART.

This command is aborted if any other character is transmitted to the modem before the answer process is completed. Auto answer mode is entered by setting S00 (NR) to a non-zero value. NR indicates the number of rings before answering the line. After answering, the modem communicates by whatever protocol has been determined via the modem control registers in S07 (MF1). If no transmit charier signal is received from the calling modem within the time specified in S39 (CDT), the modem hangs up and enters the idle state.

D Dial
DT# Tone Dial Number
DP# Pulse Dial Number

The D commands cause the modem to dial the specified telephone number in the string following the command. The ATH1 command can be used to go off hook without detecting a dial tone or dialing.

The dial string must contain only the digits "0-9, "*", "#", "A", "B", "C", "D", or the modifiers ";", "/", or ",". A "," causes a two second delay (added to the spacing value in S04) in dialing. "/" causes a 125 ms delay in dialing (added to the spacing value in S04). The ";" returns the device to command mode after dialing and must be the last character.

If any character is received by the CC-2401 between the ATDT#<CR> command and when the connection is made ("c" or "d" is echoed), the extra character is interpreted as an abort and the CC-2401 returns to command mode ready to accept AT commands. A line feed character immediately following the <CR> is treated as an extra character and aborts the call.

If the modem does not have to dial (ATDT<CR> with no dial string), the modem assumes the call was manually established and attempts to make a connection.

Automatic Tone/Pulse Dialing

The CC-2401 can be configured to attempt DTMF dialing and automatically revert to pulse dialing if it determines that the line is not DTMF-capable.

For example, using 12345 as the number to be dialed, it is normally accomplished through either the ATDT12345 or ATDP12345 command. In the force pulse dialing mode of operation, the following string should be issued:

```
ATDT1,p12345
```

If the result code is a "t", the dialing was accomplished using DTMF dialing. If the result code is "tt", the dialing was accomplished using pulse dialing.

In the above example, the CC-2401 dials the first digit "1" using DTMF. The "," is used to pause in order to ensure that the central office has had time to accept the DTMF digit "1". When the CC-2401 processes the "p" command, it attempts to detect a dial tone. If a dial tone is detected, the DTMF digit "1" was not effective, hence, the line does not support DTMF dialing. Conversely, if the dial tone is not detected, the DTMF digit "1" was effective, and the line supports DTMF dialing. The character after the "p" may or may not be dialed depending on whether the DTMF digit "1" was effective or not. If the "1" was effective, the character after the "p" is skipped. The next DTMF digit

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to be dialed is “2”. Subsequent digits are all DTMF. If the “1” was not effective, the first character after the “p” (the “1”) is pulse dialed, and subsequent digits are all pulse dialed.

E Command Line Echo
Tells the CC-2401 whether or not to echo characters sent from the terminal.

E0
Does not echo characters sent from the terminal

E1
Echoes characters sent from the terminal.

H0 Hangup
Hang up and go into command mode.

H1 Off hook
Go off hook.

I Chip Identification
This command returns the chip revision code of the chipset. (A, B, C, etc).

I6
Displays the modem model number “2401”

:I Interrupt Read
Reports the contents of the interrupt status register (S09). The WOR, PPD, NLD, RI, OCD and REV bits are also cleared and the INT pin is deactivated.

M Speaker On/Off Options
These options are used to control the AOUT pin for use with a speaker.

M0
Speaker always off.

M1
Speaker on until carrier established.

M2
Speaker always on.

M3
Speaker on after last digit dialed, off at carrier detect.

O Return to Online Mode
This command returns the modem to online mode. It is used to return to data mode after an escape sequence to resume communications with the remote modem.

RO Turn-Around
This command initiates a V.23 “direct turnaround” sequence and returns online.

S Register Control

SR=N
Writes an S-register. This command writes the value “N” to the S-register specified by “R”. “R” is a hexadecimal number and “N” must also be a hexadecimal number from 00-FF. This command does not wait for a carriage return <CR> before taking effect. Two digits must always be entered for both “R” and “N”.

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SR?
Read an S-register. This command causes the CC-2401 to return the value of the S-register specified by R in hex format. R must be a hexadecimal number. Two digits must always be entered for "R".

w## **Write S-Register in Binary**
This command writes a register in binary format. The first byte following the "w" is the address in binary format and the second byte is the data in binary format. This is a faster method to write registers than the "SR=N" command and is recommended for use by a host controller.

r# **Read S-Register in Binary**
This command reads a register in binary format. The byte following the "r" is the address in binary format. The modem returns the contents of this register in binary format. This is a faster method to read registers than the "SR?" command and is recommended for use by a host controller.

rm# **Monitor S-Register in Binary**
This command monitors a register in binary format. The byte following the "m" is the address in binary. The CC-2401 constantly transmits the contents of the register at the set baud rate until a new byte is transmitted to the device. The new byte is ignored and viewed as a stop command. The modem result codes should be disabled before using this command.

q# **Read S-Register in Binary**
This command is the same as the r# command. The response from the CC-2401 is formatted as 0x55 followed by the contents of the register in binary. This guarantees that the register contents are always preceded by 0x66 and allows the result codes to remain enabled.

V **Result Code Options**
V0
Result codes reported according to Table 14. <SC>
V1
Result codes reported with an additional carriage return and line feeds (default).

Z **Software Reset**
This command initiates a software reset causing all registers, except E0 to default to their powerup value.

z **Wakeup on Ring (lower case "z")**
The CC-2401 enters a low power mode. In this mode, only the line side of the modem is functional. An incoming ring signal or line transient causes the modem to power up and send a "R" to the UART. Any other character received on the RXD pin also causes the modem to exit the wakeup on ring state. Return from wake on ring cal also be set to trigger the INT# pin by setting S08[6] (WORM) = 1.

Alarm Industry AT Commands

The CC-2401 supports a complete set of commands necessary for making connections in security industry systems. The CC-2401 is configurable in two modes for these applications. The first mode uses DTMF messaging and is selected with the "!1" command. The second mode uses FSK transmit with a tone acknowledgement and is selected by "!2".

The following are a few general comments about the use of "!" commands. Specific details for each command are given below. The first instance of the "!" must be on the same line as the ATDT or ATDP command. DRT must be set to data mode (SE4[5:4](DRT) = 0_b) before attempting to send tones after a "!" command. The three data-mode escape sequence ("+++", "escape" pin and "ninth-

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bit") only function in "!2" mode. However, using the "+++" or "ninth-bit" is not recommended because characters could be sent to and misinterpreted by the remote modem. Only the "escape pin" <SC> is recommended for use in the "!2" mode. The "!1" mode has a special escape provision described below. The AT commands for Alarm Industry applications are described in the following table.

Command	Function
!1	Dial and switch to DTMF security mode
!2	Dial and switch to "SIA Format"
X1	SIA half-duplex mode search
X2	SIA half-duplex return online as transmitter
X3	SIA half-duplex return online as receiver

!1
Dial number and follow the DTMF security protocol. The format for this command is as follows:

ATDT<phone number>!1<message 1><CR>
K
!<message 2><CR>
K
!<message 3><CR>
K
K
!<message n><CR>

The modem dials the phone number and returns "r" (ring), "b" (busy), and "c" (connect) as appropriate. "c" returns only after the modem detects the Handshake Tone. After a 250 ms delay, the modem sends the DTMF tones containing the first message data and listens for a Kissoff Tone. If a Kissoff Tone shorter than or equal to the value stored in S36(KTL)(default = 1 second) is detected, the CC-2401 echoes a "K". A "k" is sent if the length of the Kissoff Tone is longer than the S36(KTL) value. The controller can then send the next message. All messages must be preceded by a "!" and followed by a <CR> and received by the CC-2401 within 250 ms after the "K" is echoed. Setting S0C[0](MCH) = 1 causes a "." to be echoed when the DTMF tone is turned on and a "/" character to be echoed when the DTMF tone is turned off. This helps the host monitor the status of the message being sent. The previous message can be resent if the host responds with a "-" after the CC-2401 echoes a "K". Any character other than a "!" or a "~" sent to the modem immediately after the "K" causes the modem to escape to the command mode and remain off hook. Any character except "!" and "~" sent during the transmission of a message causes the message to be aborted and the modem to return to command mode.

If the Kissoff Tone is not received within 1.25 seconds, the modem echoes a "^". A "~" from the host causes the last message to be resent. Any character other than a "!" or a "~" sent to the modem immediately after the "^" causes the modem to escape to command mode and remain off hook.

!2
Dial the number and follow the "SIA Format" protocol for Alarm System Communications.

The modem dials the phone number and echoes "r" (ring), "b" (busy), and "c" (connect) as appropriate. "c" echoes only after the CC-2401 detects the Handshake Tone and the speed synchronization signal is sent. The signaling is at 300 bps, half-duplex FSK. The host can send

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the first SIA block after the “c” is received. Once the block is transmitted, the modem can monitor for the acknowledge tone by completing the following sequence:

1. Place the CC-2501 in command mode by pulsing the ESCAPE pin. The “+++” and “ninth-bit” escape modes operate in the “!2” mode but are not recommended because they can send unwanted characters to the remote modem.
2. Issue the “ATX1” command to turn the modem transmitter off and begin monitoring for the acknowledgement tones.
3. Monitor for a positive (negative) acknowledgement “P” (“N”) after the tone has been detected for at least 400 ms.
4. The modem, still in command mode, can be placed online as a transmitter by issuing the “ATX2” command or a receiver by issuing the “ATX3” command. If tonal acknowledgement is not used, the host can toggle the ESCAPE pin to place the CC-2401 in command mode and issue an “ATX2” or an “ATX3” command to reverse data direction.

This sequence can be repeated for long messages.

Modem Result Codes and Call Progress

The following table shows the modem result codes that can be used in call progress monitoring. All result codes are a single character to speed up communication and ease host processing.

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Command	Function
a	British Telecom Caller ID Idle Tone Alert Detected
b	Busy Tone Detected
c	Connect
d	Connect 1200 bps (when programmed as V.22bis modem)
f	Hookswitch Flash or Battery Reversal Detected
H	Modem Automatically Hanging Up in !2, !1.
I	Intrusion Completed (parallel phone back on hook)
i	Intrusion Detected (parallel phone off hook and on the line)
K	Kissoff Tone Detected
k	Contact ID Kissoff Tone too long (!1)
L	Phone Line Detected
l	No Phone Line Detected
m	Caller ID Mark Signal Detected
N	No Carrier Detected
n	No Dial tone (time-out set by CW[S02])
O	Modem OK Response
R	Incoming Ring Signal Detected
r	Ringback Tone Detected
t	Dial Tone
v	Connect 75 bps TX (V.23 originate only)
x	Overcurrent State Detected After and Off Hook Event
^	Kissoff tone detection required
.	Dialing Complete

Automatic Call Progress Detection

The CC-2401 has the ability to detect dial, busy and ringback tones automatically. The following is a description of the algorithms that have been implemented for these three tones.

- **Dial Tone.** The dial tone detector looks for a dial tone after going off hook and before dialing is initiated. This can be bypassed by enabling blind dialing (set S07[6](BD) = 1). After going off hook, the modem waits the number of seconds in S01 (DW) before searching for the dial tone. In order for a dial tone to be detected, it must be present for the length of time programmed in S1C (DTT). Once the dial tone is detected, dialing commences. If a dial tone is not detected within the time programmed in S02 (CW), the CC-2401 hangs up and returns an “n” to the user.
- **Busy/Ringback Tone**. After dialing is completed, the CC-2401 monitors for Busy/Ringback and modem answer tones. The busy and ringback tone detectors both use the call progress energy detector. The registers that set the cadence for busy and ringback are listed in the following table.

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Register	Name	Function	Units
S16	BTON	Busy tone on time	10 ms
S17	BTOF	Busy tone off time	10 ms
S18	BTOD	Busy tone delta time	10 ms
S19	RTON	Ringback tone on time	53.333 ms
S1A	RTOF	Ringback tone off time	53.333 ms
S1B	RTOD	Ringback tone Delta time	53.333 ms

Manual Call Progress Detection

Because other call progress tones beyond those described above may exist, the CC-2401 supports manual call progress. This requires the host to read and write the low-level DSP registers and may require realtime control by the host. Manual call progress may be required for detection of application specific ringback, dial tone and busy signals. The section on DSP level control should be read before attempting manual call progress detection.

The call progress biquad filters can be programmed to have a custom frequency response and detection level.

Four dedicated user defined frequency detectors can be programmed to search for individual tones. The four detectors have center frequencies that can be set by registers UDFD1-4. SE5[6][TDET] [SE8 = 0x02] Read Only Definition can be monitored, along with TONE, to detect energy at these user defined frequencies. The default trip-threshold for UDFD1-4 is -43 dBm but can be modified with register UDFSL.

By issuing the “ATDT;” command, the modem goes off hook and returns to command mode. The user can then put the DSP into call progress monitoring by first setting SE8 = 0x02. Next, set Se5(DSP2) = 0x00 so no tones are transmitted, and set SE6 (DSP3) to the appropriate code, depending on which types of tones are to be detected.

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Global Ringer and Busy Tone Cadence Settings

Country	RTON	RTOF	RTOD	BTON	BTOF	STOD
	S18	S1A	S1B	S16	S17	S18
Australia	0x07	0x03	0x01	0x25	0x25	0x04
Austria	0x12	0x5D	0x0A	0x1E	0x1E	0x03
Belgium	0x12	0x38	0x06	0x32	0x32	0x05
Brazil	0x12	0x4B	0x08	0x19	0x19	0x03
Bulgaria	0x12	0x4B	0x08	0x14	0x32	0x05
China	0x12	0x4B	0x08	0x23	0x23	0x04
Cyprus	0x1C	0x38	0x06	0x32	0x32	0x05
Czech Republic	0x12	0x4B	0x08	0x18	0x24	0x0A
Denmark	0x0E	0x8C	0x0F	0x19	0x19	0x03
Finland	0x0E	0x5D	0x0A	0x1E	0x1E	0x03
France	0x1C	0x41	0x07	0x32	0x32	0x05
Germany	0x12	0x4B	0x08	0x32	0x32	0x05
Great Britain	0x07	0x03	0x01	0x25	0x25	0x04
Greece	0x12	0x4B	0x08	0x1E	0x1E	0x03
Hong Kong, New Zealand	0x07	0x03	0x01	0x32	0x32	0x05
Hungary	0x17	0x46	0x0F	0x1E	0x1E	0x03
Iceland	0x16	0x58	0x09	0x19	0x19	0x03
India	0x07	0x03	0x01	0x4B	0x4B	0x08
Ireland	0x07	0x03	0x01	0x32	0x32	0x05
Italy, Netherlands, Norway, Thailand, Switzerland, Israel	0x12	0x4B	0x08	0x32	0x32	0x05
Japan, Korea	0x12	0x25	0x04	0x32	0x32	0x05
Luxembourg	0x12	0x4B	0x08	0x30	0x30	0x05
Malaysia	0x07	0x03	0x01	0x23	0x41	0x07
Malta	0x00	0x00	0x00	0x00	0x00	0x00
Mexico	0x12	0x4B	0x08	0x19	0x19	0x03
Poland	0x12	0x4B	0x10	0x32	0x32	0x05
Portugal	0x12	0x5D	0x0A	0x32	0x32	0x05
Singapore	0x07	0x03	0x01	0x4B	0x4B	0x08
Spain	0x1C	0x38	0x06	0x14	0x14	0x02
Sweden	0x12	0x5D	0x0A	0x19	0x19	0x03
Taiwan	0x12	0x25	0x04	0x32	0x32	0x05
U.S., Canada (default)	0x25	0x4B	0x08	0x32	0x32	0x05

At this point, users can program their own algorithm to monitor the detected tones. If the host dials, it should do so by blind dialing, setting the dial timeout S01 (DW) to zero seconds and issuing an “ATDT<Phone Number>;<CR>”. This causes the modem to dial and return to command mode.

Once the host has detected an answer tone using manual call progress, the host should immediately execute the “ATDT” command in order to make a connection. This causes the CC-2401 to search for the modem answer tone and begin the correct connect sequence.

In manual call progress, the DSP can be programmed to detect specific tones. The result of the detection is reported in SE5 (SE8 = 0x2) as described above. The output is priority encoded such that if multiple tones are detected, the one with the highest priority whose detection is also enabled is reported .

In manual call progress, the modem can be programmed to generate specific tones. For example, setting SE5[2:0](TONC) = 110b generates the user defined tone (as indicated by UFRQ).

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DTMF Code	Keyboard Equivalent	Contact ID Digit	Tones	
			Low	High
0	0	0	941	1336
1	1	1	697	1209
2	2	2	697	1336
3	3	3	697	1447
4	4	4	770	1209
5	5	5	770	1336
6	6	6	770	1477
7	7	7	852	1209
8	8	8	852	1336
9	9	9	852	1447
10	D	-	941	1633
11	*	B	941	1209
12	#	C	941	1447
13	A	D	697	1633
14	B	E	770	1633
15	C	F	852	1633

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Low Level DSP Control

Although not necessary for most applications, the low-level control functions are available for very specific applications requiring direct DSP control.

DSP registers

Several DSP registers are accessible through the CC-2401 controller via S-registers. SE5, SE6 and SE8 are used to write data to specific DSP registers and read status. SE8 defines the function of SE5 and SE6 depending on whether they are being written or read from. Care must be exercised when writing to DSP registers. DSP registers can only be written while the CC-2401 is on hook and in command mode. Writing to any register address not listed or writing out of range values is likely to cause the DSP to exhibit unpredictable behavior.

The DSP register address is 16 bit, and the DSP data field is 14 bits wide. DSP register addresses and data are written in hexadecimal. To write a value to a DSP register the register address is written and then the data. When SE8 = 0x00, SE5(DADL) is written with the low bits [7:0] of the DSP register address, and SE6(DADH) is written with the high bits ([15:8]) of the data word corresponding to the previously written address.

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Low Level DSP Parameters

DSP Reg. Addr.	Name	Description	Function	Default (dec)
0x0002	SMTL	DAA modem full-scale transmit level, default =-10 dBm	Level = $20\log_{10}$ (XTML/4096) -10 dBm	4096
0x0003	DTML	DTMF high-tone transmit level, default = -5.5 dBm	Level=$20\log_{10}$ (DTML/4868) -5.5 dBm	4868
0x0004	DTMT	DTMF twist ratio (low/high), Default = -2 dBm.	Level = $20\log_{10}$ (DTMT/3277) – 2 dB	3277
0x0005	UFRQ	User-defined transmit tone frequency. See register SE5 (SE8=0x02(Write Only)).	f = (9600/512) UFRQ (Hz)	91
0x0006	CPDL	Call progress detect level, default = -43 dBm	Level = $20\log_{10}$ (4096/CPDL) -43 dBm	4096
0x0007	UDFD1	User-defined frequency detector 1. Center frequency for detector 1.	UDFD1 = 8192 cos (2π f/9600)	4987
0x0008	UDFD2	User-defined frequency detector 2. Center frequency for detector 2.	UDFD2 = 8192 cos (2π f/9600)	536
0x0009	UDFD3	User-defined frequency detector 3. Center frequency for detector 3.	UDFD3 = 8192 cos (2π f/9600)	4987
0x000A	UDFD4	User-defined frequency detector 4. Center frequency for detector 4.	UDFD4 = 8192 cos (2π f/9600)	536
0x000B	TGNL	Tone generation level associated with TONC (SE5(SE8 = 0x02) Write Only Definition), default = -10 dBm.	Level = $20\log_{10}$ (TGNL/2896) - 10 dBm	2896
0x000E	UDFSL	Sensitivity setting for UDFD1-4 detectors, default = -43 dBm.	Sensitivity = $10\log_{10}$ (UDFSL/4096) -43 dBm	4096
0x0024	CONL	Carrier ON level. Carrier is valid once it reaches this level.	Level = $20\log_{10}$ (2620/CONL) – 43 dBm.	
0x0025	COFL	Carrier OFF level. Carrier is invalid once it falls below this level.	Level = $20\log_{10}$(3300/COFL) – 45.5 dBm.	3300
0x0026	AONL	Answer ON level. Answer tone is valid once it reaches this level.	Level = $10\log_{10}$(AONL/107) – 43 dBm.	67
0x0027	AOFL	Answer OFF level. Answer tone is invalid once it falls below this level.	Level = $10\log_{10}$(AOFL/58) – 45.5 dBm.	37

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SE8		SE6		SE5	
	R/W	**Name**	**Description**	**Name**	**Description**
0x00	W	DADH	DSP register address bits [15:8]	DADL	DSP Register address bits [7:0]
0x01	W	DDH	DSP register data bits [15:8]	DDL	DSP register data bits [7:0]
0x02	R			DSP1	7 = DSP data available 6 = Tone detected 5 = Reversed 4:0 = Tone type
0x02	W	DSP3	7 = Enable squaring function 6 = Call progress cascade disable 5 = Reserved 4 = User tone 3 and 4 reporting 3 = User tone 1 and 2 reporting 2 = V.23 tone reporting 1 = Answer tone reporting 0 = DTMF tone reporting	DSP2	7 = Reserved 6:3 = DTMF tone to transmit 2:0 = Tone type

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Call Progress Filters

The programmable call progress filter coefficients are located in DSP address locations 0x0010 through 0x0023. There are two independent 4th order filters, A and B, each consisting of two biquads, for a total of 20 coefficients. Coefficients are 14 bits (-8192 to 8191) and are interpreted as, for example, b0 = value/4096, thus giving a floating point value of approximately -2.0 to 2.0. Output of each biquad is calculated:

w[x] = k0 x x[n] + a1 x w[n - 1] + a2 x w[n - 2]

y[n] = w[n] + b1 x w[n - 1] + b2 x w[n - 2]

The output of the filters is input to an energy detector and then compared to a fixed threshold with hysteresis (CPDL). Defaults shown are a bandpass filter from 290-630 Hz (03 dB). These registers are located in the DSP and must be written in the same manner described in "DSP Registers".

The filters may be configured in either parallel or cascade through SE6[6] (CPCD) with SE8 = 0x02, and the output filter B may be squared by selecting SE6[7] (CPSQ) = 1.

Call Progress Filters

DSP Register Address	Coefficient	Default (dec)
0x0010	A1_k0	256
0x0011	A1_b1	-8184
0x0012	A1_b2	4096
0x0013	A1_a1	7737
0x0014	A1_a2	-3801
0x0015	A2_k0	1236
0x0016	A2_b1	133
0x0017	A2_b2	4096
0x0018	A2_a1	7109
0x0019	A2_a2	-3565
0x001A	B1_k0	256
0x001B	B1_b1	-8184
0x001C	B1_b2	4096
0x001D	B1_a1	7737
0x001E	B1_a2	-3801
0x001F	B2_k0	1236
0x0020	B2_b1	133
0x0021	B2_b2	4096
0x0022	B2_a1	7109
0x0023	B2_a2	-3565

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S Registers

Any register not documented here is reserved and should not be written. Bold selection in the bit mapped registers indicates default values.

S-Register Summary

"S" Register	Register Address (hex)	Name	Function	Reset
S00	0x00	NR	Number of rings before answer; 0 suppresses auto answer.	0x00
S01	0x01	DW	Number of seconds modem waits before dialing after going off-hook (maximum of 109 seconds).	0x02
S02	0x02	CW	Number of seconds modem waits for a dial tone before hang-up added to time specified by DW (maximum of 109 seconds).	0x03
S03	0x03	CLW	Duration that the modem waits (53.33 ms units) after loss of carrier before hanging up.	0x0E
S04	0x04	TD	Both duration and spacing (5/3 ms units) of DTMF dialed tones.	0x30
S05	0x05	OFFPD	Duration of off-hook time (5/3 ms units) for pulse dialing.	0x18
S06	0x06	ONPD	Duration of on-hook time (5/3 ms units) for pulse dialing	0x24
S07	0x07	MF1	This is a bit-mapped register*	0x06
S08	0x08	INTM	This is a bit-mapped register*	0x00
S09	0x09	INTS	This is a bit-mapped register*	0x00
S0C	0x0C	MF2	This is a bit-mapped register*	0x00
S0D	0x0D	MF3	This is a bit-mapped register*	0x00
S0E	0x0E	DIT	Pulse dialing interdigit time (10 ms units added to a minimum time of 64 ms).	0x46
S0F	0x0F	TEC	TIES escape character. Default is "+"	0x2B
S10	0x10	TDT	TIES delay time (53.33 ms units).	0x13
S11	0x11	OFHI	This is a bit-mapped register*	0x04
S12	0x12	ACL	Absolute Current Level. When S13[4](OFHD) = 0_b, ACL represents the absolute current threshold used by the off hook intrusion algorithm (1 mA units)	0x00
S13	0x13	MF4	This is a bit-mapped register*	0x10
S15	0x15	MLC	This is a bit-mapped register*	0x04
S16	0x16	BTON	Busy tone on. Time that the busy tone must be on (10 ms units) for busy tone detector.	0x32
S17	0x17	BTOF	Busy tone off. Time that the busy tone must be off (10 ms units) for busy tone detector	0x32
*__NOTE__: These registers are explained in detail in the following section.				

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S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
S18	0x18	BTOD	Busy tone delta time (10 ms units). A busy tone is detected to be valid if (BTON – BTOD < on time < BTON + BTOD) and (BTOF – BTOD < off time < BTOF + BTOD).	0x0F
S19	0x19	RTON	Ringback tone on. Time that the ringback tone must be on (53.333 ms units) for ringback tone detector.	0x26
S1A	0x1A	RTOF	Ringback tone off. Time that the ringback tone must be off (53.333 ms units) for ringback tone detector.	0x4B
S1B	0x1B	RTOD	Detector time delta (53.333 ms units). A ringback tone is determined to be valid if (RTON – RTOD < on time < RTON + RTOD) and (RTOF – RTOD < off time < RTOF + RTOD).	0x07
S1C	0x1C	DTT	Dial tone detect time. The time that the dial tone must be valid before being detected (10 ms units).	0x0A
S1E	0x1E	TATL	Transmit answer tone length. Answer tone length in seconds when answering a call (1 s units).	0x03
S1F	0x1F	ARM3	Answer tone to transmit delay. Delay between answer tone end and transmit data start (5/3 ms units).	0x2D
S20	0x20	UNL	Unscrambled ones length. Minimum length of time required for detection of unscrambled binary ones during V.22 handshaking by a calling modem (5/3 ms units).	0x5D
S21	0x21	TSOD	Transmit scrambled ones delay. Time between unscrambled binary one detection and scrambled binary one transmission by a call mode V.22 modem (53.3 ms units).	0x09
S22	0x22	TSOL	Transmit scrambled ones length. Length of time scrambled ones are sent by a call mode V.22 modem (5/3 ms units).	0xA2
S23	0x23	VDDL	V.22X data delay low. Delay between handshake complete and data connection for a V.22X call mode modem (5/3 ms units added to the time specified by VDDH).	0xCB
S24	0x24	VDDH	V.22X data delay high. Delay between handshake complete and data connection for a V.22X call mode modem (256 x 5/3 ms units added to the time specified by VDDL).	0x08
S25	0x25	SPTL	S1 pattern time length. Amount of time the unscrambled S1 pattern is sent by a call mode V.22bis modem (5/3 ms units).	0x3C
S26	0x26	VTSO	V.22bis 1200 bps scrambled ones length. Minimum length of time for transmission of 1200 bps scrambled binary ones by a call mode V.22bis modem after the end of pattern S1 detection (53.3 ms).	0x0C
S27	0x27	VTSOL	V.22bis 2400 bps scrambled ones length low. Minimum length of time for transmission of 2400 bps scrambled binary ones by a call mode V.22bis modem (5/3 ms units).	0x78
*__NOTE__: These registers are explained in detail in the following section.				

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S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
S28	0x28	VTSOH	V.22bis 2400 bps scrambled ones length high. Minimum length of time for transmission of 2400 bps scrambled binary ones by a call mode V.22bis modem (256 x 5/3 ms units added to the time specified by VTSOL).	0x08
S29	0x29	IS	Intrusion suspend. When S82[2:1](IB) = 10b, this register sets the length of time from when dialing begins that the off hook intrusion algorithm is blocked (suspended)(500 ms units).	0x00
S2A	0x2A	RSO	Receive scrambled ones V.22bis (2400 bps) length. Minimum length of time required for detection of scrambled binary ones during V.22bis handshaking by the answering modem after S1 pattern conclusion (5/3 ms units).	0xD2
S2B	0x2B	DTL	V.23 direct turnaround carrier length. Minimum length of time that a master mode V.23 modem must detect carrier when searching for a direct turnaround sequence (5/3 ms units).	0x18
S2C	0x2C	DTTO	V.23 direct turnaround timeout. Length of time that the modem searches for a direct turnaround carrier (5/3 ms units added to a minimum time of 426.66 ms).	0x08
S2D	0x2D	SDL	V.23 slave carrier detect loss. Minimum length of time that a slave mode V.23 modem must lose carrier before searching for a reverse turnaround sequence (5/3 ms units).	0x0C
S2E	0x2E	RTCT	V.23 reverse turnaround carrier timeout. Amount of time a slave mode V.23 modem searches for carriers during potential reverse turnaround sequences (5/3 ms units).	0xF0
S2F	0x2F	FCD	FSK connection delay low. Amount of time delay added between end of answer tone handshake and the actual modem connection for FSK modem connections (5/3 ms units).	0x3C
S30	0x30	FCDH	FSK connection delay high. Amount of time delay added between end of answer tone handshake and the actual modem connection for FSK modem connections (256 x 5/3 ms units).	0x00
S31	0x31	RATL	Receive answer tone length. Minimum length of time required for detection of a CCITT answer tone (5/3 ms units).	0x3C
S32	0x32	OCDT	The time after going off hook when the loop current sense bits are checked for overcurrent status (5/3 ms units).	0x0C
S34	0x34	TASL	Answer tone length when answering a call (5/3 ms units). This register is only used if TATL (1E) has a value of zero.	0x5A
S35	0x35	RSOL	Receive scrambled ones V.22 length (5/3 ms units). Minimum length of time that an originating V.22 (1200 bps) modem must detect 1200 bps scrambled ones during a V.22 handshake.	0xA2
S36	0x36	ARM1	Second kissoff tone detector length. The security modes, A1 and !1, echo a "k" if a kissoff tone longer than the value stored in SKDTL is detected (10 ms units).	0x30
* **NOTE**: These registers are explained in detail in the following section.				

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S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
S37	0x37	CRD	Carrier detect return. Minimum length of time that a carrier must return and be detected in order to be recognized after a carrier loss is detected (5/3 ms units).	0x20
S39	0x39	CDT	Carrier detect timeout. Amount of time modem waits for carrier detect before aborting a call (1 second units).	0x3C
S3A	0x3A	ATD	Delay between going off hook and answer tone generation when in answer mode (53.33 ms units).	0x29
S3B	0x3B	RP	Minimum number of consecutive ring pulses per ring burst.	0x03
S3C	0x3C	CIDG	This is a bit-mapped register*	0x01
S62	0x62	RC	This is a bit-mapped register*	0x41
S82	0x82	IST	This is a bit-mapped register*	0x08
SDB	0xDB	LVS	Line Voltage Status. Eight bit signed 2's complement number representing the tip-ring voltage. Each bit represents 1 volt. Polarity of the voltage is represented by the MSB (sign bit). 0000_0000 = Measured voltage is < 3V.	
SDF	0xDF	DGSR	This is a bit-mapped register*	0x0C
SE0	0xE0	CF1	This is a bit-mapped register*	0x22
SE1	0xE1	GPIO1	This is a bit-mapped register*	0x04
SE2	0xE2	GPIO2	This is a bit-mapped register*	0x00
SE3	0xE3	GPD	This is a bit-mapped register*	0x00
SE4	0xE4	CF5	This is a bit-mapped register*	0x00
SE5	0xE5	DADL	(SE8 = 0x00) Write only definition. DSP register address lower bits [7:0].*	0x00
SE5	0xE5	DDL	(SE8 = 0x01) Write only definition. DSP data word lower bits [7:0].*	0x00
SE5	0xE5	DSP1	(SE8 = 0x02) Read only definition. This is a bit-mapped register*	0x00
SE5	0xE5	DSP2	(SE8 = 0x02) Write only definition. This is a bit-mapped register*	0x00
SE6	0xE6	DADH	(SE8 = 0x00) Write only definition. DSP register address upper bits [15:8].	0x00
SE6	0xE6	DDH	(SE8 = 0x01) Write only definition. DSP data word upper bits [13:8].	0x00
SE6	0xE6	DSP3	(SE8 = 0x02) Write only definition. This is a bit-mapped register*	0x00
SE8	0xE8	DSPR4	Set the mode to define E5 and E6 for low level DSP control.	0x00
SEB	0xEB	TPD	This is a bit-mapped register*	0x00
SEC	0xEC	RV1	This is a bit-mapped register*	0x88
SED	0xED	RV2	This is a bit-mapped register*	0x19
SEE	0xEE	RV3	This is a bit-mapped register*	0x16
SF0	0xF0	DAA0	This is a bit-mapped register*	0x40
SF1	0xF1	DAA1	This is a bit-mapped register*	0x0C
SF2	0xF2	DAA2	This is a bit-mapped register*	0x00
SF3	0xF3	DAA3	Line current Status. 8 bit value returning the loop current. Each bit represents 1.1 mA of loop current. Accuracy is not guaranteed if the loop current is less than required for normal operation	0x00

*__NOTE__: These registers are explained in detail in the following section.

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S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
SF4	0xF4	DAA4	This is a bit-mapped register*	0x0F
SF5	0xF5	DAA5	This is a bit-mapped register*	0x00
SF6	0xF6	DAA6	This is a bit-mapped register*	0xF0
SF7	0xF7	DAA7	This is a bit-mapped register*	0x00
SF8	0xF8	DAA8	This is a bit-mapped register*	----
SF9	0xF9	DAA9	This is a bit-mapped register*	0x20
*__NOTE__: These registers are explained in detail in the following section.				

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Bit Mapped Register Summary

"S" Register	Register Address (hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Binary
S07	0x07	MF1		BD	V23R	V23T		BAUD	CCITT	FSK	0000_0110
S08	0x08	INTM	CDM	WORM	PPDM	NVDM	RIM	CIDM	OCDM	REVM	0000_0000
S09	0x09	INTS	CD	WOR	PPD	NVD	RI	CID	OCD	REV	0000_0000
S0C	0X0C	MF2	CDE	CIDM[1:0]			9BF	BDL	MLB		0000_0000
S0D	0x0D	MF3		RI	INTP	RBTS	HER	EHB	EHI	EHE	0000_0000
S11	0x11	OFHI					DCL[3:0]				0000_0100
S13	0x13	MF4		BTID		OFHD		CIDB	HDEN		0001_0000
S15	0x15	MLC	ATPRE	VCTE	FHGE	EHGE	STB	BDA[1:0]		NBE	0000_0100
S3C	0x3C	CIDG						CIDG[2:0]			0000_0100
S62	0x62	RC		OCR				IR	NLR	RR	0100_0001
S82	0x82	IST	IST[3:0]				LCLD	IB[1:0]			0000_1000
SDF	0xDF	DGSR		DGSR[6:0]							0000_1100
SE0	0xE0	CF1			ICTS		ND	SD[2:0]			0010_0010
SE1	0xE1	GPIO1							GPD5	GPIO5	0000_0000
SE2	0xE2	GPIO2	GPIO4[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]		0000_0000
SE3	0xE3	GPD					GPD4	GPD3	GPD2	GPD1	0000_0000
SE4	0xE4	CF5	NBCK	SBCK	DRT		GPE				0000_0000
SE5	0xE5	DSP1	DDAV	TDET		TONE[4:0]					0000_0000
SE5	0xE5	DSP2		DTM[3:0]				TONC[2:0]			0000_0000
SE6	0xE6	DSP3	CPSQ	CPCD		USEN2	USEN1	V23E	ANSE	DTMFE	0000_0000
SEB	0xEB	TPD					PDDE				0000_0000
SEC	0xEC	RVC1	RNGV	RDLY[2:0]			RCC[2:0]				1000_1000
SED	0xED	RVC2			RAS[5:0]						0001_1001
SEE	0xEE	RVC3	RTO[3:0]				RMX[3:0]				0001_0110
SF0	0xF0	DAA0	FOH[1:0]						LM[1:0]		0100_0000
SF1	0xF1	DAA1	BTE	PDN	PDL	LVFD		HBE			0000_1100
SF2	0xF2	DAA2					FDT				0000_0000

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Bit Mapped Register Summary

"S" Register	Register Address (hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Binary
S07	0x07	MF1		BD	V23R	V23T		BAUD	CCITT	FSK	0000_0110
S08	0x08	INTTM	CDM	WORM	PPDM	NVDM	RIM	CIDM	OCDM	REVM	0000_0000
S09	0x09	INTS	CD	WOR	PPD	NVD	RI	CID	OCD	REV	0000_0000
S0C	0x0C	MF2	CDE	CIDM[1:0]			9BF	BDL	MLB		0000_0000
S0D	0x0D	MF3		RI	INTP	RBTS	HER	EHB	EHI	EHE	0000_0000
S11	0x11	OFHI					DCL[3:0]				0000_0100
S13	0x13	MF4		BTID		OFHD		CIDB	HDEN		0001_0000
S15	0x15	MLC	ATPRE	VCTE	FHGE	EHGE	STB	BDA[1:0]		NBE	0000_0100
S3C	0x3C	CIDG						CIDG[2:0]			0000_0100
S62	0x62	RC		OCR				IR	NLR	RR	0100_0001
S82	0x82	IST	IST[3:0]				LCLD	IB[1:0]			0000_1000
SDF	0xDF	DGSR		DGSR[6:0]							0000_1100
SE0	0xE0	CF1			ICTS		ND	SD[2:0]			0010_0010
SE1	0xE1	GPIO1							GPD5	GPIO5	0000_0000
SE2	0xE2	GPIO2	GPIO4[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO[1:0]		0000_0000
SE3	0xE3	GPD					GPD4	GPD3	GPD2	GPD1	0000_0000
SE4	0xE4	CF5	NBCK	SBCK	DRT		GPE				0000_0000
SE5	0xE5	DSP1	DDAV	TDET		TONE[4:0]					0000_0000
SE5	0xE5	DSP2		DTM[3:0]				TONC[2:0]			0000_0000
SE6	0xE6	DSP3	CPSQ	CPCD		USEN2	USEN1	V23E	ANSE	DTMFE	0000_0000
SEB	0xEB	TPD					PDDE				0000_0000
SEC	0xEC	RVC1	RNGV	RDLY[2:0]			RCC[2:0]				1000_1000
SED	0xED	RVC2			RAS[5:0]						0001_1001
SEE	0xEE	RVC3	RTO[3:0]				RMX[3:0]				0001_0110
SF0	0xF0	DAA0	FOH[1:0]						LM[1:0]		0100_0000
SF1	0xF1	DAA1	BTE	PDN	PDL	LVFD		HBE			0000_1100
SF2	0xF2	DAA2					FDT				0000_0000
SF4	0xF4	DAA4					ARL[1:0]		ATL[1:0]		0000_1111
SF5	0xF5	DAA5			OHS[1:0]		ILIM	RZ		RT	0000_1000
SF6	0xF6	DAA6	MINI[1:0]		DCV[1:0]		ACT[3:0]				1111_0000
SF8	0xF8	DAA8	LRV[3:0]						DCR		----
SF9	0xF9	DAA9					BTD		ROV		0010_0000
SFC	0xFC	DAAFC	CTSM								0000_1111

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S07 (MF1), Modem Functions 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		BD	V23R	V23T		BAUD	CCITT	FSK
Type		R/W	R/W	R/W		R/W	R/W	R/W

Reset Settings = 0000_0110 (0x06)

Bit	Name	Function
7	Reserved	Read Returns zero.
6	BD	Blind Dialing **0 = Disable** 1 = Enabled (blind dialing occurs immediately after “ATDT#” command).
5	V23R	**V.23 Receive** V.23 75 bps send/600 (BAUD = 0) or 1200 (BAUD = 1) bps receive. **0 = Disable** 1 = Enable
4	V23T	**V.23 Transmit** V.23 600 (BAUD = 0) or 1200 (BAUD = 1) bps send/75 bps receive. **0 = Disable** 1 = Enable
3	Reserved	Read returns zero.
2	BAUD	**2400/1200 Baud Select** 2500/1200 baud select (V23R = 0 and V23T = 0) 0 = 1200 **1 = 2400** 600/1200 baud select (V23R = 1 and V23T = 1) 0 = 600 **1 = 1200**
1	CCITT	**CCITT/Bell Mode** 0 = Bell **1 = CCITT**
0	FSK	**300 bps FSK** **0 = Disable** 1 = Enable

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S08 (INTM), Interrupt Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CDM	WORM	PPDM	NVDM	RIM	CIDM	OCDM	REVM
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7	CDM	**Carrier Detect Mask** **0 = Change in CD does not affect INT.** 1 = A high to low transition in CD (S09, bit 7), which indicates loss of carrier, activates INT.
6	WORM	**Wake On Ring Mask** **0 = Change in CD does not affect INT** 1 = A low to high transition in WOR (S09, bit 6) activates INT.
5	PPDM	**Parallel Phone Line Detect Mask** **0 = Change in PPD does not affect INT.** 1 = A low to high transition in PPD (S09, bit 5) activates INT.
4	NVDM	**No Phone Line Detect Mask** **0 = Change in NLD does not affect INT.** 1 = A low to high transition in NLD (S09, bit 4) activates INT.
3	RIM	**Ring Indicator Mask** **0 = Change in RI does not affect INT.** 1 = A low to high transition (S09, bit 3) activates INT.
2	CIDM	**Caller ID Mask** **0 = Change in CID does not affect INT.** 1 = A low to high transition in CID (S09, bit 2) activates INT.
1	OCDM	**Overcurrent Detect Mask** **0 = Change in OCD does not affect INT.** 1 = A low to high transition in OCD (S09, bit 1) activates INT.
0	REVM	**V.23 Reversal Detect Mask** **0 = Change in REV does not affect INT.** 1 = A low to high transition in REV (S09, bit 0) activates INT.

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S09 (INTS), Interrupt Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CD	WOR	PPD	NVD	RI	CID	OCD	REV
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7	CD	**Carrier Detect (sticky).** Active high bit indicates carrier detected (equivalent to inverse of CD pin). Clears on :I read.
6	WOR	**Wake On Ring (sticky).** Wake on ring has occurred. Clears on :I read.
5	PPD	**Parallel Phone Detect (sticky).** No line phone detected since last off hook event. Clears on :I read.
4	NVD	**No Phone Line Detect (sticky).** No line phone detected. Clears on :I read.
3	RI	**Ring Indicator (sticky).** Active high bit when the CC-2401 is on hook. Indicates ring event has occurred. Clears on :I read.
2	CID	**Caller ID (sticky).** Caller ID preamble has been detected; data soon follows. Clears on :I read.
1	OCD	**Overcurrent Detect (sticky).** Overcurrent condition has occurred. Clears on :I read.
0	REV	**V.23 Reversal Detect (sticky).** V.23 reversal condition has occurred. Clears on :I read.

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S0C (MF2), Modem Functions 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CDE	CIDM[1:0]			9BF	BDL	MLB	
Type	R/W	R/W			R/W	R/W	R/W	

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7	CDE	**Carrier Detect Enable.** **0 = Disable.** 1 = Enable GPIO2 as an active low carrier detect pin (must also set SE2[3:2] [GPIO2] = 01).
6:5	CIDM[1:0]	**Caller ID Monitor.** **00 = Caller ID monitor disabled.** 01 = Caller ID monitor enabled. CC-2401 must detect channel seizure signal followed by marks in order to report caller ID data. (Normal Bellcore caller ID). 10 = Reserved. 11 = Caller ID monitor enabled. CC-2401 must only detect marks in order to report caller ID data.
4	Reserved	Read returns zero.
3	9BF	**Ninth Bit Function.** Only valid if the ninth bit escape is set S15[0] (NBE). **0 = Ninth bit equivalent to ALERT.** 1 = Ninth bit equivalent to HDLC EOFR.
2	BDL	**Blind Dialing.** **0 = Blind dialing disabled.** 1 = Enables blind dialing after dial timeout register S02 (CW) expires.
1	MLB	**Modem Loopback** **0 = Not swapped.** 1 = Swaps frequency bands in modem algorithm to do a loopback in a test mode.
0	Reserved	Read Returns zero.

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S0D (MF3), Modem Functions 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RI	INTP	RBTS	HER	EHB	EHI	EHE
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7	Reserved	**Read returns Zero**
6	RI	**Ring Indicator** Specifies the functionality of pin 36. **0 = Pin 36 functions as GPIO5 controlled by register SE1.** 1 = Pin 36 functions as RI#. RI# asserts during a ring and negates when no ring is present.
5	INP	**INT Polarity** Specifies the polarity of the INT function on pin 56. **0 = An interrupt forces pin 56 low.** 1 = An interrupt forces pin 56 high.
4	RBTS	**Ringback Tone Selector** Controls the unit step size for registers S19, S1A and S1B. **0 = 53.33 ms units. Necessary for detecting a ringback tone.** 1 = 10 ms units. Necessary for detecting a reorder tone.
3	EHR	**Enable Hangup on Reorder.** Modem is placed on hook if a ringback or reorder tone is detected (see S0D[4]. **0 = Disable.** 1 = Enable.
2	EHB	**Enable Hangup on Busy.** Modem is placed on hook if a busy signal is detected. **0 = Disable.** 1 = Enable.
1	EHI	**Enable Hangup on Intrusion.** Modem is placed on hook if parallel intrusion is detected. **0 = Disable.** 1 = Enable.
0	EHE	**Enable Hangup on Escape.** Modem is placed on hook if an ESC signal is detected. **0 = Disable.** 1 = Enable.

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S11 (OFHI), Off Hook Intrusion

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					DCL[3:0]			
Type					R/W			

Reset Settings = 0000_0100 (0x04)

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	DCL[3:0]	**Differential Current Level.** Differential current level to detect intrusion event (1 mA units).

S13 (MF3), Modem Functions 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		BTID		OFHD		CIDB	HDEN	
Type		R/W		R/W		R/W	R/W	

Reset Settings = 0001_0000 (0x10)

Bit	Name	Function
7	Reserved	**Read returns Zero**
6	BTID	**BT Caller ID Wetting Pulse.** **0 = Enable.** 1 = Disable.
5	Reserved	Read returns zero.
4	OFHD	**Off Hook Intrusion Detect Method.** 0 = Absolute. **1 = Differential.**
3	Reserved	Read returns zero.
2	CIDB	**Britis Telcom Caller ID Decode.** **0 = Disable.** 1 = Enable. When set, S0C[6:5] is overwritten by the modem as needed.
1	HDEN	**HDLC Framing.** **0 = Disable.** 1 = Enable.
0	Reserved	Read returns zero.

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S15 (MLC), Modem Link Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATPRE	VCTE	FHGE	EHGE	STB	BDA[1:0]		NBE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Settings = 0000_0100 (0x04)

Bit	Name	Function
7	ATPRE	**Answer Tone Phase Reversal.** **0 = Disable.** 1 = Enable answer tone phase reversal.
6	VCTE	**V.25 Calling Tone.** **0 = Disable.** 1 = Enable V.25 calling tone.
5	FHGE	**550 Hz Guardtone.** **0 = Disable.** 1 = Enable 550 Hz guardtone.
4	EHGE	**1800 Hz Guardtone.** **0 = Disable.** 1 = Enable 1800 Hz guardtone.
3	STB	**Stop Bits.** **0 = 1 stop bit.** 1 = 2 stop bits.
2:1	BDA[1:0]	**Bit Data.** 00 = 6 bit data. 01 = 7 bit data. **10 = 8 bit data.** 11 = 9 bit data.
0	NBE	**Ninth Bit Enable.** **0 = Disable.** 1 = Enable ninth bit as Escape and ninth bit function (register C).

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S3C (CIDG), Caller ID Gain

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						CIDG[2:0]		
Type						R/W		

Reset Settings = 0000_0001 (0x01)

Bit	Name	Function
7:3	Reserved	Read returns Zero
2:0	CIDG[2:0]	**Caller ID Gain.** The CC-2401 dynamically sets the on hook analog receive gain SF4[6:4] (ARG) to CIDG during a caller ID event (or continuously if S0C[6:5] (CIDM = 11). This field should be set prior to caller ID operation. **000 = 0 dB** 001 = 3dB 010 = 6 dB 011 = 9 dB 100 = 12 dB

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S62 (RC), Result Codes Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		OCR				IR	NLR	RR
Type		R/W				R/W	R/W	R/W

Reset Settings = 0100_0001 (0x41)

Bit	Name	Function
7	Reserved	Read returns Zero
6	OCR	**Overcurrent Result Code ("x").** 0 = Enable. **1 = Disable.**
5:3	Reserved	Read returns zero.
2	IR	**Intrusion Result Code ("I" and "I").** **0 = Disable.** 1 = Enable.
1	NLR	**No Phone Line Result Code ("L" and "I").** **0 = Disable.** 1 = Enable.
0	RR	**Ring Result Code ("R").** 0 = Disable **1 = Enable.**

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S82 (IST), Intrusion

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IST[3:0]				LCLD	IB[1:0]		
Type	R/W				R/W	R/W		

Reset Settings = 0000_1000 (0x08)

Bit	Name	Function
7:4	IST[3:0]	**Intrusion Settling Time.** **0000 = IST equals 1 second.** Delay between the time the CC-2401 goes off hook and the off hook intrusion algorithm begins (250 ms units).
3	LCLD	**Loop Current Loss Detect.** 0 = Disable. **1 = Enables the reporting of "I" and "L" result codes while off hook. Asserts INT# if GPIO4 (SE2[7:6]) is enabled as INT#.**
2:1	IB[1:0]	**Intrusion Blocking.** This feature only works when SDF ≠ 0x00. Defines the method used to block the off hook intrusion algorithm from operating after dialing has begun. **00 = No intrusion blocking.** 01 = Intrusion disabled from start of dial to end of dial. 10 = Intrusion disabled from start of dial to register S29 time out. 11 = Intrusion disabled from start of dail to carrier detect or to "N" or "n" result code.
0	Reserved	Read returns zero.

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SDF (DGSR), Intrusion Deglitch

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DGSR[6:0]						
Type		R/W						

Reset Settings = 0000_1100 (0x0C)

Bit	Name	Function
7	Reserved	Read returns Zero.
6:0	DGSR[6:0]	**Deglitch Sample Rate.** Sets the sample rate for the deglitch algorithm and the off hook intrusion algorithm (40 ms units). 0000000 = Disables the deglitch algorithm, and sets the off hook intrusion sample rate to 200 ms and delay between compared samples to 800 ms.

SE0 (CF1), Chip Functions 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			ICTS		ND	SD[2:0]		
Type			R/W		R/W	R/W		

Reset Settings = 0010_0010 (0x22)

Bit	Name	Function
7:6	Reserved	Read returns zero
5	ITCS	**Invert CTS# Pin** 0 = Inverted (CTS). **1 = Normal (CTS).**
4	Reserved	Read returns zero.
3	ND	**0 = 8N1.** 1 = 9N1 (hardware UART only.
2:0	SD[2:0]	**Serial Dividers** 000 = 300 bps serial link. 001 = 1200 bps serial link. **010 = 2400 bps serial link.** 011 = 9600 bps serial link. 100 = 19200 bps serial link. 101 = 38400 bps serial link. 110 = 115200 bps serial link. 111 = 307200 bps serial link.

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SE1 (GPIO1), General Purpose Input/Output 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							GPD5	GPIO5
Type							R/W	R/W

Reset Settings = 0000_0100 (0x04)

Bit	Name	Function
7:2	Reserved	Read returns Zero.
1	GPD5	**GPIO5 Data.**
0	GPIO5	**GPIO5.** **0 = Digital input.** 1 = Digital output (relay drive).

SE2 (GPIO2), General Purpose Input/Output 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	GPIO4[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]	
Type	R/W		R/W		R/W		R/W	

Reset Settings = 0010_0010 (0x22)

Bit	Name	Function
7:6	GPIO4[1:0]	**GPIO4.** **00 = Digital Input.** 01 = Digital output (relay drive). 10 = AOUT. 11 = INT# function defined by S08.
5:4	GPIO3[1:0]	**GPIO3.** **00 = Digital Input.** 01 = Digital output (relay drive). 10 = Reserved. 11 = ESC function (digital input).
3:2	GPIO2[1:0]	**GPIO2.** **00 = Digital Input.** 01 = Digital output (relay drive; also used for CD# function). 10 = Reserved. 11 = Digital input.
1:0	GPIO1[1:0]	**GPIO1*.** **00 = Digital Input.** 01 = Digital output (relay drive). 10 = Reserved. 11 = Reserved.
*Note: To be used as a GPIO pin; SE4[3] (GPE) must equal zero.		

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SE3 (GPD), GPIO Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					GPD4	GPD3	GPD2	GPD1
Type					R/W	R/W	R/W	R/W

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	GPD4	**GPIO4 Data.**
2	GPD3	**GPIO3 Data.**
1	GPD2	**GPIO2 Data.**
0	GPD1	**GPIO1 Data.**

SE4 (CF5), Chip Functions 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NBCK	SBCK	DRT		GPE			
Type	R	R	R/W		R/W			

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7	NBCK	**9600 Baud Clock (Read Only).**
6	SBCK	**600 Baud Clock (Read Only).**
5	DRT	**Data Routing.** **0 = Data mode, DSP output transmitted to line, line received by DSP input.** 1 = Loopback mode, TXD through microcontroller (DSP) to RXD.
4	Reserved	Read returns zero.
3	GPE	**GPIO1 Enable.** **0 = Disable** 1 = Enable GPIO1 to be HDLC end of frame flag.
2:0	Reserved	Read returns zero.

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SE5 (DSP1). (SE8 = 0x02) Read Only Definition.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DDAV	TDET		TONE[4:0]				
Type	R	R		R				

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function		
7	DDAV	**DSP Data Available.**		
6	TDET	**Tone Detected.** Indicates a TONE (any of type 0-25 below) has been detected **0 = Not detected.** 1 = Detected.		
5	Reserved	Read returns zero.		
4:0	TONE[4:0]	**Tone Type Detected.** When TDET goes high, TONE indicates which tone has been detected from the following.		
		TONE	**Tone Type**	**Priority**
		00000-01111	DTMF 0-15 (DTMFE = 1)[1]	1
		10000	Answer tone detected 2100 Hz (ANSE = 1)[2]	2
		10001	Bell 103 answer tone detected 2225 Hz (ANSE = 1)	2
		10010	V.23 forward channel mark 1300 Hz (V23E = 1)[3]	3
		10011	V.23 backward channel mark 390 Hz (V23E = 1)	3
		10100	User defined frequency 1 (USEN1 = 1)[4]	4
		10101	User defined frequency 2 (USEN1 = 1)	4
		10110	Call progress filter A detected	5
		10111	User defined frequency 3 (USEN2 = 1)[5]	5
		11000	User defined frequency 4 (USEN2 = 1)	5
		11001	Call progress filter B detected	6

Notes:

1. SE6[0] (DTMFE) SE8 = 0x02.
2. SE6[1] (ANSE) SE8 = 0x02.
3. SE6[2] (V23E) SE8 = 0x02.
4. SE6[3] (USEN1) SE8 = 0x02.
5. SE6[4] (USEN2) SE8 = 0x02.

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SE5 (DSP1). (SE8 = 0x02) Write Only Definition.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DTM[3:0]				TONC[2:0]		
Type		W				W		

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function	
7	Reserved	Always write zero.	
6:3	DTM[3:0]	**Tone Type Generated.** DTMF ton (-0 – 15) to transmit when selected by TONC = 001.	
2:0	TONC[2:0]	**DTMF Tone Selector**	
		Tone	**Tone Type**
		000	**Mute**
		001	DTMF
		010	2225 Hz Bell mode answer tone with phase reversal
		011	2100 Hz CCITT mode answer tone with phase reversal
		100	2225 Hz Bell mode answer tone without phase reversal
		101	2100 Hz CCITT mode answer tone without phase reversal
		110	User defined programmable frequency tone (UFRQ)
		111	1300 Hz V.25 calling tone

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SE6 (DSP3), (SE8 = 0x02) Write Only Definition

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPSQ	CPCD		USEN2	USEN1	V23E	ANSE	DTMFE
Type	W	W		W	W	W	W	W

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7	CPSQ	**Call Progress Squaring Filter.** **0 = Disable** 1 = Enables a squaring function on the output of filter B before the input to A (cascade only).
6	CPCD	**Call Progress Cascade Disable.** **0 = Call progress filter B output is input into call progress filter A. Output from filter A is used in the detector.** 1 = Cascade disabled. Two independent fourth order filters available (A and B). The largest output of the two is used in the detector.
5	Reserved	
4	USEN2	**User Tone Reporting Enable 2.** **0 = Disable.** 1 = Enable the reporting of user defined frequency tones 3 and 4 through TONE.
3	USEN1	**User Tone Reporting Enable 1.** **0 = Disable.** 1 = Enable the reporting of user defined frequency tones 1 and 2.
2	V23E	**V.23 Tone Reporting Enable.** **0 = Disable.** 1 = Enable the reporting of V.23 tones, 390 Hz and 1300 Hz.
1	ANSE	**Answering Tone Reporting Enable.** **0 = Disable.** 1 = Enable the reporting of answer tones.
0	DTMFE	**DTMF Tone Reporting Enable.** **0 = Disable.** 1 = Enable the reporting of DTMF tones.

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SEB (TPD), Timer and Powerdown

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					PDDE			
Type					R/W			

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7:4	Reserved	Read returns Zero.
3	PDDE	**Powerdown DSP Engine.** **0 = Power one.** 1 = Powerdown.
2:0	Reserved	Read returns zero.

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SEC (RVC1), Ring Validation Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV	RDLY[2:0]			RCC]2:0]			
Type	R/W	R/W			R/W			

Reset Settings = 1000_1000 (0x88)

Bit	Name	Function	
7	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. **1 = Ring validation feature is enabled in both normal operating mode and low power mode.**	
6:4	RDLY[2:0]	**Ring Delay** These bits set the amount of time between when a ring signal is validated and when a valid ring signal is indicated.	
		RDLY[2:0]	**Delay**
		000	**0 ms**
		001	256 ms
		010	512 ms
		-	
		-	
		-	
		111	1792 ms
3:1	RCC[2:0]	**Ring Confirmation Count.** These bits set the amount of time that the ring frequency must be within the tolerances set by the RAS[5:0] bits and the RMX[3:0] bits to be classified as a valid ring signal.	
		RDLY[2:0]	**Delay**
		000	**0 ms**
		001	256 ms
		010	512 ms
		-	
		-	
		-	
		111	1792 ms
0	Reserved	This bit must always be written to zero.	

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SED (RVCZ), Ring Validation Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			RAS[5:0]					
Type			R/W					

Reset Settings = 0001_1001 (0x19)

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. If a second or subsequent TIP/RING event occurs after the timer has timed out, the frequency of the ring is too low, and the ring is invalidated. The difference between RAS[5:0 and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RAS[5:0] value for a frequency range [f_min, f_max], the following equation should be used: RAS[5:0] = 1 / (2 x f_min).

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SEE (RVC3), Ring Validation Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTO[3:0]				RMX[3:0]			
Type	R/W				R/W			

Reset Settings = 0001_0110 (0x16)

Bit	Name	Function	
7:4	RTO[3:0]	**Ring Timeout.** These bits set when a ring signal is determined to be over after the most recent ring threshold crossing.	
		RTO[3:0]	**Ring Timeout**
		0000	80 ms
		0001	128 ms
		0010	256 ms
		-	
		-	
		-	
		1111	1920 ms
3:0	RMX[3:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[3:0] field, and if it exceeds the value in RMX[3:0], the frequency of the ring is too high, and the ring is invalidated. The difference between RAS[5:0] and RMX[3:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RMX[3:0] value for a frequency range [f_min, f_max], the following equation should be used: RMX[3:0] x 2 ms = RAS[5:0] – 2 ms – (1 / (2 x f_max)).	

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SF0 (DAA0), DAA Low Level Functions 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FOH[1:0]						LM[1:0]	
Type	R/W						R/W	

Reset Settings = 0100_0000 (0x40)

Bit	Name	Function
7:6	FOH[1:0]	**Fast Off-Hook Selection.** These bits determine the length of the off-hook counter. The default setting is 128 ms. 00 = 512 ms **01 = 128 ms** 10 = 64 ms 11 = 8 ms
5:2	Reserved	Read returns zero.
1:0	LM[1:0]	**Line Mode.** These bits determine the line status of the CC-2401.* 00 = On-hook 01 = Off-hook 10 = On-hook line monitor mode 11 = Reserved
*Note: Under normal operation, the CC-2401 internal microcontroller automatically sets these bits appropriately.		

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SF1 (DAA1), DAA Low Level Functions 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BTE	PDN	PDL	LVFD		HBE		
Type	R/W	R/W	R/W	R/W		R/W		

Reset Settings = 0000_1100 (0x0C)

Bit	Name	Function
7	BTE	**Billing Tone Enable.** When the line-side device detects a billing tone, SF9[3] (BTD is set. **0 = Disable.** 1 = Enable.
6	PDN	**Powerdown.** **0 = Normal operation.** 1 = Powerdown the CC-2401.
5	PDL	**Always write zero to this bit.**
4	LVFD	**Line Voltage Force Disable.** **0 = Normal operation.** 1 = The circuitry that forces the LVS register to all 0s and 3V or less is disabled. This rgister may display unpredictable values at voltages between 0 and 2V. All 0s are displayed if the line voltage is 0V.
3	Reserved	Do not modify.
2	HBE	**Hybrid Transmit Path Correct.** 0 = Disable. **1 = Enable.**
1:0	Reserved	Do not modify.

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SF2 (DAA2), DAA Low Level Functions 2

This register is for factory test use only.

SF4 (DAA4), DAA Low Level Functions 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					ARL[1:0]		ATL[1:0]	
Type					R/W		R/W	

Reset Settings = 0000_1111 (0x0F)

Bit	Name	Function
7	Reserved	Read returns zero.
3:2	ARL[1:0]	**AOUT Receive – Path Level.** DAA receive path signal AOUT gain. 00 = 0 dB 01 = -6 dB 10 = -12 dB **11 = Mute**
1:0	ATL[1:0]	**AOUT Transmit – Path Level.** DAA transmit path signal AOUT gain. 00 = -18 dB 01 = -24 dB 10 = -30 dB **11 = Mute**
4	LVFD	**Line Voltage Force Disable.** **0 = Normal operation.** 1 = The circuitry that forces the LVS register to all 0s and 3V or less is disabled. This rgister may display unpredictable values at voltages between 0 and 2V. All 0s are displayed if the line voltage is 0V.
3	Reserved	Do not modify.
2	HBE	**Hybrid Transmit Path Correct.** 0 = Disable. **1 = Enable.**
1:0	Reserved	Do not modify.

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SF5 (DAA5), DAA Low Level Functions 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			OHS[1:0]		ILIM	RZ		RT
Type			R/W		R/W	R/W		R/W

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function	
7:6	Reserved	Read returns zero.	
5:4	OHS[1:0]	**On-Hook Speed** These bits set the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the register is written until loop current equals zero.	
		OHS[1:0]	**Mean On-Hook Speed**
		00	**Less than 0.5 ms**
		01	3 ms ±10% (Meets ETSI standard)
		1X	20 ms ±10% (Meets Australian spark quenching specification)
3	ILIM	**Current Limiting Enable.** **0 = Current limiting mode disabled.** 1 = Current limiting mode enabled. This mode limits loop current to a maximum of 60 mA per the TBR21 specification.	
2	RZ	**Ringer Impedance.** **0 = Maximum (high) ringer impedance.** 1 = Synthesized ringer impedance used to satisfy a maximum ringer impedance specification in countries, such as Poland, South Africa, and Slovenia.	
1	Reserved	Do not modify	
0	RT	**Ringer Threshold Select.** Used to satisfy country requirements on ring detection. Signals below the lower level do not generate a ring detection; Signals above the upper level are guaranteed to generated a ring detection. **0 = 13.5 to 16.5 V_{RMS}** 1 = 19.35 to 23.65 V_{RMS}	

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SF6 (DAA6), DAA Low Level Functions 6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MINI[1:0]		DCV[1:0]		ACT[3:0]			
Type	R/W		R/W		R/W			

Reset Settings = 1111_0000 (0xF0)

Bit	Name	Function	
7:6	MINI[1:0]	**Minimum Operation Loop Current.** Adjusts the minimum loop current at which the DAA can operate. Increasing the minimum operational loop current can improve signal headroom at a lower TIP/RING voltage.	
		MINI[1:0]	**Minimum Loop Current**
		00	10 mA
		01	12 mA
		10	14 mA
		11	**16 mA**
5:4	DCV[1:0]	**TIP/RING Voltage Adjust.** These bits adjust the TIP/RING voltage on the line. Low voltage countries should use a lower TIP/RING voltage. Raising the TIP/RING voltage can improve signal headroom.	
		DCV[1:0]	**DCT Pin Voltage**
		00	3.1 V
		01	3.2 V
		10	3.35 V
		11	**3.5 V**
3:0	ACT[3:0]	**AC Termination Select.**	
		ACT[3:0]	**AC Termination**
		0000	**Real 600 Ω termination that satisfies the impedance requirements of FCC part 68, JATE, and other countries.**
		0011	Global complex impedance. Complex impedance that satisfies global impedance requirements EXCEPT New Zealand. May achieve higher return loss for countries requiring complex ac termination. [220 Ω + (620 Ω || 120 nF) and 220 Ω + (820 Ω || 115 nF)].
		0100	Complex impedance for use in New Zealand. [370 Ω + (620 Ω || 310 nF)]
		1111	Complex impedance that satisfies global impedance requirements.

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SF8 (DAA8), DAA Low Level Functions 8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LRV[3:0]						DCR	
Type	R						R/W	

Reset Settings = Vary with line-side version.

Bit	Name	Function
7:4	LRV[3:0]	**Line-Side Device Revision Number.** 0001 = Rev A 0010 = Rev B 0011 = Rev C 0100 = Rev D 0101 = Rev E
3:2	Reserved	Read returns an non-deterministic value.
1	DCR	**DC Impedance Selection.** **0 = 50 Ω dc termination. This mode should be used for all standard applications.** 1 = 800 Ω dc termination.
0	Reserved	Do not modify

SF9 (DAA9), DAA Low Level Functions 9 Read Only

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					BTD	OVL	ROV	
Type					R/W	R	R/W	

Reset Settings = 0010_0000 (0x20)

Bit	Name	Function
7:4	Reserved	Do not modify.
3	BTD	**Billing Tone Detect (sticky).** **0 = No billing tone detected.** 1 = Billing tone detected.
2	OVL	**Receive Overload.** Same as ROV, except not sticky.
1	ROV	**Receive Overload (sticky).** **0 = No excessive level detected.** 1 = Excessive input level detected.
0	Reserved	Do not modify.

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SFC (DAAC), DAA Low Level Functions C

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CTSM							
Type	R/W							

Reset Settings = 0000_0000 (0x00)

Bit	Name	Function
7	CTSM	**CTS Mode.** **0 = CTS# pin is negated as soon as a start bit is detected and reasserted when the transmit FIFO is empty.** 1 = CTS# pin is negated when the FIFO is ≥ 70% full and reasserted when the FIFO is ≤ 30% full.
6:0	Reserved	Read returns zero.

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FCC Compliance

Certification Number: US:COPMM00BCC-xxK2
AC-REN: 0.0B
DC-REN: NA
Connectors: RJ11C
Compliance: FCC Part 15 and Part 68

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CE DECLARATION OF CONFORMITY

Application of Council Directive(s): 89/336/EEC with Amending Directives: 92/31/EEC, 93/68/EEC, 98/13/EEC

Standard(s) to which conformity is declared:

STANDARDS	**ENVIRONMENTAL PHENOMENA**
EN61000-6-3: 2001	Emissions (EN55022: 1998)
EN55024: 1998, Amendment A1: 2001	Electrostatic Discharge (EN61000-4-2: 1995, A1: 1998, A2: 2001)
EN55024: 1998, Amendment A1: 2001	Radiated Immunity (EN 61000-4-3: 2002, A1: 2002)
TBR 21: 1998	Telecommunication Performance (TBR 21: 1998)

Manufacturer's Name: Copeland Communications, Inc.

Manufacturer's Address:
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Type of Equipment: Information Technology Equipment

Model No.: CC-xxK2 World Modem II

Year of Manufacture: 2004

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Revision Information

Revision 1.0

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