

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

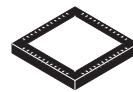
For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

| Part Number | Package Description | Original (gold wire) package document number | Current (copper wire) package document number |
|---------------|---------------------|---|--|
| MC68HC908JW32 | 48 QFN | 98ARH99048A | 98ASA00466D |
| MC9S08AC16 | | | |
| MC9S908AC60 | | | |
| MC9S08AC128 | | | |
| MC9S08AW60 | | | |
| MC9S08GB60A | | | |
| MC9S08GT16A | | | |
| MC9S08JM16 | | | |
| MC9S08JM60 | | | |
| MC9S08LL16 | | | |
| MC9S08QE128 | | | |
| MC9S08QE32 | | | |
| MC9S08RG60 | | | |
| MCF51CN128 | | | |
| MC9RS08LA8 | 48 QFN | 98ARL10606D | 98ASA00466D |
| MC9S08GT16A | 32 QFN | 98ARH99035A | 98ASA00473D |
| MC9S908QE32 | 32 QFN | 98ARE10566D | 98ASA00473D |
| MC9S908QE8 | 32 QFN | 98ASA00071D | 98ASA00736D |
| MC9S08JS16 | 24 QFN | 98ARL10608D | 98ASA00734D |
| MC9S08QB8 | | | |
| MC9S08QG8 | 24 QFN | 98ARL10605D | 98ASA00474D |
| MC9S08SH8 | 24 QFN | 98ARE10714D | 98ASA00474D |
| MC9RS08KB12 | 24 QFN | 98ASA00087D | 98ASA00602D |
| MC9S08QG8 | 16 QFN | 98ARE10614D | 98ASA00671D |
| MC9RS08KB12 | 8 DFN | 98ARL10557D | 98ASA00672D |
| MC9S08QG8 | | | |
| MC9RS08KA2 | 6 DFN | 98ARL10602D | 98ASA00735D |

MC9S08QE32 Series

Covers: MC9S08QE32 and MC9S08QE16

MC9S08QE32



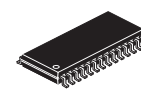
48-QFN
Case 1314
7 mm × 7 mm



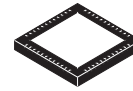
44-LQFP
Case 824D
10 mm × 10 mm



32-LQFP
Case 873A
7 mm × 7 mm



28-SOIC
Case 751F



32-QFN
Case 1582
5 mm × 5 mm

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
 - Up to 50.33 MHz HCS08 CPU at 3.6 V to 2.4 V, 40 MHz CPU at 2.4 V to 2.1 V and 20 MHz CPU at 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
 - HC08 instruction set with added BGND instruction
 - Support for up to 32 interrupt/reset sources
- On-Chip Memory
 - Flash read/program/erase over full operating voltage and temperature
 - Random-access memory (RAM)
 - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
 - Two very low power stop modes
 - Reduced power wait mode
 - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode.
 - Very low power external oscillator that can be used in run, wait, and stop modes to provide accurate clock source to real time counter.
 - 6 μs typical wakeup time from stop3 mode
- Clock Source Options
 - Oscillator (XOSCVP) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - Internal clock source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports CPU frequencies from 4 kHz to 50.33 MHz.
- System Protection
 - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock.
 - Low-voltage warning with interrupt.
 - Low-voltage detection with reset or interrupt
 - Selectable trip points.
 - Illegal opcode detection with reset
 - Illegal address detection with reset
 - Flash block protection
- Development Support
 - Single-wire background debug interface
 - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus three breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints
- Peripherals
 - **ADC** — 10-channel, 12-bit resolution; 2.5 μs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
 - **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
 - **SCIx** — Two serial communications interface modules with optional 13-bit break. Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake on active edge.
 - **SPI** — One serial peripheral interface; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
 - **IIC** — One IIC; up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
 - **TPMx** — One 6-channel (TPM3) and two 3-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel;
 - **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components; runs in all MCU modes
- Input/Output
 - 40 GPIOs, including 1 output-only pin and 1 input-only pin
 - 16 KBI interrupts with selectable polarity
 - Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.
- Package Options
 - 48-pin QFN, 44-pin LQFP, 32-pin LQFP/QFN, 28-pin SOIC

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

| Revision | Date | Description of Changes |
|----------|------------|---|
| 1 | 7/2/2008 | Initial public released. |
| 2 | 10/7/2008 | Updated the Stop2 and Stop3 mode supply current, and $R_{I_{DD}}$ in FEI mode with all modules on at 25.165 MHz in the Table 8 Supply Current Characteristics. Replaced the stop mode adders section from Table 8 with an individual Table 9 Stop Mode Adders with new specifications. |
| 3 | 11/4/2008 | Updated operating voltage in Table 7 . |
| 4 | 5/4/2009 | Added 10×10 mm information to 44 LQFP in the front page. In Table 7 , added I_{OZTOT} . In Table 11 , updated typicals and Max. for t_{IRST} . In Table 16 , removed the Rev. Voltage High item. Updated Table 17 . |
| 5 | 8/27/2009 | Updated f_{int_t} and f_{int_ut} in the Table 11 . |
| 6 | 10/13/2009 | Corrected the package size descriptions on the cover |
| 7 | 9/16/2011 | Added new package of 32-pin QFN. |

Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9S08QE32RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9S08QE32 MCU.

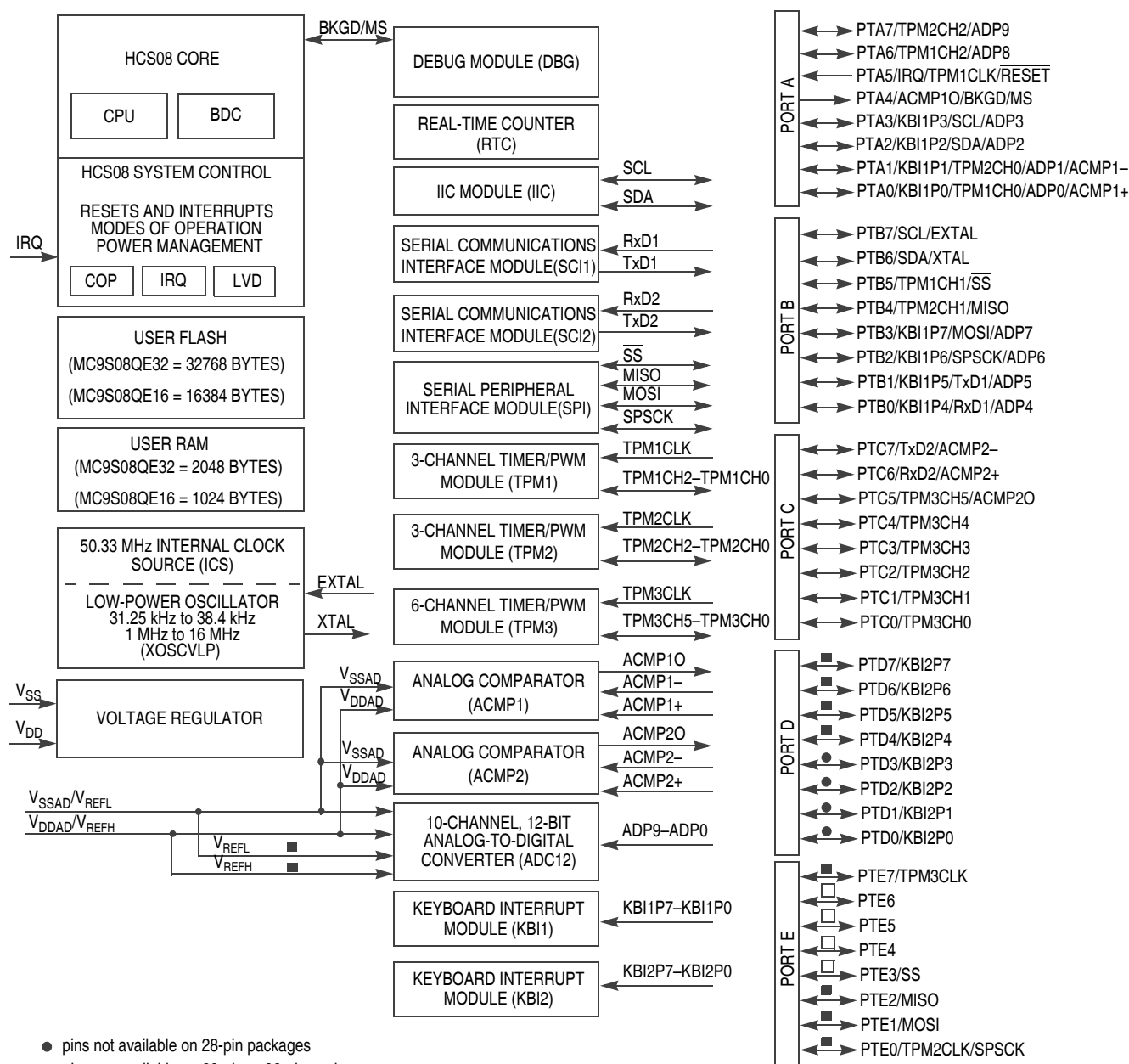
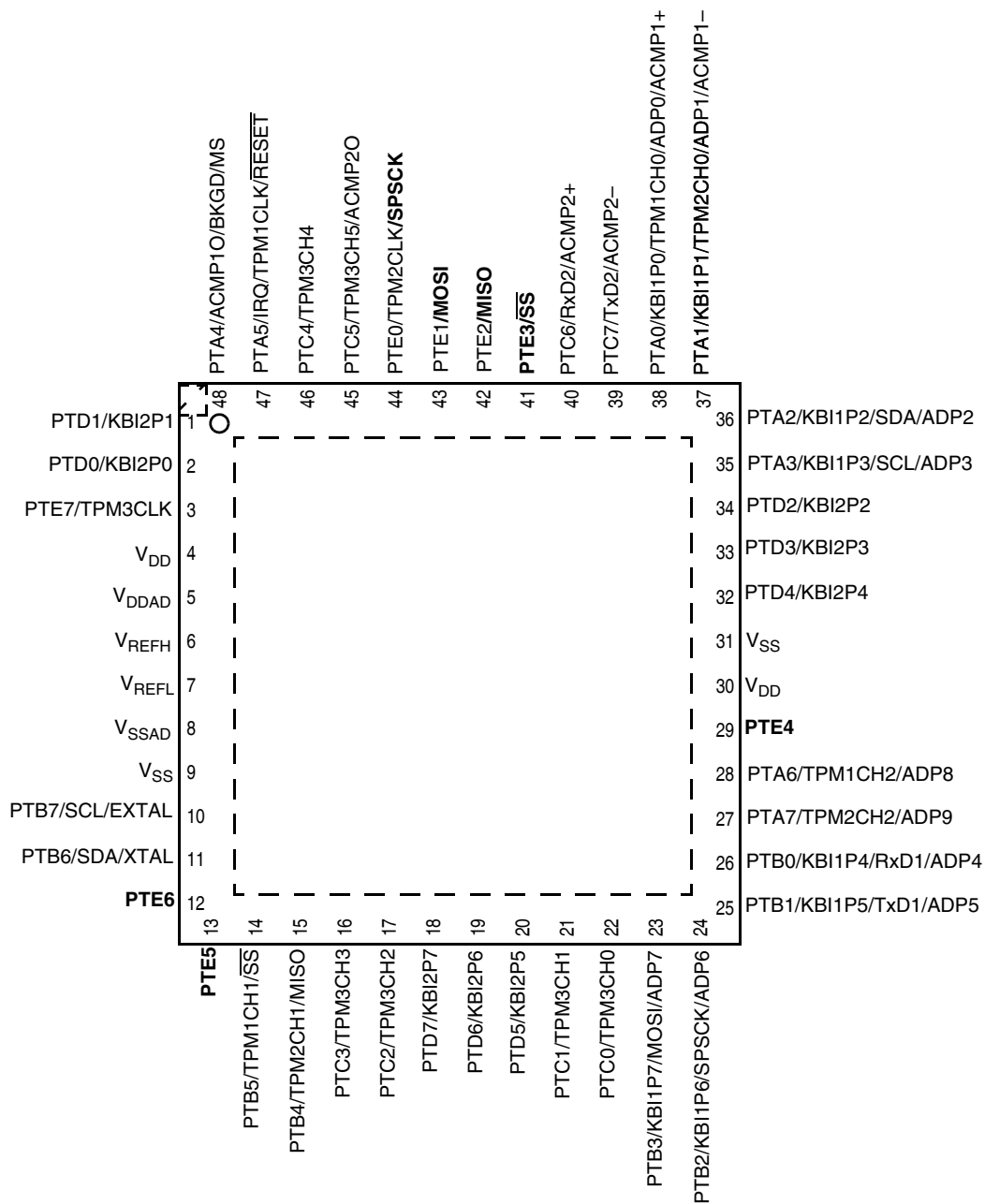


Figure 1. MC9S08QE32 Series Block Diagram

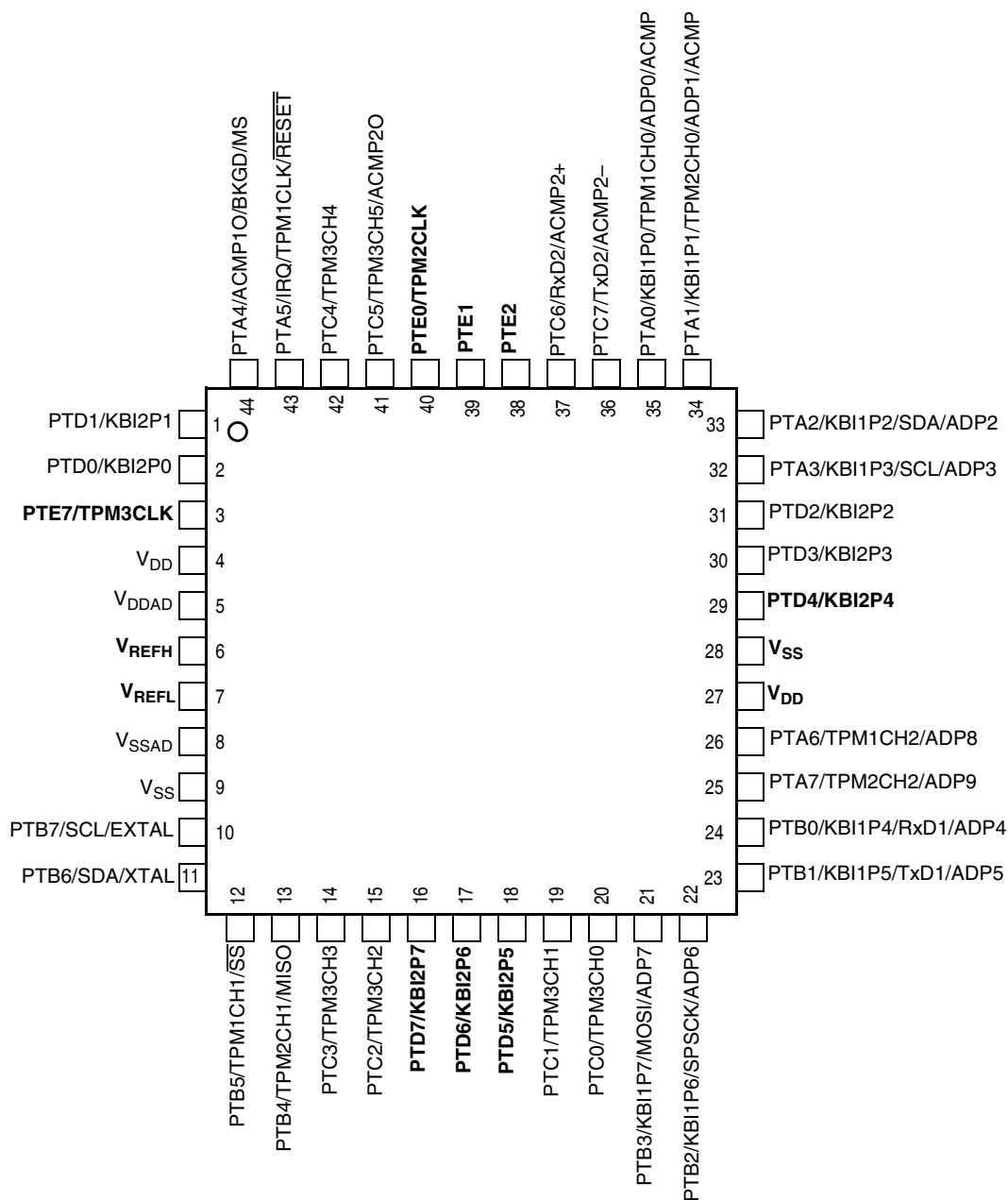
2 Pin Assignments

This section shows the pin assignments for the MC9S08QE32 series devices.



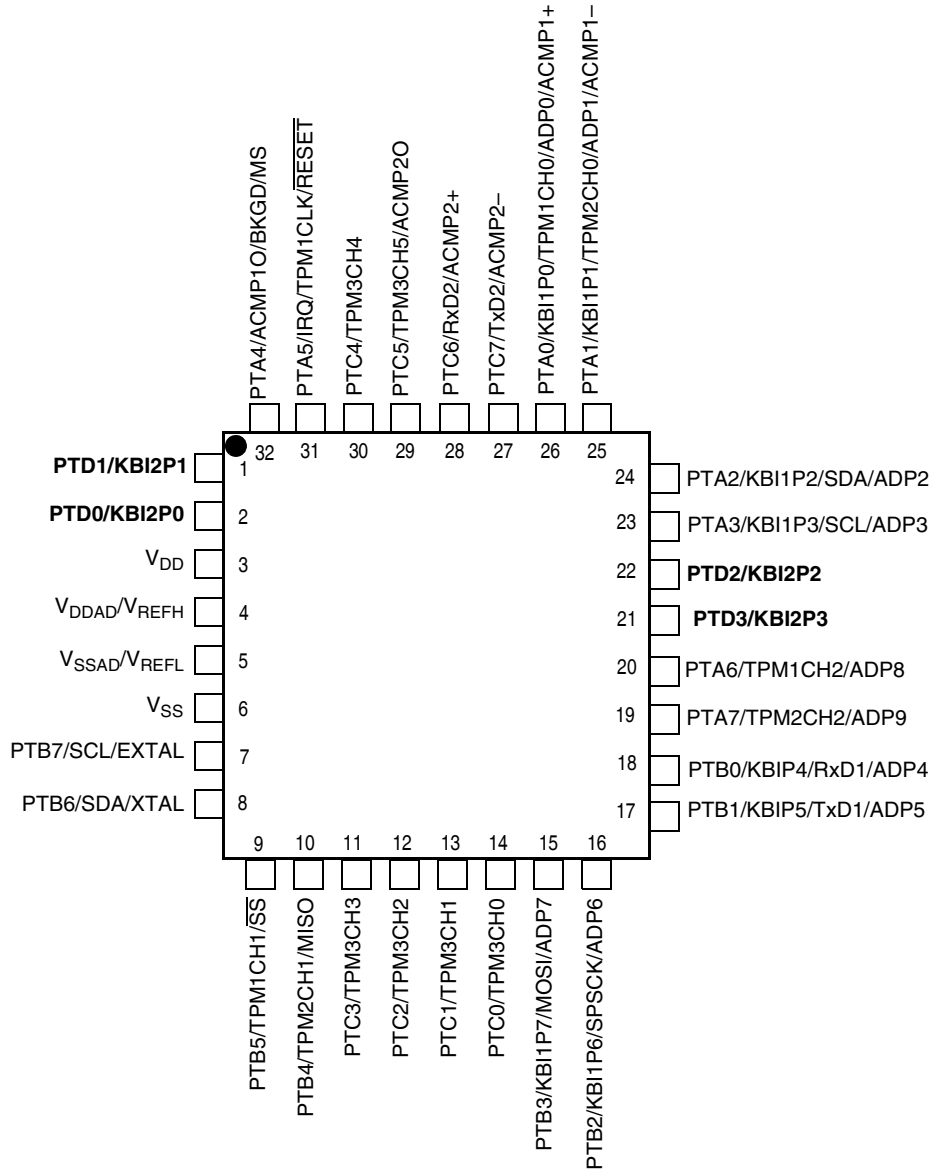
Pins in **bold** are lost in the next lower pin count package.

Figure 2. 48-Pin QFN



Pins in **bold** are lost in the next lower pin count package.

Figure 3. 44-Pin LQFP



Pins in **bold** are lost in the next lower pin count package.

Figure 4. 32-Pin LQFP/QFN

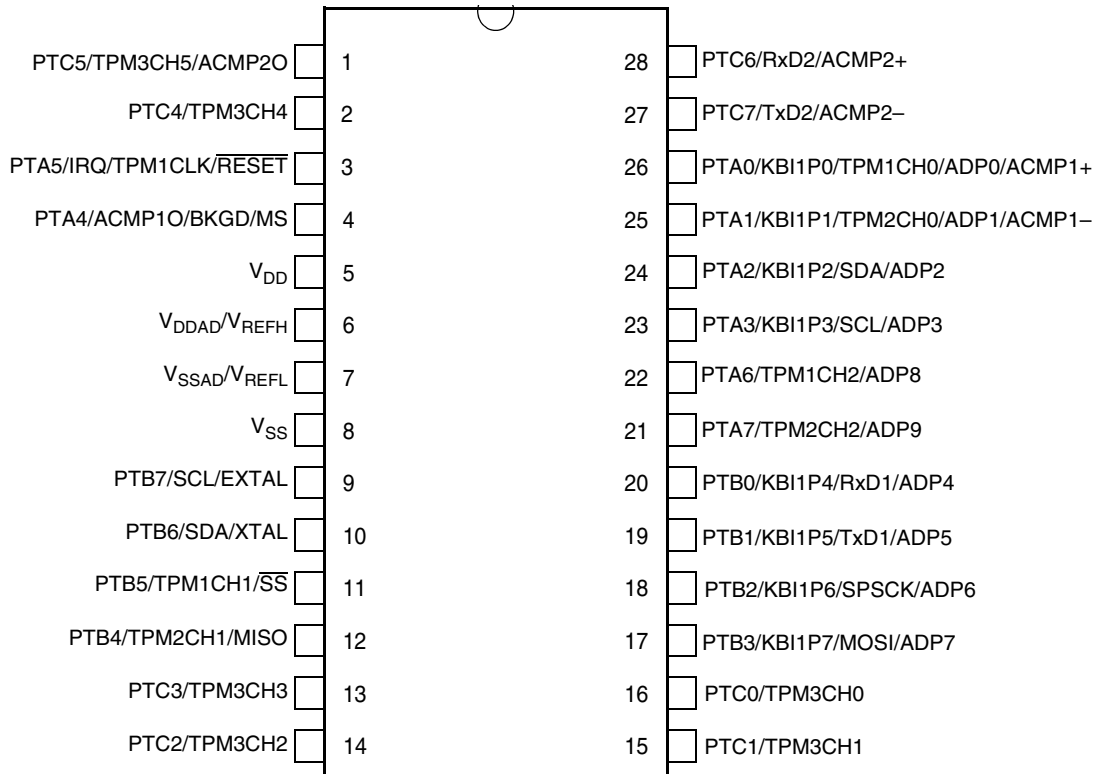


Figure 5. 28-Pin SOIC

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority

| Pin Number | | | | <-- Lowest Priority --> Highest | | | | |
|------------|----|----|----|---------------------------------|------------------|-------------------|-------|-------------------|
| 48 | 44 | 32 | 28 | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 1 | 1 | 1 | — | PTD1 | KBI2P1 | | | |
| 2 | 2 | 2 | — | PTD0 | KBI2P0 | | | |
| 3 | 3 | — | — | PTE7 | TPM3CLK | | | |
| 4 | 4 | 3 | 5 | | | | | V _{DD} |
| 5 | 5 | 4 | 6 | | | | | V _{DDAD} |
| 6 | 6 | | | | | | | V _{REFH} |
| 7 | 7 | 5 | 7 | | | | | V _{REFL} |
| 8 | 8 | | | | | | | V _{SSAD} |
| 9 | 9 | 6 | 8 | | | | | V _{SS} |
| 10 | 10 | 7 | 9 | PTB7 | SCL ¹ | | | EXTAL |
| 11 | 11 | 8 | 10 | PTB6 | SDA ¹ | | | XTAL |
| 12 | — | — | — | PTE6 | | | | |
| 13 | — | — | — | PTE5 | | | | |
| 14 | 12 | 9 | 11 | PTB5 | TPM1CH1 | SS ² | | |
| 15 | 13 | 10 | 12 | PTB4 | TPM2CH1 | MISO ² | | |
| 16 | 14 | 11 | 13 | PTC3 | TPM3CH3 | | | |
| 17 | 15 | 12 | 14 | PTC2 | TPM3CH2 | | | |
| 18 | 16 | — | — | PTD7 | KBI2P7 | | | |

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority (continued)

| Pin Number | | | | <-- Lowest Priority --> Highest | | | | |
|------------|----|----|----|---------------------------------|------------------------------|--------------------|--------------------|---------------------|
| 48 | 44 | 32 | 28 | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 19 | 17 | — | — | PTD6 | KBI2P6 | | | |
| 20 | 18 | — | — | PTD5 | KBI2P5 | | | |
| 21 | 19 | 13 | 15 | PTC1 | TPM3CH1 | | | |
| 22 | 20 | 14 | 16 | PTC0 | TPM3CH0 | | | |
| 23 | 21 | 15 | 17 | PTB3 | KBI1P7 | MOSI ² | | ADP7 |
| 24 | 22 | 16 | 18 | PTB2 | KBI1P6 | SPSCK ² | | ADP6 |
| 25 | 23 | 17 | 19 | PTB1 | KBI1P5 | TxD1 | | ADP5 |
| 26 | 24 | 18 | 20 | PTB0 | KBI1P4 | RxD1 | | ADP4 |
| 27 | 25 | 19 | 21 | PTA7 | TPM2CH2 | | | ADP9 |
| 28 | 26 | 20 | 22 | PTA6 | TPM1CH2 | | | ADP8 |
| 29 | — | — | — | PTE4 | | | | |
| 30 | 27 | — | — | | | | | V _{DD} |
| 31 | 28 | — | — | | | | | V _{SS} |
| 32 | 29 | — | — | PTD4 | KBI2P4 | | | |
| 33 | 30 | 21 | — | PTD3 | KBI2P3 | | | |
| 34 | 31 | 22 | — | PTD2 | KBI2P2 | | | |
| 35 | 32 | 23 | 23 | PTA3 | KBI1P3 | SCL ¹ | | ADP3 |
| 36 | 33 | 24 | 24 | PTA2 | KBI1P2 | SDA ¹ | | ADP2 |
| 37 | 34 | 25 | 25 | PTA1 | KBI1P1 | TPM2CH0 | ADP1 ³ | ACMP1– ³ |
| 38 | 35 | 26 | 26 | PTA0 | KBI1P0 | TPM1CH0 | ADP0 ³ | ACMP1+ ³ |
| 39 | 36 | 27 | 27 | PTC7 | TxD2 | | | ACMP2– |
| 40 | 37 | 28 | 28 | PTC6 | RxD2 | | | ACMP2+ |
| 41 | — | — | — | PTE3 | \overline{SS} ² | | | |
| 42 | 38 | — | — | PTE2 | MISO ² | | | |
| 43 | 39 | — | — | PTE1 | MOSI ² | | | |
| 44 | 40 | — | — | PTE0 | TPM2CLK | SPSCK ² | | |
| 45 | 41 | 29 | 1 | PTC5 | TPM3CH5 | | | ACMP2O |
| 46 | 42 | 30 | 2 | PTC4 | TPM3CH4 | | | |
| 47 | 43 | 31 | 3 | PTA5 | IRQ | TPM1CLK | \overline{RESET} | |
| 48 | 44 | 32 | 4 | PTA4 | ACMP1O | BKGD | MS | |

¹ IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2; default reset locations are PTA3 and PTA2.

² SPI pins (\overline{SS} , MISO, MOSI, and SPSCK) can be repositioned using SPIPS in SOPT2. Default locations are PTB5, PTB4, PTB3, and PTB2.

³ If ADC and ACMP1 are enabled, both modules will have access to the pin.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE32 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

| | |
|----------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|-----------|------------------------|------|
| Supply voltage | V_{DD} | -0.3 to +3.8 | V |
| Maximum current into V_{DD} | I_{DD} | 120 | mA |
| Digital input voltage | V_{In} | -0.3 to $V_{DD} + 0.3$ | V |
| Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3} | I_D | ±25 | mA |
| Storage temperature range | T_{stg} | -55 to 150 | °C |

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

| Rating | Symbol | Value | Unit |
|--|---------------|-----------------------------|------|
| Operating temperature range (packaged) | T_A | T_L to T_H -40 to 85 | °C |
| Maximum junction temperature | T_{JM} | 95 | °C |
| Thermal resistance | | | |
| Single-layer board | | | |
| 48-pin QFN | θ_{JA} | 81 | °C/W |
| 44-pin LQFP | | 68 | |
| 32-pin LQFP | | 66 | |
| 32-pin QFN | | 92 | |
| 28-pin SOIC | | 57 | |
| Thermal resistance | | | |
| Four-layer board | | | |
| 48-pin QFN | θ_{JA} | 26 | °C/W |
| 44-pin LQFP | | 46 | |
| 32-pin LQFP | | 54 | |
| 32-pin QFN | | 33 | |
| 28-pin SOIC | | 42 | |

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|-----------------------------|--------|-------|----------|
| Human Body | Series resistance | R1 | 1500 | Ω |
| | Storage capacitance | C | 100 | pF |
| | Number of pulses per pin | — | 3 | |
| Machine | Series resistance | R1 | 0 | Ω |
| | Storage capacitance | C | 200 | pF |
| | Number of pulses per pin | — | 3 | |
| Latch-up | Minimum input voltage limit | | -2.5 | V |
| | Maximum input voltage limit | | 7.5 | V |

Table 6. ESD and Latch-Up Protection Characteristics

| No. | Rating ¹ | Symbol | Min | Max | Unit |
|-----|--|-----------|------------|-----|------|
| 1 | Human body model (HBM) | V_{HBM} | ± 2000 | — | V |
| 2 | Machine model (MM) | V_{MM} | ± 200 | — | V |
| 3 | Charge device model (CDM) | V_{CDM} | ± 500 | — | V |
| 4 | Latch-up current at $T_A = 85^\circ\text{C}$ | I_{LAT} | ± 100 | — | mA |

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

| Num | C | Characteristic | Symbol | Condition | Min | Typical ¹ | Max | Unit |
|-----|---|---|------------------------|---------------------------------------|----------------------|----------------------|----------------------|------------|
| 1 | | Operating Voltage V_{DD} rising V_{DD} falling | | | 2.0 1.8 | — | 3.6 | V |
| 2 | C | Output high voltage ² All I/O pins, low-drive strength | V_{OH} | 1.8 V, $I_{Load} = -2$ mA | $V_{DD} - 0.5$ | — | — | V |
| | P | | | 2.7 V, $I_{Load} = -10$ mA | $V_{DD} - 0.5$ | — | | |
| | T | 2.3 V, $I_{Load} = -6$ mA | | $V_{DD} - 0.5$ | — | | | |
| | C | 1.8 V, $I_{Load} = -3$ mA | | $V_{DD} - 0.5$ | — | | | |
| 3 | D | Output high current Max total I_{OH} for all ports | I_{OHT} | | — | — | 100 | mA |
| 4 | C | Output low voltage All I/O pins, low-drive strength | V_{OL} | 1.8 V, $I_{Load} = 2$ mA | — | — | 0.5 | V |
| | P | | | 2.7 V, $I_{Load} = 10$ mA | — | — | 0.5 | |
| | T | 2.3 V, $I_{Load} = 6$ mA | | — | — | 0.5 | | |
| | C | 1.8 V, $I_{Load} = 3$ mA | | — | — | 0.5 | | |
| 5 | D | Output low current Max total I_{OL} for all ports | I_{OLT} | | — | — | 100 | mA |
| 6 | P | Input high voltage all digital inputs | V_{IH} | $V_{DD} > 2.3$ V | $0.70 \times V_{DD}$ | — | — | V |
| | C | | | $V_{DD} \leq 1.8$ V | $0.85 \times V_{DD}$ | — | — | |
| 7 | P | Input low voltage all digital inputs | V_{IL} | $V_{DD} > 2.7$ V | — | — | $0.35 \times V_{DD}$ | |
| | C | | | $V_{DD} \leq 1.8$ V | — | — | $0.30 \times V_{DD}$ | |
| 8 | C | Input hysteresis all digital inputs | V_{hys} | | $0.06 \times V_{DD}$ | — | — | mV |
| 9 | P | Input leakage current all input only pins (Per pin) | I_{In} | $V_{In} = V_{DD}$ or V_{SS} | — | — | 1 | μ A |
| 10 | P | Hi-Z (off-state) leakage current all input/output (per pin) | I_{OZ} | $V_{In} = V_{DD}$ or V_{SS} | — | — | 1 | μ A |
| 11 | C | Total leakage combined for all inputs and Hi-Z pins All input only and I/O | I_{OZTOT} | $V_{In} = V_{DD}$ or V_{SS} | — | — | 2 | μ A |
| 11 | P | Pullup, Pulldown resistors all digital inputs, when enabled | R_{PU} , R_{PD} | | 17.5 | — | 52.5 | k Ω |
| 12 | D | DC injection current ^{3, 4, 5} Single pin limit Total MCU limit, includes sum of all stressed pins | I_{IC} | $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ | -0.2 | — | 0.2 | mA |
| | | | | | -5 | — | 5 | mA |
| 13 | C | Input Capacitance, all pins | C_{In} | | — | — | 8 | pF |
| 14 | C | RAM retention voltage | V_{RAM} | | — | 0.6 | 1.0 | V |
| 15 | C | POR re-arm voltage ⁶ | V_{POR} | | 0.9 | 1.4 | 2.0 | V |

Table 7. DC Characteristics (continued)

| Num | C | Characteristic | Symbol | Condition | Min | Typical ¹ | Max | Unit |
|-----|---|--|------------|-------------------------------------|--------------|----------------------|--------------|---------|
| 16 | D | POR re-arm time | t_{POR} | | 10 | — | — | μ s |
| 17 | P | Low-voltage detection threshold — high range | V_{LVDH} | V_{DD} falling V_{DD} rising | 2.11 2.16 | 2.16 2.21 | 2.22 2.27 | V |
| 18 | P | Low-voltage detection threshold — low range | V_{LVDL} | V_{DD} falling V_{DD} rising | 1.80 1.88 | 1.82 1.90 | 1.91 1.99 | V |
| 19 | P | Low-voltage warning threshold — high range | V_{LVWH} | V_{DD} falling V_{DD} rising | 2.36 2.36 | 2.46 2.46 | 2.56 2.56 | V |
| 20 | P | Low-voltage warning threshold — low range | V_{LVWL} | V_{DD} falling V_{DD} rising | 2.11 2.16 | 2.16 2.21 | 2.22 2.27 | V |
| 21 | C | Low-voltage inhibit reset/recover hysteresis | V_{hys} | | — | 80 | — | mV |
| 22 | P | Bandgap Voltage Reference ⁷ | V_{BG} | | 1.15 | 1.17 | 1.18 | V |

¹ Typical values are measured at 25 °C. Characterized, not tested

² As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL} .

³ All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD} .

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁶ Maximum is highest voltage that POR is guaranteed.

⁷ Factory trimmed at $V_{DD} = 3.0$ V, Temp = 25 °C

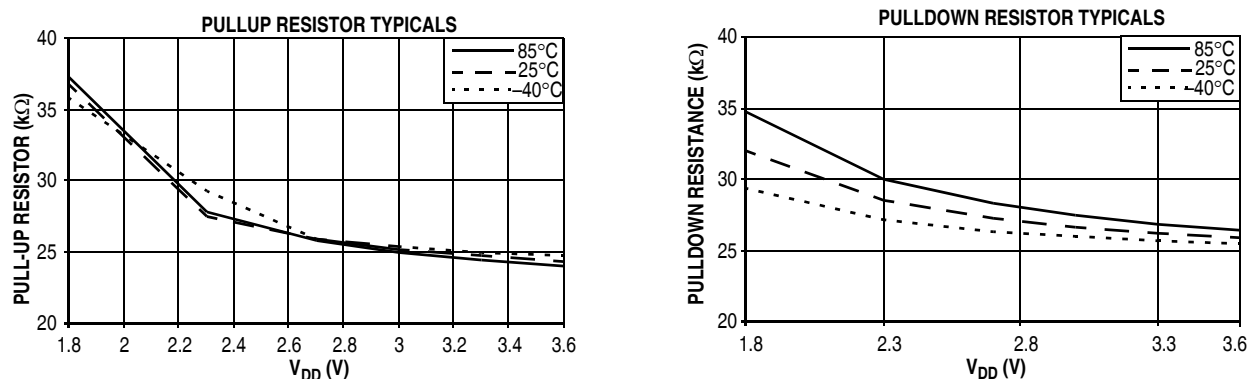


Figure 6. Pullup and Pulldown Typical Resistor Values ($V_{DD} = 3.0$ V)

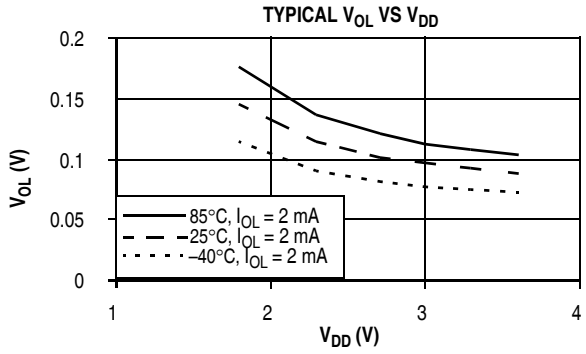
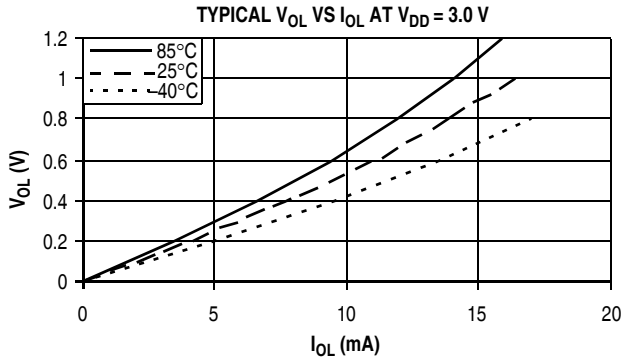


Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

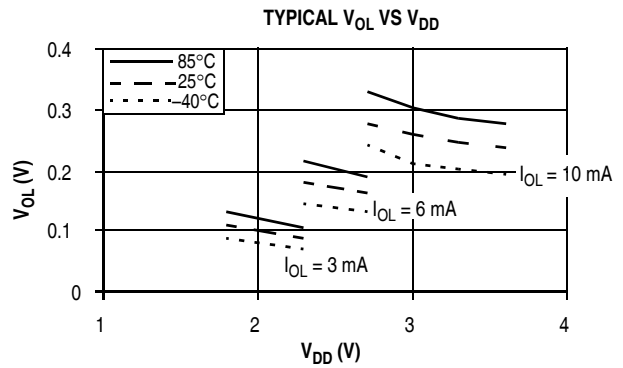
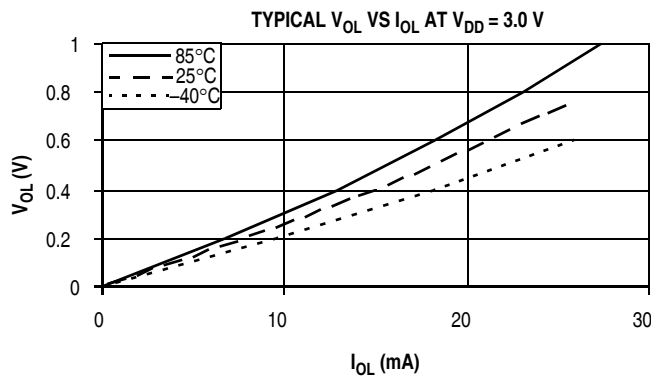


Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

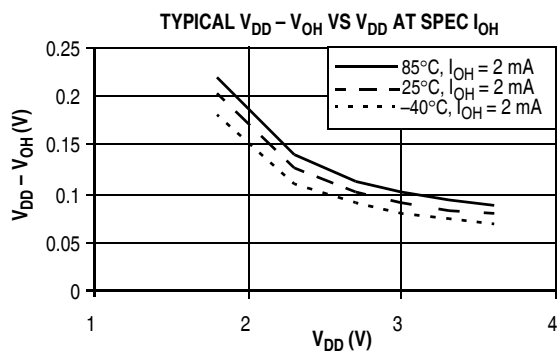
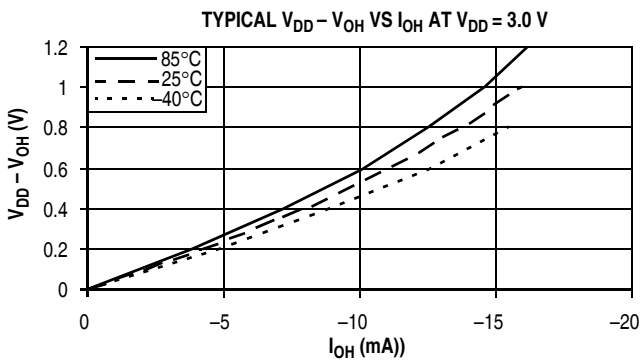


Figure 9. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

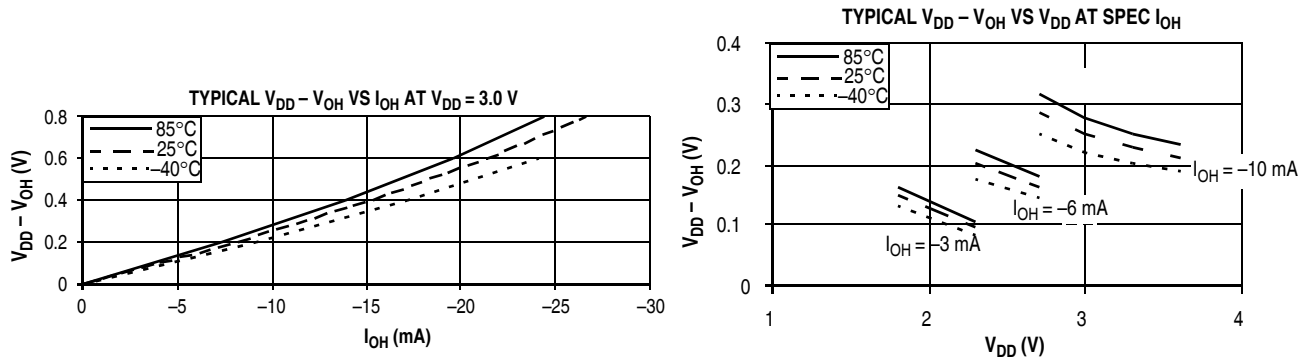


Figure 10. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

| Num | C | Parameter | Symbol | Bus Freq | V _{DD} (V) | Typical ¹ | Max | Unit | Temp (°C) | |
|-----|---|--|-------------------|--------------|---------------------|----------------------|-------|------|-----------|-----------|
| 1 | P | Run supply current FEI mode, all modules on | R _I DD | 25.165 MHz | 3 | 13 | 14 | mA | -40 to 25 | |
| | P | | | | | 14 | 15 | | | 85 |
| | T | | | | | 20 MHz | 13.75 | | — | -40 to 85 |
| | T | | | | | 8 MHz | 5.59 | | — | |
| | T | | | | | 1 MHz | 1.03 | | — | |
| 2 | C | Run supply current FEI mode, all modules off | R _I DD | 25.165 MHz | 3 | 11.5 | 12.3 | mA | -40 to 85 | |
| | T | | | | | 20 MHz | 9.5 | | | — |
| | T | | | | | 8 MHz | 4.6 | | | — |
| | T | | | | | 1 MHz | 1.0 | | | — |
| 3 | T | Run supply current LPRS = 0, all modules off | R _I DD | 16 kHz FBILP | 3 | 152 | — | μA | -40 to 85 | |
| | T | | | | | 16 kHz FBELP | 115 | | | — |
| 4 | T | Run supply current LPRS = 1, all modules off, running from Flash | R _I DD | 16 kHz FBELP | 3 | 21.9 | — | μA | -40 to 85 | |
| | T | Run supply current LPRS = 1, all modules off, running from RAM | | | | 7.3 | — | | | |
| 5 | C | Wait mode supply current FEI mode, all modules off | W _I DD | 25.165 MHz | 3 | 5.74 | 6.00 | mA | -40 to 85 | |
| | T | | | | | 20 MHz | 4.57 | | | — |
| | T | | | | | 8 MHz | 2 | | | — |
| | T | | | | | 1 MHz | 0.73 | | | — |

Table 8. Supply Current Characteristics (continued)

| Num | C | Parameter | Symbol | Bus Freq | V _{DD} (V) | Typical ¹ | Max | Unit | Temp (°C) | |
|-----|---|---|-------------------|----------|---------------------|----------------------|------|------|------------|----|
| 6 | P | Stop2 mode supply current | S2I _{DD} | — | 3 | 0.35 | 0.65 | μA | –40 to 25C | |
| | C | | | — | | 0.8 | 1.0 | | 70 | |
| | P | | | — | | 2.0 | 4.5 | | 85 | |
| | C | | | — | 2 | 0.25 | 0.50 | | –40 to 25 | |
| | C | | | — | | 0.65 | 0.85 | | 70 | |
| | C | | | — | | 1.5 | 3.5 | | 85 | |
| 7 | P | Stop3 mode supply current no clocks active | S3I _{DD} | — | 3 | 0.45 | 1.00 | μA | –40 to 25 | |
| | C | | | — | | 1.5 | 2.3 | | 70 | |
| | P | | | — | | 4 | 8 | | 85 | |
| | C | | | — | 2 | 0.35 | 0.70 | | –40 to 25 | |
| | C | | | — | | 1 | 2 | | 70 | |
| | C | | | — | | 3.5 | 6.0 | | 85 | |
| 8 | T | Low power mode adders: | EREFSTEN=1 | 32 kHz | 3 | 500 | — | nA | –40 to 85 | |
| 9 | T | | IREFSTEN=1 | 32 kHz | | 70 | — | | | μA |
| 10 | T | | TPM PWM | 100 Hz | | 12 | — | | | μA |
| 11 | T | | SCI, SPI, or IIC | 300 bps | | 15 | — | | | μA |
| 12 | T | | RTC using LPO | 1 kHz | | 200 | — | | | nA |
| 13 | T | | RTC using ICSECLK | 32 kHz | | 1 | — | | | μA |
| 14 | T | | LVD | n/a | | 100 | — | | | μA |
| 15 | T | | ACMP | n/a | | 20 | — | | | μA |

¹ Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

| Num | C | Parameter | Condition | Temperature | | | | Units |
|-----|---|-----------------------|--|-------------|------|------|------|-------|
| | | | | –40°C | 25°C | 70°C | 85°C | |
| 1 | T | LPO | — | 50 | 75 | 100 | 150 | nA |
| 2 | T | EREFSTEN | RANGE = HGO = 0 | 1000 | 1000 | 1100 | 1500 | nA |
| 3 | T | IREFSTEN ¹ | — | 63 | 70 | 77 | 81 | μA |
| 4 | T | RTC | Does not include clock source current | 50 | 75 | 100 | 150 | nA |
| 5 | T | LVD ¹ | LVDSE = 1 | 90 | 100 | 110 | 115 | μA |
| 6 | T | ACMP ¹ | Not using the bandgap (BGBE = 0) | 18 | 20 | 22 | 23 | μA |
| 7 | T | ADC ¹ | ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0) | 95 | 106 | 114 | 120 | μA |

Electrical Characteristics

¹ Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Reference [Figure 11](#) and [Figure 12](#) for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = -40 to 85°C Ambient)

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----------------------------|---|---|----------------|---------|--|------|------------|
| 1 | C | Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) | | | | | |
| | | Low range (RANGE = 0) | f_{lo} | 32 | — | 38.4 | kHz |
| | | High range (RANGE = 1), high gain (HGO = 1) | f_{hi} | 1 | — | 16 | MHz |
| | | High range (RANGE = 1), low power (HGO = 0) | f_{hi} | 1 | — | 8 | MHz |
| 2 | D | Load capacitors | | | | | |
| | | Low range (RANGE=0), low power (HGO=0) Other oscillator settings | C_1 C_2 | | See Note ² See Note ³ | | |
| 3 | D | Feedback resistor | | | | | |
| | | Low range, low power (RANGE=0, HGO=0) ² | R_F | — | — | — | M Ω |
| | | Low range, High Gain (RANGE=0, HGO=1) | | — | 10 | — | |
| High range (RANGE=1, HGO=X) | — | 1 | | — | | | |
| 4 | D | Series resistor — | | | | | |
| | | Low range, low power (RANGE = 0, HGO = 0) ² | R_S | — | — | — | k Ω |
| | | Low range, high gain (RANGE = 0, HGO = 1) | | — | 100 | — | |
| | | High range, low power (RANGE = 1, HGO = 0) | | — | 0 | — | |
| | | High range, high gain (RANGE = 1, HGO = 1) | | — | 0 | 0 | |
| | | ≥ 8 MHz | | — | 0 | 10 | |
| 4 MHz | — | 0 | | 20 | | | |
| | | 1 MHz | — | 0 | 20 | | |
| 5 | C | Crystal start-up time ⁴ | | | | | |
| | | Low range, low power | t_{CSTL} | — | 200 | — | ms |
| | | Low range, high power | | — | 400 | — | |
| | | High range, low power | t_{CSTH} | — | 5 | — | |
| | | High range, high power | | — | 15 | — | |
| | | | | | | | |
| 6 | D | Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) | | | | | |
| | | FEE mode | f_{extal} | 0.03125 | — | 40 | MHz |
| | | FBE or FBELP mode | | 0 | — | 40 | MHz |

¹ Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.

² Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

³ See crystal or resonator manufacturer's recommendation.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

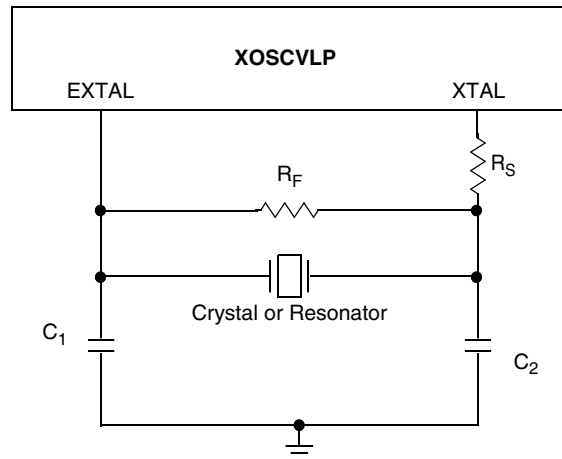


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

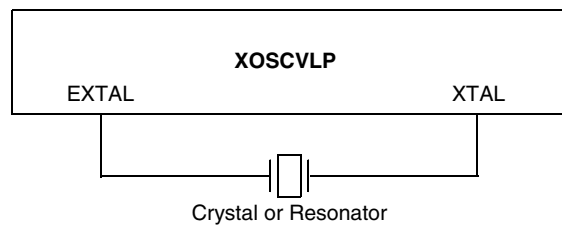


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

 Table 11. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit | |
|-----|---|---|--|-----------------------|----------------------|-----------|--------------------|-----|
| 1 | P | Average internal reference frequency — factory trimmed | f_{int_t} | — | 32.768 | — | kHz | |
| 2 | C | Average internal reference frequency — untrimmed | $f_{\text{int}_{ut}}$ | 31.25 | — | 39.06 | kHz | |
| 3 | T | Internal reference start-up time | t_{IRST} | — | 5 | 10 | μs | |
| 4 | P | DCO output frequency trimmed ² | f_{dco_u} | Low range (DFR = 00) | 16 | — | 20 | MHz |
| | P | | | Mid range (DFR = 01) | 32 | — | 40 | |
| | P | | | High range (DFR = 10) | 48 | — | 60 | |
| 5 | P | DCO output frequency ² reference = 32768 Hz and DMX32 = 1 | $f_{\text{dco}_{\text{DMX32}}}$ | Low range (DFR = 00) | — | 19.92 | — | MHz |
| | P | | | Mid range (DFR = 01) | — | 39.85 | — | |
| | P | | | High range (DFR = 10) | — | 59.77 | — | |
| 6 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM) | $\Delta f_{\text{dco}_{\text{res}_t}}$ | — | ± 0.1 | ± 0.2 | $\%f_{\text{dco}}$ | |
| 7 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM) | $\Delta f_{\text{dco}_{\text{res}_t}}$ | — | ± 0.2 | ± 0.4 | $\%f_{\text{dco}}$ | |

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|---------------------|-----|----------------------|-----|-------------|
| 8 | C | Total deviation of trimmed DCO output frequency over voltage and temperature | Δf_{dco_t} | — | 0.5 –1.0 | ±2 | % f_{dco} |
| 9 | C | Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C | Δf_{dco_t} | — | ±0.5 | ±1 | % f_{dco} |
| 10 | C | FLL acquisition time ³ | $t_{Acquire}$ | — | — | 1 | ms |
| 11 | C | Long term jitter of DCO output clock (averaged over 2-ms interval) ⁴ | C_{Jitter} | — | 0.02 | 0.2 | % f_{dco} |

¹ Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

³ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

| Num | C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|----------------------|-----------------------------|----------------------|--------------------|------|
| 1 | D | Bus frequency ($t_{cyc} = 1/f_{Bus}$) $V_{DD} \leq 2.1V$ $2.1 < V_{DD} \leq 2.4V$ $V_{DD} > 2.4Vs$ | f_{Bus} | DC | — | 10 20 25.165 | MHz |
| 2 | D | Internal low power oscillator period | t_{LPO} | 700 | — | 1300 | μs |
| 3 | D | External reset pulse width ² | t_{extrst} | 100 | — | — | ns |
| 4 | D | Reset low drive | t_{rstdrv} | $34 \times t_{cyc}$ | — | — | ns |
| 5 | D | BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes | t_{MSSU} | 500 | — | — | ns |
| 6 | D | BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³ | t_{MSH} | 100 | — | — | μs |
| 7 | D | IRQ pulse width Asynchronous path ² Synchronous path ⁴ | t_{ILIH}, t_{IHIL} | 100 $1.5 \times t_{cyc}$ | — — | — — | ns |

Table 12. Control Timing (continued)

| Num | C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|-------------------------|-----------------------------|----------------------|--------|---------|
| 8 | D | Keyboard interrupt pulse width Asynchronous path ² Synchronous path ⁵ | t_{LILH} , t_{HIL} | 100 $1.5 \times t_{cyc}$ | — — | — — | ns |
| 9 | C | Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) ⁵ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | t_{Rise} , t_{Fall} | — — | 8 31 | — — | ns |
| | | Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | t_{Rise} , t_{Fall} | — — | 7 24 | — — | ns |
| 10 | C | Voltage regulator recovery time | t_{VRR} | — | 4 | — | μ s |

¹ Typical values are based on characterization data at $V_{DD} = 3.0$ V, 25 °C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ To enter BDM mode following a POR, BKGD/MS must be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

⁴ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁵ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

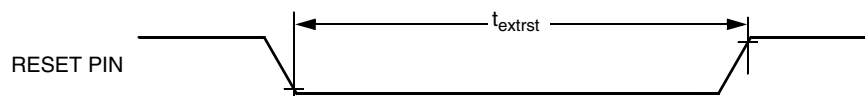
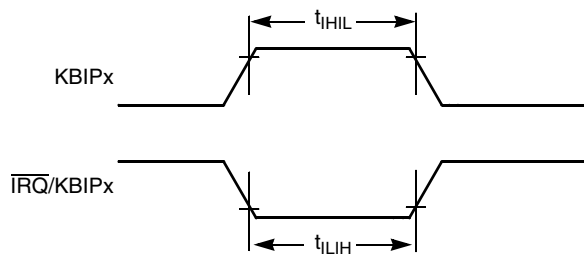


Figure 13. Reset Timing


 Figure 14. $\overline{IRQ}/KBIPx$ Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 13. TPM Input Timing

| No. | C | Function | Symbol | Min | Max | Unit |
|-----|---|---------------------------|------------|-----|-------------|-----------|
| 1 | D | External clock frequency | f_{TCLK} | 0 | $f_{Bus}/4$ | Hz |
| 2 | D | External clock period | t_{TCLK} | 4 | — | t_{cyc} |
| 3 | D | External clock high time | t_{clkh} | 1.5 | — | t_{cyc} |
| 4 | D | External clock low time | t_{clkl} | 1.5 | — | t_{cyc} |
| 5 | D | Input capture pulse width | t_{ICPW} | 1.5 | — | t_{cyc} |

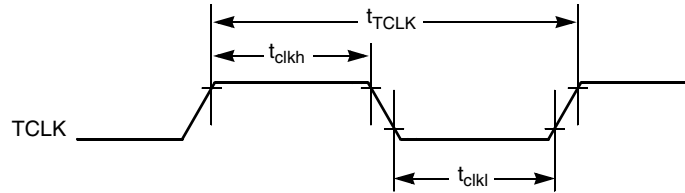


Figure 15. Timer External Clock

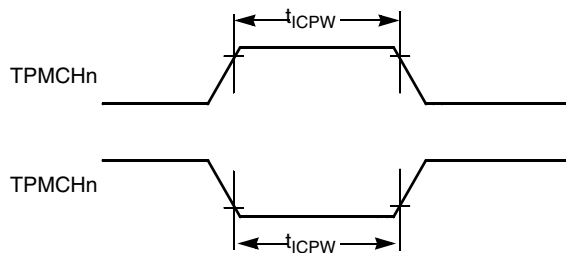


Figure 16. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 14 and Figure 17 through Figure 20 describe the timing requirements for the SPI system.

Table 14. SPI Timing

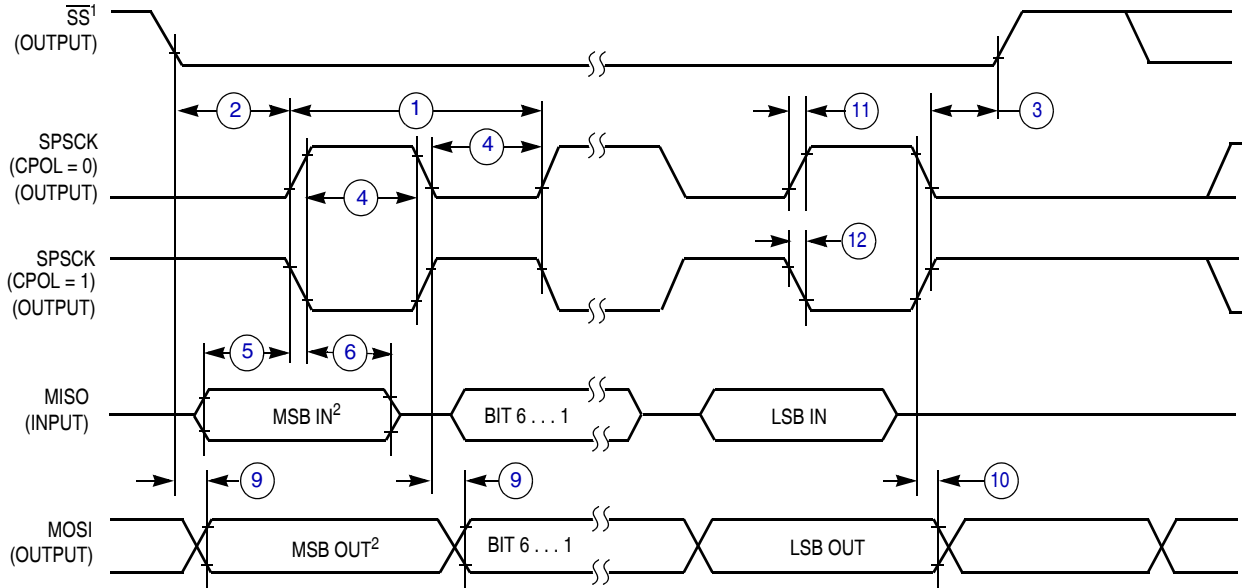
| No. | C | Function | Symbol | Min | Max | Unit |
|-----|---|--|-------------|---------------------|------------------------------|--------------------------|
| — | D | Operating frequency Master Slave | f_{op} | $f_{Bus}/2048$ 0 | $f_{Bus}/2^1$ $f_{Bus}/4$ | Hz |
| 1 | D | SPSCK period Master Slave | t_{SPSCK} | 2 4 | 2048 — | t_{cyc} t_{cyc} |
| 2 | D | Enable lead time Master Slave | t_{Lead} | 1/2 1 | — — | t_{SPSCK} t_{cyc} |
| 3 | D | Enable lag time Master Slave | t_{Lag} | 1/2 1 | — — | t_{SPSCK} t_{cyc} |

Table 14. SPI Timing (continued)

| No. | C | Function | Symbol | Min | Max | Unit |
|-----|---|--------------------------------|--------------|----------------|----------------|-----------|
| 4 | D | Clock (SPSCK) high or low time | t_{WSPSCK} | $t_{cyc} - 30$ | $1024 t_{cyc}$ | ns |
| | | Master | | $t_{cyc} - 30$ | — | ns |
| 5 | D | Data setup time (inputs) | t_{SU} | 15 | — | ns |
| | | Master | | 15 | — | ns |
| 6 | D | Data hold time (inputs) | t_{HI} | 0 | — | ns |
| | | Master | | 25 | — | ns |
| 7 | D | Slave access time | t_a | — | 1 | t_{cyc} |
| 8 | D | Slave MISO disable time | t_{dis} | — | 1 | t_{cyc} |
| 9 | D | Data valid (after SPSCK edge) | t_v | — | 25 | ns |
| | | Master | | — | 25 | ns |
| 10 | D | Data hold time (outputs) | t_{HO} | 0 | — | ns |
| | | Master | | 0 | — | ns |
| 11 | D | Rise time | t_{RI} | — | $t_{cyc} - 25$ | ns |
| | | Input | | — | 25 | ns |
| 12 | D | Fall time | t_{FI} | — | $t_{cyc} - 25$ | ns |
| | | Input | | — | 25 | ns |
| | | Output | t_{FO} | — | — | ns |

¹ Max operating frequency limited to 8 MHz when input filter disabled and high output drive strength enabled. Max operating frequency limited to 5 MHz when input filter enabled and high output drive strength disabled.

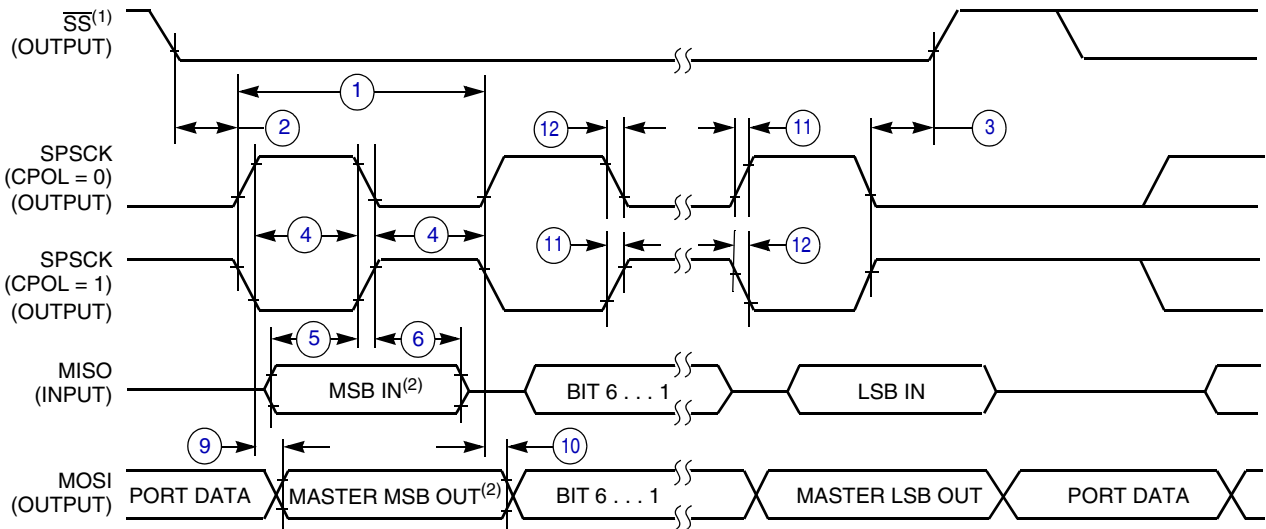
Electrical Characteristics



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

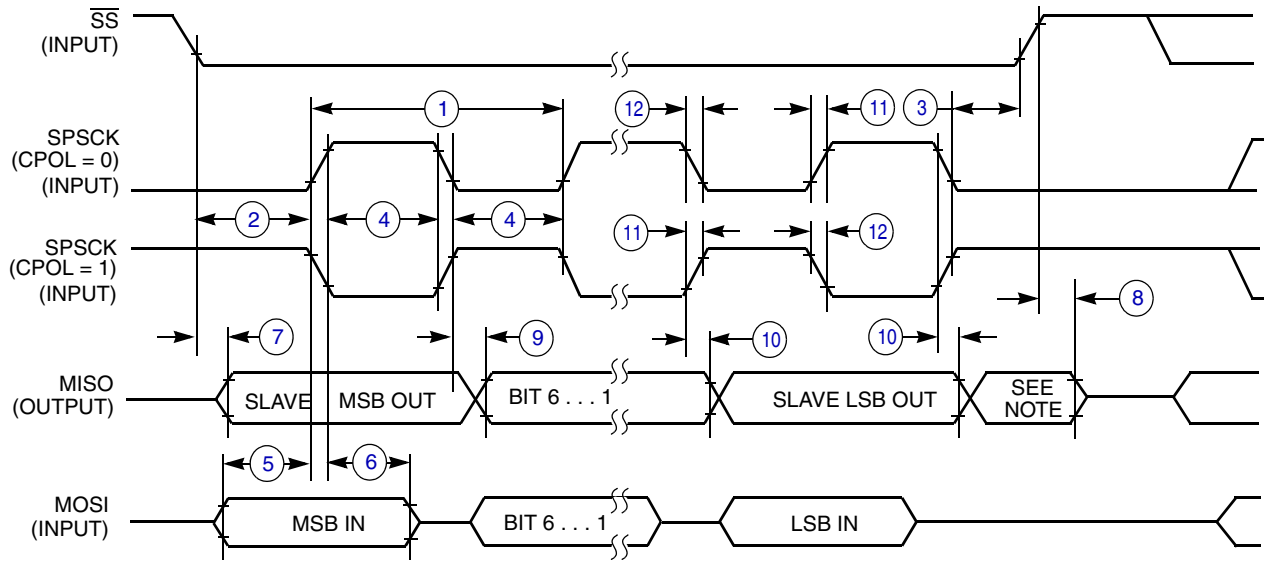
Figure 17. SPI Master Timing (CPHA = 0)



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

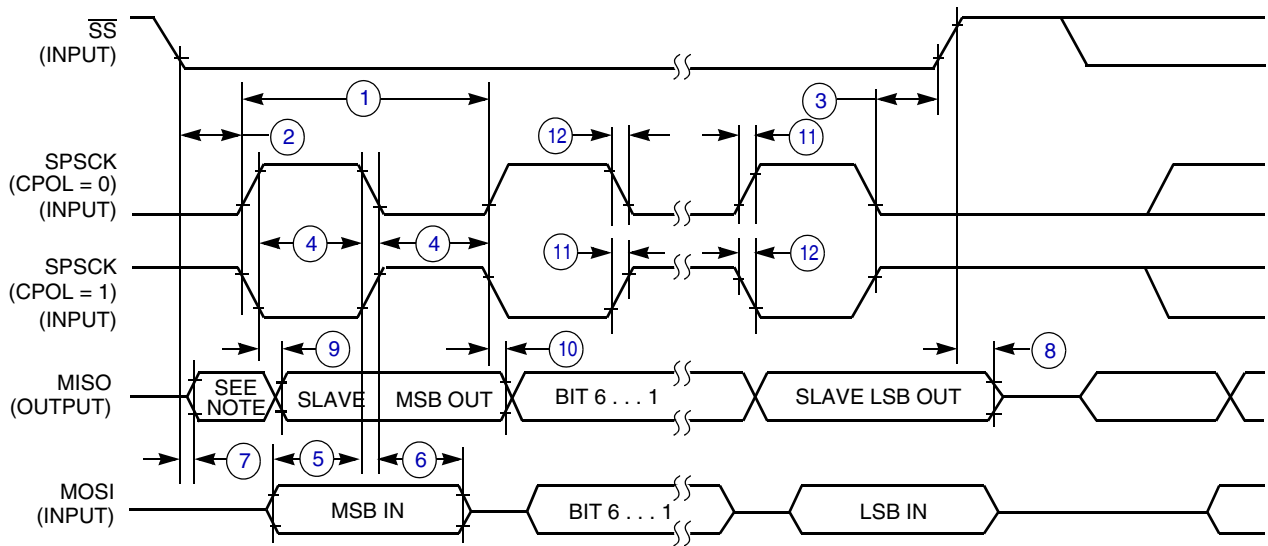
Figure 18. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 19. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 20. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

| C | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|--|-------------|----------------|---------|----------|---------|
| D | Supply voltage | V_{DD} | 1.8 | — | 3.6 | V |
| P | Supply current (active) | I_{DDAC} | — | 20 | 35 | μA |
| D | Analog input voltage | V_{AIN} | $V_{SS} - 0.3$ | — | V_{DD} | V |
| P | Analog input offset voltage | V_{AIO} | — | 20 | 40 | mV |
| C | Analog comparator hysteresis | V_H | 3.0 | 9.0 | 15.0 | mV |
| P | Analog input leakage current | I_{ALKG} | — | — | 1.0 | μA |
| C | Analog comparator initialization delay | t_{AINIT} | — | — | 1.0 | μs |

3.12 ADC Characteristics

Table 16. 12-Bit ADC Operating Conditions

| C | Characteristic | Conditions | Symb | Min | Typical ¹ | Max | Unit | Comment |
|---|----------------------------|---|-------------------|------------|----------------------|------------|------------|-----------------|
| D | Supply voltage | Absolute | V_{DDAD} | 1.8 | — | 3.6 | V | — |
| | | Delta to V_{DD} ($V_{DD} - V_{DDAD}$) ² | ΔV_{DDAD} | -100 | 0 | 100 | mV | — |
| D | Ground voltage | Delta to V_{SS} ($V_{SS} - V_{SSAD}$) ² | ΔV_{SSAD} | -100 | 0 | 100 | mV | — |
| D | Input voltage | — | V_{ADIN} | V_{REFL} | — | V_{REFH} | V | — |
| C | Input capacitance | — | C_{ADIN} | — | 4.5 | 5.5 | pF | — |
| C | Input resistance | — | R_{ADIN} | — | 5 | 7 | k Ω | — |
| C | Analog source resistance | 12-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | R_{AS} | — | — | 2 | k Ω | External to MCU |
| | | 10-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | | — | — | 5 | | |
| | | 8-bit mode (all valid f_{ADCK}) | | — | — | 10 | | |
| D | ADC conversion clock freq. | High speed (ADLPC = 0) | f_{ADCK} | 0.4 | — | 8.0 | MHz | — |
| | | Low power (ADLPC = 1) | | 0.4 | — | 4.0 | | |

¹ Typical values assume $V_{DDAD} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

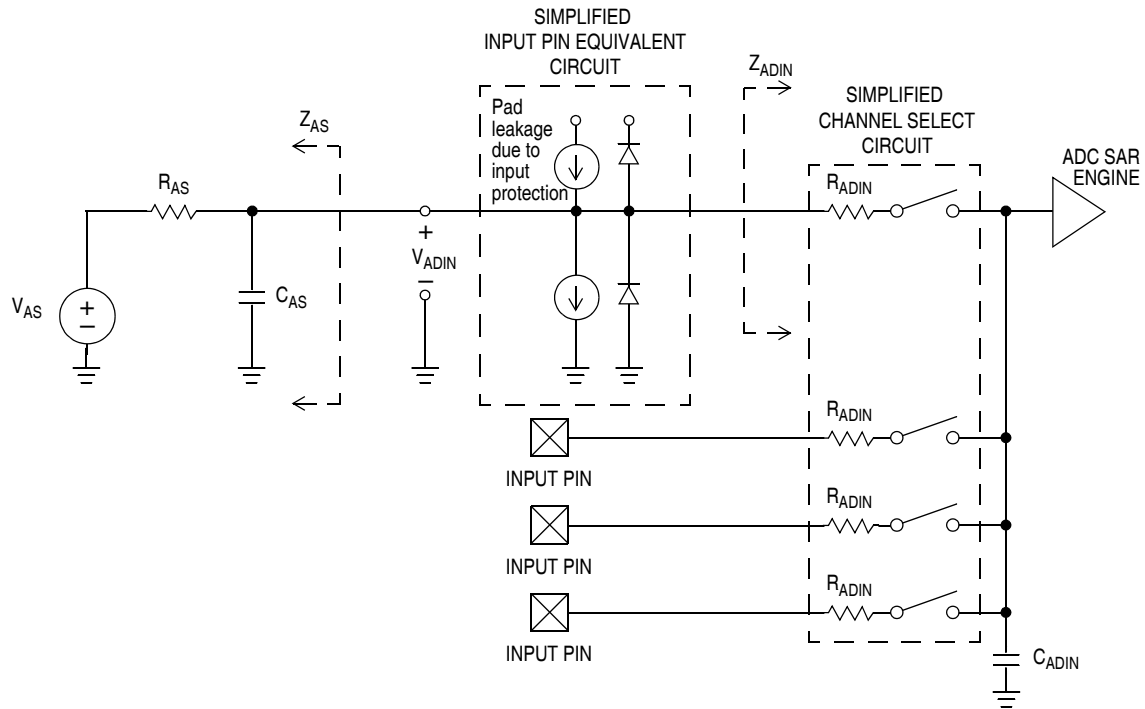


Figure 21. ADC Input Impedance Equivalency Diagram

Table 17. ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

| C | Characteristic | Conditions | Symbol | Min | Typ ¹ | Max | Unit | Comment |
|---|---|------------------------|-------------|------|------------------|-----|---------------|---------------------------|
| T | Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1 | | I_{DDAD} | — | 120 | — | μA | |
| T | Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1 | | I_{DDAD} | — | 202 | — | μA | |
| T | Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1 | | I_{DDAD} | — | 288 | — | μA | |
| P | Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1 | | I_{DDAD} | — | 0.532 | 1 | mA | |
| P | ADC asynchronous clock source | High speed (ADLPC = 0) | f_{ADACK} | 2 | 3.3 | 5 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | | Low power (ADLPC = 1) | | 1.25 | 2 | 3.3 | | |

Electrical Characteristics

Table 17. ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$) (continued)

| C | Characteristic | Conditions | Symbol | Min | Typ ¹ | Max | Unit | Comment |
|---|---|--------------------------------------|--------------|-----|------------------|--------------|------------------|--|
| P | Conversion time (including sample time) | Short sample (ADLSMP = 0) | t_{ADC} | — | 20 | — | ADCK cycles | See reference manual for conversion time variances |
| | | Long sample (ADLSMP = 1) | | — | 40 | — | | |
| P | Sample time | Short sample (ADLSMP = 0) | t_{ADS} | — | 3.5 | — | ADCK cycles | |
| | | Long sample (ADLSMP = 1) | | — | 23.5 | — | | |
| D | Temp sensor slope | -40 °C– 25 °C | m | — | 1.646 | — | mV/°C | |
| | | 25 °C– 85 °C | | — | 1.769 | — | | |
| D | Temp sensor voltage | 25 °C | V_{TEMP25} | — | 701.2 | — | mV | |
| T | Total unadjusted error | 12-bit mode, $3.6 > V_{DDAD} > 2.7$ | E_{TUE} | — | -1 to 3 | -2.5 to 5.5 | LSB ² | Includes quantization |
| T | | 12-bit mode, $2.7 > V_{DDAD} > 1.8V$ | | — | -1 to 3 | -3.0 to 6.5 | | |
| P | | 10-bit mode | | — | ±1 | ±2.5 | | |
| P | | 8-bit mode | | — | ±0.5 | ±1.0 | | |
| T | Differential non-linearity | 12-bit mode | DNL | — | ±1.0 | -1.5 to 2.0 | LSB ² | |
| P | | 10-bit mode ³ | | — | ±0.5 | ±1.0 | | |
| P | | 8-bit mode ³ | | — | ±0.3 | ±0.5 | | |
| T | Integral non-linearity | 12-bit mode | INL | — | ±1.5 | -2.5 to 2.75 | LSB ² | |
| T | | 10-bit mode | | — | ±0.5 | ±1.0 | | |
| T | | 8-bit mode | | — | ±0.3 | ±0.5 | | |
| T | Zero-scale error | 12-bit mode | E_{ZS} | — | ±1.5 | ±2.5 | LSB ² | $V_{ADIN} = V_{SSAD}$ |
| P | | 10-bit mode | | — | ±0.5 | ±1.5 | | |
| P | | 8-bit mode | | — | ±0.5 | ±0.5 | | |
| T | Full-scale error | 12-bit mode | E_{FS} | — | ±1.0 | -3.5 to 1.0 | LSB ² | $V_{ADIN} = V_{DDAD}$ |
| P | | 10-bit mode | | — | ±0.5 | ±1 | | |
| P | | 8-bit mode | | — | ±0.5 | ±0.5 | | |
| D | Quantization error | 12-bit mode | E_Q | — | -1 to 0 | — | LSB ² | |
| | | 10-bit mode | | — | — | ±0.5 | | |
| | | 8-bit mode | | — | — | ±0.5 | | |
| D | Input leakage error | 12-bit mode | E_{IL} | — | ±2 | — | LSB ² | Pad leakage ⁴ * R_{AS} |
| | | 10-bit mode | | — | ±0.2 | ±4 | | |
| | | 8-bit mode | | — | ±0.1 | ±1.2 | | |

- ¹ Typical values assume $V_{DDAD} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^\circ\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.
- ² $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
- ³ Monotonicity and No-missing-codes guaranteed in 10-bit and 8-bit modes
- ⁴ Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for flash memory. Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see MC9S08QE32 Series Reference Manual Chapter 4 Memory.

Table 18. Flash Characteristics

| C | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|--|-------------------------|--------|--------------|--------|-------------------|
| D | Supply voltage for program/erase -40 °C to 85 °C | $V_{\text{prog/erase}}$ | 1.8 | — | 3.6 | V |
| D | Supply voltage for read operation | V_{Read} | 1.8 | — | 3.6 | V |
| D | Internal FCLK frequency ¹ | f_{FCLK} | 150 | — | 200 | kHz |
| D | Internal FCLK period (1/FCLK) | t_{FcyC} | 5 | — | 6.67 | μs |
| P | Byte program time (random location) ⁽²⁾ | t_{prog} | 9 | | | t_{FcyC} |
| P | Byte program time (burst mode) ⁽²⁾ | t_{Burst} | 4 | | | t_{FcyC} |
| P | Page erase time ² | t_{Page} | 4000 | | | t_{FcyC} |
| P | Mass erase time ⁽²⁾ | t_{Mass} | 20,000 | | | t_{FcyC} |
| | Byte program current ³ | R_{IDDBP} | — | 4 | — | mA |
| | Page erase current ³ | R_{IDDPE} | — | 6 | — | mA |
| C | Program/erase endurance ⁴ T_L to $T_H = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ $T = 25\text{ }^\circ\text{C}$ | | 10,000 | — 100,000 | — — | cycles |
| C | Data retention ⁵ | $t_{\text{D_ret}}$ | 15 | 100 | — | years |

¹ The frequency of this clock is controlled by software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information is supplied for calculating approximate time to program and erase.

³ The program and erase currents are additional to the standard run I_{DD} . These values are measured at room temperatures with $V_{DD} = 3.0\text{ V}$, bus frequency = 4.0 MHz.

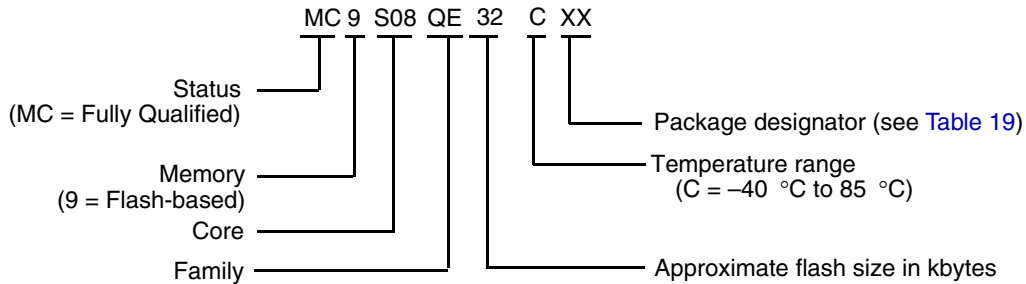
⁴ **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

⁵ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

4 Ordering Information

This section contains ordering information for the MC9S08QE32 series of MCUs.

Example of the device numbering system:



5 Package Information

Table 19. Package Descriptions

| Pin Count | Package Type | Abbreviation | Designator | Case No. | Document No. |
|-----------|----------------------------------|--------------|------------|----------|-----------------------------|
| 48 | Quad Flat No-Leads | QFN | FT | 1314 | 98ARH99048A |
| 44 | Low Quad Flat Package | LQFP | LD | 824D | 98ASS23225W |
| 32 | Low Quad Flat Package | LQFP | LC | 873A | 98ASH70029A |
| 32 | Quad Flat No-Leads | QFN | FM | 1582 | 98ARE10566D |
| 28 | Small Outline Integrated Circuit | SOIC | WL | 751F | 98ASB42345B |

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 19. For the latest available drawings please visit our web site (<http://www.freescale.com>) and enter the package's document number into the keyword search box.

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