



HIGH-SPEED 3.3V 256K x 36 SYNCHRONOUS BANK-SWITCHABLE DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

IDT70V7519S

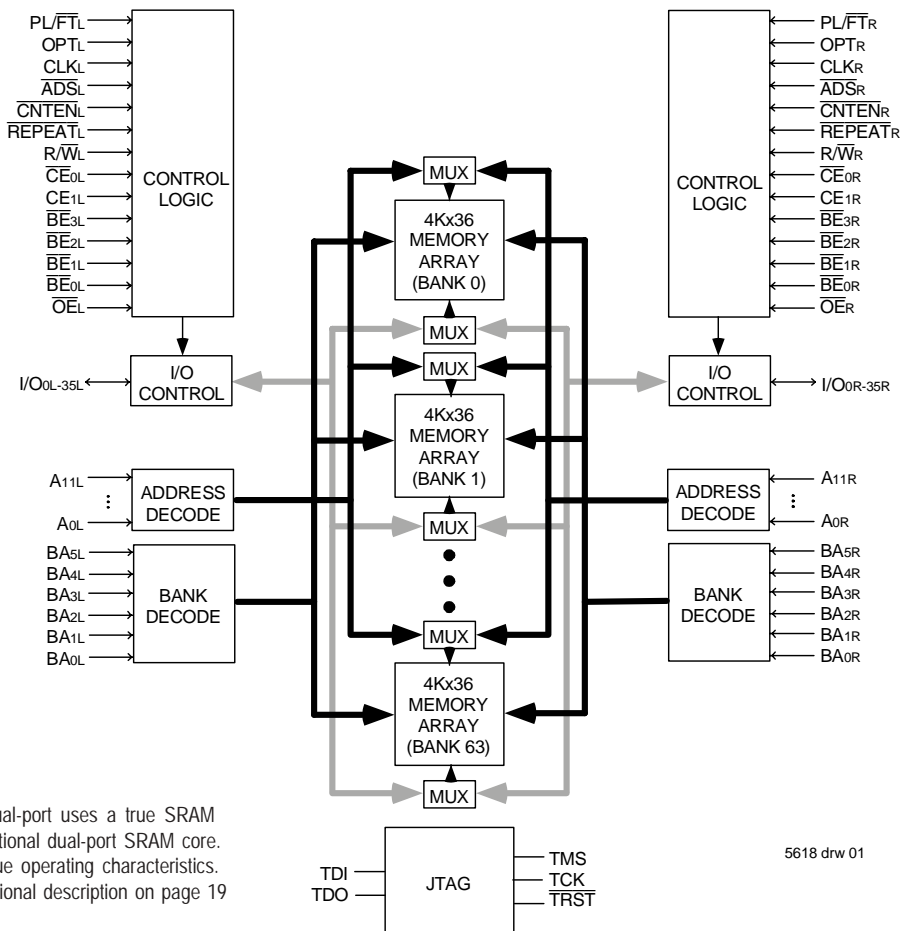
LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features:

- ◆ 256K x 36 Synchronous Bank-Switchable Dual-ported SRAM Architecture
 - 64 independent 4K x 36 banks
 - 9 megabits of memory on chip
- ◆ Bank access controlled via bank address pins
- ◆ High-speed data access
 - Commercial: 3.4ns(200MHz)/3.6ns(166MHz)/4.2ns(133MHz) (max.)
 - Industrial: 3.6ns(166MHz)/4.2ns(133MHz) (max.)
- ◆ Selectable Pipelined or Flow-Through output mode
- ◆ Counter enable and repeat features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 5ns cycle time, 200MHz operation (14Gbps bandwidth)
 - Fast 3.4ns clock to data out

- 1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz
- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, 3.3V (±150mV) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available at 166MHz and 133MHz
- ◆ Available in a 208-pin Plastic Quad Flatpack (PQFP), 208-pin fine pitch Ball Grid Array (fpBGA), and 256-pin Ball Grid Array (BGA)
- ◆ Supports JTAG features compliant with IEEE 1149.1
- ◆ Green parts available, see ordering information

Functional Block Diagram



NOTE:

1. The Bank-Switchable dual-port uses a true SRAM core instead of the traditional dual-port SRAM core. As a result, it has unique operating characteristics. Please refer to the functional description on page 19 for details.

JUNE 2015

Description:

The IDT70V7519 is a high-speed 256Kx36 (9Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 4Kx36 banks. The device has two independent ports with separate control, address, and I/O pins for each port, allowing each port to access any 4Kx36 memory block not already accessed by the other port. Accesses by the ports into specific banks are controlled via the bank address pins under the user's direct control.

Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data

register, the IDT70V7519 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by CE0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode. The dual chip enables also facilitate depth expansion.

The 70V7519 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V. Please refer also to the functional description on page 19.

Pin Configuration^(1,2,3,4)

A1 IO19L	A2 IO18L	A3 VSS	A4 TDO	A5 NC	A6 BA4L	A7 BA0L	A8 A8L	A9 BE1L	A10 VDD	A11 CLKL	A12 CNTENL	A13 A4L	A14 A0L	A15 OPTL	A16 IO17L	A17 VSS	
B1 IO20R	B2 VSS	B3 IO18R	B4 TDI	B5 BA5L	B6 BA1L	B7 A9L	B8 BE2L	B9 CE0L	B10 VSS	B11 ADSL	B12 A5L	B13 A1L	B14 VSS	B15 VDDQR	B16 IO16L	B17 IO15R	
C1 VDDQL	C2 IO19R	C3 VDDQR	C4 PL/FTL	C5 NC	C6 BA2L	C7 A10L	C8 BE3L	C9 CE1L	C10 VSS	C11 R/WL	C12 A6L	C13 A2L	C14 VDD	C15 IO16R	C16 IO15L	C17 VSS	
D1 IO22L	D2 VSS	D3 IO21L	D4 IO20L	D5 BA3L	D6 A11L	D7 A7L	D8 BE0L	D9 VDD	D10 OEL	D11 REPEATL	D12 A3L	D13 VDD	D14 IO17R	D15 VDDQL	D16 IO14L	D17 IO14R	
E1 IO23L	E2 IO22R	E3 VDDQR	E4 IO21R	<p style="text-align: center;">70V7519BF BF208⁽⁵⁾</p> <p style="text-align: center;">208-Pin fpBGA Top View⁽⁶⁾</p>										E14 IO12L	E15 IO13R	E16 VSS	E17 IO13L
F1 VDDQL	F2 IO23R	F3 IO24L	F4 VSS											F14 VSS	F15 IO12R	F16 IO11L	F17 VDDQR
G1 IO26L	G2 VSS	G3 IO25L	G4 IO24R											G14 IO9L	G15 VDDQL	G16 IO10L	G17 IO11R
H1 VDD	H2 IO26R	H3 VDDQR	H4 IO25R											H14 VDD	H15 IO9R	H16 VSS	H17 IO10R
J1 VDDQL	J2 VDD	J3 VSS	J4 VSS											J14 VSS	J15 VDD	J16 VSS	J17 VDDQR
K1 IO28R	K2 VSS	K3 IO27R	K4 VSS											K14 IO7R	K15 VDDQL	K16 IO8R	K17 VSS
L1 IO29R	L2 IO28L	L3 VDDQR	L4 IO27L											L14 IO6R	L15 IO7L	L16 VSS	L17 IO8L
M1 VDDQL	M2 IO29L	M3 IO30R	M4 VSS											M14 VSS	M15 IO6L	M16 IO5R	M17 VDDQR
N1 IO31L	N2 VSS	N3 IO31R	N4 IO30L											N14 IO3R	N15 VDDQL	N16 IO4R	N17 IO5L
P1 IO32R	P2 IO32L	P3 VDDQR	P4 IO35R											P5 TRST	P6 BA4R	P7 BA0R	P8 A8R
R1 VSS	R2 IO33L	R3 IO34R	R4 TCK	R5 BA5R	R6 BA1R	R7 A9R	R8 BE2R	R9 CE0R	R10 VSS	R11 ADSR	R12 A5R	R13 A1R	R14 VSS	R15 VDDQL	R16 IO1R	R17 VDDQR	
T1 IO33R	T2 IO34L	T3 VDDQL	T4 TMS	T5 NC	T6 BA2R	T7 A10R	T8 BE3R	T9 CE1R	T10 VSS	T11 R/WR	T12 A6R	T13 A2R	T14 VSS	T15 IO0R	T16 VSS	T17 IO2R	
U1 VSS	U2 IO35L	U3 PL/FTR	U4 NC	U5 BA3R	U6 A11R	U7 A7R	U8 BE0R	U9 VDD	U10 OER	U11 REPEATR	U12 A3R	U13 A0R	U14 VDD	U15 OPTR	U16 IO0L	U17 IO1L	

5618 drw 02c

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)70V7519BC
BC256⁽⁵⁾256-Pin BGA
Top View⁽⁶⁾

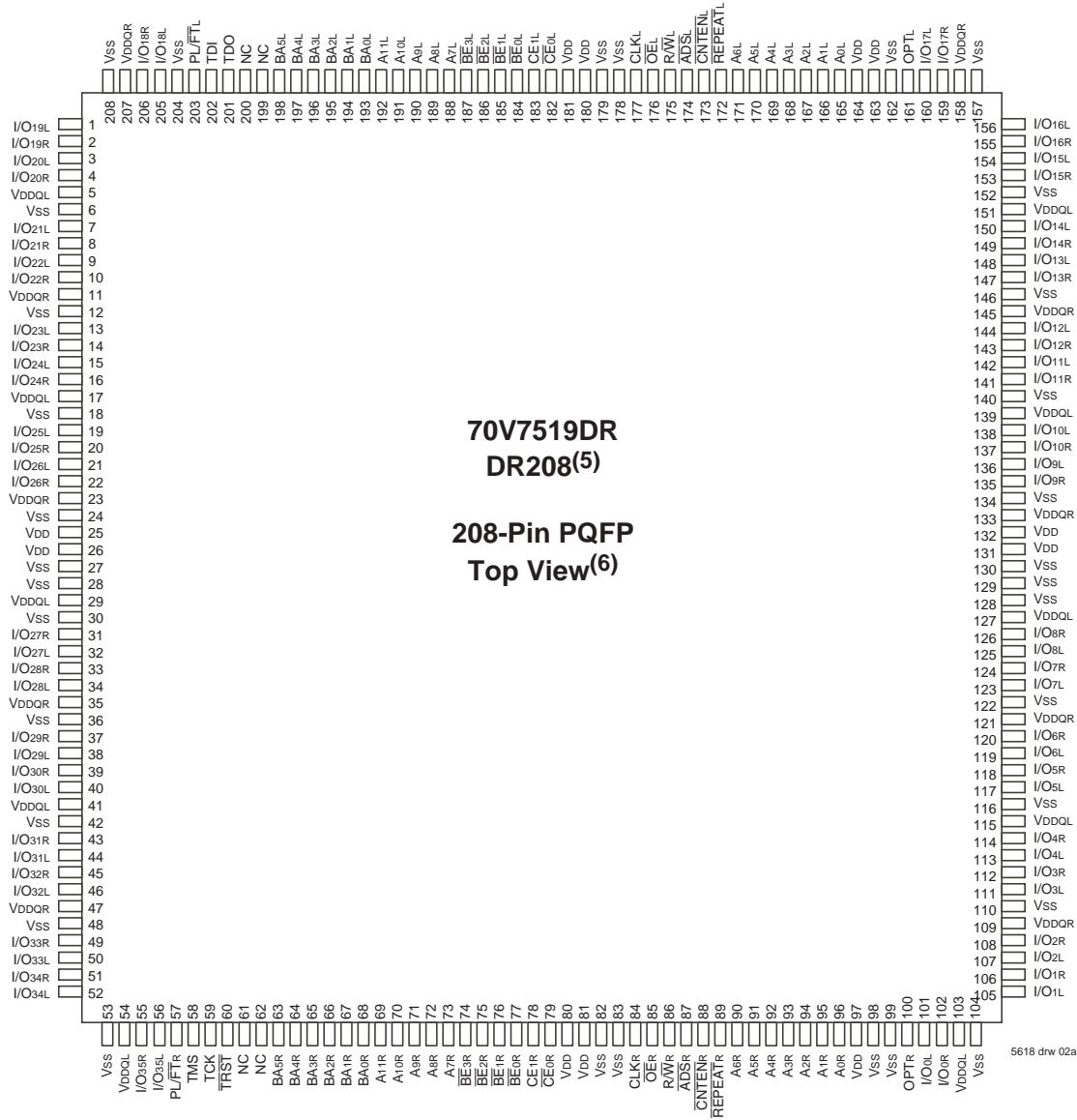
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
NC	TDI	NC	BA5L	BA2L	A11L	A8L	$\overline{BE}2L$	CE1L	$\overline{OE}L$	$\overline{CNTEN}L$	A5L	A2L	A0L	NC	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16
I/O18L	NC	TDO	NC	BA3L	BA0L	A9L	$\overline{BE}3L$	$\overline{CE}0L$	R/WL	$\overline{REPEAT}L$	A4L	A1L	VDD	I/O17L	NC
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16
I/O18R	I/O19L	VSS	BA4L	BA1L	A10L	A7L	$\overline{BE}1L$	$\overline{BE}0L$	CLKL	$\overline{ADS}L$	A6L	A3L	OPTL	I/O17R	I/O16L
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
I/O20R	I/O19R	I/O20L	PL/ $\overline{FT}L$	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDD	I/O15R	I/O15L	I/O16R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16
I/O21R	I/O21L	I/O22L	VDDQL	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQR	I/O13L	I/O14L	I/O14R
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16
I/O23L	I/O22R	I/O23R	VDDQL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQR	I/O12R	I/O13R	I/O12L
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
I/O24R	I/O24L	I/O25L	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O10L	I/O11L	I/O11R
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16
I/O26L	I/O25R	I/O26R	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O9R	I/O9L	I/O10R
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
I/O27L	I/O28R	I/O27R	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O8R	I/O7R	I/O8L
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16
I/O29R	I/O29L	I/O28L	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O6R	I/O6L	I/O7L
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
I/O30L	I/O31R	I/O30R	VDDQR	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQL	I/O5L	I/O4R	I/O5R
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16
I/O32R	I/O32L	I/O31L	VDDQR	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQL	I/O3R	I/O3L	I/O4L
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16
I/O33L	I/O34R	I/O33R	PL/ $\overline{FT}R$	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDD	I/O2L	I/O1R	I/O2R
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
I/O35R	I/O34L	TMS	BA4R	BA1R	A10R	A7R	$\overline{BE}1R$	$\overline{BE}0R$	CLKR	$\overline{ADS}R$	A6R	A3R	I/O0L	I/O0R	I/O1L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
I/O35L	NC	\overline{TRST}	NC	BA3R	BA0R	A9R	$\overline{BE}3R$	$\overline{CE}0R$	R/WR	$\overline{REPEAT}R$	A4R	A1R	OPTR	NC	NC
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
NC	TCK	NC	BA5R	BA2R	A11R	A8R	$\overline{BE}2R$	CE1R	$\overline{OE}R$	$\overline{CNTEN}R$	A5R	A2R	A0R	NC	NC

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NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)



NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE _{1L}	\overline{CE}_{0R} , CE _{1R}	Chip Enables
R/ \overline{WL}	R/ \overline{WR}	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
BA _{0L} - BA _{5L}	BA _{0R} - BA _{5R}	Bank Address ⁽⁴⁾
A _{0L} - A _{11L}	A _{0R} - A _{11R}	Address
I/O _{0L} - I/O _{35L}	I/O _{0R} - I/O _{35R}	Data Input/Output
CLK _L	CLK _R	Clock
PL/ \overline{FT}_L	PL/ \overline{FT}_R	Pipeline/Flow-Through
\overline{ADS}_L	\overline{ADS}_R	Address Strobe Enable
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{REPEAT}_L	\overline{REPEAT}_R	Counter Repeat ⁽³⁾
\overline{BE}_{0L} - \overline{BE}_{3L}	\overline{BE}_{0R} - \overline{BE}_{3R}	Byte Enables (9-bit bytes)
V _{DD0L}	V _{DD0R}	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾
OPT _L	OPT _R	Option for selecting V _{DD0x} ^(1,2)
V _{DD}		Power (3.3V) ⁽¹⁾
V _{SS}		Ground (0V)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz)
TMS		Test Mode Select
\overline{TRST}		Reset (Initialize TAP Controller)

5618 tbl 01

NOTES:

1. V_{DD}, OPT_x, and V_{DD0x} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. OPT_x selects the operating voltage levels for the I/Os and controls on that port. If OPT_x is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DD0x} must be supplied at 3.3V. If OPT_x is set to VIL (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DD0x} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
3. When \overline{REPEAT}_x is asserted, the counter will reset to the last valid address loaded via \overline{ADS}_x .
4. Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e., BA_{0L} - BA_{5L} ≠ BA_{0R} - BA_{5R}). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

Truth Table I—Read/Write and Enable Control^(1,2,3,4)

\overline{OE}^3	CLK	\overline{CE}_0	CE ₁	\overline{BE}_3	\overline{BE}_2	\overline{BE}_1	\overline{BE}_0	R/W	Byte 3 I/O ₂₇₋₃₅	Byte 2 I/O ₁₈₋₂₆	Byte 1 I/O ₉₋₁₇	Byte 0 I/O ₀₋₈	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	D _{IN}	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	High-Z	High-Z	D _{IN}	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	D _{IN}	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	D _{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	D _{IN}	D _{IN}	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	D _{IN}	D _{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	D _{IN}	D _{IN}	D _{IN}	D _{IN}	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	D _{OUT}	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	D _{OUT}	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	D _{OUT}	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	D _{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	D _{OUT}	D _{OUT}	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	D _{OUT}	D _{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	D _{OUT}	D _{OUT}	D _{OUT}	D _{OUT}	Read All Bytes
H	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{REPEAT} are set as appropriate for address access. Refer to Truth Table II for details.
- \overline{OE} is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

5618 tbl 03

Truth Table II—Address and Address Counter Control^(1,2,7)

Address	Previous Address	Addr Used	CLK	\overline{ADS}	\overline{CNTEN}	$\overline{REPEAT}^{(6)}$	I/O ⁽³⁾	MODE
A _n	X	A _n	↑	L ⁽⁴⁾	X	H	D _{I/O} (n)	External Address Used
X	A _n	A _n + 1	↑	H	L ⁽⁵⁾	H	D _{I/O} (n+1)	Counter Enabled—Internal Address generation
X	A _n + 1	A _n + 1	↑	H	H	H	D _{I/O} (n+1)	External Address Blocked—Counter disabled (A _n + 1 reused)
X	X	A _n	↑	X	X	L ⁽⁴⁾	D _{I/O} (0)	Counter Set to last valid \overline{ADS} load

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/W, \overline{CE}_0 , CE₁, \overline{BE}_n and \overline{OE} .
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- \overline{ADS} and \overline{REPEAT} are independent of all other memory control signals including \overline{CE}_0 , CE₁ and \overline{BE}_n .
- The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including \overline{CE}_0 , CE₁, \overline{BE}_n .
- When \overline{REPEAT} is asserted, the counter will reset to the last valid address loaded via \overline{ADS} . This value is not set at power-up: a known location should be loaded via \overline{ADS} during initialization if desired. Any subsequent \overline{ADS} access during operations will update the \overline{REPEAT} address location.
- The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0. Refer to Timing Waveform of Counter Repeat, page 18. Care should be taken during operation to avoid having both counters point to the same bank (i.e., ensure BA_{0L} - BA_{5L} ≠ BA_{0R} - BA_{5R}), as this condition will invalidate the access for both ports. Please refer to the functional description on page 19 for details.

5618 tbl 03

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

5618 tbl 04

NOTE:

1. This is the parameter T_A. This is the "instant on" case temperature.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

5618 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.4	2.5	2.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs)	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

5618 tbl 05a

NOTES:

1. Undershoot of V_{IL} ≥ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

5618 tbl 05b

NOTES:

1. Undershoot of V_{IL} ≥ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance⁽¹⁾

(TA = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10.5	pF

5618 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V7519S		Unit
			Min.	Max.	
I _L	Input Leakage Current ⁽¹⁾	V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ}	—	10	μA
I _{LO}	Output Leakage Current ⁽¹⁾	$\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}$, V _{OUT} = 0V to V _{DDQ}	—	10	μA
V _{OL} (3.3V)	Output Low Voltage ⁽²⁾	I _{OL} = +4mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (3.3V)	Output High Voltage ⁽²⁾	I _{OH} = -4mA, V _{DDQ} = Min.	2.4	—	V
V _{OL} (2.5V)	Output Low Voltage ⁽²⁾	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (2.5V)	Output High Voltage ⁽²⁾	I _{OH} = -2mA, V _{DDQ} = Min.	2.0	—	V

5618 tbl 08

NOTES:

- At V_{DD} ≤ 2.0V leakages are undefined.
- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁵⁾ ($V_{DD} = 3.3V \pm 150mV$)

Symbol	Parameter	Test Condition	Version	70V7519S200 ⁽⁷⁾ Com'l Only		70V7519S166 ⁽⁶⁾ Com'l & Ind		70V7519S133 Com'l & Ind		Unit	
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	815	950	675	790	550	645	mA
			IND	S	—	—	675	830	550	675	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	340	410	275	340	250	295	mA
			IND	S	—	—	275	355	250	310	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	690	770	515	640	460	520	mA
			IND	S	—	—	515	660	460	545	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	S	10	30	10	30	10	30	mA
			IND	S	—	—	10	40	10	40	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	690	770	515	640	460	520	mA
			IND	S	—	—	515	660	460	545	

5618 tbl 09

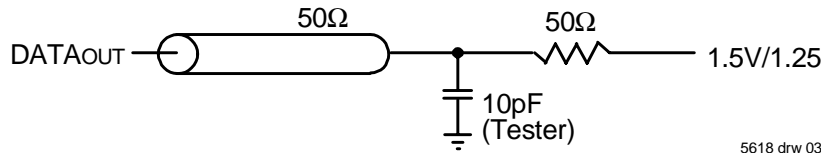
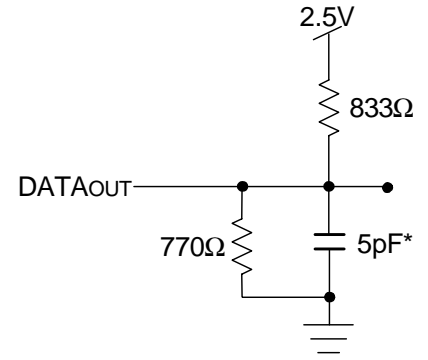
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} dc(f=0) = 120mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DDQ} - 0.2V$
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$ or $CE_{1X} \leq 0.2V$
"X" represents "L" for left port or "R" for right port.
- 166MHz Industrial Temperature not available in BF208 package.
- This speed grade available when $V_{DDQ} = 3.3V$ for a specific port (i.e., $OPTX = V_{IH}$). This speed grade available in BC-256 package only.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V)

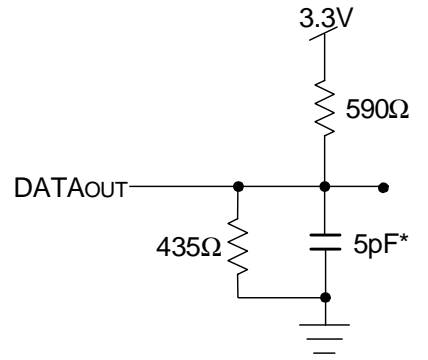
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5618 tbl 10



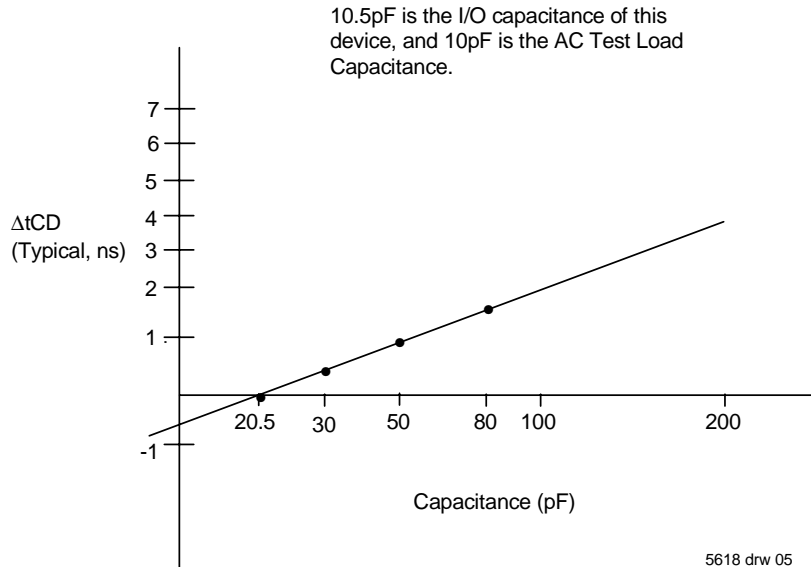
5618 drw 03

Figure 1. AC Output Test load.



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Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.



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Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(2,3) ($V_{DD} = 3.3V \pm 150mV$, $T_A = 0^\circ C$ to $+70^\circ C$)

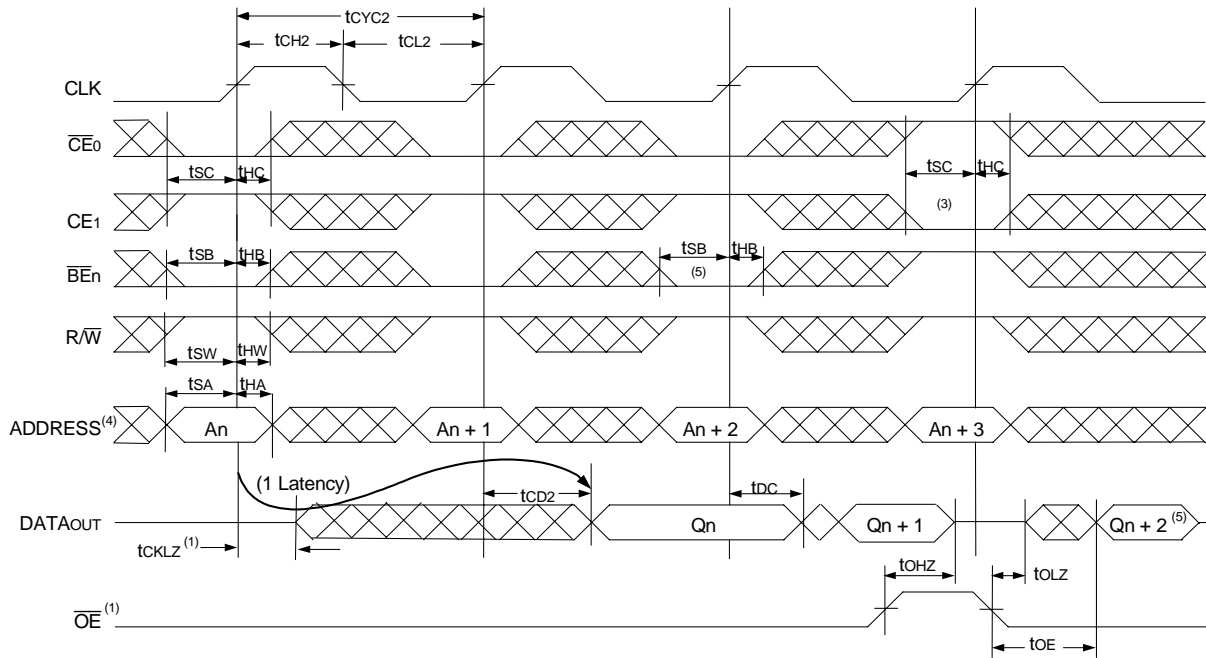
Symbol	Parameter	70V7519S200 ⁽⁹⁾ Com'1 Only		70V7519S166 ^(3,4) Com'1 & Ind		70V7519S133 ⁽³⁾ Com'1 & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽¹⁾	15	—	20	—	25	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽¹⁾	5	—	6	—	7.5	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽¹⁾	5	—	6	—	7	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽¹⁾	5	—	6	—	7	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	2.0	—	2.1	—	2.6	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽¹⁾	2.0	—	2.1	—	2.6	—	ns
t _R	Clock Rise Time	—	1.5	—	1.5	—	1.5	ns
t _F	Clock Fall Time	—	1.5	—	1.5	—	1.5	ns
t _{SA}	Address Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SC}	Chip Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HC}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SB}	Byte Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HB}	Byte Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SW}	R/W Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HW}	R/W Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SD}	Input Data Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HD}	Input Data Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SAD}	\overline{ADS} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HAD}	\overline{ADS} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SCN}	CNTEN Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HCN}	CNTEN Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SRPT}	\overline{REPEAT} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HRPT}	\overline{REPEAT} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{OE}	Output Enable to Data Valid	—	4.0	—	4.0	—	4.2	ns
t _{OLZ}	Output Enable to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
t _{OHZ}	Output Enable to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽¹⁾	—	10	—	12	—	15	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽¹⁾	—	3.4	—	3.6	—	4.2	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t _{CKHZ}	Clock High to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CKLZ}	Clock High to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
Port-to-Port Delay								
t _{CO}	Clock-to-Clock Offset	5.0	—	6.0	—	7.5	—	ns

5618 tbl 11

NOTES:

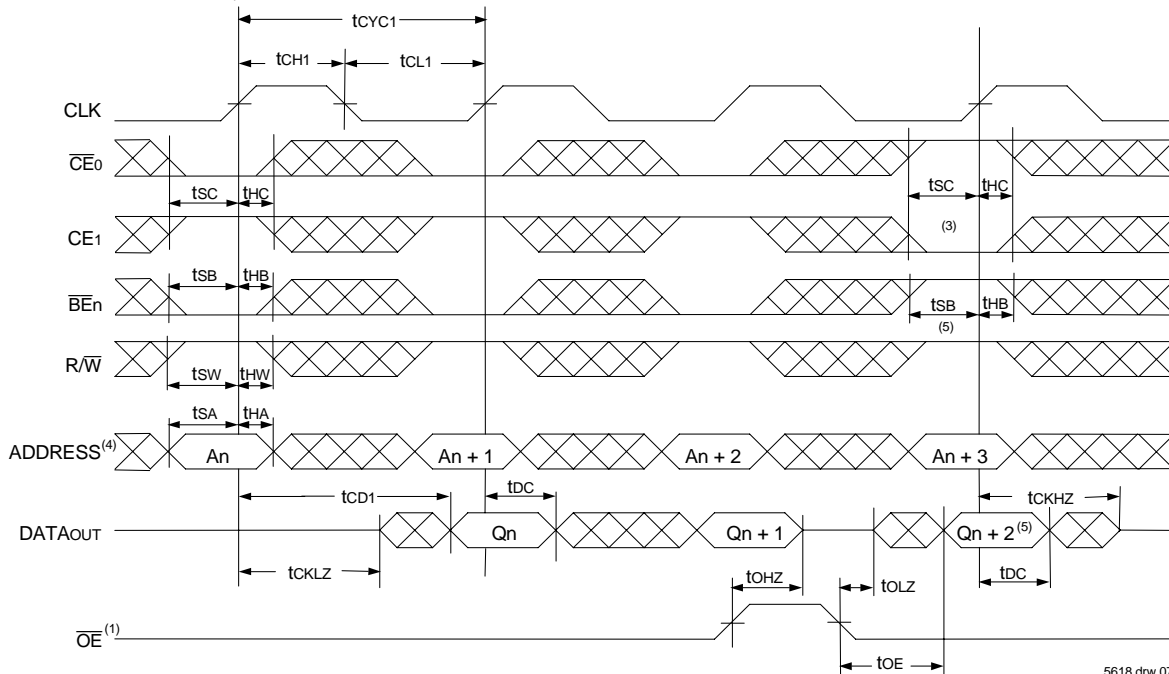
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}/PIPEX = V_{IH}$. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPEX = V_{IL}$ for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}) and $\overline{FT}/PIPE$. $\overline{FT}/PIPE$ should be treated as a DC signal, i.e. steady state during operation.
- These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 5 for details on selecting the desired operating voltage levels for each port.
- 166MHz Industrial Temperature not available in BF208 package.
- This speed grade available when $V_{DDQ} = 3.3V$ for a specific port (i.e., OPTx = VIH). This speed grade available in BC256 package only.

Timing Waveform of Read Cycle for Pipelined Operation (**ADS** Operation) ($\overline{\text{FT}}/\text{PIPE}'x' = V_{IH}$)⁽²⁾



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Timing Waveform of Read Cycle for Flow-through Output (**FT**/PIPE"x" = V_{IL})^(2,6)

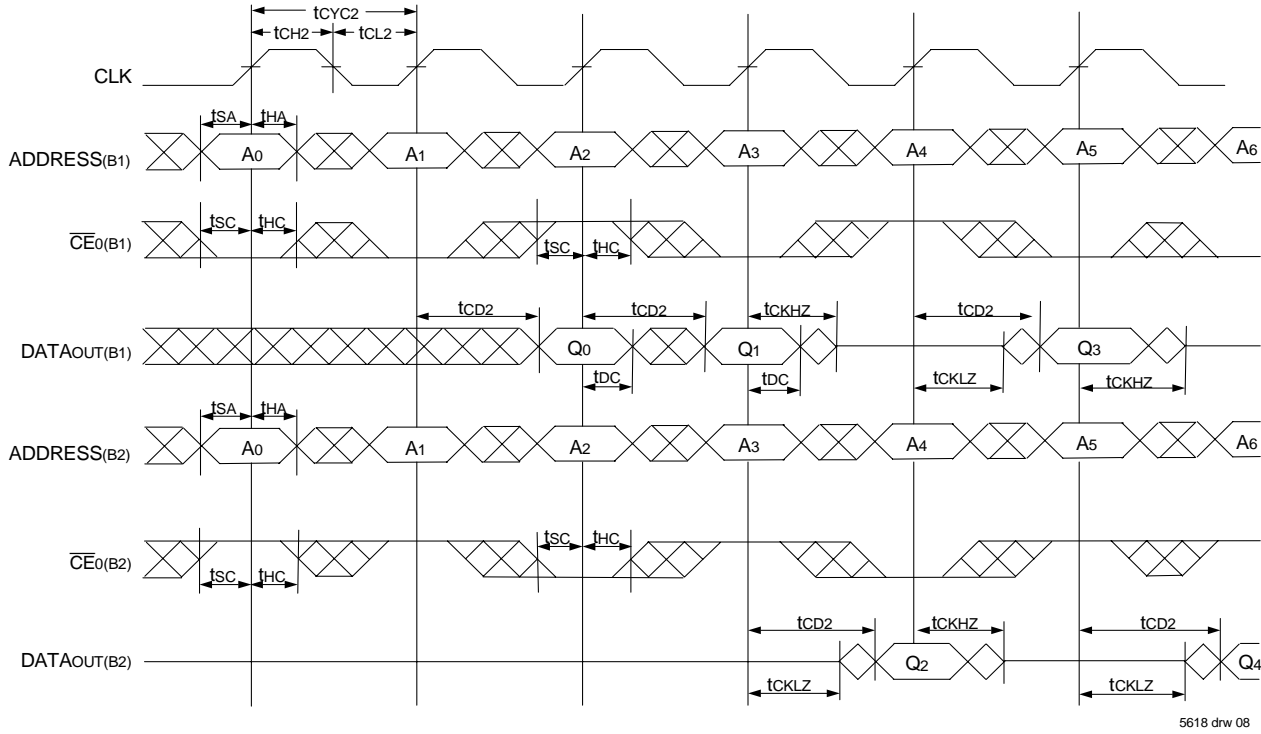


5618 drw 07

NOTES:

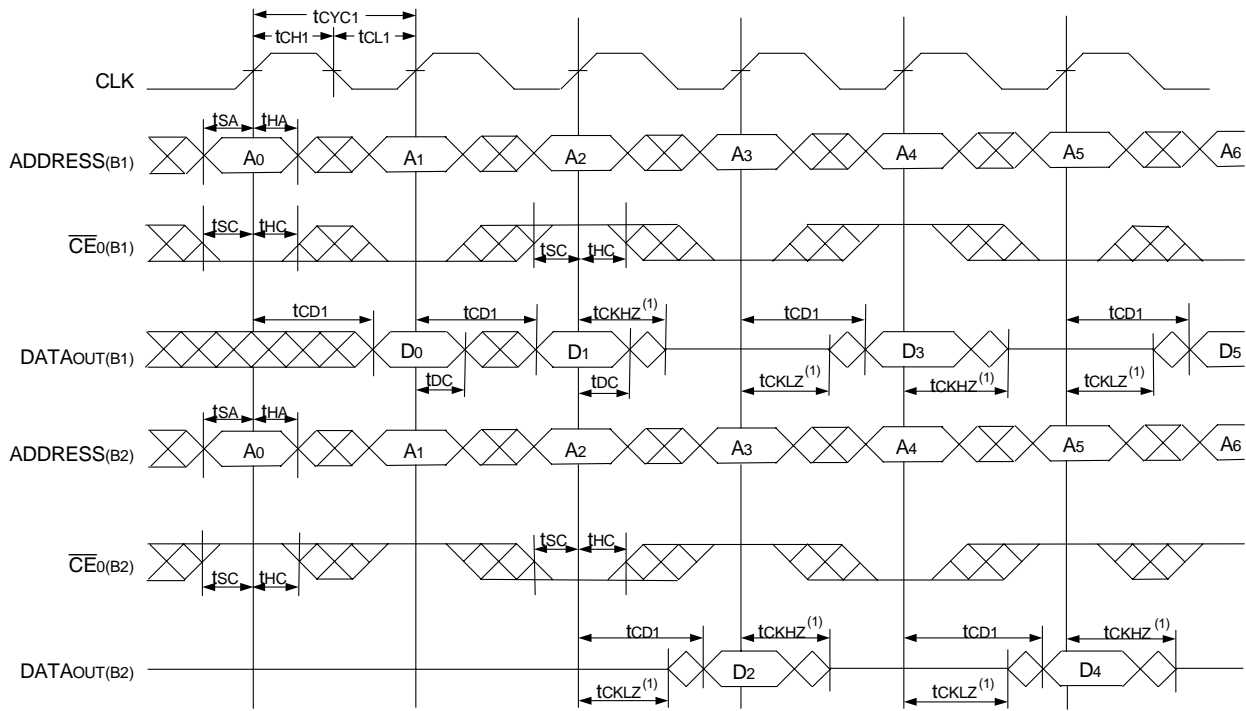
1. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{\text{ADS}} = V_{IL}$, $\overline{\text{CNTEN}}$ and $\overline{\text{REPEAT}} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0 = V_{IH}$, $\text{CE}_1 = V_{IL}$, $\overline{\text{BE}}_n = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{\text{BE}}_n$ was HIGH, then the appropriate Byte of DATAout for $Q_n + 2$ would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read^(1,2)



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Timing Waveform of a Multi-Device Flow-Through Read^(1,2)

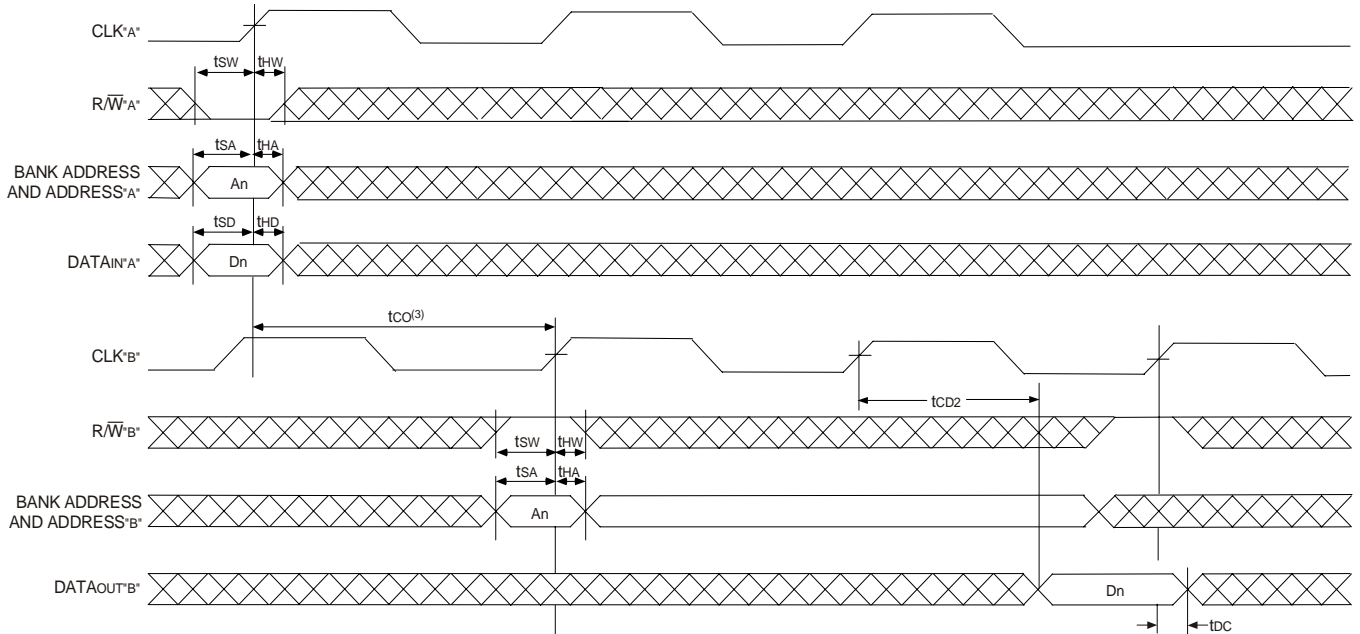


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NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V7519 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. BE_n, OE, and ADS = VIH; CE1(B1), CE1(B2), R/W, CNTEN, and REPEAT = VIH.

Timing Waveform of Port A Write to Pipelined Port B Read^(1,2,4)

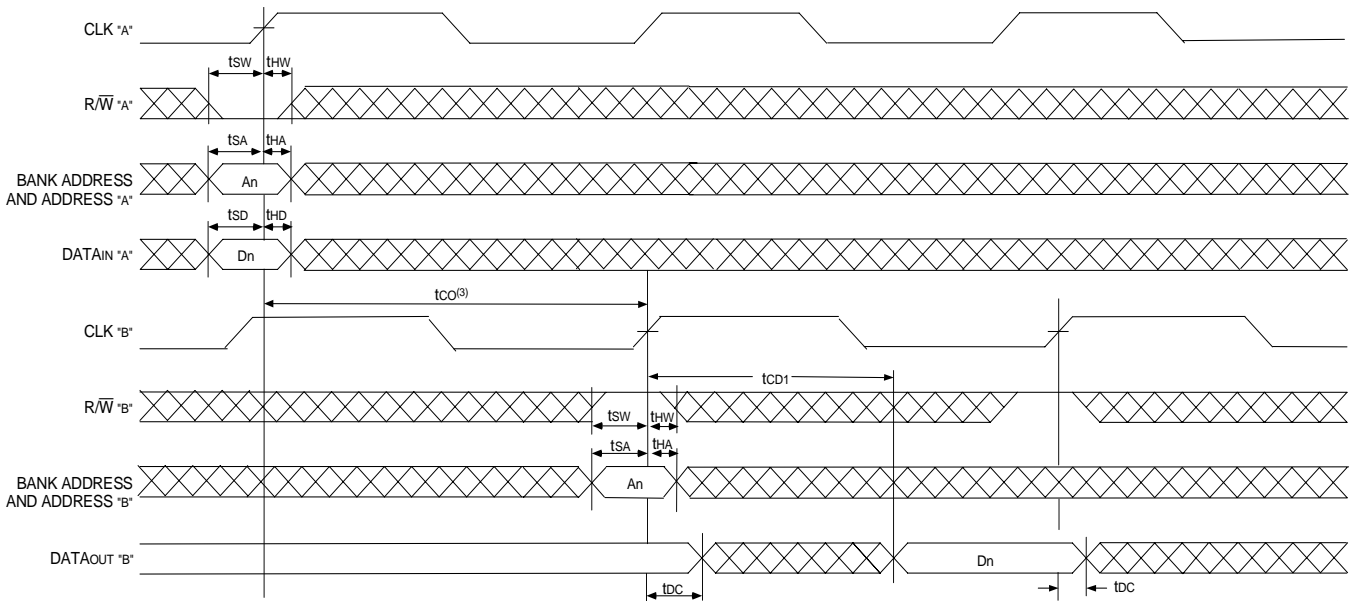


NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for Port "B", which is being read from. $\overline{OE} = V_{IH}$ for Port "A", which is being written to.
3. If $t_{CO} <$ minimum specified, then operations from both ports are INVALID. If $t_{CO} \geq$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

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Timing Waveform with Port-to-Port Flow-Through Read^(1,2,4)



NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{CO} <$ minimum specified, then operations from both ports are INVALID. If $t_{CO} \geq$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CD1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

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Timing Waveform of Pipelined Read-to-Write-to-Read

($\overline{OE} = V_{IL}$)⁽²⁾

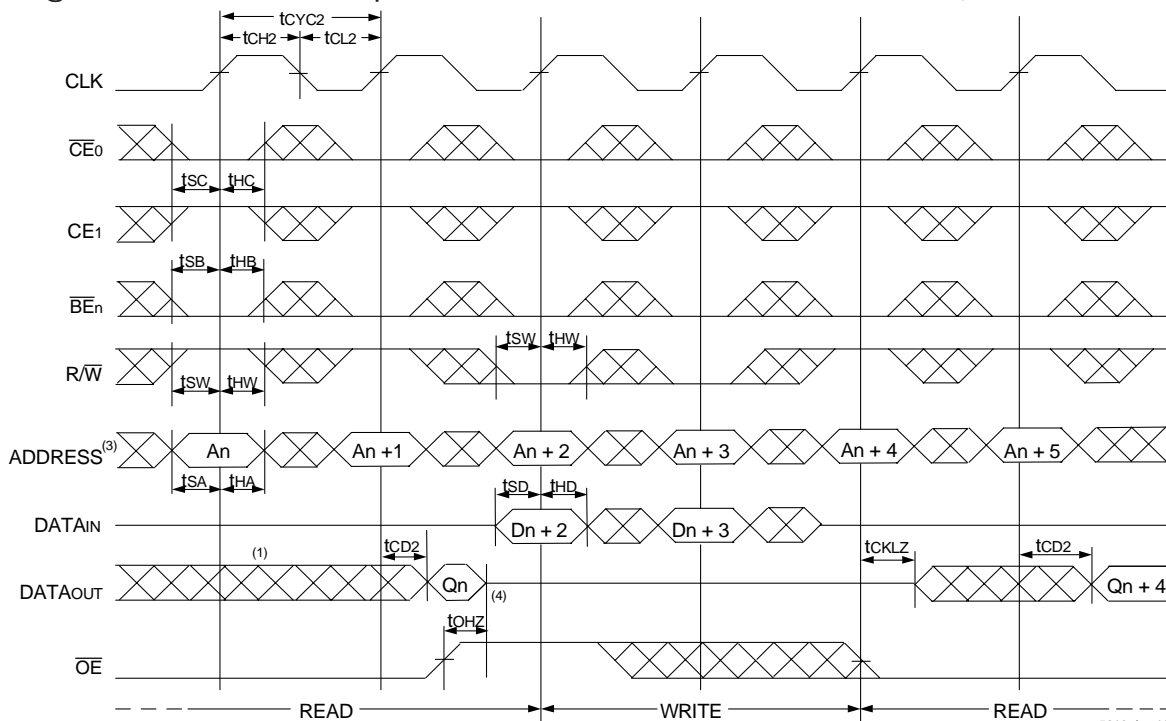


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $REPEAT = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾

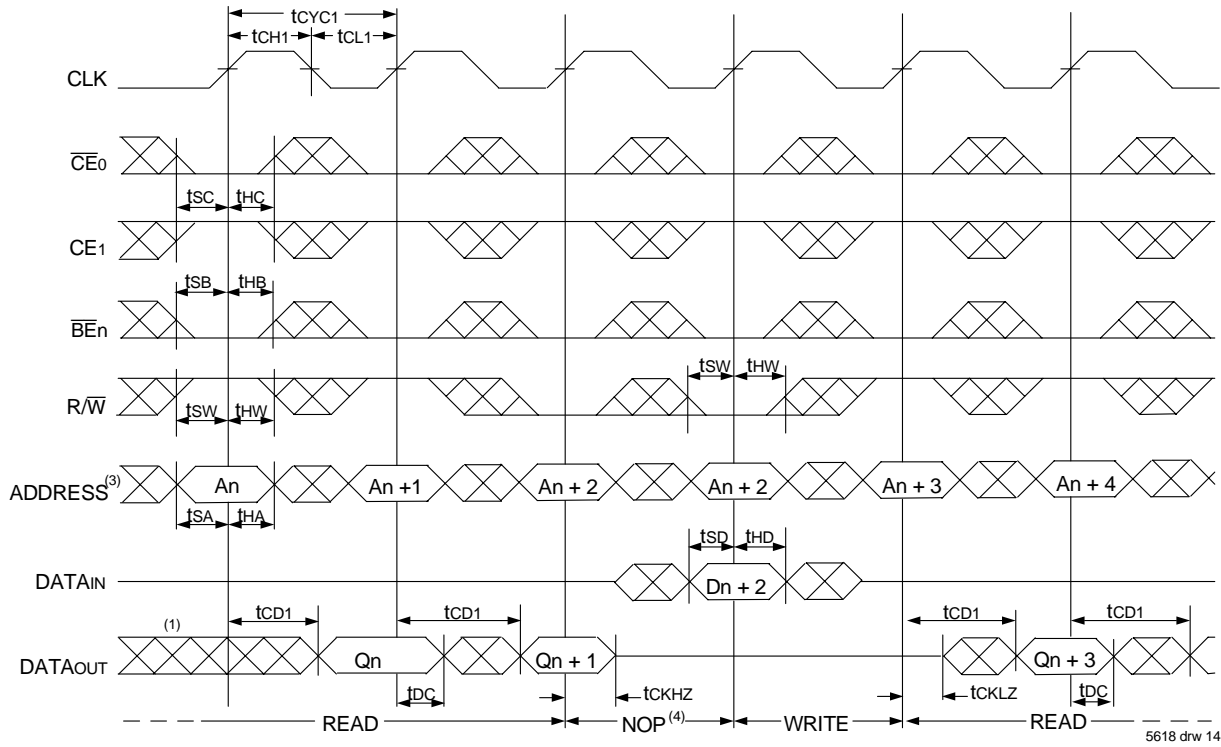


NOTES:

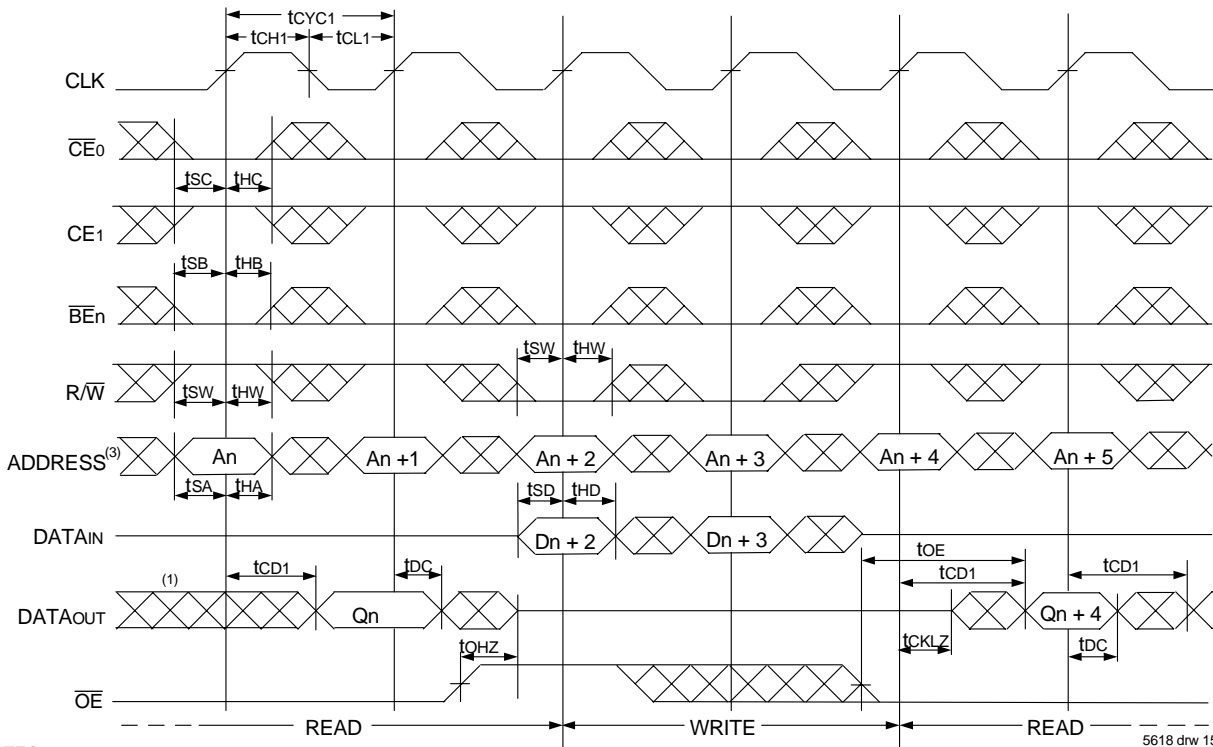
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $REPEAT = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

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Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



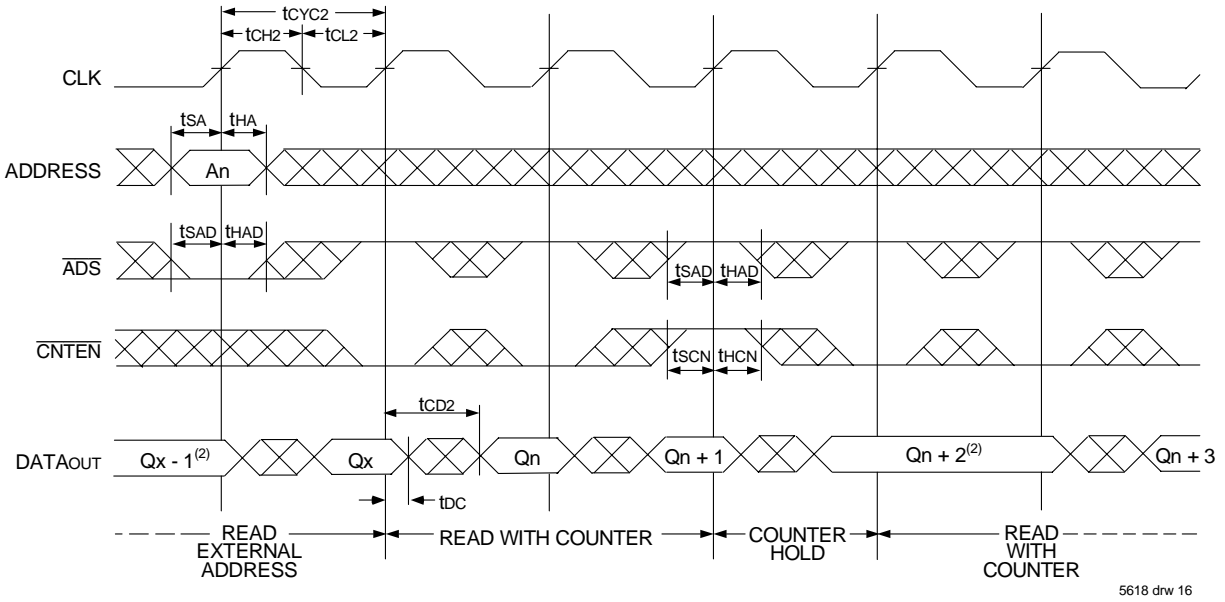
Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾



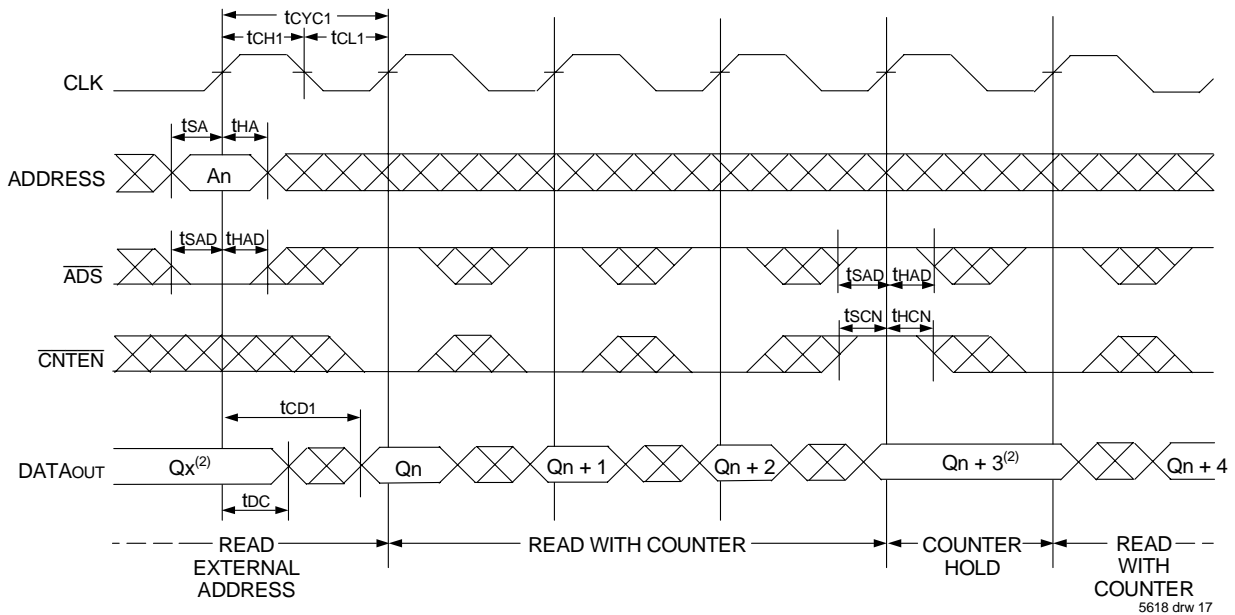
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE0}$, \overline{BEn} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$, \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



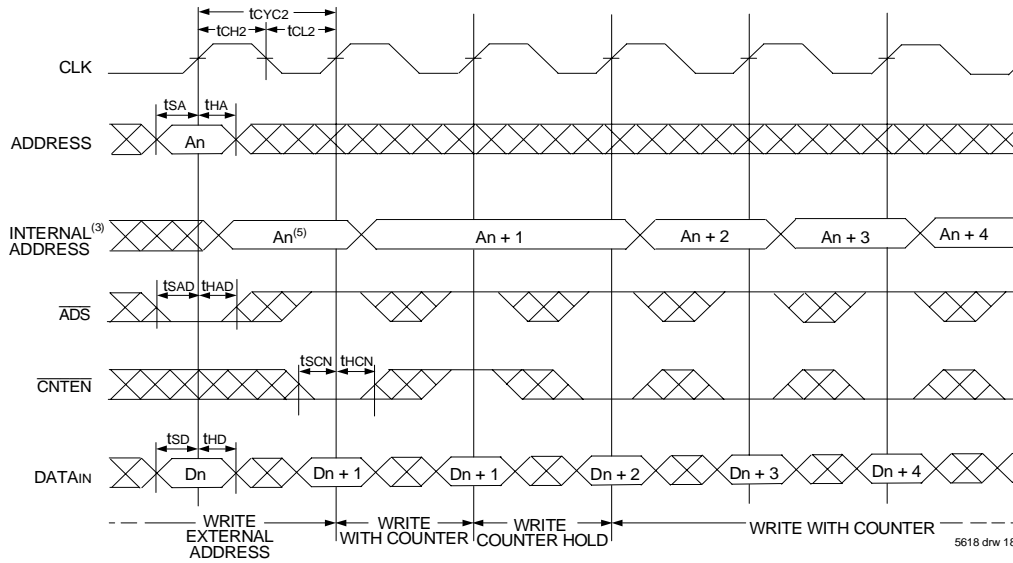
Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾



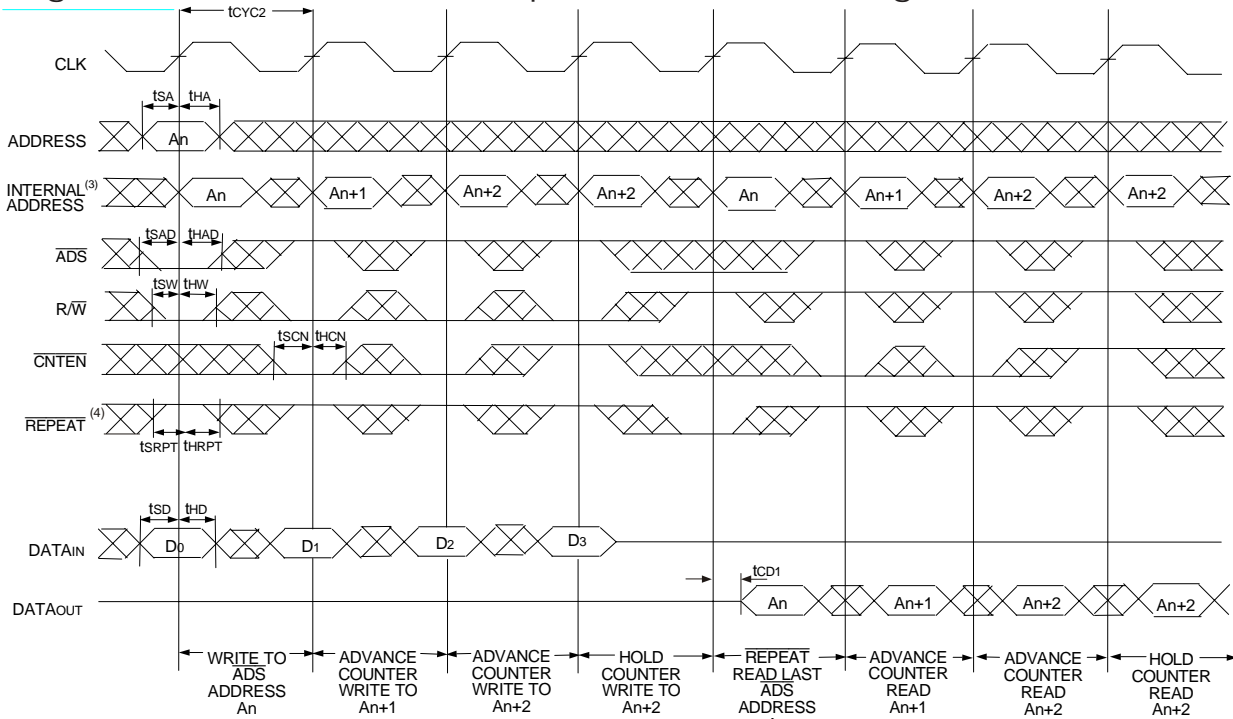
NOTES:

1. $\overline{CE}_0, \overline{OE}, \overline{BE}_n = V_{IL}; CE_1, R/\overline{W}, \text{ and } \overline{REPEAT} = V_{IH}.$
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)^(1,6)



Timing Waveform of Counter Repeat for Flow Through Mode^(2,6,7)



NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{REPEAT} = V_{IH}$.
2. \overline{CE}_0 , $\overline{BE}_n = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. No dead cycle exists during \overline{REPEAT} operation. A READ or WRITE cycle may be coincidental with the counter \overline{REPEAT} cycle: Address loaded by last valid \overline{ADS} load will be accessed. For more information on \overline{REPEAT} function refer to Truth Table II.
5. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.
6. The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0.
7. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

Functional Description

The IDT70V7519 is a high-speed 256Kx36 (9 Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 4Kx36 banks. Based on a standard SRAM core instead of a traditional true dual-port memory core, this bank-switchable device offers the benefits of increased density and lower cost-per-bit while retaining many of the features of true dual-ports. These features include simultaneous, random access to the shared array, separate clocks per port, 166 MHz operating speed, full-boundary counters, and pinouts compatible with the IDT70V3599 (128Kx36) dual-port family.

The two ports are permitted independent, simultaneous access into separate banks within the shared array. Access by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e., $BA_{0L} - BA_{5L} \neq BA_{0R} - BA_{5R}$). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

The IDT70V7519 provides a true synchronous Dual-Port Static RAM

interface. Registered inputs provide minimal setup and hold times on address, data and all critical control inputs.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on \overline{CE}_0 or a LOW on CE_1 for one clock cycle will power down the internal circuitry on each port (individually controlled) to reduce static power consumption. Dual chip enables allow easier banking of multiple IDT70V7519s for depth expansion configurations. Two cycles are required with \overline{CE}_0 LOW and CE_1 HIGH to read valid data on the outputs.

Depth and Width Expansion

The IDT70V7519 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V7519 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

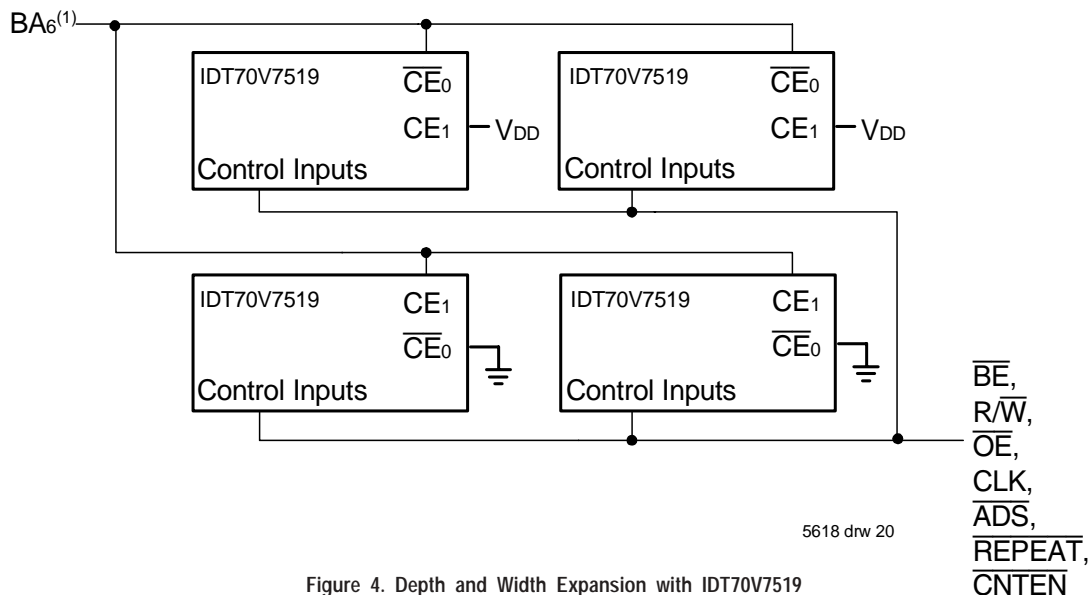


Figure 4. Depth and Width Expansion with IDT70V7519

NOTE:

1. In the case of depth expansion, the additional address pin logically serves as an extension of the bank address. Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory within the shared array that is not currently being accessed by the opposite port (i.e., $BA_{0L} - BA_{6L} \neq BA_{0R} - BA_{6R}$). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the parts within that bank may be corrupted (in the case that either or both parts are writing) or may result in invalid output (in the case that both ports are trying to read).

JTAG Timing Specifications

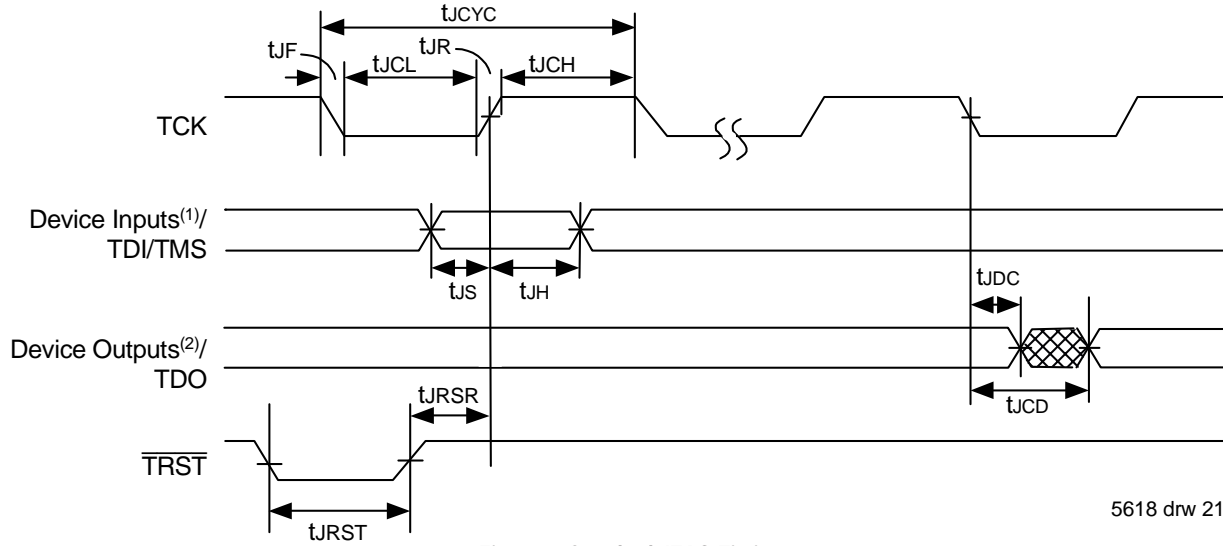


Figure 5. Standard JTAG Timing

NOTES:

1. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics^(1,2,3,4)

Symbol	Parameter	70V7519		
		Min.	Max.	Units
t _{JCYC}	JTAG Clock Input Period	100	—	ns
t _{JCH}	JTAG Clock HIGH	40	—	ns
t _{JCL}	JTAG Clock Low	40	—	ns
t _{JR}	JTAG Clock Rise Time	—	3 ⁽¹⁾	ns
t _{JF}	JTAG Clock Fall Time	—	3 ⁽¹⁾	ns
t _{JRST}	JTAG Reset	50	—	ns
t _{JRSR}	JTAG Reset Recovery	50	—	ns
t _{JCD}	JTAG Data Output	—	25	ns
t _{JDC}	JTAG Data Output Hold	0	—	ns
t _{JS}	JTAG Setup	15	—	ns
t _{JH}	JTAG Hold	15	—	ns

5618 tbl 12

NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x300	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5618 tbl 13

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5618 tbl 14

System Interface Parameters

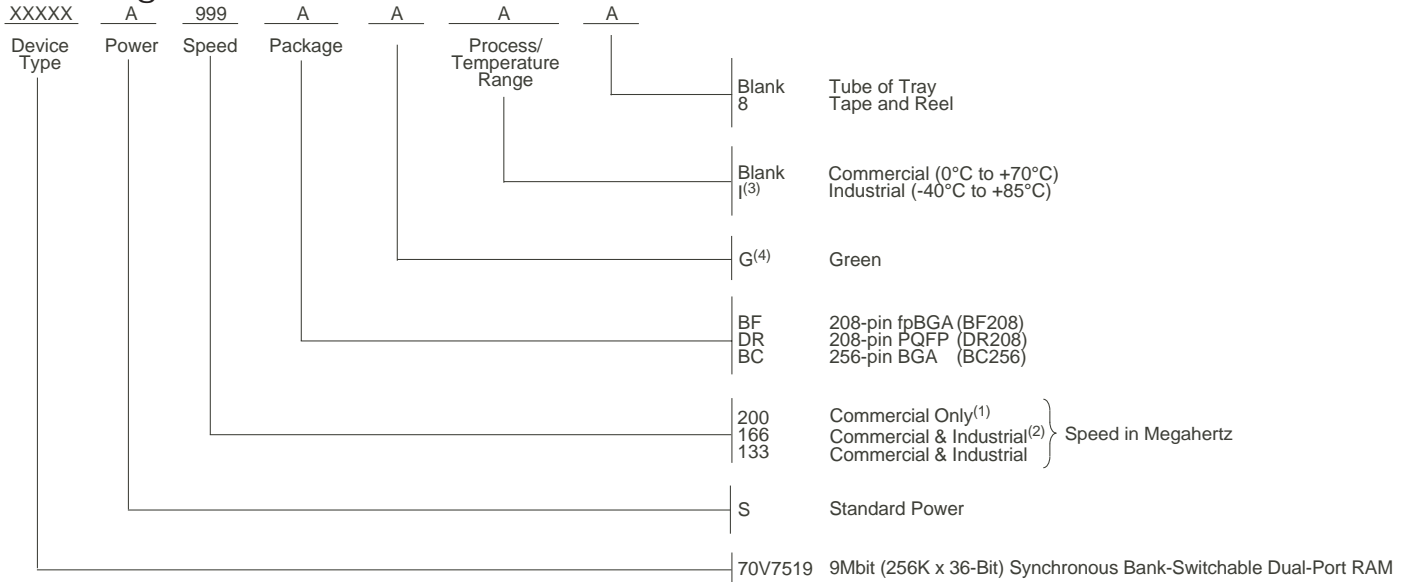
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ and outputs ⁽¹⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5618 tbl 15

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



NOTES:

1. Available in BC256 package only.
 2. Industrial Temperature at 166Mhz not available in BF208 package.
 3. Contact your local sales office for industrial temp range for other speeds, packages and powers.
 4. Green parts available. For specific speeds, packages and powers contact your local sales office.
- LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History:

- 01/05/00: Initial Public Offering
- 10/19/01: Page 2, 3 & 4 Added date revision for pin configurations
Page 9 Changed I_SB3 values for commercial and industrial DC Electrical Characteristics
Page 11 Changed to E value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05
Page 20 Increased t_{CD} from 20ns to 25ns, please refer to Errata #SMEN-01-04
Page 1 & 22 Replaced ™ logo with ® logo
- 01/11/02: Page 2 Corrected BF-208 pinout configuration fpBGA A15
- 03/18/02: Page 1, 9, 11 & 22 Added 200MHz specification
Page 9 Tightened power numbers in DC Electrical Characteristics
Page 14 Changed waveforms to show INVALID operation from opposite ports if t_{CO} < minimum specified
Page 1 - 22 Removed "Preliminary" status
- 12/04/02: Page 9, 11 & 22 Designated 200Mhz speed grade available in BC-256 package only
- 01/16/04: Page 11 Added byte enable setup time and byte enable hold time parameters and values to all speed grades in the AC Electrical Characteristics Table
- 07/25/08: Page 9 Corrected a typo in the DC Chars table
- 01/29/09: Page 22 Removed "IDT" from orderable part number
- 06/04/15: Page 1 Added Green availability to Features
Page 2, 3, 4 & 22 The package codes for BF-208 changed to BF208, BC-256 changed to BC256, and DR-208 changed to DR208 respectively to match the standard package codes
Page 2, 3 & 4 Removed the date from all of the pin configurations BF208, BC256 & DR208
Page 22 Added Green and T&R indicators and the correlating footnotes to Ordering Information
- 06/22/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018



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