

# CAT823, CAT824, CAT825

## System Supervisory Voltage Reset with Watchdog and Manual Reset

### Description

The CAT823, CAT824, and CAT825 provide basic reset and monitoring functions for the electronic systems. Each device monitors the system voltage and maintains a reset output until that voltage reaches the device's specified trip value and then maintains the reset output active condition until the device's internal timer, after a minimum timer of 140 ms; to allow the systems power supply to stabilize.

The CAT823 and CAT824 also have a watchdog input which can be used to monitor a system signal and cause a reset to be issued if the signal fails to change state prior to a timeout condition.

The CAT823 and CAT825 also provide a manual reset input which can be used to initiate reset if pulled low. This input can be directly attached to a push-button or a processor signal.

### Features

- Automatically Restarts Microprocessor after Power Failure
- Monitors Pushbutton for External Override
- Accurate Under Voltage System Monitoring
- Brownout Detection System Reset for use with 3.0, 3.3, and 5.0 Volt Systems
- Pin and Function Compatible with the MAX823/24/25 Products
- Operating Range from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in TSOT-23 5-lead and SC-70 Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Microprocessor and Microcontroller Based Systems
- Intelligent Instruments
- Control Systems
- Critical  $\mu\text{P}$  Monitors
- Portable Equipment

### PIN FUNCTIONS

Pin Name	Function
RESET	CMOS Push-Pull Active Low Reset Output
GND	Ground
MR	Manual Reset input – Pulled high Internally by a 52 k $\Omega$ resistor designed to be driven low by a mechanical pushbutton, open drain output or CMOS output.
RESET	CMOS Push-Pull Active High Reset Output
WDI	Watchdog Timer Input – Designed to be driven by a processor output or can be disabled by tri-stating or leaving open.
V <sub>CC</sub>	Power Supply



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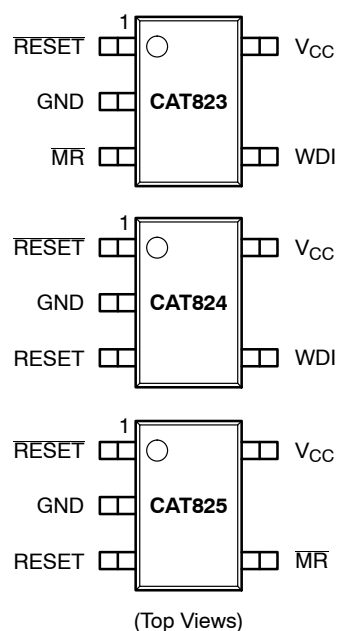


SC-70  
SD SUFFIX  
CASE 419AC

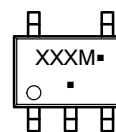


TSOT-23  
TD SUFFIX  
CASE 419AE

### PIN CONNECTIONS



### MARKING DIAGRAM



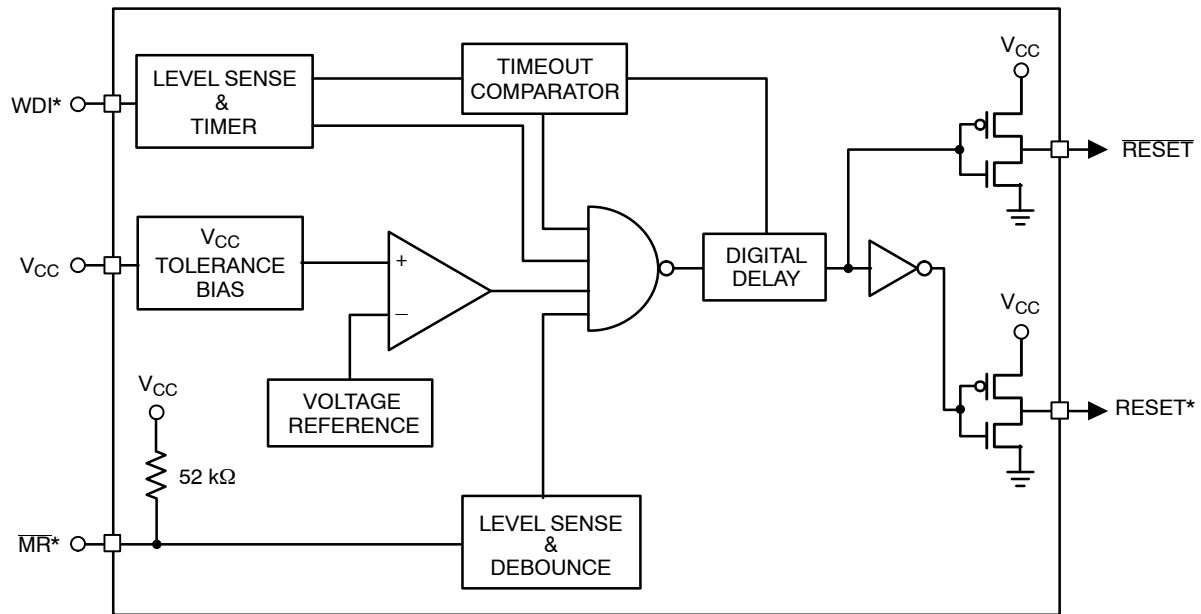
XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package\*

(\*Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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\* Functions Available by Device

Figure 1. Block Diagram

Device	RESET	RESET	MR	WDI
CAT823	x		x	x
CAT824	x	x		x
CAT825	x	x	x	

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage	6	V
All other pins	-0.3 to (V <sub>CC</sub> + 0.3)	V
Input Current, V <sub>CC</sub>	20	mA
Output Current RESET, $\overline{\text{RESET}}$	20	mA
Continuous Power Dissipations (T <sub>A</sub> = +70°C) SC-70 5-lead (derate 3.1 mW/°C above +70°C) TSOT-23 5-lead (derate 7.1 mW/°C above +70°C)	247 571	mW
Storage Temperature	-65 to 150	°C
Operating Ambient Temperature	-40 to +85	°C
Lead Soldering (10 seconds max)	+300	°C
ESD Rating: Low Voltage Pins Human Body Model Machine Model	2000 200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. RECOMMENDED OPERATING CONDITIONS

Parameter	Range	Units
V <sub>CC</sub> (T <sub>A</sub> = 0°C to +70°C)	1.0 to 5.5	V
V <sub>CC</sub> (T <sub>A</sub> = -40°C to +85°C)	1.2 to 5.5	V
All Other Pins	-0.1 to (V <sub>CC</sub> + 0.1)	V
Ambient Temperature	-40 to +85	°C

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**Table 3. ELECTRICAL OPERATING CHARACTERISTICS** (DC Characteristics:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  for L/M versions;  $V_{CC} = 2.0\text{ V}$  to  $3.6\text{ V}$  for the R/S/T/U/Y/Z version,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  unless otherwise noted. Typical Values at  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 5\text{ V}$  for L/M versions;  $V_{CC} = 3.3\text{ V}$  for the T/S versions;  $V_{CC} = 3.0\text{ V}$  for the R version; and  $V_{CC} = 2.5\text{ V}$  for the U/Y/Z versions.) (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{CC}$	Supply Current	CAT823 (L/M Versions) CAT824 (L/M Versions)		6	17	$\mu\text{A}$
		CAT823 (R/S/T/Y/Z Versions) CAT824 (R/S/T/U/Y/Z Versions)		4	12	
		CAT825 (L/M Versions)		3	8	
		CAT825 (R/S/T/Y/Z Versions)		2	6	
$V_{RST}$	Reset Threshold	CAT82_L at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	4.50	4.63	4.75	V
		CAT82_M at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	4.25	4.38	4.50	
		CAT82_T at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	3.00	3.08	3.15	
		CAT82_S at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	2.85	2.93	3.00	
		CAT82_R at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	2.55	2.63	2.70	
		CAT82_Z at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	2.25	2.32	2.38	
		CAT82_Y at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	2.13	2.19	2.25	
		CAT824U at $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	1.95	2.00	2.05	
	Reset Threshold Tempco			40		ppm/ $^{\circ}\text{C}$
	Reset Threshold Hysteresis	CAT82_L/M		10		mV
		CAT82_R/S/T/Y/Z, CAT824U		5		
$t_{RD}$	$V_{CC}$ to Reset Delay (Note 2)	$V_{CC} = V_{TH}$ to $(V_{TH} - 100\text{ mV})$		20		$\mu\text{s}$
$t_{RP}$	Reset Active Timeout Period		140	200	400	ms
$V_{OH}$	RESET Output High Voltage	CAT82_L/M, $V_{CC} = V_{RST\text{ max}}$ , $I_{SOURCE} = -120\ \mu\text{A}$	$V_{CC} - 1.5\text{ V}$			V
		CAT82_T/S/R/Z/Y, CAT824U, $V_{CC} = V_{RST\text{ max}}$ , $I_{SOURCE} = -30\ \mu\text{A}$	$0.8 \times V_{CC}$			
$V_{OL}$	RESET Output Low Voltage	CAT82_L/M, $V_{CC} = V_{RST\text{ min}}$ , $I_{SINK} = 3.2\text{ mA}$			0.4	V
		CAT82_T/S/R/Z/Y, CAT824U, $V_{CC} = V_{RST\text{ min}}$ , $I_{SINK} = 1.2\text{ mA}$			0.3	
		$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{CC} = 1\text{ V}$ , $V_{CC}$ falling, $I_{SINK} = 50\ \mu\text{A}$			0.3	
		$T_A = T_{MIN}$ to $T_{MAX}$ , $V_{CC} = 1.2\text{ V}$ , $V_{CC}$ falling, $I_{SINK} = 100\ \mu\text{A}$			0.3	
$I_{SOURCE}$	RESET Output Short-Circuit Current	CAT82_L/M, Reset = 0 V, $V_{CC} = 5.5\text{ V}$			1.5	mA
		CAT82_L/M, Reset = 0 V, $V_{CC} = 3.6\text{ V}$			0.8	
$V_{OH}$	Reset Output Voltage	$V_{CC} > 1.8\text{ V}$ , $I_{SOURCE} = -150\ \mu\text{A}$	$0.8 \times V_{CC}$			V
$V_{OL}$		CAT824L/M & CAT825L/M, $V_{CC} = V_{RST\text{ max}}$ , $I_{SINK} = 3.2\text{ mA}$			0.4	
		CAT824R/S/T/U/Y/Z & CAT825R/S/T/Y/Z, $V_{CC} = V_{RST\text{ max}}$ , $I_{SINK} = 1.2\text{ mA}$			0.3	

- Over-temperature limits are guaranteed by design and not production tested.
- The RESET short-circuit current is the maximum pull-up current when reset is driven low by a bidirectional output.
- WDI is internally serviced within the watchdog period if WDI is left open.
- The WDI input current is specified as an average input current when the WDI input is driven high or low. The WDI input if connected to a three-stated output device can be disabled in the tristate mode as long as the leakage current is less than  $10\ \mu\text{A}$  and a maximum capacitance of less than  $200\text{ pF}$ . To clock the WDI input in the active mode the drive device must be able to source or sink at least  $200\ \mu\text{A}$  when active.

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**Table 3. ELECTRICAL OPERATING CHARACTERISTICS** (DC Characteristics:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  for L/M versions;  $V_{CC} = 2.0\text{ V}$  to  $3.6\text{ V}$  for the R/S/T/U/Y/Z version,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  unless otherwise noted. Typical Values at  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 5\text{ V}$  for L/M versions;  $V_{CC} = 3.3\text{ V}$  for the T/S versions;  $V_{CC} = 3.0\text{ V}$  for the R version; and  $V_{CC} = 2.5\text{ V}$  for the U/Y/Z versions.) (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>WATCHDOG INPUT (CAT823 &amp; CAT824)</b>						
$t_{WD}$	Watchdog Timeout Period		1.12	1.60	3.20	s
$t_{WDI}$	WDI Pulse Width	$V_{IL} = 0.4\text{ V}$ , $V_{IH} = 0.8 \times V_{CC}$	50			ns
$V_{IL}$	WDI Input Voltage (Note 3)				$0.3 \times V_{CC}$	V
$V_{IH}$			$0.7 \times V_{CC}$			
	WDI Input Current (Note 4)	WDI = $V_{CC}$ , Time Average		120	160	$\mu\text{A}$
		WDI = $0\text{ V}$ , Time Average	-20	-15		
<b>MANUAL RESET INPUT (CAT823 &amp; CAT825)</b>						
$V_{IL}$	$\overline{\text{MR}}$ Input Voltage				$0.3 \times V_{CC}$	V
$V_{IH}$			$0.7 \times V_{CC}$			
$t_{PB}$	$\overline{\text{MR}}$ Pulse Width		1			$\mu\text{s}$
$t_{PDLY}$	$\overline{\text{MR}}$ low to Reset Delay				5	$\mu\text{s}$
	$\overline{\text{MR}}$ Noise Immunity	Pulse Width with No Reset		100		ns
	$\overline{\text{MR}}$ Pullup Resistance (internal)		35	52	75	$\text{k}\Omega$

- Over-temperature limits are guaranteed by design and not production tested.
- The RESET short-circuit current is the maximum pull-up current when reset is driven low by a bidirectional output.
- WDI is internally serviced within the watchdog period if WDI is left open.
- The WDI input current is specified as an average input current when the WDI input is driven high or low. The WDI input if connected to a three-stated output device can be disabled in the tristate mode as long as the leakage current is less than  $10\text{ }\mu\text{A}$  and a maximum capacitance of less than  $200\text{ pF}$ . To clock the WDI input in the active mode the drive device must be able to source or sink at least  $200\text{ }\mu\text{A}$  when active.

## TYPICAL ELECTRICAL OPERATING CHARACTERISTICS

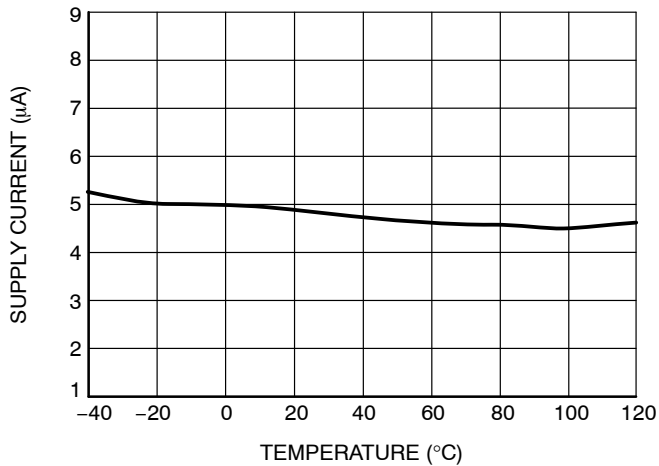


Figure 2.  $V_{CC}$  Supply Current vs. Temperature

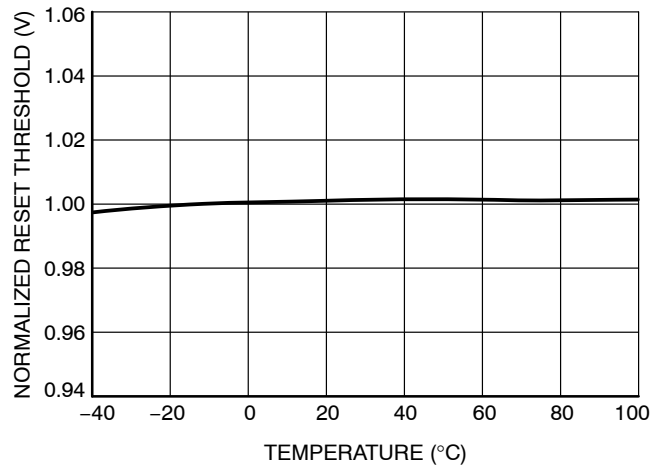


Figure 3. Normalized Reset Threshold Voltage vs. Temperature

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## FUNCTIONAL DESCRIPTION

### Processor RESET

The CAT823–825 detect supply voltage ( $V_{CC}$ ) conditions that are below the specified voltage trip value ( $V_{RST}$ ) and provide a reset output to maintain correct system operation. On power-up,  $\overline{RESET}$  (and RESET if available) are kept active for a minimum delay  $t_{RP}$  of 140 ms after the supply voltage ( $V_{CC}$ ) rises above  $V_{RST}$  to allow the power supply and processor to stabilize. When  $V_{CC}$  drops below the voltage trip value ( $V_{RST}$ ), the reset output signals  $\overline{RESET}$  (and RESET) are pulled active.  $\overline{RESET}$  (and RESET if available) is specifically designed to provide the reset input signals for processors. This provides reliable and consistent operation as power is turned on, off or during brownout conditions by maintaining the processor operation in known conditions.

### Manual RESET

The CAT823 and CAT825 each have a Manual Reset ( $\overline{MR}$ ) input to allow for alternative control of the reset outputs. The  $\overline{MR}$  input is designed for direct connection to a pushbutton (see Figure 4). The  $\overline{MR}$  input is internally pulled up by 52 k $\Omega$  resistor and must be pulled low to cause the reset outputs to go active. Internally, this input is debounced and timed such that  $\overline{RESET}$  (and RESET) signals of at least 140 ms minimum will be generated. The min 140 ms  $t_{RP}$  delay commences as the Manual Reset input is released from the low level. (see Figure 5)

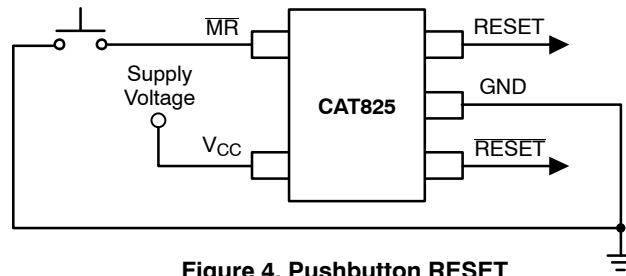


Figure 4. Pushbutton RESET

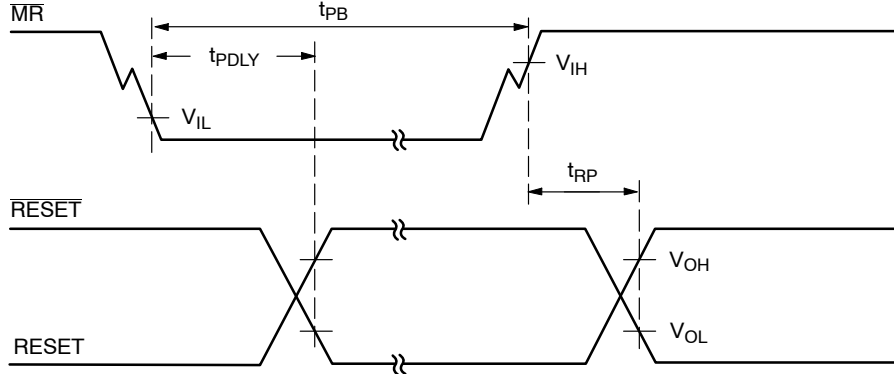


Figure 5. Timing Diagram – Pushbutton RESET

# CAT823, CAT824, CAT825

## Watchdog Timer

The CAT823 and CAT824 provide a Watchdog input (WDI). The watchdog timer function forces  $\overline{\text{RESET}}$  (and RESET in the CAT824) signals active when the WDI input does not have a transition from low-to-high or high-to-low within 1.12 seconds. Timeout of the watchdog starts when  $\overline{\text{RESET}}$  (RESET on the CAT824) becomes inactive. If a transition occurs on the WDI input pin prior to the watchdog time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the reset output(s) will go active for  $t_{RP}$  and once released will repeat the watchdog timeout process.

Figure 6 below shows a typical implementation of a watchdog function. Any processor signal that repeats dependant on the normal operation of the processor or directed by the software operating on the processor can be

used to strobe the watchdog input. The most reliable is a dedicated I/O output transitioned by a specific software instruction.

The watchdog can be disabled by floating (or tri-stating) the WDI input (see Figure 7). If the watchdog is disabled the WDI pin will be pulled low for the first 7/8<sup>th</sup>'s of the watchdog period ( $t_{WD}$ ) and pulled high for the last 1/8<sup>th</sup> of the watchdog period. This pulling low of the WDI input and then high is used to detect an open or tri-state condition and will continue to repeat until the WDI input is driven high or low.

For most efficient operation of devices with the watchdog function the WDI input should be held low the majority of the time and only strobed high as required to reset the watchdog timer.

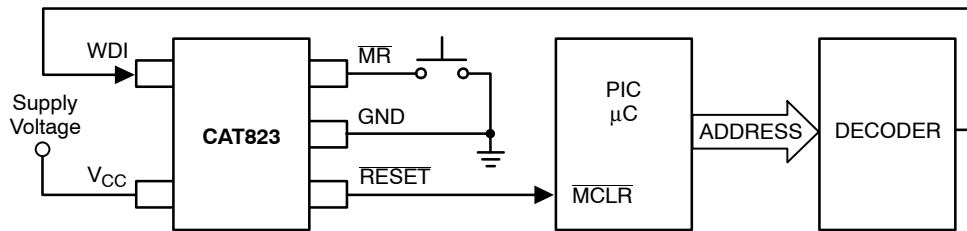


Figure 6. Watchdog Timer

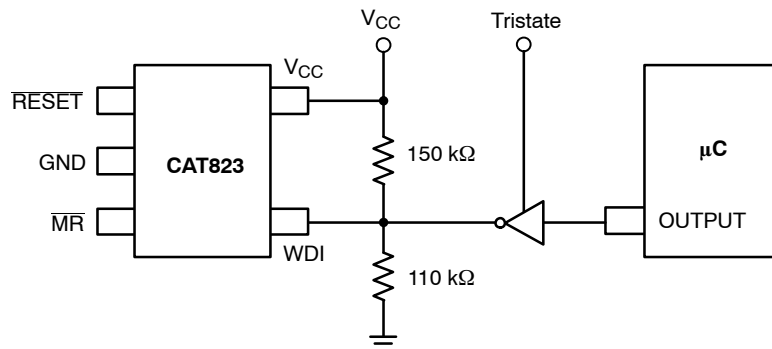


Figure 7. Watchdog Disable Circuit

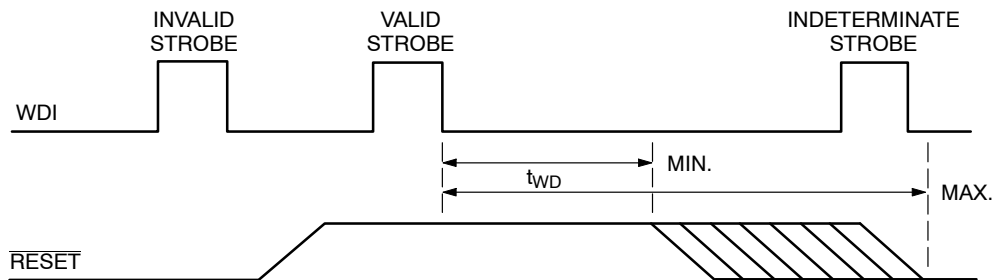


Figure 8. Timing Diagram – Strobe Input

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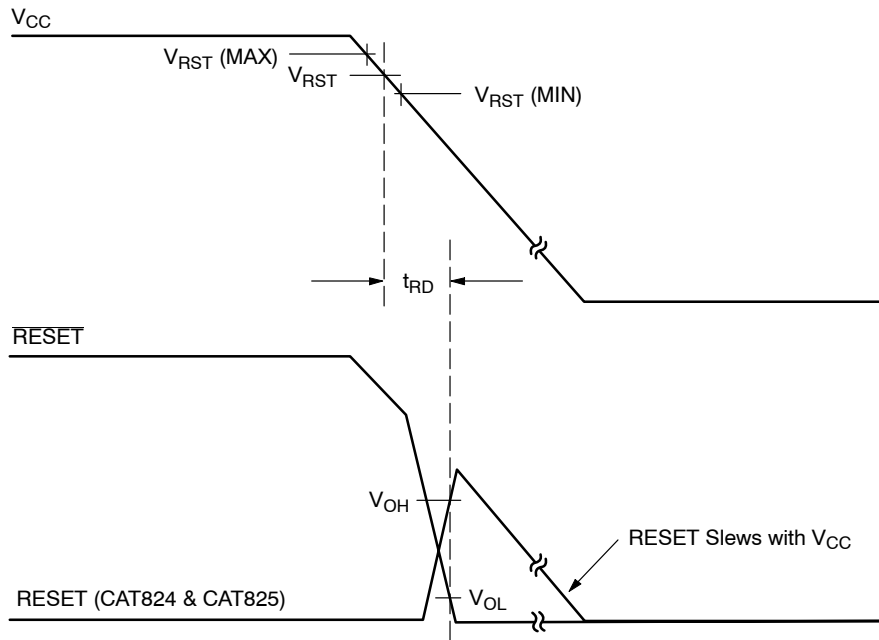


Figure 9. Timing Diagram – Power Down

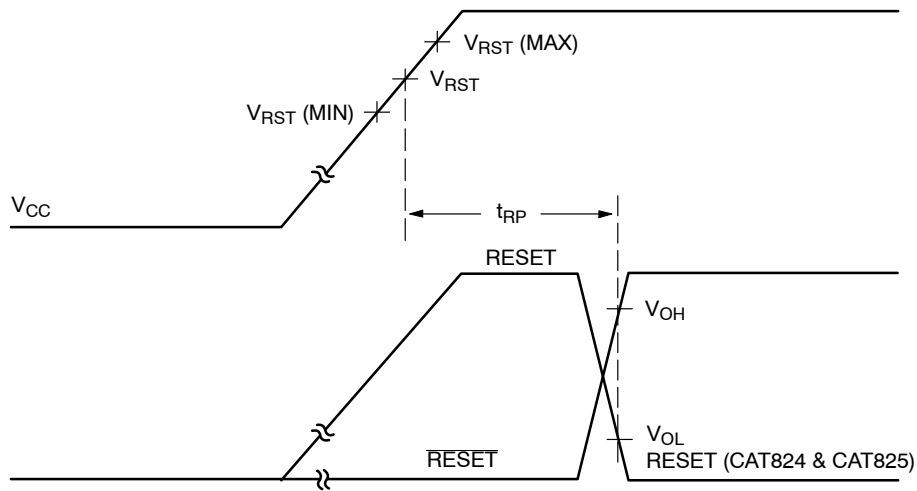


Figure 10. Timing Diagram – Power Up

# CAT823, CAT824, CAT825

## Application Notes

### $\mu$ P's with Bidirectional Reset Pins

The  $\overline{\text{RESET}}$  output can be pulled low by processors like the 68HC11 allowing for a system reset issued by the processor. The maximum pullup current that can be sourced by the CAT82\_L/M is 1.5 mA (and by the CAT82\_T/R/S/Z/Y is 800  $\mu$ A) allowing the processor to pull the output low even when the CAT82x is pulling it high.

### Power Transients

Generally short duration negative-going transients of less than 2  $\mu$ s on the power supply at  $V_{\text{RST}}$  minimum will not cause a reset condition. However the lower the voltage of the transient the shorter the required time to cause a reset output. These issues can usually be remedied by the proper location of bypass capacitance on the circuit board.

### Output Valid Conditions

The  $\overline{\text{RESET}}$  output uses a push-pull output which can maintain a valid output down to a  $V_{\text{CC}}$  of 1.0 volts. To sink current below 0.8 V a resistor can be connected from  $\overline{\text{RESET}}$  to Ground (see Figure 11.) This arrangement will maintain a valid value on the  $\overline{\text{RESET}}$  output during both power up and down but will draw current when the  $\overline{\text{RESET}}$  output is in the high state. A resistor value of about 100 k $\Omega$  should be adequate in most situations to maintain a low condition valid output down to  $V_{\text{CC}}$  equal to 0 V.

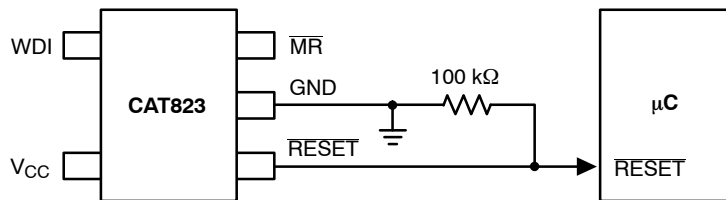


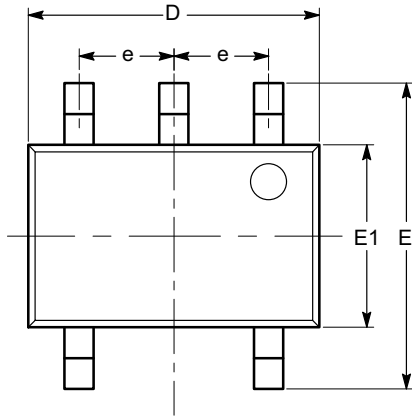
Figure 11.  $\overline{\text{RESET}}$  Valid to 0 Volts  $V_{\text{CC}}$



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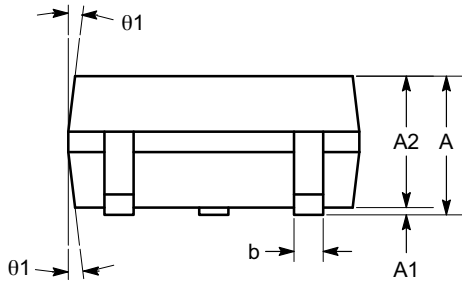
## PACKAGE DIMENSIONS

SC-70, 5 Lead, 1.25x2  
 CASE 419AC-01  
 ISSUE O

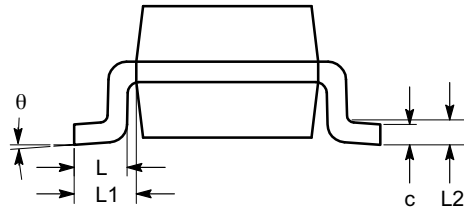


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
$\theta$	0°		8°
$\theta_1$	4°		10°



SIDE VIEW



END VIEW

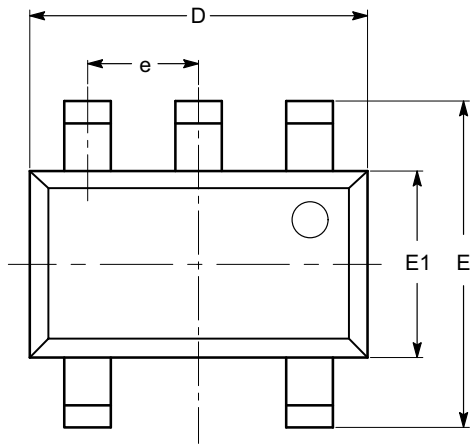
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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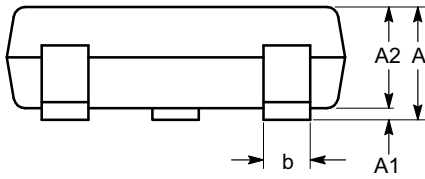
## PACKAGE DIMENSIONS

TSOT-23, 5 LEAD  
CASE 419AE-01  
ISSUE O

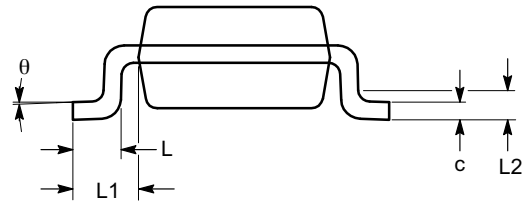


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 TYP		
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
$\theta$	0°		8°



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-193.

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## ORDERING INFORMATION

Order Number	Voltage	Top Mark	Inputs		Outputs		Package	Quantity per Reel
NiPdAu		NiPdAu	MR	WDI	RESET	RESET		
CAT823LTDI-GT3	4.63 V	ETA	*	*	*		TSOT-23-5	3,000
CAT823MTDI-GT3	4.38 V	ETA	*	*	*			
CAT823TTDI-GT3	3.08 V	ETA	*	*	*			
CAT823STDI-GT3	2.93 V	ETA	*	*	*			
CAT823RTDI-GT3	2.63 V	ETA	*	*	*			
CAT823ZTDI-GT3	2.32 V	ETA	*	*	*			
CAT823YTDI-GT3	2.19 V	ETA	*	*	*			
CAT823LSDI-GT3	4.63 V	ETA	*	*	*		SC-70-5	
CAT823MSDI-GT3	4.38 V	ETA	*	*	*			
CAT823TSDI-GT3	3.08 V	ETA	*	*	*			
CAT823SSDI-GT3	2.93 V	ETA	*	*	*			
CAT823RSDI-GT3	2.63 V	ETA	*	*	*			
CAT823ZSDI-GT3	2.32 V	ETA	*	*	*			
CAT823YSDI-GT3	2.19 V	ETA	*	*	*			
CAT824LTDI-GT3	4.63 V	EFA		*	*	*	TOST-23-5	3,000
CAT824MTDI-GT3	4.38 V	EFA		*	*	*		
CAT824TTDI-GT3	3.08 V	EFA		*	*	*		
CAT824STDI-GT3	2.93 V	EFA		*	*	*		
CAT824RTDI-GT3	2.63 V	EFA		*	*	*		
CAT824ZTDI-GT3	2.32 V	EFA		*	*	*		
CAT824YTDI-GT3	2.19 V	EFA		*	*	*		
CAT824UTDI-GT3	2.00 V	EFA		*	*	*	SC-70-5	
CAT824LSDI-GT3	4.63 V	EFA		*	*	*		
CAT824MSDI-GT3	4.38 V	EFA		*	*	*		
CAT824TSDI-GT3	3.08 V	EFA		*	*	*		
CAT824SSDI-GT3	2.93 V	EFA		*	*	*		
CAT824RSDI-GT3	2.63 V	EFA		*	*	*		
CAT824ZSDI-GT3	2.32 V	EFA		*	*	*		
CAT824YSDI-GT3	2.19 V	EFA		*	*	*		


5. All packages are RoHS-compliant (Lead-free, Halogen-free).
6. The standard lead finish is NiPdAu.
7. Contact factory for package availability.
8. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
9. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)

# CAT823, CAT824, CAT825

## ORDERING INFORMATION

Order Number	Voltage	Top Mark	Inputs		Outputs		Package	Quantity per Reel
NiPdAu		NiPdAu	MR	WDI	RESET	RESET		
CAT825LTDI-GT3	4.63 V	ECA	*		*	*	TSOT-23-5	3,000
CAT825MTDI-GT3	4.38 V	ECA	*		*	*		
CAT825TTDI-GT3	3.08 V	ECA	*		*	*		
CAT825STDI-GT3	2.93 V	ECA	*		*	*		
CAT825RTDI-GT3	2.63 V	ECA	*		*	*		
CAT825ZTDI-GT3	2.32 V	ECA	*		*	*		
CAT825YTDI-GT3	2.19 V	ECA	*		*	*		
CAT825LSDI-GT3	4.63 V	ECA	*		*	*	SC-70-5	
CAT825MSDI-GT3	4.38 V	ECA	*		*	*		
CAT825TSDI-GT3	3.08 V	ECA	*		*	*		
CAT825SSDI-GT3	2.93 V	ECA	*		*	*		
CAT825RSDI-GT3	2.63 V	ECA	*		*	*		
CAT825ZSDI-GT3	2.32 V	ECA	*		*	*		
CAT825YSDI-GT3	2.19 V	ECA	*		*	*		

5. All packages are RoHS-compliant (Lead-free, Halogen-free).
6. The standard lead finish is NiPdAu.
7. Contact factory for package availability.
8. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
9. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)

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