MAX16952

36V, 2.2MHz Step-Down Controller with Low Operating Current

General Description

The MAX16952 is a current-mode, synchronous PWM step-down controller designed to operate with input voltages from 3.5V to 36V while using only 50µA of quiescent current at no load. The switching frequency is adjustable from 1MHz to 2.2MHz by an external resistor and can be synchronized to an external clock up to 2.4MHz. The MAX16952 output voltage is pin programmable to be either 5V fixed, or adjustable from 1V to 10V. The wide input voltage range, along with its ability to operate in dropout during undervoltage transients, makes it ideal for automotive and industrial applications.

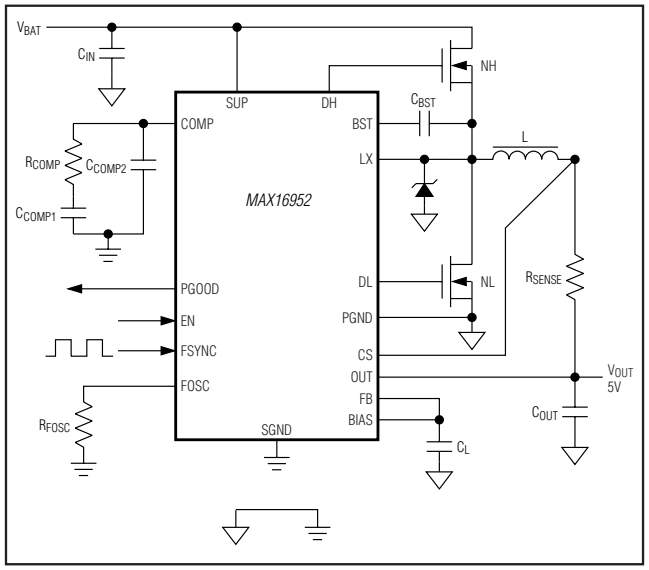
The MAX16952 operates in fixed-frequency PWM mode and low quiescent current skip mode. It features an enable logic input, which is compatible up to 42V to disable the device and reduce its shutdown current to 10µA. Protection features include overcurrent limit, overvoltage, undervoltage, and thermal shutdown with automatic recovery. The device also features a power-good monitor to ease power-supply sequencing.

The MAX16952 is available in a thermally enhanced 16-pin TSSOP package with an exposed pad, and is specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Automotive
- Industrial
- Military
- Point of Load

Typical Operating Circuit



Benefits and Features

- Meets Stringent Automotive Quality and Reliability Requirements
  - +3.5V to +36V Input Voltage Range Allows Operation in “Cold Crank” Conditions
  - High Duty Cycle During Undervoltage Transients
  - Tolerates Input-Voltage Transients to +42V
  - Enable-Pin Compatible from +3.3V Logic Level to +42V
  - Current-Limit, Thermal Shutdown, and Overvoltage Protection
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified
- Increased Efficiency and Reduced BOM Cost and Board Space
  - Lowest BOM Count for Current-Mode-Control Architecture
  - 10-Pin TDFN-EP or 16-Pin TSSOP-EP Packages
- Low Quiescent Current Helps Designers Meet Stringent OEM Current Requirements
  - 50µA Quiescent Current During Skip Mode Operation
- High Switching Frequency Allows Use of Small, Low-Cost External Components
  - 1MHz to 2.2MHz Adjustable Switching Frequency
  - 2.1MHz Switching Frequency with Three Modes of Operation
  - Skip Mode for Efficient, Low-Power Operation
  - Forced Fixed-Frequency Operation
  - External Frequency Synchronization
- Adjustable Output Voltage Supports a Diverse Range of Applications
  - 1V to 10V Output Voltage with ±2% Accuracy

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16952AUE+	-40°C to +125°C	16 TSSOP-EP*
MAX16952AUE/V+	-40°C to +125°C	16 TSSOP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

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Absolute Maximum Ratings

SUP and EN to SGND .....-0.3V to +42V
LX to PGND (Note 1) .....-1V to +42V
BST to LX (Note 1).....-0.3V to +6V
BIAS, FB, PGOOD, FSYNC to SGND .....-0.3V to +6V
DH to LX (Note 1) .....-0.3V to +6V
DL to PGND (Note 1) .....-0.3V to (V_{BIAS} + 0.3V)
FOSC to SGND .....-0.3V to (V_{BIAS} + 0.3V)
CS and OUT to SGND.....-0.3V to +11V
PGND to SGND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 26.1mW/°C above +70°C).....2088.8mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....38.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....3°C/W

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, C_{IN} = 10µF, C_{OUT} = 94µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 14.3kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUP Input Voltage Range	V_{SUP}	(Note 4)	3.5		36	V
SUP Operating Supply Current	I_{SUP}	Fixed 5V output, fixed-frequency, PWM mode, V_{FB} = V_{BIAS}, no external FETs connected		1		mA
Skip Mode Supply Current	I_{SKIP}	No load, fixed 5V output		50	90	µA
SUP Shutdown Supply Current	$I_{SHDN,SUP}$	V_{EN} = 0V		10	20	µA
BIAS Voltage	V_{BIAS}	V_{SUP} = 3.5V, I_{BIAS} = 45mA		3.0		V
		6V < V_{SUP} < 36V	4.7	5.0	5.3	
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising		3.1	3.4	V
BIAS Undervoltage Lockout Hysteresis		V_{BIAS} falling		200		mV
BIAS Minimum Load	$I_{BIAS(MIN)}$	V_{SUP} - V_{BIAS} > 200mV		45		mA
OUTPUT VOLTAGE (OUT)						
Output Voltage Adjustable Range			1.0		10	V
OUT Pulldown Resistance	R_{PULL_D}	V_{EN} = 0V or fault condition active		30		
Output Voltage (5V Fixed Mode)	V_{OUT}	V_{SUP} = 6V to 36V, V_{FB} = V_{BIAS}, fixed-frequency mode (Note 5)	4.925	5.0	5.075	V
FB Feedback Voltage (Adjustable Mode)	V_{FB}	V_{SUP} = 6V to 36V, 0V < (V_{CS} - V_{OUT}) < 80mV, fixed-frequency mode	0.99	1.0	1.01	V
FB Current	I_{FB}	V_{FB} = 1.0V		0.02		µA
FB Line Regulation		V_{EN} = V_{SUP}, 6V < V_{SUP} < 36V (Note 5)		0.02		%/V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, C_{IN} = 10µF, C_{OUT} = 94µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 14.3kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transconductance (from FB to COMP)	$g_{m,EA}$			1200		µS
Error-Amplifier Output Impedance	$R_{OUT,EA}$			30		MΩ
Operating Frequency	f_{SW}	R_{FOSC} = 30.1kΩ		1000		kHz
		R_{FOSC} = 14.3kΩ	1800	2000	2200	
Minimum On-Time	$t_{ON(MIN)}$			80		ns
Maximum FSYNC Frequency	$f_{FSYNC(MAX)}$			2400		kHz
Minimum FSYNC Frequency	$f_{FSYNC(MIN)}$	f_{FSYNC} > 110% of internal frequency (20% duty cycle), f_{SW} = 1000kHz		1100		kHz
FSYNC Logic-High Threshold	$V_{FSYNC,HI}$		1.4			V
FSYNC Logic-Low Threshold	$V_{FSYNC,LO}$				0.4	V
FSYNC Internal Pulldown Resistance				1		MΩ
CURRENT LIMIT						
CS Input Current	I_{CS}	V_{CS} = V_{OUT} = 0V or V_{BIAS} (Note 6)	-1		+1	µA
OUT Input Current	I_{OUT}	During normal operation		22		µA
		V_{FB} = V_{BIAS}		32		
CS Current-Limit Voltage Threshold	V_{LIMIT}	V_{CS} - V_{OUT}, V_{BIAS} = 5V, V_{OUT} ≥ 2.5V	68	80	92	mV
FAULT DETECTION						
Output Overvoltage Trip Threshold	$V_{FB,OV}$	V_{OUT} = V_{FB}, rising edge	108	113	118	%V_{FB}
Output Overvoltage Trip Hysteresis				2.5		%
Output Overvoltage Fault Propagation Delay	t_{OVP}	Rising edge		25		µs
		Falling edge		25		
Output Undervoltage Trip Threshold	$V_{FB,UV}$	V_{OUT} = V_{FB}; with respect to slewed FB threshold, falling edge	83	88	93	%V_{FB}
Output Undervoltage Trip Hysteresis				2.5		%
Output Undervoltage Propagation Delay		Falling edge		25		µs
		Rising edge (excluding startup)		25		
PGOOD Output Low Voltage	$V_{PGOOD,L}$	I_{SINK} = 3mA			0.4	V
PGOOD Leakage Current	I_{PGOOD}			1		µA
Thermal-Shutdown Threshold	T_{SHDN}	(Note 6)		+175		°C
Thermal-Shutdown Hysteresis		(Note 6)		15		°C

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, C_{IN} = 10µF, C_{OUT} = 94µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 14.3kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

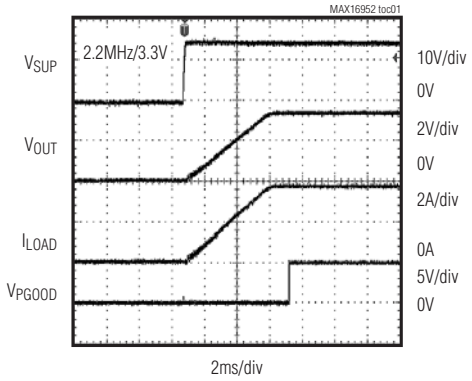
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVE						
DH Gate-Driver On-Resistance	R_{DH}	DH = high state		10		
		DH = low state		2		
DL Gate-Driver On-Resistance	R_{DL}	DL = high state		3.5		
		DL = low state		2		
DH/DL Dead Time (Note 6)	t_{DEAD}	DL rising		30		ns
		DH rising		30		
BST Input Current	I_{BST}	V_{LX} = 0V, V_{BST} = 5V, V_{DH} - V_{LX} = V_{DL} - V_{PGND} = 0V		1		µA
BST On-Resistance		(Note 6)		5	15	
ENABLE INPUT						
EN Input Threshold Low	$V_{EN,LO}$				1.2	V
EN Input Threshold High	$V_{EN,HI}$		2.2			V
EN Threshold Voltage Hysteresis				0.2		V
EN Input Current	I_{EN}			0.5		µA
SOFT-START						
Soft-Start Ramp Time	t_{SS}			5		ms

Note 3: Devices tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 4: For 3.5V operation, the n-channel MOSFET's threshold voltage should be compatible to (lower than) this input voltage.
Note 5: Device not in dropout condition.
Note 6: Guaranteed by design; not production tested.

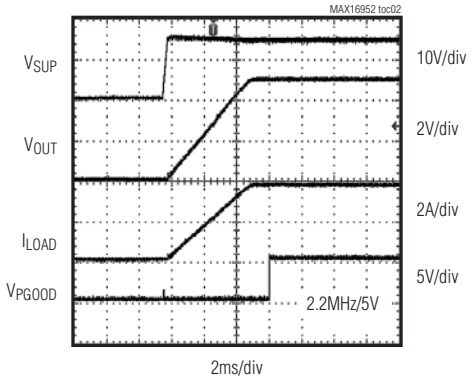
Typical Operating Characteristics

(V_{SUP} = V_{EN} = 14V, C_{IN} = 47µF, C_{OUT} = 94µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 13kΩ, V_{FB} = V_{BIAS}, R_{BST} = 75Ω, T_A = +25°C, unless otherwise noted.)

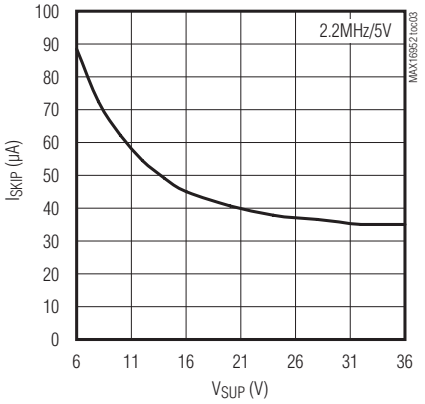
STARTUP RESPONSE (SKIP MODE)



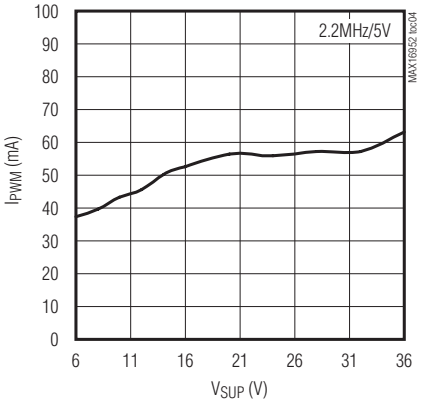
STARTUP RESPONSE (SKIP MODE)



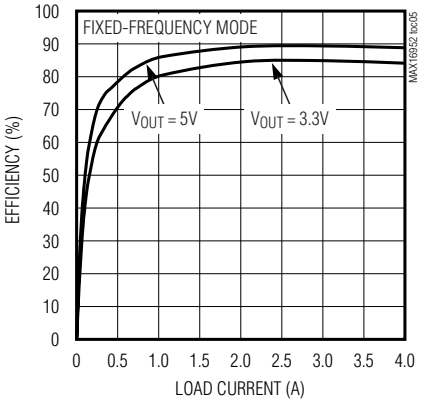
SKIP MODE SUPPLY CURRENT vs. V_{SUP}



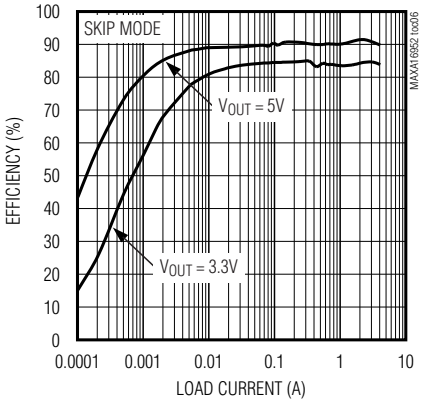
PWM MODE SUPPLY CURRENT vs. V_{SUP}



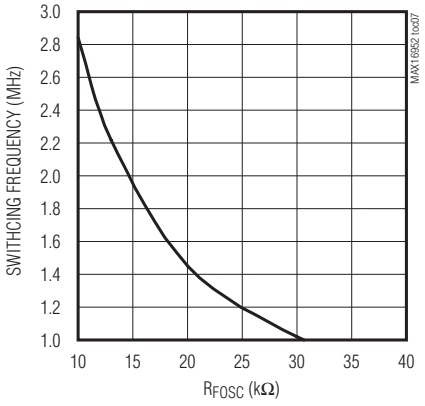
EFFICIENCY vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT



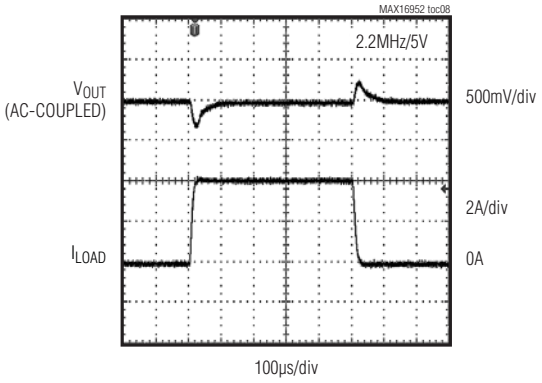
SWITCHING FREQUENCY vs. R_{FOSC}



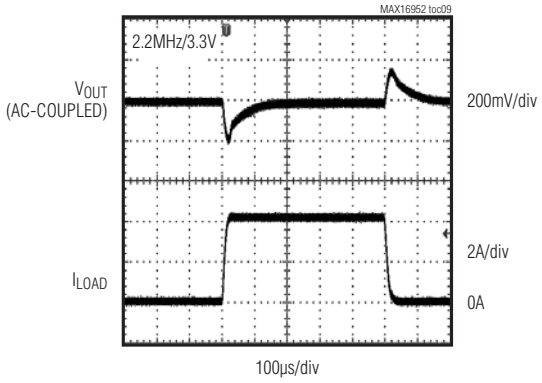
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, C_{IN} = 47µF, C_{OUT} = 94µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 13kΩ, V_{FB} = V_{BIAS}, R_{BST} = 75Ω, T_A = +25°C, unless otherwise noted.)

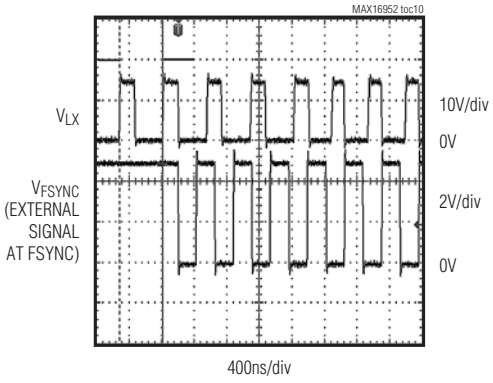
LOAD TRANSIENT (PWM MODE)



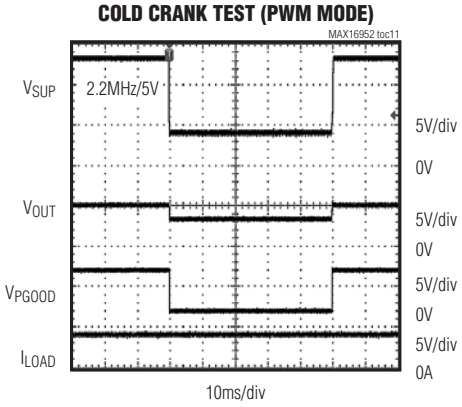
LOAD TRANSIENT (PWM MODE)



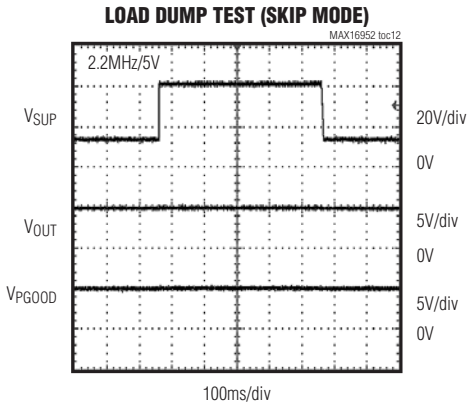
SYNCHRONIZATION WITH EXTERNAL SIGNAL AT FSYNC



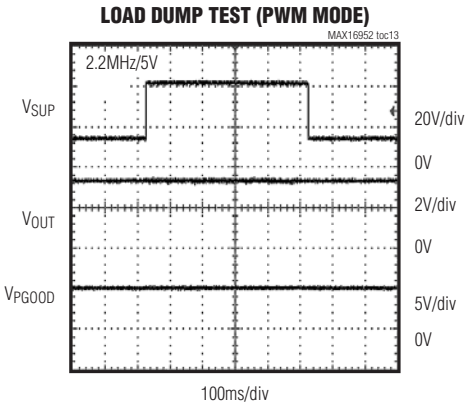
COLD CRANK TEST (PWM MODE)



LOAD DUMP TEST (SKIP MODE)



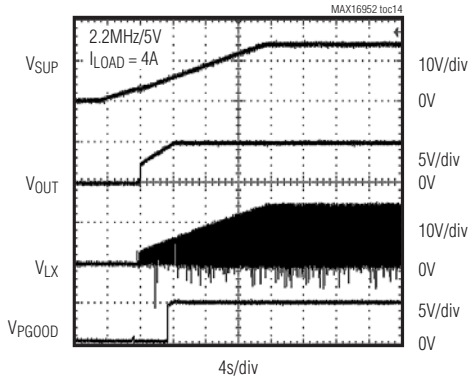
LOAD DUMP TEST (PWM MODE)



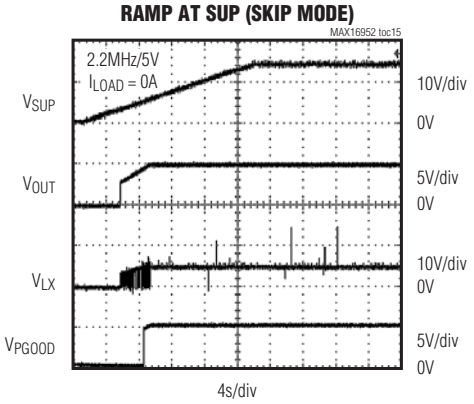
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, C_{IN} = 47µF, C_{OUT} = 94µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 13kΩ, V_{FB} = V_{BIAS}, R_{BST} = 75Ω, T_A = +25°C, unless otherwise noted.)

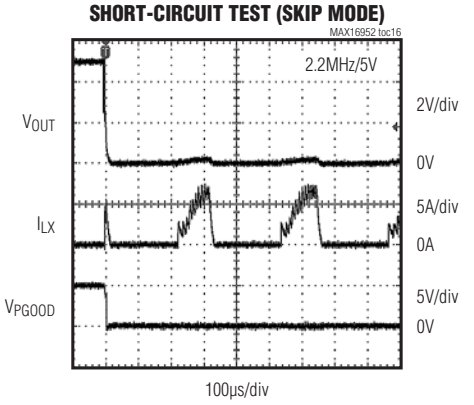
OUTPUT RESPONSE TO SLOW RAMP AT SUP (PWM MODE)



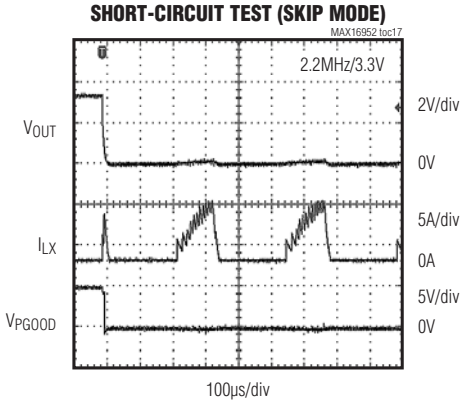
OUTPUT RESPONSE TO SLOW RAMP AT SUP (SKIP MODE)



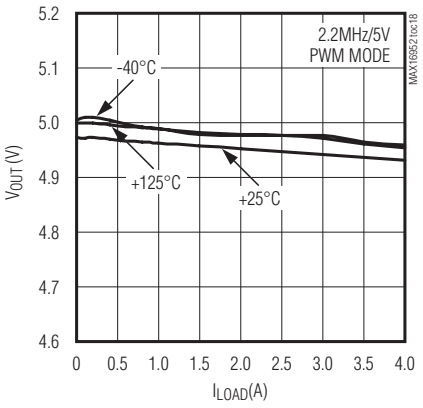
SHORT-CIRCUIT TEST (SKIP MODE)



SHORT-CIRCUIT TEST (SKIP MODE)



LOAD REGULATION (PWM MODE)



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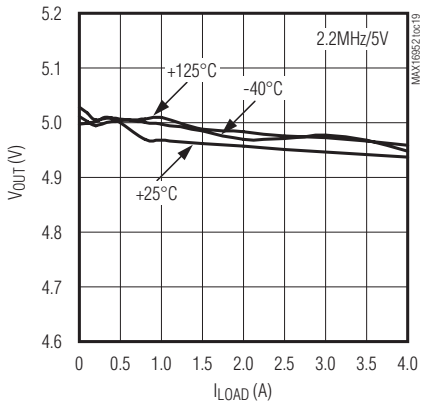
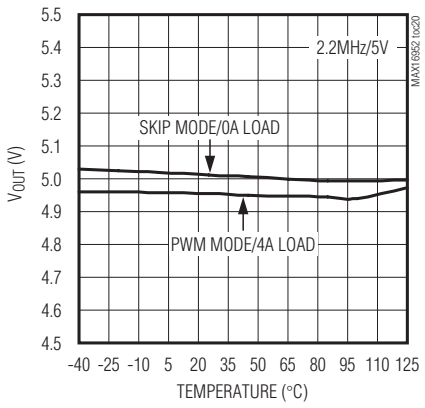


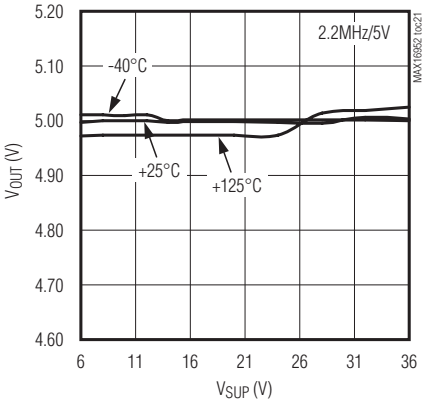
VOUT vs. TEMPERATURE



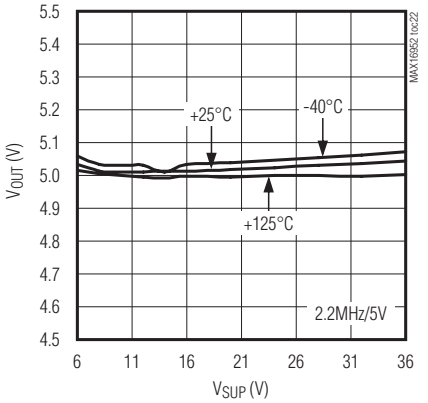
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, C_{IN} = 47µF, C_{OUT} = 94µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 13kΩ, V_{FB} = V_{BIAS}, R_{BST} = 75Ω, T_A = +25°C, unless otherwise noted.)

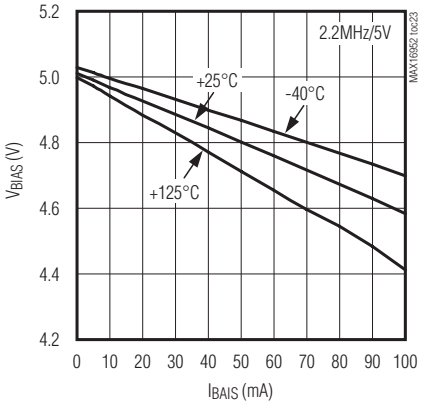
LINE REGULATION (PWM MODE)



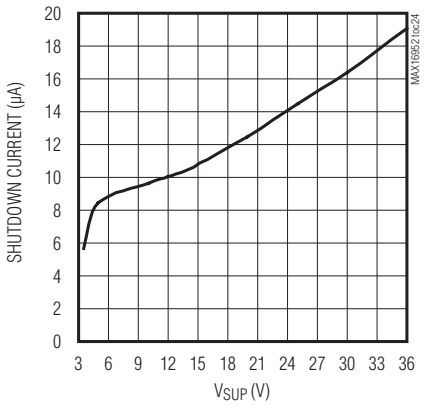
LINE REGULATION (SKIP MODE)



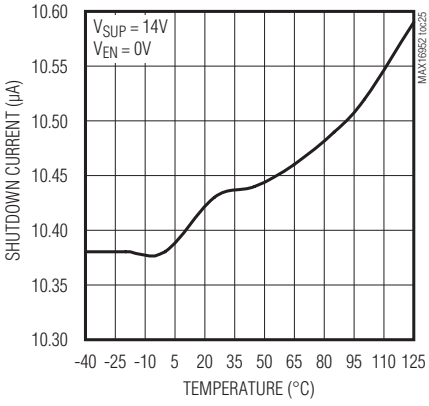
V_{BIAS} vs. I_{BIAS}



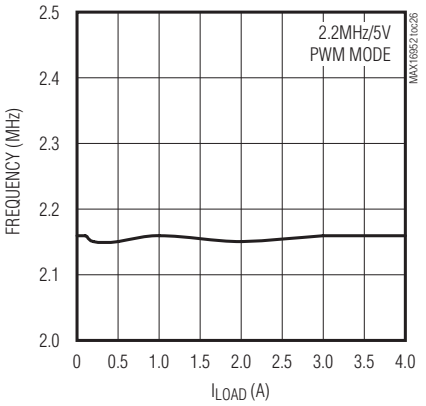
SHUTDOWN CURRENT vs. V_{SUP}



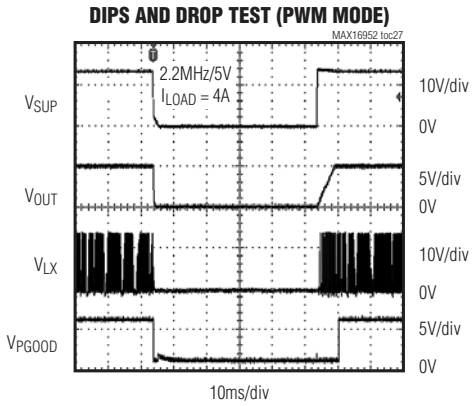
SHUTDOWN CURRENT vs. TEMPERATURE



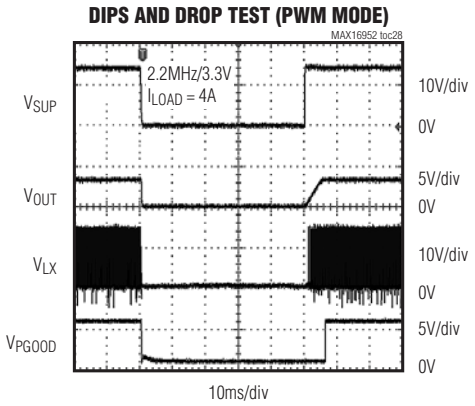
SWITCHING FREQUENCY vs. LOAD CURRENT



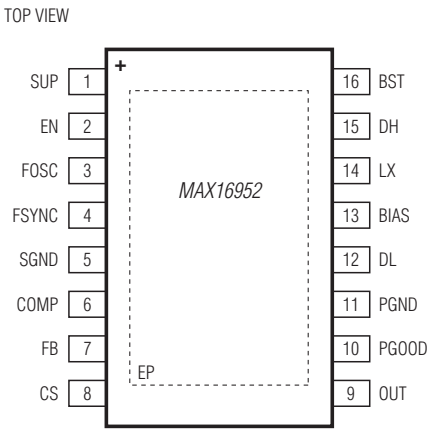
DIPS AND DROP TEST (PWM MODE)



DIPS AND DROP TEST (PWM MODE)



Pin Configuration



TSSOP

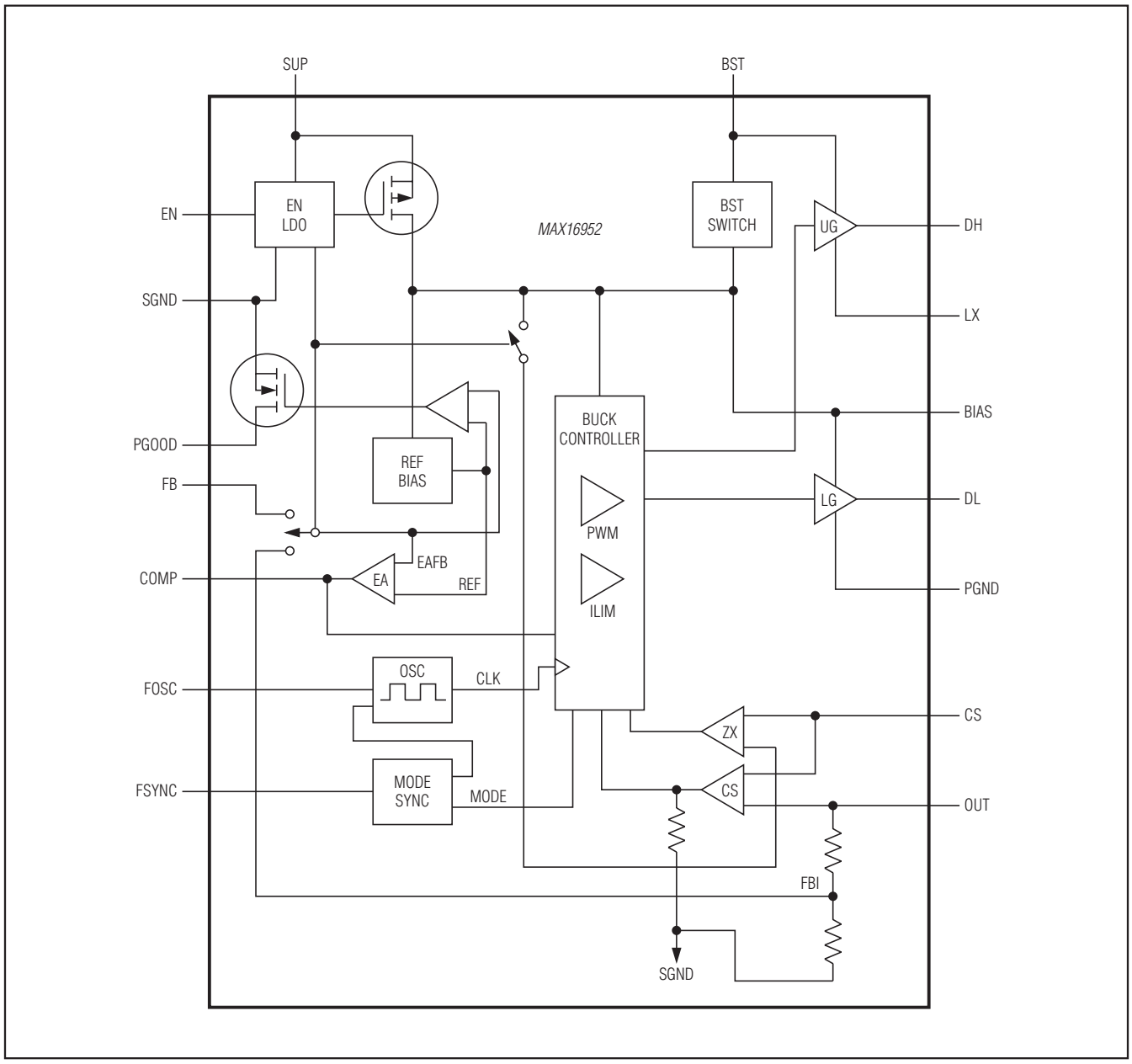
Pin Description

PIN	NAME	FUNCTION
1	SUP	Input Supply Voltage. SUP is the input voltage to the internal linear regulator. Bypass SUP to PGND with a 1µF minimum value ceramic capacitor.
2	EN	Active-High Enable Input. EN is compatible with 5V and 3.3V logic levels. Drive EN logic-high to enable the output or drive EN logic-low to put the controller in low-power shutdown mode. Connect EN to SUP for always-on operation. Do not leave EN unconnected.
3	FOSC	Oscillator-Timing Resistor Input. Connect a resistor from FOSC to SGND to set the oscillator frequency from 1MHz to 2.2MHz. See the *Setting the Switching Frequency* section.
4	FSYNC	Synchronization and Mode Selection Input. Connect FSYNC to BIAS to select fixed-frequency PWM mode and disable skip mode. Connect FSYNC to SGND to select skip mode. Connect FSYNC to an external clock for synchronization. FSYNC is internally pulled down to ground with a 1M_ resistor.
5	SGND	Signal Ground. Connect SGND directly to the local ground plane. Connect SGND to PGND at a single point.
6	COMP	Error Amplifier Output. Connect COMP to the compensation feedback network. See the *Compensation Design* section.
7	FB	Feedback Regulation Point. Connect FB to BIAS for a fixed 5V output voltage. In adjustable mode, connect to the center tap of a resistive divider from the output (V_{OUT}) to SGND to set the output voltage. The FB voltage regulates to 1V (typ).
8	CS	Positive Current-Sense Input. Connect CS to the positive terminal of the current-sense element. Figure 4 shows two different current-sensing options: 1) accurate sense with a sense resistor or 2) lossless inductor DCR sensing.

Pin Description (continued)

PIN	NAME	FUNCTION
9	OUT	Output Sense and Negative Current-Sense Input. When using the internal preset 5V feedback divider (FB = BIAS), the controller uses OUT to sense the output voltage. Connect OUT to the negative terminal of the current-sense element.
10	PGOOD	Open-Drain Power-Good Output. A logic-high voltage on PGOOD indicates that the output voltage is in regulation. PGOOD is pulled low when the output voltage is out of regulation. Connect a 10k_ pullup resistor from PGOOD to the digital interface voltage.
11	PGND	Power Ground. Connect the input and output filter capacitors' negative terminals to PGND. Connect PGND externally to SGND at a single point.
12	DL	Low-Side Gate-Driver Output. DL swings from V_{BIAS} to PGND. If a resistor is needed between DL and the gate of the MOSFET, the proper resistance value could be provided based on application circuit review result.
13	BIAS	Internal 5V Linear Regulator Output. BIAS provides power for bias and gate drive. Connect a 2.2µF to 10µF ceramic capacitor from BIAS to PGND.
14	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver.
15	DH	High-Side Gate-Driver Output. DH swings from LX to BST. If a resistor is needed between DH and the gate of the MOSFET, the proper resistance value could be provided based on application circuit review result.
16	BST	Boost Flying Capacitor Connection. Connect a ceramic capacitor between BST and LX. See the *Boost-Flying Capacitor Selection* section for details.
—	EP	Exposed Pad. Internally connected to ground. Connect EP to a large contiguous copper plane at SGND potential to improve thermal dissipation. Do not use as the main ground connection.

Functional Diagram



Detailed Description

The MAX16952 is a current-mode, synchronous PWM buck controller designed to drive logic-level MOSFETs. The device tolerates a wide input voltage range from 3.5V to 42V and generates an adjustable 1V to 10V or fixed 5V output voltage. This device can operate in dropout mode, making it ideal for automotive and industrial applications with undervoltage transients.

The internal switching frequency is adjustable from 1MHz to 2.2MHz with an external resistor and can be synchronized to an external clock. The high switching frequency reduces output ripple and allows the use of small external components. The device operates in both fixed-frequency PWM mode and a low quiescent current skip mode. While working in skip mode, the operating current is as low as 50µA.

The device features an enable logic input to disable the device and reduce its shutdown current to 10µA. Protection features include cycle-by-cycle current limit, overvoltage detection, and thermal shutdown. The device also features integrated soft-start and a power-good monitor to help with power sequencing.

Supply Voltage Range (SUP)

The supply voltage range (V_{SUP}) of the MAX16952 is compatible to the typical automotive battery voltage range from 3.5V to 36V and can tolerate up to 42V transients.

Slow Ramp-Up of the Input Voltage

If the input voltage (V_{SUP}) ramps up slowly, the device operates in dropout mode until V_{SUP} is greater than the regulated output voltage. The dropout mode is detected by monitoring high-side FET on for eight clock cycles. Once dropout mode is detected, the controller issues a forced low-side pulse at the rising edge of switching clock to refresh the BST capacitor. This maintains the proper BST voltage to turn on the high-side MOSFET when the device is in dropout mode.

System Enable (EN) and Soft-Start

An enable control input (EN) activates the MAX16952 from its low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3.5V. The high-voltage compatibility allows EN to be connected to SUP, KEY/KL30, or the inhibit pin (INH) of a CAN transceiver.

A logic-high at EN turns on the internal regulator. Once V_{BIAS} is above the internal lockout level, V_{UVL} = 3.1V (typ), the controller starts up with a 5ms fixed soft-start time. Once regulation is reached, PGOOD goes high impedance.

A logic-low at EN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 10µA (typ).

To protect the low-side MOSFET during shutdown, the step-down regulator cannot be enabled until the output voltage drops below 1.25V. An internal 30Ω pulldown switch helps discharge the output. If the EN pin is toggled low then high, the switching regulator shuts down and remains off until the output voltage decays to 1.25V. At this point, the MAX16952 turns on using the soft-start sequence.

Fixed 5V Linear Regulator (BIAS)

The MAX16952 has an internal 5V linear regulator to provide its own 5V bias from a high-voltage input supply at SUP. This bias supply powers the gate drivers for the external n-channel MOSFETs and provides the power required for the analog controller, reference, and logic blocks. The bias rail needs to be stabilized by a 2.2µF or greater capacitance at BIAS, and can provide up to 45mA (typ) total current.

Oscillator Frequency and External Synchronization

The MAX16952 provides an internal oscillator adjustable from 1MHz to 2.2MHz. To set the switching frequency, connect a resistor from FOSC to SGND. See the *Setting the Switching Frequency* section.

The MAX16952 can also be synchronized to an external clock by connecting the external clock signal to FSYNC. For proper frequency synchronization, FSYNC's input frequency must be at least 10% higher than the programmed internal oscillator frequency. A rising clock edge on FSYNC is interpreted as a synchronization input. If the FSYNC signal is lost, the internal oscillator takes control of the switching rate, returning to the switching frequency set by the resistor connected to FOSC. This maintains output regulation even with intermittent FSYNC signals. The maximum synchronizable frequency is 2.4MHz.

When FSYNC is connected to SGND, the device operates in skip mode. When FSYNC is connected to BIAS or driven by an external clock, the MAX16952 operates in skip mode during soft-start and transitions to fixed-frequency PWM mode after soft-start is over.

Error Detection and Fault Behavior

Several error-detection mechanisms prevent damage to the MAX16952 and the application circuit:

- Overcurrent protection
- Output overvoltage protection
- Undervoltage lockout at BIAS
- Power-good detection of the output voltage
- Overtemperature protection of the IC

Overcurrent Protection

The MAX16952 provides cycle-by-cycle current limiting as long as the FB voltage is greater than 0.7V (i.e., 70% of the regulated output voltage). If the output voltage drops below 70% of the regulation point due to overcurrent event, 16 consecutive current-limit events initiate restart. If the overcurrent is still present during restart, the MAX16952 shuts down and initiates restart. This automatic restart continues until the overcurrent condition disappears. If the overcurrent condition disappears at any restart attempt, the device enters the normal soft-start routine.

Output Overvoltage Protection

The MAX16952 features an internal output overvoltage protection. If V_{OUT} increases by 13% (typ) of the intended regulation voltage, the high-side MOSFET turns off and the low-side MOSFET turns on. The low-side MOSFET stays on until V_{OUT} goes back into regulation. Once V_{OUT} is in regulation, the normal switching cycles continue.

Undervoltage Lockout (UVLO)

The BIAS input undervoltage lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its UVLO threshold, 3.1V (typ). If the BIAS voltage drops below the UVLO threshold, the controller stops switching and turns off both high-side and low-side gate drivers until the BIAS voltage recovers.

Power-Good Detection (PGOOD)

The MAX16952 includes a power-good comparator with added hysteresis to monitor the step-down controller's output voltage and detect the power-good threshold. The PGOOD output is open drain and should be pulled up with an external resistor to the supply voltage of the logic input it drives. This voltage should not exceed 6V. Pullup resistor should not be less than 1kΩ , such that pulldown voltage is less than 400mV with a 5V supply. PGOOD can sink up to 3mA of current while low.

PGOOD asserts low during the following conditions:

- Standby mode
- Undervoltage with V_{OUT} below 88% (typ) its set value
- Overvoltage with V_{OUT} above 113% (typ) its set value

The power-good levels are measured at FB if a feedback divider is used. If the MAX16952 is used in 5V mode with FB connected to BIAS, OUT is used as a feedback path for voltage regulation and power-good determination.

Overtemperature Protection

Thermal-overload protection limits total power dissipation in the MAX16952. When the junction temperature exceeds +175°C (typ), an internal thermal sensor shuts down the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C and the output voltage has dropped below 1.25V (typ).

A continuous overtemperature condition can cause on-/off-cycling of the device.

Fixed-Frequency, Current-Mode PWM Controller

The MAX16952's step-down controller uses a PWM, current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is an open-loop comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus the slope compensation ramp, which are summed into the main PWM comparator to preserve inner-loop stability and eliminate inductor stair-casing. At each falling edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips, the maximum duty cycle is reached, or the peak current limit is reached. During this on-time, current ramps up through the inductor, storing energy in its magnetic field and sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. The circuit acts as a switch-mode transconductance amplifier and eliminates the influence of the output LC filter double pole.

During the second half of the cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the output. The output capacitor stores charge when the inductor current

exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under soft-overload conditions, when the peak inductor current exceeds the selected current limit, the high-side MOSFET is turned off immediately. The low-side MOSFET is turned on and remains on to let the inductor current ramp down until the next clock cycle.

Forced Fixed-Frequency PWM Mode

The low-noise forced fixed-frequency PWM mode (FSYNC connected to BIAS or an external clock) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-driver waveform to constantly be the complement of the high-side gate-drive waveform. The inductor current reverses at light loads while DH maintains a duty factor of V_{OUT}/V_{SUP}.

The benefit of forced fixed-frequency PWM mode is to keep the switching frequency fairly constant. However, forced fixed-frequency PWM operation comes at a cost: the no-load 5V supply current can be up to 45mA, depending on the external MOSFETs and switching frequency. Forced fixed-frequency PWM mode is most useful for avoiding audio frequency noises and improving load-transient response.

Light-Load Low-Quiescent Operating (Skip) Mode

The MAX16952 includes a light-load operating mode control input (FSYNC = SGND) used to enable or disable the zero-crossing comparator. When the zero-crossing comparator is enabled, the regulator forces DL low when the current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitor and forces the regulator to skip pulses under light-load conditions to avoid overcharging the output.

The lowest operating currents can be achieved in skip mode. When the MAX16952 operates in skip mode with no external load current, the overall current consumption can be as low as 50µA. A disadvantage of skip mode is that the operating frequency is not fixed.

Skip-Mode Current-Sense Threshold

When skip mode is enabled, the on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the idle-mode current-sense threshold ($V_{CS,IDLE}$). See Figure 1. Under light-load conditions, the on-time duration depends solely on the skip-mode current-sense threshold, which is 25mV (typ). This forces the controller to source a minimum amount of power with each cycle. To avoid overcharging the output, another on-time cannot begin until the output voltage drops below the feedback threshold. Because the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses. Therefore, the controller regulates the valley of the output ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to pulse frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across CS to OUT. Once (V_{CS} - V_{OUT}) drops below the 6mV zero-crossing, current-sense threshold, the comparator forces DL low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is given by:

$$I_{LOAD(SKIP)}[A] = \frac{(V_{SUP} - V_{OUT})V_{OUT}}{2 \times V_{SUP} \times f_{SW}[MHz] \times L[\mu H]}$$

The switching waveforms can appear noisy and asynchronous when light-loading causes pulse-skipping operation. This is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce higher efficiency under light load, while higher values result in higher full-load efficiency (assuming that the coil resistance remains constant) and less output-voltage ripple. Drawbacks of using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

MOSFET Gate Drivers (DH and DL)

The DH and DL drivers are optimized for driving logic-level n-channel power MOSFETs. The DH high-side n-channel MOSFET driver is powered by charge pumping at BST, while the DL synchronous rectifier drivers are powered directly by the 5V linear regulator (BIAS).

An adaptive dead-time circuit monitors the DH and DL outputs and prevents the opposite-side MOSFET from turning on until the other MOSFET is fully off. Thus, the circuit allows the high-side driver to turn on only when the DL gate driver has been turned off. Similarly, it prevents the low-side (DL) from turning on until the DH gate driver has been turned off.

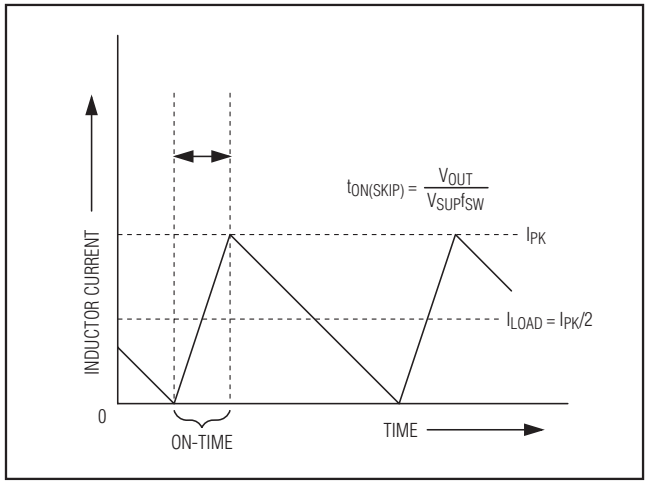


Figure 1. Pulse-Skipping/Discontinuous Crossover Point

The adaptive driver dead-time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. To minimize stray impedance, use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the controller).

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal low-side Schottky catch diode with a low-resistance MOSFET switch. The internal pulldown transistor that drives DL low is robust, with a 2Ω (typ) on-resistance. This low on-resistance helps prevent DL from being pulled up during the fast rise time of the LX node, due to capacitive coupling from the drain to the gate of the low-side synchronous rectifier MOSFET. Applications with high-input voltages and long-inductive driver traces can require additional gate-to-source capacitance. This ensures that fast-rising LX edges do not pull up the low-side MOSFET's gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{GD} = C_{RSS}), gate-to-source capacitance (C_{GS} = C_{ISS} - C_{GD}), and additional board parasitic should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{SUP}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Although a low-resistive path from DH and DL to the MOSFET gates is encouraged, there are cases where series resistors can be added. For instance, a series resistor can be added to the DL path. However, in this case, the design should have at least as much resistance in series with the BST cap in order to help prevent shootthrough current.

High-Side Gate-Drive Supply (BST)

The high-side MOSFET is turned on by closing an internal switch between BST and DH. This provides the necessary g ate-to-source voltage to turn on the high-side MOSFET, an action that boosts the gate-drive signal above V_{SUP}. The boost capacitor connected between BST and LX holds up the voltage across the flying gate driver during the high-side MOSFET on-time.

The charge lost by the boost capacitor for delivering the gate charge is refreshed when the high-side MOSFET is turned off and the LX node swings down to ground. When the LX node is low, an internal high-voltage switch connected between BIAS and BST recharges the boost capacitor to the BIAS voltage. See the *Boost-Flying Capacitor Selection* section to choose the right size of the boost capacitor.

Dropout Behavior During Undervoltage Transients

The controller generates a low-side pulse every eight clock cycles to refresh the BST capacitor during low-dropout operation. This guarantees that the MAX16952 operates in dropout mode during undervoltage transients like cold crank. See the *Boost-Flying Capacitor Selection* section for more details.

Current Limiting and Current-Sense Inputs (CS and OUT)

The current-limit circuit uses differential current-sense inputs (CS and OUT) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM controller turns off the high-side MOSFET. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT}/V_{SUP}). See the *Current Sensing* section.

Design Procedure

Effective Input Voltage Range

Although the MAX16952 controller can operate from input supplies up to 42V and regulate down to 1V, the minimum voltage conversion ratio (V_{OUT}/V_{SUP}) might be limited by the minimum controllable on-time. For proper fixed-frequency PWM operation, the voltage conversion ratio should obey the following condition:

$$\frac{V_{OUT}}{V_{SUP}} > t_{ON(MIN)} \times f_{SW}$$

where $t_{ON(MIN)}$ is 80ns and f_{SW} is the switching frequency in Hz. If the desired voltage conversion does

not meet the above condition, then pulse skipping occurs to decrease the effective duty cycle. To avoid this, decrease the switching frequency or lower the input voltage (V_{SUP}).

Setting the Output Voltage

Connect FB to BIAS to enable the fixed step-down controller output voltage (5V), set by a preset, internal resistive voltage-divider connected between the output (OUT) and SGND.

To achieve other output voltages between 1V to 10V, connect a resistive divider from OUT to FB to SGND (Figure 2). Select R_{FB2} (FB to SGND resistor) less than or equal to 100kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 1V (typ) (see the *Electrical Characteristics* table) and V_{OUT} can range from 1V to 10V.

Setting the Switching Frequency

The switching frequency, f_{SW}, is set by a resistor (R_{FOSC}) connected from FOSC to SGND. See Figure 3 to select the correct R_{FOSC} value for the desired switching frequency.

For example, a 2MHz switching frequency is set with R_{FOSC} = 14.3kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX16952: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT}\left(V_{SUP(MIN)} - V_{OUT}\right)}{V_{SUP(MIN)} \times f_{SW} \times I_{OUT(MAX)} \times \ LIR}$$

where $V_{SUP(MIN)}$ is the minimum supply voltage, V_{OUT} is the typical output voltage, and $I_{OUT(MAX)}$ is the maximum load current. The switching frequency is set by R_{FOSC} (see the *Setting the Switching Frequency* section).

The MAX16952 uses internal frequency independent slope compensation to ensure stable operation at duty cycles above 50%. Use the equation below to select the inductor value:

$$\frac{V_{OUT}[V]}{L[\mu H] \times f_{SW}[MHz]} = 1 \pm 25\%$$

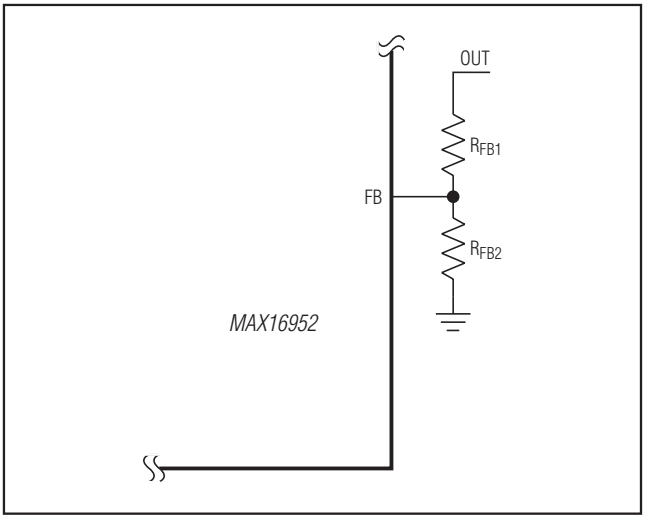


Figure 2. Adjustable Output Voltage

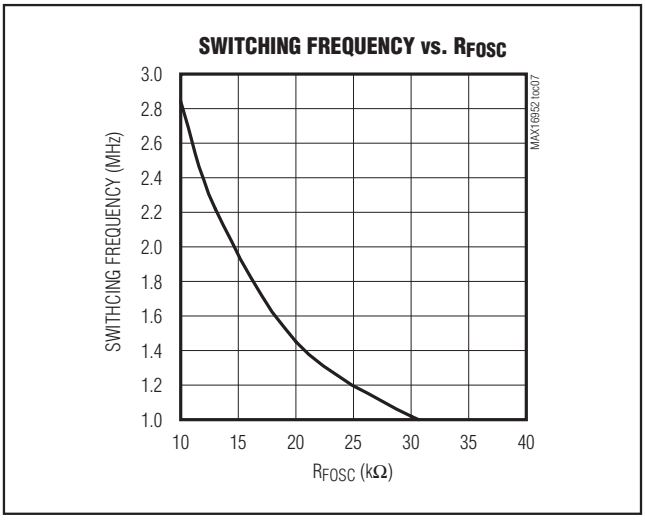


Figure 3. Switching Frequency vs. R_{FOSC}

However, if it is necessary, higher inductor values can be selected.

The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, efficiency, and transient response requirements. Table 1 shows a comparison between small and large inductor sizes.

Table 1. Inductor Size Comparison

INDUCTOR SIZE	
SMALLER	**LARGER**
Lower price	Smaller ripple
Smaller form factor	Higher efficiency
Faster load response	Larger fixed-frequency range in skip mode

The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 25% and 45% ripple current. When pulse skipping (FSYNC low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{SUP} - V_{OUT})}{V_{SUP} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in mA, L is in µH, and f_{SW} is in kHz.

The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Transient Response

The inductor ripple current also impacts transient response performance, especially at low V_{SUP} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The total output voltage sag is the sum of the voltage sag while the inductor is ramping up and the voltage sag before the next pulse can occur:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2C_{OUT}((V_{SUP} \times D_{MAX}) - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)}(t - \Delta t)}{C_{OUT}}$$

where D_{MAX} is the maximum duty factor, L is the inductor value in µH, C_{OUT} is the output capacitor value in µF, t is the switching period ($1/f_{SW}$) in µs, and Δt equals (V_{OUT}/V_{SUP}) $\times t$ when in fixed-frequency PWM mode, or $L \times 0.2 \times I_{MAX}/(V_{SUP} - V_{OUT})$ when in skip mode. The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

Current Sensing

For the most accurate current sensing, use a current-sense resistor (R_{SENSE}) between the inductor and the output capacitor. Connect CS to the inductor side of R_{SENSE}, and OUT to the capacitor side. Size R_{SENSE} such that its maximum current (I_{OC}) induces a voltage of V_{LIMIT} (68mV minimum) across R_{SENSE}.

If a higher voltage drop across R_{SENSE} must be tolerated, divide the voltage across the sense resistor with a voltage-divider between CS and OUT to reach V_{LIMIT} (68mV minimum).

The current-sense method (Figure 4) and magnitude determine the achievable current-limit accuracy and power loss. Typically, higher current-sense limits provide tighter accuracy, but also dissipate more power. For the best current-sense accuracy and overcurrent protection, use a ±1% tolerance current-sense resistor with low parasitic inductance between the inductor and output as shown in Figure 4a.

Alternatively, high-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 4b) with an equivalent time constant:

$$R_{CSHL} = \left(\frac{R_2}{R1 + R2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left(\frac{1}{R1} + \frac{1}{R2}\right)$$

where R_{CSHL} is the required current-sense resistor and R_{DCR} is the inductor's series DC resistance. Use the typical inductance and R_{DCR} values provided by the inductor manufacturer.

Carefully observe the PCB layout guidelines to ensure the noise and DC errors do not corrupt the differential current-sense signals seen by CS and OUT. Place the sense resistor close to the IC with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

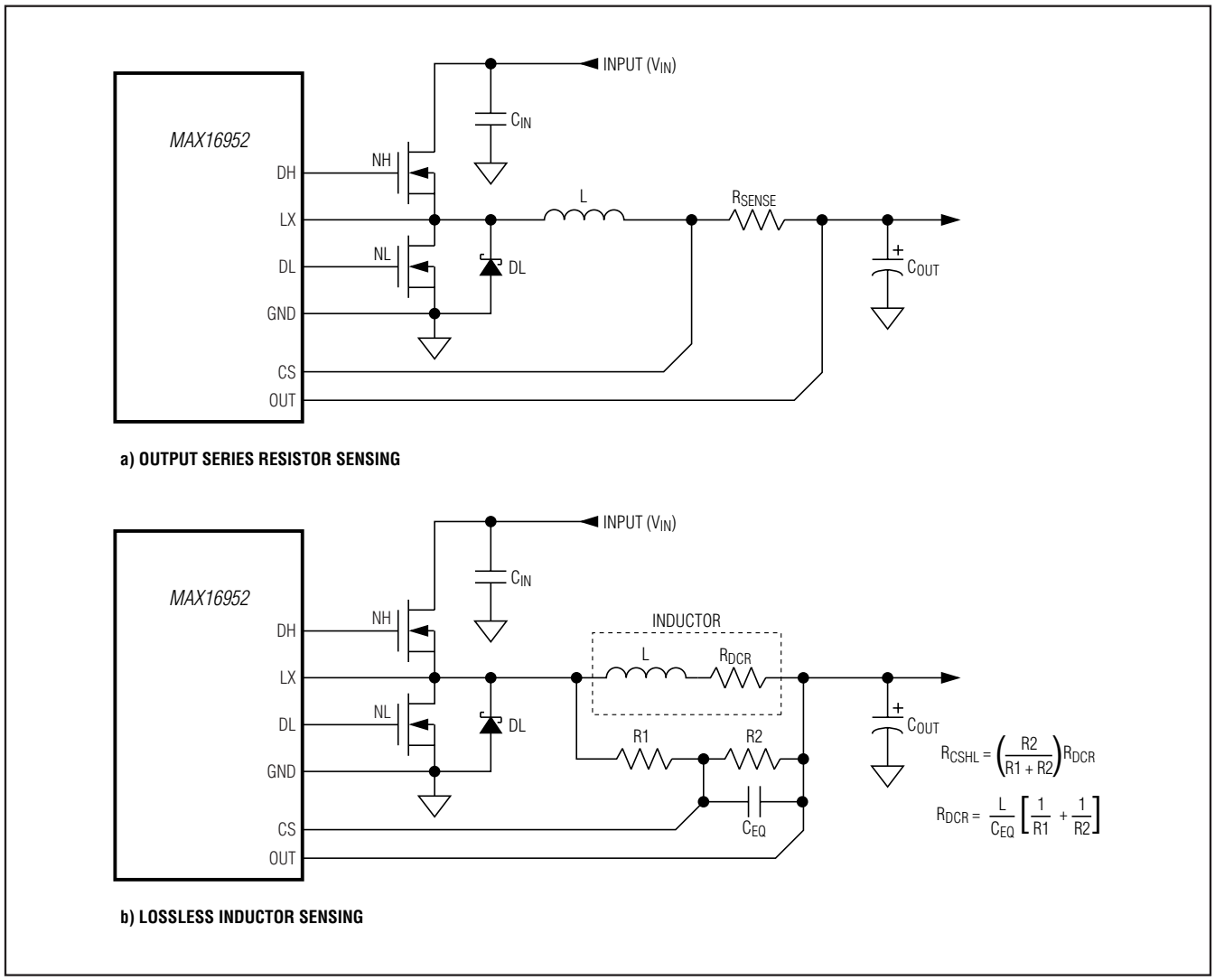


Figure 4. Current-Sense Configurations

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{SUP} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high-ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$D = \frac{V_{OUT}}{V_{SUP}}$$

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple. The size of the output capacitor depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

In skip mode, the inductor current becomes discontinuous, with the peak current set by the skip-mode current-sense threshold (V_{SKIP} = 32mV, typ). In skip mode, the no-load output ripple can be determined as follows:

$$V_{RIPPLE(P-P)} = \frac{V_{SKIP} \times ESR}{R_{SENSE}}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-value filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-value filter capacitors typically have high-ESR zeros that can affect the overall stability.

Compensation Design

The MAX16952 uses an internal transconductance error amplifier with its inverting input and its output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability. The inductor and the output capacitor are chosen based on performance, size, and cost. Additionally, the compensation network optimizes the control-loop stability.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The MAX16952 uses the voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a

smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. A simple single-series resistor (R_C) and capacitor (C_C) are required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (Figure 5). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to SGND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The power modulator has a DC gain set by $g_{mc} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations determine the approximate value for the gain of the power modulator ($GAIN_{MOD(dc)}$), neglecting the effect of the ramp stabilization. Ramp stabilization is necessary when the duty cycle is above 50% and is internally and automatically done for the MAX16952:

$$GAIN_{MOD(dc)} \cong g_{mc} \times \frac{R_{LOAD} \times f_{SW} \times L}{R_{LOAD} + (f_{SW} \times L)}$$

where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$ in Ω, f_{SW} is the switching frequency in MHz, L is the output inductance in µH, and $g_{mc} = 1/(A_{V_CS} \times R_{DC})$ in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 11V/V. R_{DC} is the DC-resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor, its ESR, and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times f_{SW} \times L}{R_{LOAD} + (f_{SW} \times L)} + ESR \right)}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of n identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and $ESR = ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of like capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(dc)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error amplifier transconductance, and $R_{OUT,EA}$ is the output resistance of the error amplifier. Use $g_{m,EA}$ of 2500µS (max) and $R_{OUT,EA}$ of 30MΩ (typ) for compensation design with the highest phase margin.

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C), the compensation resistor (R_C), and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)).

Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5 the switching frequency and much higher than the power-modulator pole (f_{pMOD}):

$$f_{pMOD} << f_C \le \frac{f_{SW}}{5}$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error amplifier gain at f_C should be equal to 1. So:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(fC)} = 1$$

For the case where f_{zMOD} is greater than f_C:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor, C_F, from COMP to SGND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

For the case where f_{zMOD} is less than f_C:

The power-modulator gain at f_C is:

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C} = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT} \times f_C}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(f_C)} \times f_{zMOD}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD} (f_{zEA} = f_{pMOD}):

$$C_C = \frac{1}{2\pi \times f_{2MOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor C_F from COMP to SGND. Set f_{pEA} = f_{zMOD} and calculate C_F as follows:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

MOSFET Selection

The MAX16952's controller drives two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Minimum threshold voltage ($V_{TH(MIN)}$)
- Total gate charge (Q_G)
- Reverse-transfer capacitance (C_{RSS})
- Power dissipation

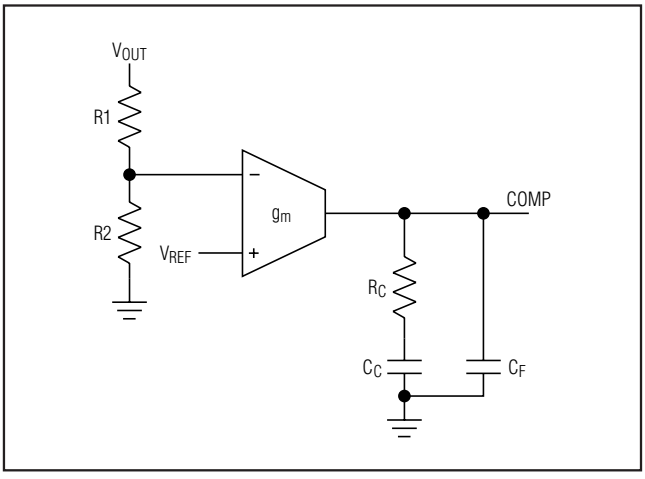


Figure 5. Compensation Network

Both n-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Ensure that the conduction losses at minimum input voltage do not exceed MOSFET package thermal limits or violate the overall thermal budget. Also, ensure that the conduction losses, plus switching losses at the maximum input voltage, do not exceed package ratings or violate the overall thermal budget. The MAX16952's DL gate driver must drive the low-side MOSFET (NL). In particular, check that the dV/dt caused by the high-side MOSFET (NH) turning on does not pull up the NL gate through its drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Therefore, if the drive current is taken from the internal LDO regulator, the power dissipation due to drive losses must be checked. Both MOSFETs must be selected so that their total gate charge is low enough; therefore, BIAS can power both drivers without overheating the IC:

$$P_{DRIVE} = (V_{SUP} - V_{BIAS}) \times Q_{G_TOTAL} \times f_{SW}$$

where Q_{G_TOTAL} is the sum of the gate charges of both MOSFETs.

Boost-Flying Capacitor Selection

The bootstrap capacitor stores the gate voltage for the internal switch. Its size is constrained by the switching frequency and the gate charge of the high-side MOSFET. Ideally the bootstrap capacitance should be at least nine times the gate capacitance:

$$C_{BST(TYP)} = 9 \times \frac{Q_G}{V_{BIAS}}$$

This results in a 10% voltage drop when the gate is driven. However, if this value becomes too large to be recharged during the minimum off-time, a smaller capacitor must be chosen.

During recharge, the internal bootstrap switch acts as a resistor, resulting in an RC circuit with the associated time constants. Two τs (time constants) are necessary to charge from 90% to 99%. The maximum allowable capacitance is, therefore:

$$C_{BST(MAX)} = \frac{t_{OFF(MIN)}}{2 \times R_{BST(MAX)}}$$

The minimum off-time allowed for the MAX16952 is 100ns (typ). If eight consecutive 100ns pulses are detected, the LSFET is forced on for one-half clock cycle minimum. This is to ensure that the charge on the boost capacitor is replenished fully.

The worst case operation is when the MAX16952 is close to dropout, but not fully in dropout with no load on the output. This means consecutive minimum off-time pulses are < 8. In this scenario, ensure that the amount of charge lost per cycle is replenished in 100ns.

In some applications external boost resistor is added to slow down the turn-on time for the HSFET. This causes an extra voltage drop on the BST capacitor per cycle and can require a parallel boostrap diode.

Let us assume:

Q_G = total gate charge for HSFET

Q_{BST} = BST charge lost per cycle

V_L = BIAS voltage = 5V (typ)

V_{BST} = BST voltage (BST - LX)

R_{BST_EXT} = external boost resistor used (connected between BST capacitor and BST pin)

R_{BST} = internal boost switch resistance = 5Ω (typ)

With the above set of parameters ensure that:

$Q_{BST} > Q_G$ for every 100ns minimum off-time

$Q_{BST} = (V_L - V_{BST})/(R_{BST_EXT} + R_{BST}) \times 100ns$

The threshold voltage (V_{TH}) of the external HSFET used determines the $V_L - V_{BST}$ number. If 3V is the external HSFET threshold voltage, $V_L - V_{BST}$ = 2V.

Now, if $Q_{BST} > Q_G$ is not satisfied, an external parallel bootstrap Schottky diode is required.

Applications Information

PCB Layout Guidelines

Make the controller ground connections as follows: create a small analog ground plane near the IC by using any of the PCB layers. Connect this plane to SGND and use this plane for the ground connection for the SUP bypass capacitor, compensation components, feedback dividers, and FOSC resistor.

Place all power components on the top side of the board and run the power stage currents, especially large high-frequency components, using traces or copper fills on the top side only, without adding vias.

On the top side, lay out a large PGND copper area for the output, and connect the bottom terminals of the high-frequency input capacitors, output capacitors, and the source terminals of the low-side MOSFET to that area.

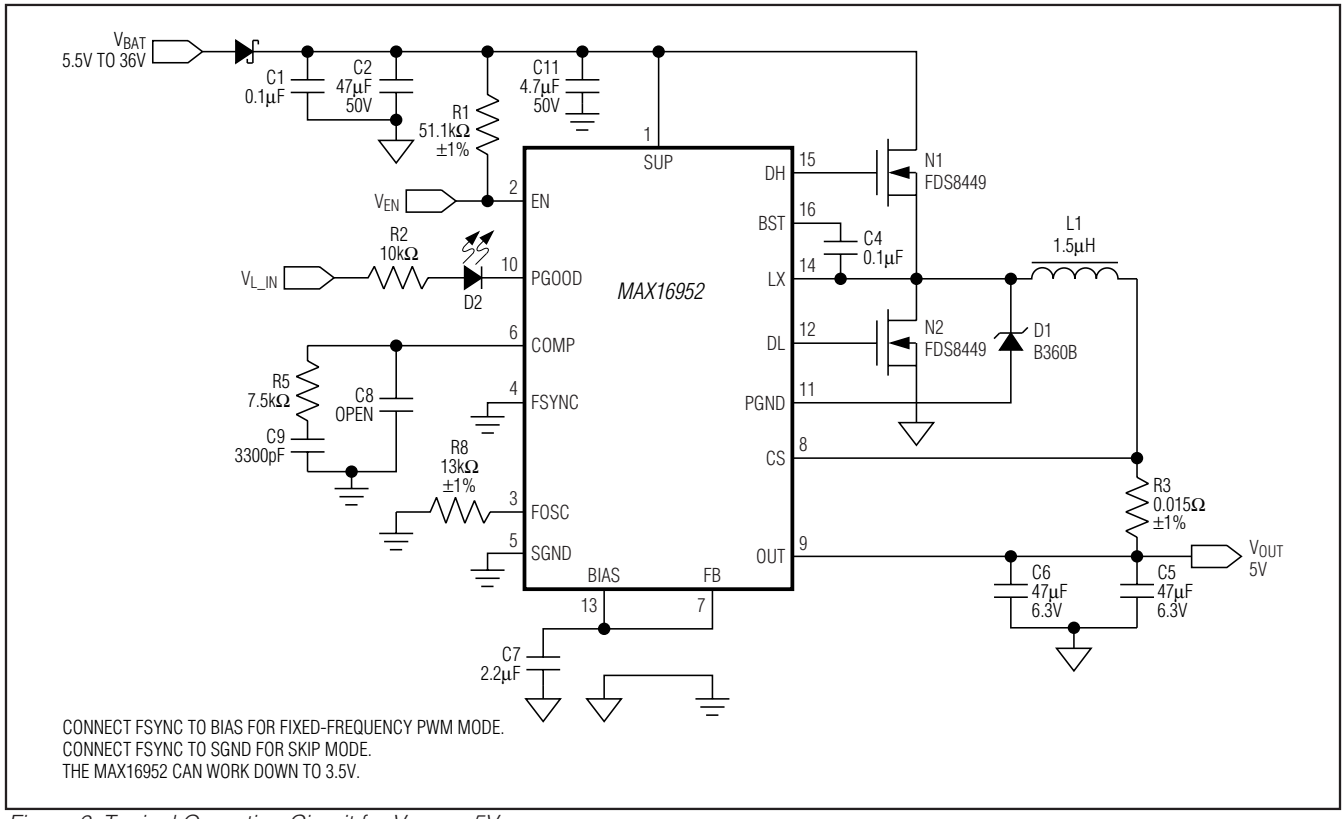


Figure 6. Typical Operating Circuit for V_{OUT} = 5V

Keep the power traces and load connections short, especially at the ground terminals. This practice is essential for high efficiency and jitter-free operation. Use thick copper PCBs (2oz vs. 1oz) to enhance efficiency.

Place the controller IC adjacent to the synchronous rectifier MOSFET (NL) and keep the connections for LX, PGND, DH, and DL short and wide. Use multiple small vias to route these signals from the top to the bottom side, if these signals need to be routed in the bottom layer. The gate current traces must be short and wide, measuring 50 mils to 100 mils wide if the low-side MOSFET is 1in from the controller IC. Connect the PGND trace from the IC close to the source terminal of the low-side MOSFET.

Route high-speed switching nodes (BST, LX, DH, and DL) away from the sensitive analog areas (FOSC, COMP, and FB). Group all SGND-referred and feedback components close to the IC. Keep the FB and compensation network nets as small as possible to prevent noise pickup. Place the sense resistor close to the IC with short, direct traces, making a Kelvin-sense connection to the current-sense resistor. Place BIAS capacitor close to the IC and minimize vias in the path in order to minimize transients on the BIAS line.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP-EP	U16E+3	21-0108	90-0120

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—
1	10/12	Changed V_{OUT} limit to 10V	1, 2, 12, 16
2	1/13	Added MAX16952AUE+ to *Ordering Information*	1
3	12/13	Updated *Transient Response* section	17
4	10/14	Updated GATE DRIVE section in *Electrical Characteristics*, pins 12 and 15 in *Pin Description*, *Fixed 5V Linear Regulator (BIAS)*, *Overcurrent Protection*, *Power-Good Detection (PGOOD)*, *Automatic Pulse-Skipping Crossover*, *MOSFET Gate Drivers (DH and DL)*, and *PCB Layout Guidelines* sections	4, 10, 12–15, 22, 23
5	1/15	Updated *Benefits and Features* section	1
6	3/15	Added new Note 1 in *Absolute Maximum Ratings* section and renumbered remaining notes in *Package Thermal Characteristics* and *Electrical Characteristics* sections	2–4

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