UJA1018

LIN system basis chip with LED drivers

Rev. 1 — 10 July 2012 Product data sheet

1. General description

The UJA1018 is a LIN 2.0/2.1/2.2/SAE J2602 transceiver with an integrated low-drop voltage regulator. The voltage regulator can deliver up to 70 mA at 5.0 V. The UJA1018 facilitates the development of compact nodes in LIN bus systems. In addition, the UJA1018 supports LIN node address assignment in daisy chain networks via a LIN bus switch. To support robust designs, the UJA1018 offers strong ElectroStatic Discharge (ESD) performance and can withstand high voltages on the LIN bus. In order to minimize current consumption, the UJA1018 supports a Sleep mode in which the LIN transceiver and the voltage regulator are powered down while still having wake-up capability via the LIN bus.

Three high-side switches are integrated into the UJA1018. They are intended to support a variety of applications, including LED control for ambient lighting.

The UJA1018 comes in a 3.5 mm × 5.5 mm HVSON16 package to help minimize board size. The exposed center pad in the HVSON16 package provides enhanced thermal performance.

2. Features and benefits

2.1 General

- LIN 2.0/2.1/2.2 compliant
- SAE J2602 compliant
- Downward compatible with LIN 1.3
- Internal LIN slave termination resistor
- Slave Node Position Detection (SNPD) supported by LIN bus switch
- Voltage regulator offering 5 V, 70 mA capability
- ±2 % voltage regulator accuracy over specified temperature and supply ranges
- Voltage regulator output undervoltage detection with reset output
- Voltage regulator short-circuit proof to ground
- Voltage regulator stable with ceramic, tantalum and aluminum electrolyte capacitors
- 3 high-side switches delivering up to 30 mA (e.g. to provide complete control over color blending and brightness in LEDs)
- Robust ESD performance; 8 kV according to IEC61000-4-2 for pins LIN and BAT
- Pins LIN and BAT protected against transients in the automotive environment (ISO 7637)
- Very low LIN bus leakage current of <2 μA when battery not connected
- LIN pin short-circuit proof to battery and ground

- Transmit data (TXD) dominant time-out function
- Thermally protected
- Very low ElectroMagnetic Emissions (EME)
- High ElectroMagnetic Immunity (EMI)
- Typical Standby mode current of 47 μA
- Typical Sleep mode current of 14 μA
- LIN bus wake-up function
- K-line compatible
- Leadless HVSON16 package with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UJA1018TK	HVSON16	plastic thermal enhanced very thin small outline package; no leads; 16 terminals; body 3.5 × 5.5 × 0.85 mm	SOT1308-1

4. Marking

Table 2. Marking codes

Type number	Marking code
UJA1018TK	UJA1018

5. Block diagram

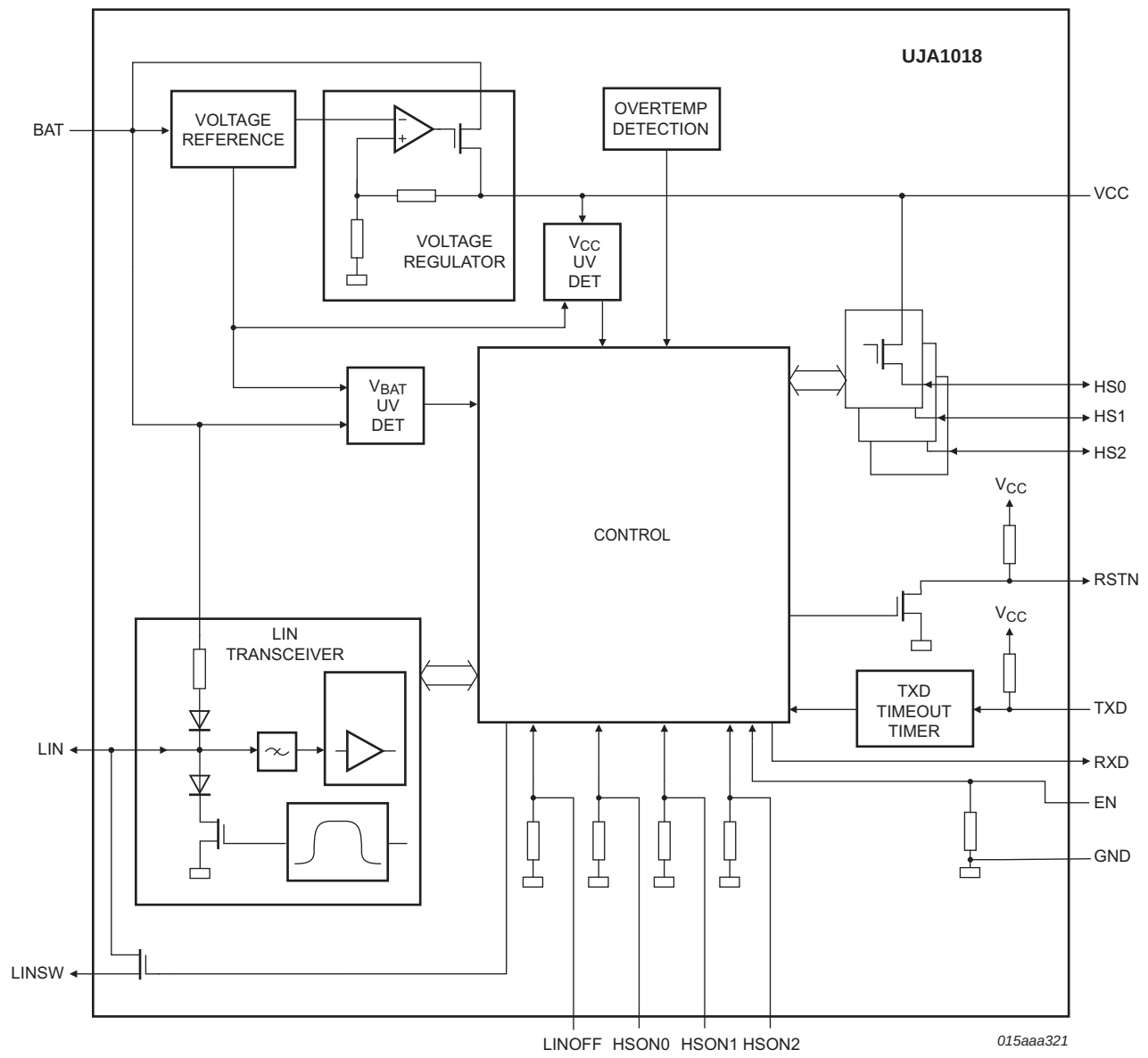


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

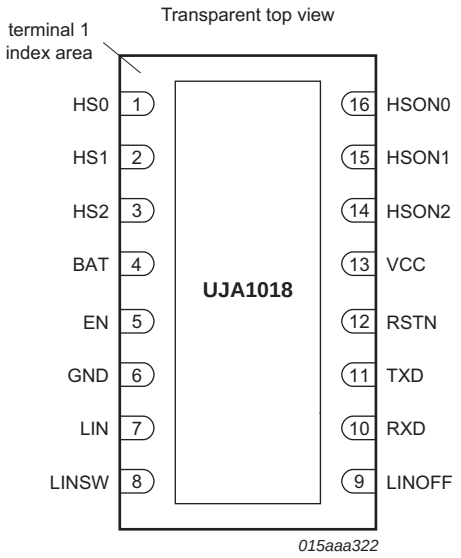


Fig 2. Pin configuration diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
HS0	1	high-side switch output 0
HS1	2	high-side switch output 1
HS2	3	high-side switch output 2
BAT	4	battery supply for UJA1018
EN	5	enable input
GND	6[1]	ground
LIN	7	LIN bus line
LINSW	8	LIN switch
LINOFF	9	LIN switch control input
RXD	10	LIN receive data output
TXD	11	LIN transmit data input
RSTN	12	reset output (active LOW)
VCC	13	voltage regulator output
HSON2	14	high-side switch input 2
HSON1	15	high-side switch input 1
HSON0	16	high-side switch input 0

[1] For enhanced thermal and electrical performance, the exposed center pad of the HVSON16 package should be soldered to board ground (and not to any other voltage level).

7. Functional description

The UJA1018 combines the functionality of a LIN transceiver and a voltage regulator in a single chip and supports wake-up by bus activity. The voltage regulator is designed to power the Electronic Control Unit's (ECU) microcontroller and its peripherals.

The LIN transceiver is the interface between the LIN master/slave protocol controller and the physical bus in a LIN network. According to the Open System Interconnect (OSI) model, these modules make up the LIN physical layer.

The LIN transceiver is optimized for, but not limited to, automotive applications with a transmission speed of 20 kBd (the maximum specified in the LIN standard) and excellent ElectroMagnetic Compatibility (EMC) performance.

The UJA1018 comes with three integrated high-side switches for use in applications such as LED ambient lighting. The switches are designed to drive up to 30 mA.

7.1 Slave Node Position Detection (SNPD)

The UJA1018 supports Slave Node Position Detection (SNPD). The LIN switch method (LSM) is used to detect the position of LSM slave nodes in a daisy chain LIN network. Unique addresses are assigned to individual nodes at start-up based on their position on the bus, allowing a number of functionally identical modules to be included in a network. LSM slave nodes can be combined with standard nodes in any order.

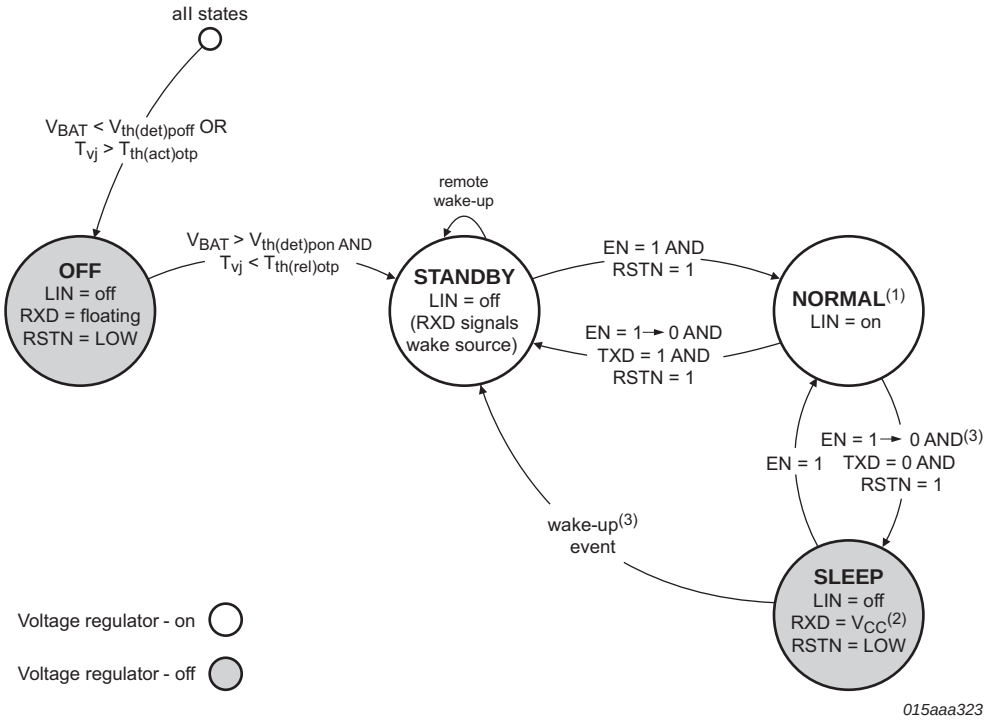
In order to detect the position of an LSM slave node in a network, a switch is connected between pins LIN and LINSW. When closed, this switch connects the LIN bus to the next node in the daisy chain, allowing the master to address each node in turn.

7.2 LIN 2.x/SAE J2602 compliant

The UJA1018 is fully LIN 2.0, LIN 2.1, LIN 2.2 and SAE J2602 compliant. Since the LIN physical layer is independent of higher OSI model layers (e.g. the LIN protocol), nodes containing a LIN 2.2-compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (i.e. LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0 and LIN 2.1).

7.3 Operating modes

The UJA1018 supports four operating modes: Normal, Standby, Sleep and Off. The operating modes, and the transitions between modes, are illustrated in Figure 3.



(1) In Normal mode, the LIN transmitter is enabled - but if EN and/or RSTN go LOW, the LIN transmitter will be disabled. Remote wake-up signaling will be activated.

(2) Until V_{CC} drops below 2 V.

(3) If a wake-up event and a go-to-sleep event occur simultaneously, the device will switch directly to Standby mode without initiating a reset.

Fig 3. State diagram

7.3.1 Off mode

The UJA1018 switches to Off mode from all other modes if the battery supply voltage drops below the power-off detection threshold ($V_{th(det)poff}$) or the junction temperature exceeds the overtemperature protection activation threshold ($T_{th(act)otp}$).

The voltage regulator and the LIN physical layer are disabled in Off mode, and pin RSTN is forced LOW.

7.3.2 Standby mode

Standby mode is a low-power mode that guarantees very low current consumption.

The UJA1018 switches from Off mode to Standby mode as soon as the battery supply voltage rises above the power-on detection threshold ($V_{BAT} > V_{th(det)pon}$), provided the junction temperature is below the overtemperature protection release threshold ($T_{vj} < T_{th(rel)otp}$).

The UJA1018 switches to Standby mode from Normal mode during the mode select window if TXD is HIGH and EN is LOW (see Section 7.3.5), provided RSTN is HIGH.

A remote wake-up event triggers a transition to Standby mode from Sleep mode. A remote wake-up event is signalled by a continuous LOW level on pin RXD.

In Standby mode, the voltage regulator is on, the LIN physical layer is disabled and remote wake-up detection is active. The wake-up source is indicated by the level on RXD (LOW indicates a remote wake-up).

7.3.3 Normal mode

If the EN pin is pulled HIGH while the UJA1018 is in Standby mode (with RSTN = 1) or Sleep mode, the device enters Normal mode. The LIN physical layer and the voltage regulator are enabled in Normal mode.

7.3.3.1 The LIN transceiver in Normal mode

The LIN transceiver is activated when the UJA1018 enters Normal mode.

In Normal mode, the transceiver can transmit and receive data via the LIN bus. The receiver detects data streams on the LIN pin and transfers them to the microcontroller via pin RXD. LIN recessive is represented by a HIGH level on RXD, LIN dominant by a LOW level.

The transmitter converts data streams received from the protocol controller into bus signals with optimized slew rate and wave shaping to minimize EME. A LOW level on the TXD input is converted to a LIN dominant level while a HIGH level is converted to a LIN recessive level.

7.3.4 Sleep mode

Sleep mode features extremely low power consumption.

The UJA1018 switches to Sleep mode from Normal mode during the mode select window if TXD and EN are both LOW (see Section 7.3.5), provided RSTN is HIGH.

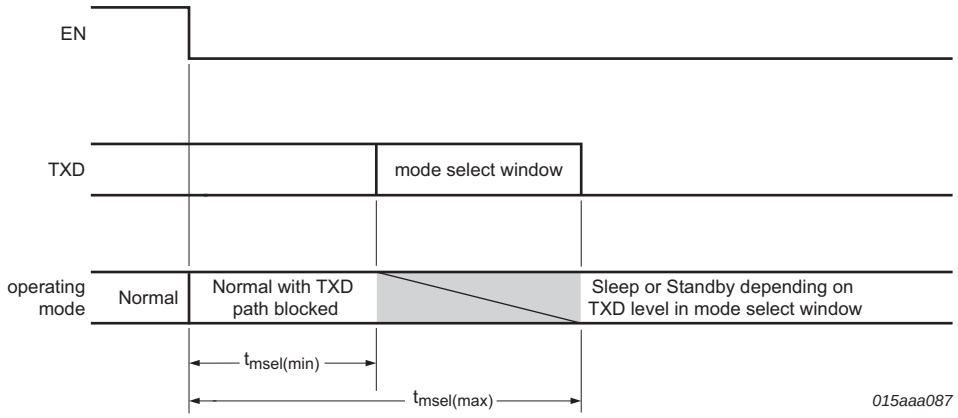
The voltage regulator and the LIN physical layer are disabled in Sleep mode. Pin RSTN is forced LOW. Remote wake-up detection is active.

7.3.5 Transition from Normal to Sleep or Standby mode

When EN is driven LOW in Normal mode, the UJA1018 disables the transmit path. The mode select window opens $t_{msel(min)}$ after EN goes LOW. It closes $t_{msel(max)}$ after EN goes LOW (see Figure 4).

The TXD pin is sampled in the mode select window. A transition to Standby mode is triggered if TXD is HIGH, or to Sleep mode if TXD is LOW. TXD must remain HIGH or LOW, as appropriate, while the mode select window is open.

To avoid complicated timing in the application, EN and TXD can be pulled LOW at the same time without affecting the LIN bus. To ensure that the remote wake-up time ($t_{wake(dom)LIN}$) is not reset on a transition to Sleep mode, TXD should be pulled LOW at least $t_{d(EN-TXD)}$ after EN goes LOW. This functionality is guaranteed by design.



TXD is sampled during the mode select window. The UJA1018 switches to Standby (TXD HIGH) or Sleep (TXD LOW) mode after sampling.

Fig 4. Transition from Normal to Sleep/Standby mode

7.4 Power supplies

7.4.1 Battery (pin BAT)

The UJA1018 contains a single supply pin, BAT. An external diode is needed in series to protect the device against negative voltages. The operating range is from 5.5 V to 18 V. The UJA1018 can handle voltages up to 40 V (max). If the voltage on pin BAT falls below $V_{th(det)poff}$, the UJA1018 switches to Off mode, shutting down the internal logic and the voltage regulator and disabling the LIN transmitter. The UJA1018 exits Off mode as soon as the voltage rises above $V_{th(det)pon}$, provided the junction temperature is below $T_{th(rel)otp}$.

7.4.2 Voltage regulator (pin VCC)

The UJA1018 contains a voltage regulator, supplied via pin BAT, that delivers up to 70 mA. It is designed to supply the microcontroller and its periphery via pin VCC.

7.4.3 Reset (pin RSTN)

The output voltage on pin VCC is monitored continuously and a system reset signal is generated (pin RSTN goes LOW) if an undervoltage event is detected ($V_{CC} < V_{uvd}$ for $t_{det(uv)(VCC)}$). Pin RSTN will go HIGH again once the voltage on VCC exceeds the undervoltage recovery threshold (V_{uvr}) for t_{rst}.

7.5 LIN transceiver

The transceiver is the interface between a LIN master/slave protocol controller and the physical bus in a LIN network. It is primarily intended for in-vehicle subnetworks using baud rates from 2.4 kBd up to 20 kBd and is LIN 2.0/LIN 2.1/LIN 2.2/SAE J2602 compliant.

7.6 Remote wake-up

A remote wake-up is triggered by a falling edge on pin LIN, followed by LIN remaining LOW for at least $t_{wake(dom)LIN}$, followed by a rising edge on pin LIN (see Figure 5).

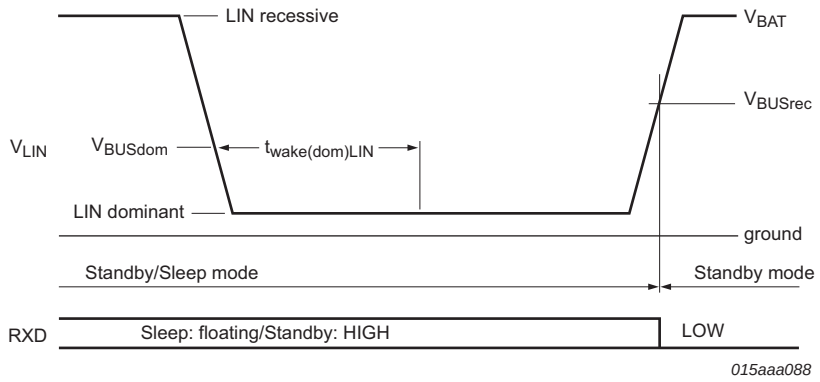


Fig 5. Remote wake-up behavior

The remote wake-up request is communicated to the microcontroller in Standby mode by a continuous LOW level on pin RXD.

Note that $t_{wake(dom)LIN}$ is measured in Sleep and Standby modes, and in Normal mode if TXD is HIGH.

7.7 LIN switch

The LIN switch is controlled via input pin LINOFF. When LINOFF is LOW, the switch is closed and the LIN bus is connected to the output pin LINSW. If pin LINOFF is HIGH, the LIN bus transmission from LIN to LINSW is interrupted.

An internal pull-down resistor ensures that a defined signal level is always present on pin LINOFF.

The input level on pin LINOFF is ignored when pin RSTN is LOW or overtemperature protection has been activated. The internal default input state is LOW (transmission activated).

7.8 High-side switches

The high-side switches on pins HS0, HS1 and HS2 are controlled via input pins HSON0, HSON1 and HSON2, respectively. A high-side switch is ON when the corresponding control input pin is HIGH.

Internal pull-down resistors on HSON0, HSON1 and HSON2 ensure that a defined level is always present on these pins when the switch is off.

The input levels on pins HSON0, HSON1 and HSON2 are ignored when RSTN is LOW. The internal default input state is LOW.

7.9 Fail-safe features

7.9.1 General fail-safe features

The following general fail-safe features have been implemented:

- An internal pull-up towards V_{CC} on pin TXD guarantees a recessive bus level if the pin is left floating by a bad solder joint or a floating microcontroller port pin.

- The current in the transmitter output stage is limited to protect the transmitter against short circuits to pin BAT.
- A loss of power (pins BAT and GND) has no impact on the microcontroller; no reverse currents flow from the bus.
- The LIN transmitter is automatically disabled when either EN or RSTN is LOW.
- After a transition to Normal mode, the LIN transmitter will only be activated when pin TXD is HIGH (LIN recessive).

7.9.2 TXD dominant time-out function

If a hardware or software application failure causes TXD to be held permanently LOW, a TXD dominant time-out timer circuit is activated. This function prevents the bus line being driven to a permanent dominant state (blocking all network communications).

The timer is triggered by a negative edge on the TXD pin. If TXD remains LOW for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, driving the bus line to a recessive state. The timer is reset by a positive edge on TXD.

7.9.3 Temperature protection

The temperature of the IC is monitored in Normal, Standby and Off modes. If the temperature is too high ($T_{vj} > T_{th(act)otp}$), the UJA1018 switches to Off mode (if in Standby or Normal modes). The voltage regulator and the LIN transmitter are switched off and the RSTN pin is driven LOW.

When the temperature falls below the overtemperature protection release threshold ($T_{vj} < T_{th(rel)otp}$), the UJA1018 switches to Standby mode.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	battery supply voltage	DC; continuous		−0.3	+40	V
V_x	voltage on pin x	DC value				
		pin VCC		−0.3	+7	V
		pins TXD, RXD, RSTN, EN, HSONx, HSx and LINOFF		−0.3	V_{CC} + 0.3	V
		pins LIN and LINSW with respect to GND; $V_{LIN} = V_{LINSW}$		−40	+40	V
		pins LINSW with respect to LIN; $V_{LINOFF} = V_{CC}$		−0.3	+18	V
$I_{(LIN-LINSW)}$	current from pin LIN to pin LINSW			−200	+200	mA
V_{ESD}	electrostatic discharge voltage	HBM	[1]			
		pins LIN, LINSW and BAT	[2]	−8	+8	kV
		any other pin		−2	+2	kV
		IEC 61000-4-2	[3]			
		pins LIN, LINSW and BAT		−8	+8	kV
		MM	[4]			
		any pin		−250	+250	V
		CDM	[5]			
		corner pins		−750	+750	V
		any other pin		−500	+500	V
V_{trt}	transient voltage	on pin BAT via reverse polarity diode/capacitor; on pins LIN and LINSW via 1 nF coupling capacitor	[6]	−150	+100	V
T_{vj}	virtual junction temperature		[7]	−40	+150	°C
T_{stg}	storage temperature			−55	+150	°C

[1] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[2] VCC and BAT connected to GND, emulating application circuit.

[3] ESD performance of pins LIN and BAT according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house.

[4] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μH, 10 Ω).

[5] Charged Device Model (CDM): according to AEC-Q100-011 (field induced charge; 4 pF).

[6] Verified by an external test house to ensure that the pins can withstand ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.

[7] Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_j = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVSON16; single-layer board	[1]	80	K/W
		HVSON16; four-layer board	[2]	40	K/W

[1] According to JEDEC JESD51-2 and JESD51-3 at natural convection on 1s board.

[2] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer.

10. Static characteristics

Table 6. Static characteristics

V_{BAT} = 5.5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply; pin BAT							
I_{BAT}	battery supply current	Standby mode; $V_{LIN} = V_{BAT}$		-	47	61	μA
		Sleep mode; $V_{LIN} = V_{BAT}$		-	14	20	μA
		Normal mode; bus recessive; $V_{LIN} = V_{BAT}$; $V_{RXD} = V_{CC}$; V_{RSTN} = HIGH		-	850	1800	μA
		Normal mode; bus dominant; V_{BAT} = 12 V; V_{TXD} = 0 V; V_{RSTN} = HIGH		-	2.0	4.5	mA
$V_{th(det)pon}$	power-on detection threshold voltage	V_{BAT} = 2 V to 28 V		-	-	5.25	V
$V_{th(det)poff}$	power-off detection threshold voltage			3	-	4.2	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage			50	-	-	mV
Supply; pin VCC							
V_{CC}	supply voltage	$V_{CC(nom)}$ = 5 V; I_{CC} = −70 mA to 0 mA		4.9	5	5.1	V
I_{Olim}	output current limit	V_{CC} = 0 V to 5.5 V		−250	-	−70	mA
V_{uvd}	undervoltage detection voltage	$V_{CC(nom)}$ = 5 V		4.5	-	4.75	V
V_{uvr}	undervoltage recovery voltage	$V_{CC(nom)}$ = 5 V		4.6	-	4.9	V
$R_{(BAT-VCC)}$	resistance between pin BAT and pin VCC	$V_{CC(nom)}$ = 5 V; V_{BAT} = 4.5 V to 5.5 V; I_{CC} = −70 mA to −5 mA; regulator in saturation	[1] [2]				
		T_{vj} = 85 °C		-	-	7	Ω
		T_{vj} = 150 °C		-	-	9	Ω
C_o	output capacitance	equivalent series resistance < 5 Ω	[2]	1.8	10	-	μF
LIN transmit data input; pin TXD							
$V_{th(sw)}$	switching threshold voltage	V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	-	0.7 × V_{CC}	V
$V_{hys(i)}$	input hysteresis voltage	V_{CC} = 4.5 V to 5.5 V		200	-	-	mV

Table 6. Static characteristics *...continued*

V_{BAT} = 5.5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pu}	pull-up resistance		5	12	25	kΩ
LIN receive data output; pin RXD						
I_{OH}	HIGH-level output current	Normal mode; $V_{LIN} = V_{BAT}$; $V_{RXD} = V_{CC} - 0.4$ V	-	-	−0.4	mA
I_{OL}	LOW-level output current	Normal mode; V_{LIN} = GND; V_{RXD} = 0.4 V	0.4	-	-	mA
Enable input; pin EN						
$V_{th(sw)}$	switching threshold voltage		0.8	-	2	V
R_{pd}	pull-down resistance		50	130	400	kΩ
High-side switch inputs; pins HSON0, HSON1 and HSON2						
$V_{th(sw)}$	switching threshold voltage	V_{CC} = 4.5 V to 5.5 V	0.3 × V_{CC}	-	0.7 × V_{CC}	V
$V_{hys(i)}$	input hysteresis voltage	V_{CC} = 4.5 V to 5.5 V	200	-	-	mV
R_{pd}	pull-down resistance		50	130	400	kΩ
LIN switch control input; pin LINOFF						
$V_{th(sw)}$	switching threshold voltage	V_{CC} = 4.5 V to 5.5 V	0.3 × V_{CC}	-	0.7 × V_{CC}	V
$V_{hys(i)}$	input hysteresis voltage	V_{CC} = 4.5 V to 5.5 V	200	-	-	mV
R_{pd}	pull-down resistance		50	130	400	kΩ
Reset output; pin RSTN						
R_{pu}	pull-up resistance	$V_{RSTN} = V_{CC} - 0.4$ V; V_{CC} = 4.5 V to 5.5 V	3	-	12	kΩ
I_{OL}	LOW-level output current	V_{RSTN} = 0.4 V; V_{CC} = 4.5 V to 5.5 V; −40 °C < T_{vj} < 195 °C	3.2	-	40	mA
V_{OL}	LOW-level output voltage	V_{CC} = 2.5 V to 5.5 V; −40 °C < T_{vj} < 195 °C	0	-	0.5	V
V_{OH}	HIGH-level output voltage	−40 °C < T_{vj} < 195 °C	0.8 × V_{CC}	-	V_{CC} + 0.3	V
High-side switch outputs; pins HS0, HS1 and HS2						
R_{on}	on-state resistance	from pin HSx to pin VCC; $V_{HSONx} = V_{CC}$; I_{HSx} = −30 mA	-	4	8	Ω
I_L	leakage current	V_{HSONx} = 0 V; V_{HSx} = 0 V	-	-	1	μA
LIN switch; pin LINSW						
R_{on}	on-state resistance	from pin LIN to pin LINSW; V_{LIN} = 1 V; V_{LINOFF} = 0 V; V_{BAT} = 4.5 V to 18 V	-	1	2	Ω
I_L	leakage current	$V_{LINOFF} = V_{CC}$; $V_{LINSW} = V_{BAT}$; measured after recessive-to-dominant transition	-	-	1	μA
LIN bus line; pin LIN						
I_{BUS_LIM}	current limitation for driver dominant state	$V_{BAT} = V_{LIN}$ = 18 V; V_{TXD} = 0 V	40	-	100	mA
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	V_{LIN} = 18 V; V_{BAT} = 5.5 V; $V_{TXD} = V_{CC}$	-	-	2	μA

Table 6. Static characteristics *...continued*

V_{BAT} = 5.5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	Normal mode; $V_{TXD} = V_{CC}$; V_{LIN} = 0 V; V_{BAT} = 12 V		−600	-	-	µA
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	V_{BAT} = 18 V; V_{LIN} = 0 V		−750	-	+10	µA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 0 V; V_{LIN} = 18 V		-	-	2	µA
V_{BUSrec}	receiver recessive state			0.6 × V_{BAT}	-	-	V
V_{BUSdom}	receiver dominant state			-	-	0.4 × V_{BAT}	V
V_{BUS_CNT}	receiver center voltage	$V_{BUS\_CNT} = (V_{BUSdom} + V_{BUSrec}) / 2$		0.475 × V_{BAT}	0.5 × V_{BAT}	0.525 × V_{BAT}	V
V_{HYS}	receiver hysteresis voltage	$V_{HYS} = V_{BUSrec} - V_{BUSdom}$		0.05 × V_{BAT}	0.15 × V_{BAT}	0.175 × V_{BAT}	V
$V_{SerDiode}$	voltage drop at the serial diode	in pull-up path with R_{slave}; $I_{SerDiode}$ = 0.9 mA	[2]	0.4	-	1.0	V
C_{LIN}	capacitance on pin LIN	with respect to GND	[2]	-	-	39	pF
$V_{O(dom)}$	dominant output voltage	Normal mode; V_{TXD} = 0 V; V_{BAT} = 7 V		-	-	1.4	V
		Normal mode; V_{TXD} = 0 V; V_{BAT} = 18 V		-	-	2.0	V
R_{slave}	slave resistance	between pins LIN and BAT V_{LIN} = 0 V; V_{BAT} = 12 V		27	40	60	kΩ
Temperature protection							
$T_{th(act)otp}$	overtemperature protection activation threshold temperature			165	180	195	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature			126	138	150	°C

[1] See Figure 1.

[2] Not tested in production; guaranteed by design.

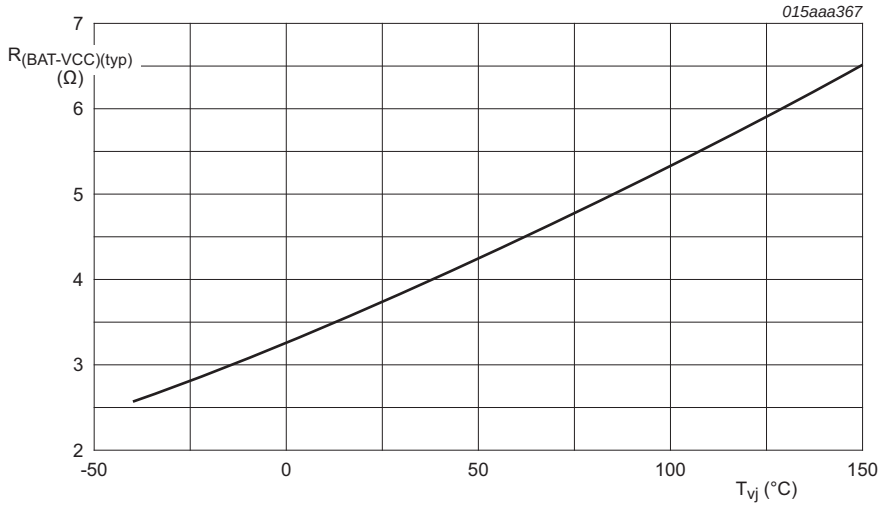


Fig 6. Graph of $R_{(BAT-VCC)(typ)}$ as a function of junction temperature (T_{vj})

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{BAT} = 5.5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Duty cycles							
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744V_{BAT}; $V_{th(dom)(max)}$ = 0.581V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7 V to 18 V	[2] [3][4]	0.396	-	-	
		$V_{th(rec)(max)}$ = 0.76V_{BAT}; $V_{th(dom)(max)}$ = 0.593V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.5 V to 7.0 V	[2] [3][4]	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.422V_{BAT}; $V_{th(dom)(min)}$ = 0.284V_{BAT}: t_{bit} = 50 µs; V_{BAT} = 7.6 V to 18 V	[3] [4][5]	-	-	0.581	
		$V_{th(rec)(min)}$ = 0.41V_{BAT}; $V_{th(dom)(min)}$ = 0.275V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 6.1 V to 7.6 V	[3] [4][5]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778V_{BAT}; $V_{th(dom)(max)}$ = 0.616V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7 V to 18 V	[2][3] [4]	0.417	-	-	
		$V_{th(rec)(max)}$ = 0.797V_{BAT}; $V_{th(dom)(max)}$ = 0.630V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5.5 V to 7 V	[2][3] [4]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389V_{BAT} $V_{th(dom)(min)}$ = 0.251V_{BAT} t_{bit} = 96 µs V_{BAT} = 7.6 V to 18 V	[3][4] [5]	-	-	0.590	
		$V_{th(rec)(min)}$ = 0.378V_{BAT}; $V_{th(dom)(min)}$ = 0.242V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 6.1 V to 7.6 V	[3][4] [5]	-	-	0.590	
Timing characteristics							
t_{rx_pd}	receiver propagation delay	rising and falling; C_{RXD} = 20 pF		-	-	6	µs
t_{rx_sym}	receiver propagation delay symmetry	C_{RXD} = 20 pF		−2	-	+2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	Sleep mode		30	80	150	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V		6	-	20	ms
t_{msel}	mode select time			3	-	20	µs
$t_{d(EN-TXD)}$	delay time from EN to TXD		[6]	0	-	1	µs
$t_{det(uv)(VCC)}$	undervoltage detection time on pin VCC	C_{RSTN} = 20 pF		1	-	15	µs
Reset output; pin RSTN							
t_{rst}	reset time			2	-	8	ms

Table 7. Dynamic characteristics *...continued*

V_{BAT} = 5.5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN switch; pin LINSW						
t_{on}	turn-on time	to switch closed	4	-	14	µs
t_{off}	turn-off time	to switch open	10	-	60	µs
High-side switch outputs; pins HS0, HS1 and HS2						
t_{on}	turn-on time	HSONx 0→1; C_L = 20 pF; R_L = 162 Ω; 90 % voltage	0.5	-	6	µs
t_{off}	turn-off time	HSONx 1→0; C_L = 20 pF; R_L = 162 Ω; 10 % voltage	0.5	-	6	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 7.

[3] Bus load conditions are: C_{BUS} = 1 nF and R_{BUS} = 1 kΩ; C_{BUS} = 6.8 nF and R_{BUS} = 660 Ω; C_{BUS} = 10 nF and R_{BUS} = 500 Ω.

[4] For V_{BAT} > 18 V, the LIN transmitter may be suppressed; the LIN transmitter output is recessive if TXD is HIGH.

[5] $\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 7.

[6] Not tested in production; guaranteed by design.

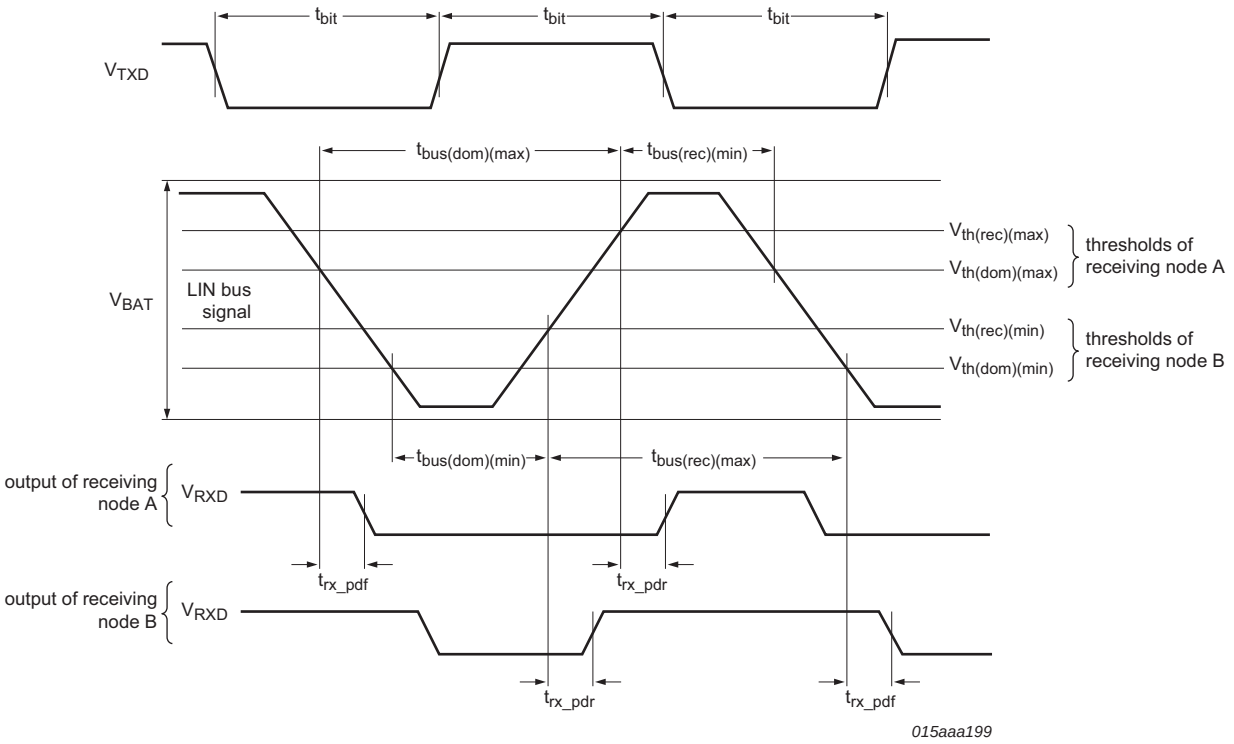


Fig 7. LIN transceiver timing diagram

12. Application information

12.1 Application diagram

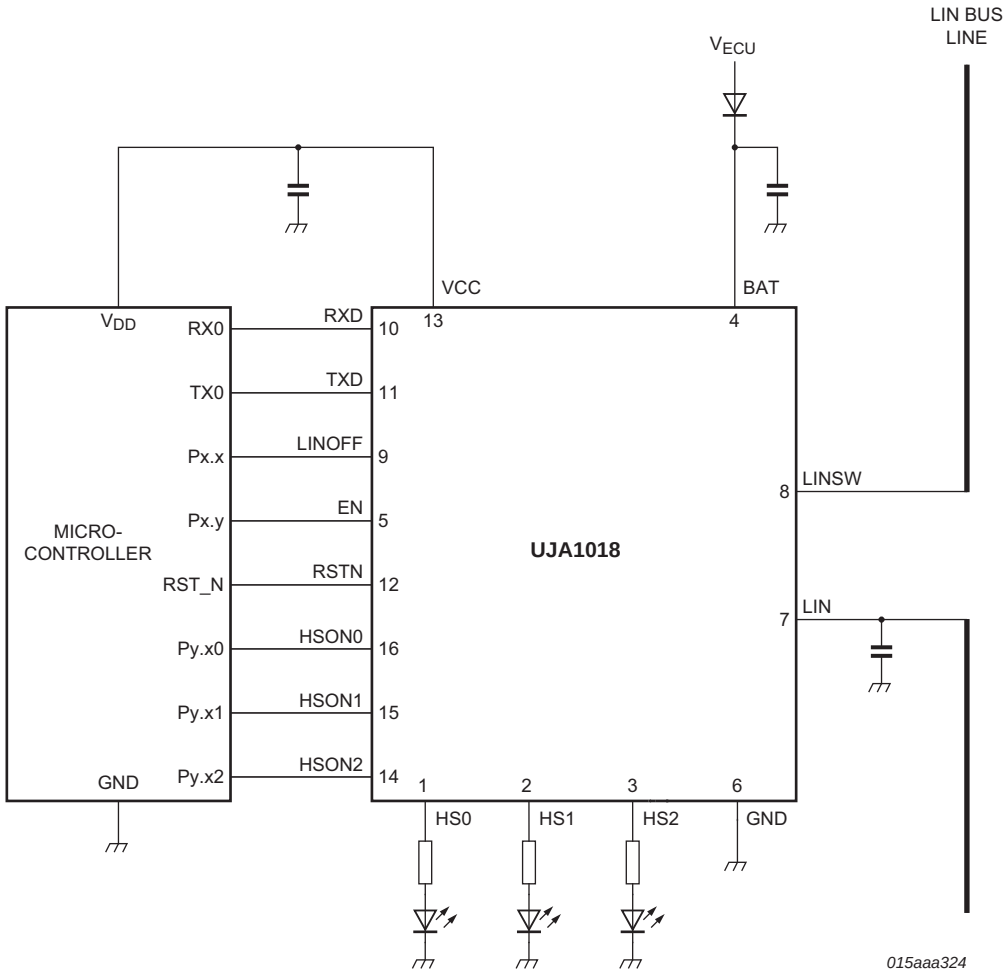


Fig 8. Application diagram

12.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

Table 8. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification

Pin	Test configuration	Value	Unit
LIN	no capacitor connected to LIN pin	±11	kV
	220 pF capacitor connected to LIN pin	±10	kV
LINSW	no capacitor connected to LINSW pin	> |11|	kV
	220 pF capacitor connected to LIN pin	> |10|	kV
V_{BAT}	100 nF capacitor connected to V_{BAT} pin	> |12|	kV

12.3 Hardware requirements for LIN interfaces in automotive applications

The UJA1018 satisfies the "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications", Version 1.2, March 2011.

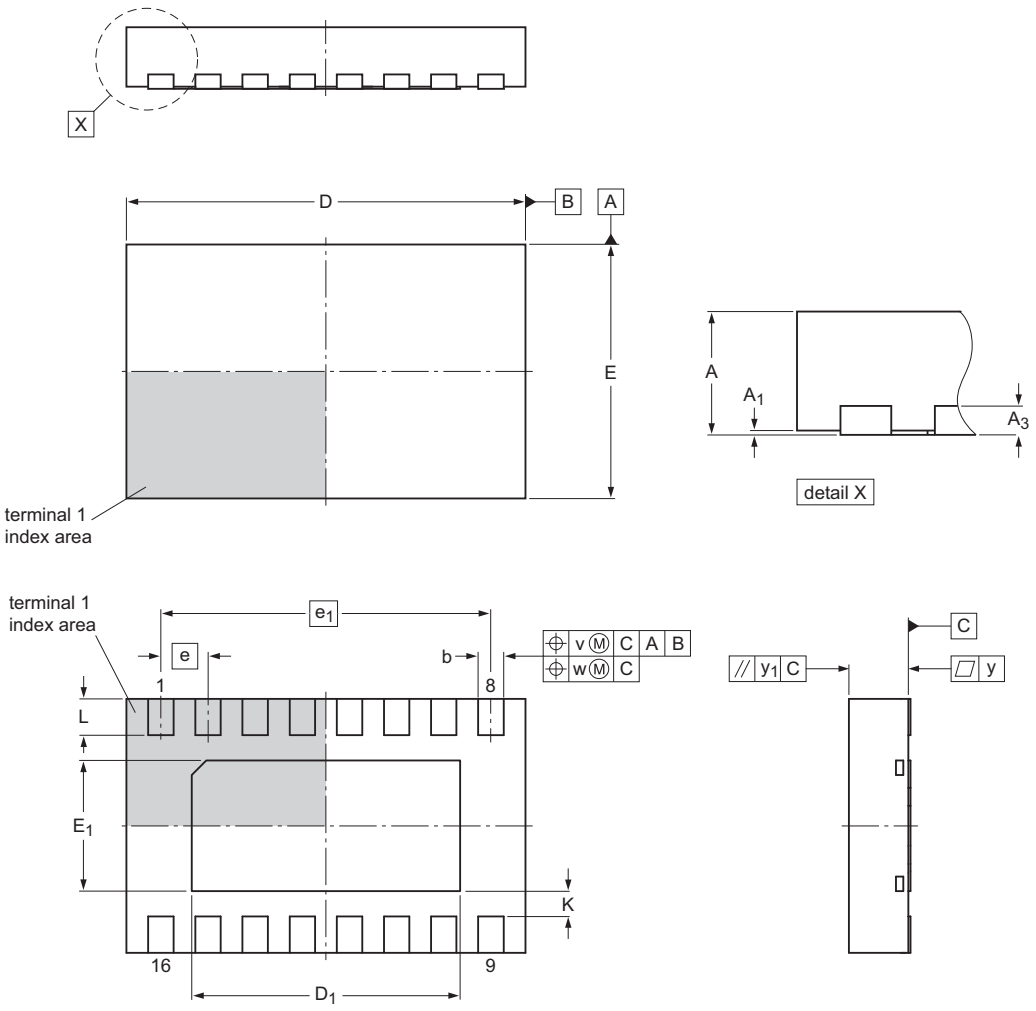
13. Test information

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14. Package outline

HVSON16: plastic thermal enhanced very thin small outline package; no leads; 16 terminals; body 3.5 x 5.5 x 0.85 mm **SOT1308-1**



0 3 6 mm

scale

Dimensions

Unit		A	A_1	A_3	b	D	D_1	E	E_1	e	e_1	k	L	v	w	y	y_1
	max	1.00	0.05		0.35	5.6	3.75	3.6	1.85				0.55				
mm	nom	0.85		0.2	0.32	5.5	3.70	3.5	1.80	0.65	4.55		0.50	0.1	0.05	0.05	0.1
	min	0.80	0.00		0.29	5.4	3.65	3.4	1.75			0.2	0.45				

sot1308-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1308-1		MO-229				~~11-07-04~~ 11-11-25

Fig 9. Package outline SOT1308 (HVSON16)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

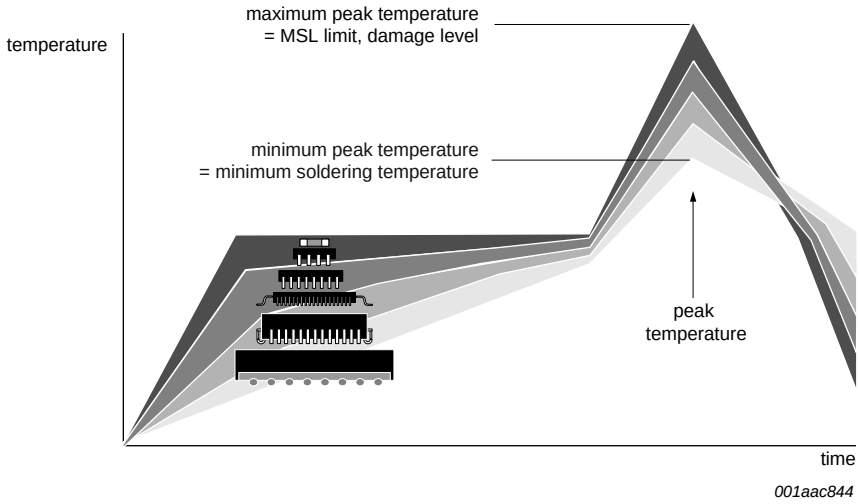
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application notes:

- *AN10365 'Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

18. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UJA1018 v.1	20120710	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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