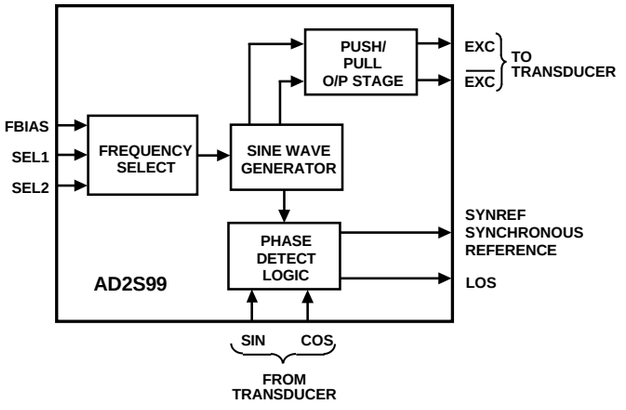
Programmable Oscillator

AD2S99

FEATURES
Programmable Sinusoidal Oscillator
Synthesized Synchronous Reference Output
Programmable Output Frequency Range: 2 kHz–20 kHz
"Loss-of-Signal" Indicator
20-Pin PLCC Package
Low Cost

APPLICATIONS
Excitation Source for:
Resolvers
Synchros
LVDTs
RVDTs
Pressure Transducers
Load Cells
AC Bridges

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S99 programmable sinusoidal oscillator provides sine wave excitation for resolvers and a wide variety of ac transducers. The AD2S99 also provides a synchronous reference output signal (3 V p-p square wave) that is phase locked to its SIN and COS inputs. In an application, the SIN and COS inputs are connected to the transducer's secondary windings.

The synchronous reference output compensates for temperature and cabling dependent phase shifts and eliminates the need for external preset phase compensation circuits. The synchronous reference output can be used as a zero crossing reference for resolver-to-digital converters such as Analog Devices' AD2S80A, AD2S82A, AD2S83 and AD2S90.

The AD2S99 is packaged in a 20-pin PLCC and operates over –40°C to +85°C.

PRODUCT HIGHLIGHTS

Dynamic Phase Compensation
The AD2S99 dynamically compensates for any phase variation in a transducer by phase locking its synchronous reference output to the transducer's secondary windings.

Programmable Excitation Frequency
The excitation frequency is easily programmed to 2 kHz, 5 kHz, 10 kHz, or 20 kHz by using the frequency select pins. Intermediate frequencies are available by adding an external resistor.

Signal Loss Detection
The AD2S99 has the ability to detect if both the transducer secondary winding connections become disconnected from its SIN and COS inputs. The "LOS" output pin pulls high when a signal loss is detected.

Integration
The AD2S99 integrates the transducer excitation, synchronous reference, and loss of signal detection functions into a small, cost effective package.

REV. B

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AD2S99–SPECIFICATIONS (V_S = ±4.75 V to ±5.25 V @ –40°C to +85°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
FREQUENCY OUTPUT RANGE					SEL1 SEL2
2 kHz		2000		Hz	V_{SS} V_{SS}
5 kHz		5000		Hz	V_{SS} GND
10 kHz		10000		Hz	GND V_{SS}
20 kHz		20000		Hz	GND GND
ACCURACY					
Frequency			±10	%	AP Grade @ +25°C
			±20	%	AP Grade –40°C to +85°C
			±5	%	BP Grade @ +25°C
			±10	%	BP Grade –40°C to +85°C
Amplitude		±3	±10	%	AP Grade @ +25°C
			±20	%	AP Grade –40°C to +85°C
		±3	±5	%	BP Grade @ +25°C
			±10	%	BP Grade –40°C to +85°C
Power Supply Rejection Ratio		0.002		V p-p/V	Output Variation as Function of Change in Power Supply Voltage
ANALOG OUTPUTS					
Amplitude					
EXC, $\overline{EXC}$		2		V rms	EXC to GND, $\overline{EXC}$ to GND
SYNREF		±3		V p-p	Square Wave
SYNREF OFFSET			±200	mV	
Current Drive Capability					
EXC, $\overline{EXC}$ V_S = ±5 V			8	mA rms	R_{LOAD} = 500 Ω $\overline{EXC}$ to EXC
					C_{LOAD} = 1000 pF
Capacitive Drive			1000	pF	
Total Harmonic Distortion					
EXC, $\overline{EXC}$		–25		dB	
ANALOG INPUTS SIN, COS					
Amplitude	1.8	2.0	2.2	V rms	
Phase Lock Range	–45		+45	Degrees	
Additional Phase Delay					
			±10	Degrees	AP Grade
			±10	Degrees	BP Grade
FREQUENCY SELECT INPUTS					
SEL1, SEL2[1]	V_{SS}		AGND	V dc	
LOS OUTPUT					
Output Low Voltage			0.7	V dc	I_{OL} = 400 μA
Output High Voltage		V_{DD}		V dc	50 kΩ Pull Up to V_{DD} (Open Drain Output)
SIN, COS LOS Threshold	0.5	0.6	0.8	V rms	
POWER SUPPLIES					
V_{DD}	+4.75		+5.25	V dc	
V_{SS}	–4.75		–5.25	V dc	
Quiescent Current I_{DD}, I_{SS}		±8	±15	mA	No Load
TEMPERATURE RANGE					
Operating	–40		+85	°C	
Storage	–65		+150	°C	

NOTES

[1]Frequency select pins SEL1 and SEL2 must be connected to appropriate voltage levels before power is applied.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} . . . . . +7 V
V_{SS} . . . . . –7 V
Operating Temperature . . . . . –40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Analog Input Voltages (SIN and COS) . . . . . V_{SS} – 0.3 V
. . . . . to V_{DD} + 0.3 V
Frequency Select (SEL1, SEL2) . . . . . V_{SS} – 0.4 V
. . . . . to AGND + 0.4 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_{DD} to V_{SS}) . . . . . ±4.75 V to ±5.25 V
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ±10%
Frequency Select (SEL1 and SEL2) . . . . . V_{SS} to AGND
Operating Temperature Range . . . . . –40°C to +85°C

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD2S99AP	–40°C to +85°C	P-20A
AD2S99BP	–40°C to +85°C	P-20A

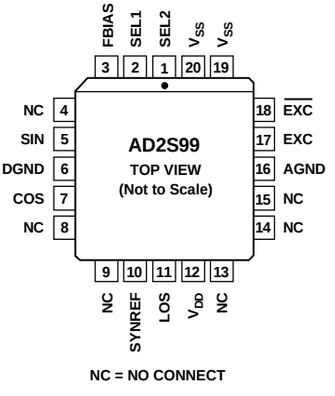
*P = PLCC.

PIN DESIGNATIONS

Pin No.	Mnemonic	Description
1	SEL2	Frequency Select 2
2	SEL1	Frequency Select 1
3	FBIAS	External Frequency Adjust Pin
5	SIN	Resolver Output SIN
6[1]	DGND	Digital Ground
7	COS	Resolver Output COS
10	SYNREF	Synthesized Reference Output
11	LOS	Indicates When Both the SIN and COS Are Below the Threshold.
12	V_{DD}	Positive Power Supply
16[1]	AGND	Analog Ground
17	EXC	Resolver Reference One
18	$\overline{EXC}$	Resolver Reference Two[3]
19[2]	V_{SS}	Negative Power Supply
20[2]	V_{SS}	Negative Power Supply

NOTES
[1]Pins 6 and 16 must be connected together.
[2]Pins 19 and 20 must be connected together.
[3]Resolver Reference two ($\overline{EXC}$) is 180° phase advanced with respect to Resolver Reference one (EXC).

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S99 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

CONNECTING THE AD2S99 OSCILLATOR

Refer to Figure 1. Positive supply voltage V_{DD} should be connected to Pin 12 and negative supply voltage V_{SS} should be connected to both Pins 19 and 20. *Reversal of these power supplies will destroy the device.* The appropriate voltage level for the power supplies is ±5 V dc ± 5%. Both V_{SS} Pins (19 and 20) must be connected together, and Digital Ground (Pin 6) must be connected to Analog Ground (Pin 16) locally at the AD2S99.

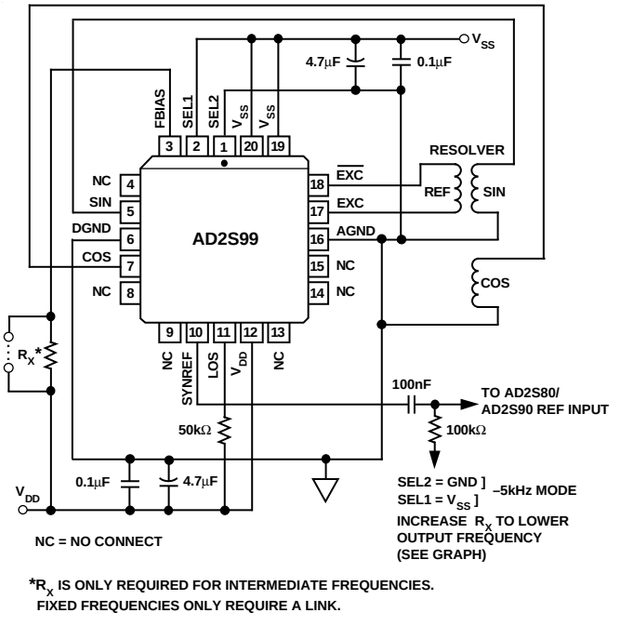


Figure 1. Typical Configuration

It is recommended that decoupling capacitors are connected in parallel between V_{DD} and Analog Ground and V_{SS} and Analog Ground in close proximity to the AD2S99. The recommended values for the decoupling capacitors are 100 nF (ceramic) and 4.7 µF (tantalum). When multiple AD2S99s are used, separate decoupling capacitors should be used for each AD2S99.

FREQUENCY ADJUSTMENT

The output frequency of the AD2S99 is programmable to four standard frequencies (2, 5, 10, or 20 kHz) using the SEL1 and SEL2 pins. The output can also be adjusted to provide intermediate frequencies by connecting a resistor from the FBIAS pin to the positive supply V_{DD}. The FBIAS pin is connected directly to V_{DD} during normal operation. A graph showing the typical added resistance values for various intermediate frequencies is provided in Figure 2. The procedure for obtaining an intermediate frequency is:

1. Set the output frequency via the SEL1, SEL2 pins to the frequency immediately above the required intermediate frequency.
2. Connect the frequency adjust pin FBIAS to V_{DD} via an external resistor.

For example: to obtain an output frequency of 8 kHz, set the nominal output frequency to 10 kHz by connecting SEL1 to GND and SEL2 to V_{SS}. Connect FBIAS to V_{DD} via a 6 kΩ resistor (refer to Figure 2).

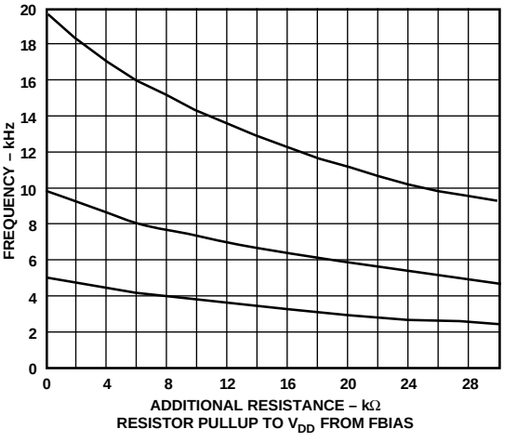


Figure 2. Typical Added Resistance Value

AD2S99 OSCILLATOR OUTPUT STAGE

The output of the AD2S99 oscillator consists of two sinusoidal signals, EXC, and $\overline{EXC}$. $\overline{EXC}$ is 180° phase advanced with respect to EXC. The excitation winding of a transducer should be connected across EXC (Pin 17) and $\overline{EXC}$ (Pin 18).

With low impedance transducers, it may be necessary to increase the output current drive of the AD2S99. In such an instance, an external buffer amplifier can be used to provide gain (as needed), and additional current drive for the excitation output (either EXC or $\overline{EXC}$) of the AD2S99, providing a single ended drive to the transducer. Refer to Figures 6, 7 and 8 for sample buffer configurations.

The amplitude modulated SIN and COS output signals from a resolver should be connected as feedback signals to the AD2S99. The SYNREF output compensates for any primary to secondary phase errors in the resolver. These errors can degrade the accuracy of a Resolver-to-Digital Converter (R/D Converter).

SIN, from the resolver, should be connected to the AD2S99 SIN input and COS should be connected to the AD2S99 COS input. The SIN Lo, COS Lo (resolver signal returns) should be connected to AGND and the R/D Converter as applicable.

The synthesized reference (SYNREF) from the AD2S99 should be connected to the reference input pin of the R/D Converter. The SYNREF signal is a square wave at the oscillator frequency of amplitude ±3 V p-p and is phase coherent with the SIN and COS inputs. If this signal is used to drive the reference input of the AD2S90 R/D Converter, a coupling capacitor and resistor to GND must be connected between the SYNREF output of the AD2S99 and the REF input of the R/D Converter (see Figure 3). Please read the appropriate R/D Converter data sheets for further clarification.

LOSS OF SIGNAL

During normal operation when both the SIN and COS signals on the resolver secondary windings are connected to the AD2S99, the LOS output pin of the AD2S99 (Pin 11) is at a Logic Lo (<0.7 V). If both the SIN and COS signals on the resolver secondary windings fall below the LOS threshold level of the AD2S99, the LOS pin of the AD2S99 will pull up to a Logic Hi (V_{DD}) level.

AD2S99/AD2S90 TYPICAL CONFIGURATION

Figure 3 shows a typical circuit configuration for the AD2S99 Oscillator and the AD2S90 Resolver-to-Digital Converter. The maximum level of the SIN and COS input signals to the AD2S90 should be 2 V rms ±10%. All the analog ground signals should be star connected to the AD2S90 AGND pin. If shielded twisted pair cables are used for the resolver signals, the shields should also be terminated at the AD2S90 AGND pin. The SYNREF output of the AD2S99 should be connected to the REF input pin of the AD2S90 via a 0.1 µF capacitor with a 100 kΩ resistor to GND. This is to block out any dc offset in the SYNREF signal. For more detailed information please refer to the AD2S90 data sheet.

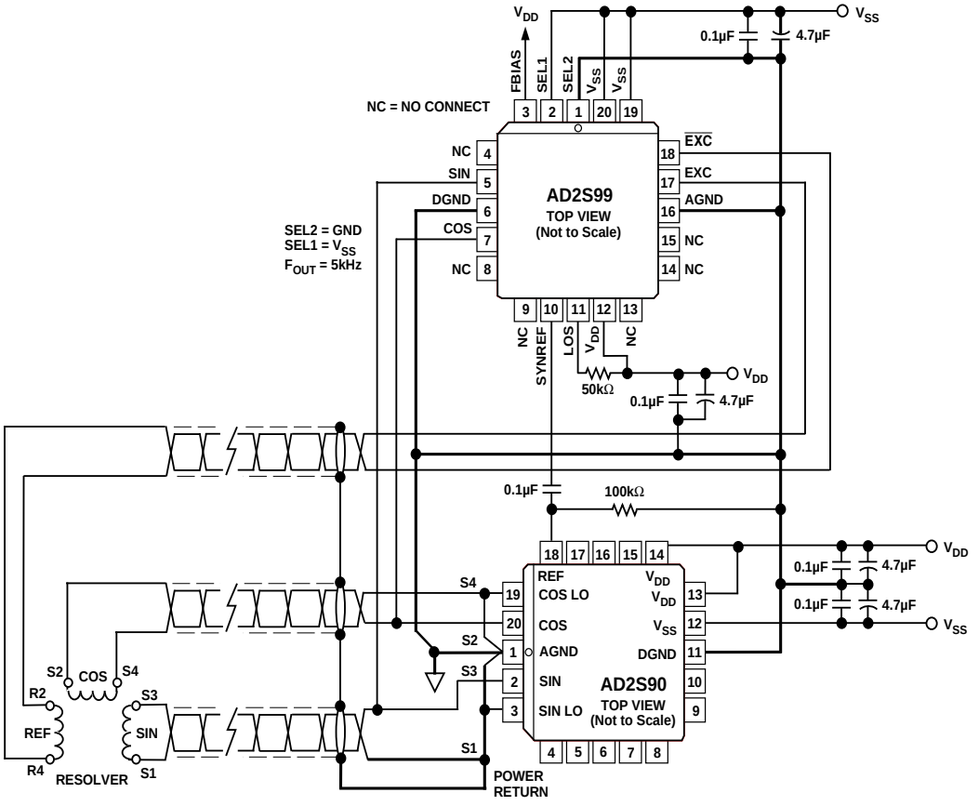


Figure 3. AD2S99 and AD2S90 Example Configuration

AD2S99/AD2S82A TYPICAL CONFIGURATION

Figure 4 shows a typical circuit configuration for the AD2S99 Oscillator and the AD2S82A Resolver-to-Digital Converter. The maximum level of the SIN and COS input signals to the AD2S82A should be 2 V rms ±10%. All the analog ground signals should be star connected to the AD2S82A AGND pin. If shielded twisted pair cables are used for the resolver signals, the shields should also be terminated at the AD2S82A AGND pin.

Coupling capacitor C3, and resistor to GND R3, between the SYNREF output of the AD2S99 and the REF input pin of the AD2S82A are optional. For additional information on selecting component values for the AD2S82A, please refer to the AD2S82A data sheet or the application note "Passive Component Selection and Dynamic Modeling for the AD2S80 Series Resolver-to-Digital Converters" (AN-266).

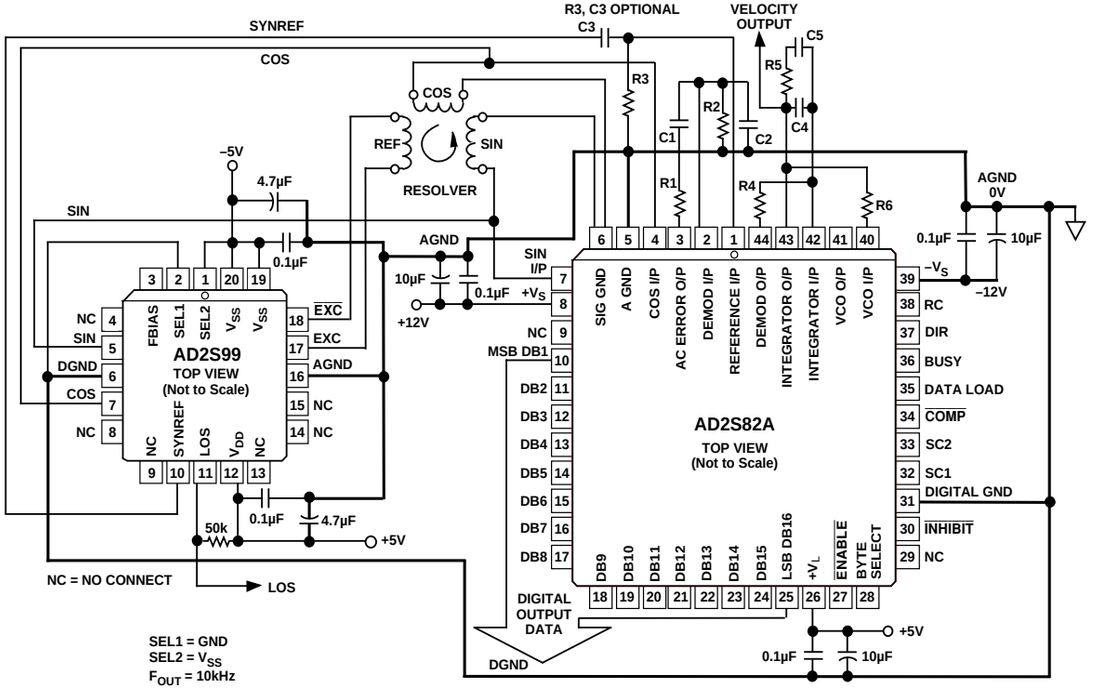


Figure 4. AD2S99 and AD2S82A Example Configuration

AD2S99/AD2S93 TYPICAL CONFIGURATION

Figure 5 shows a typical circuit configuration for the AD2S99 Oscillator and the AD2S93 LVDT-to-Digital Converter. The maximum level of the A and B transducer input signals to the AD2S93 should be 1 V rms ± 20%. All the analog ground signals should be star connected to the AD2S93 AGND pin. If shielded twisted pair cables are used for the LVDT signals, the shields should also be terminated at the AD2S93 AGND pin. The SYNREF output of the AD2S99 cannot be used as the REF input signal for the AD2S93. The zero crossing reference for the AD2S93 should be taken from the primary winding of the LVDT through a phase lead or lag network. The phase compensation network ensures that the REF input is phase coherent with the A and B input signals to the AD2S93.

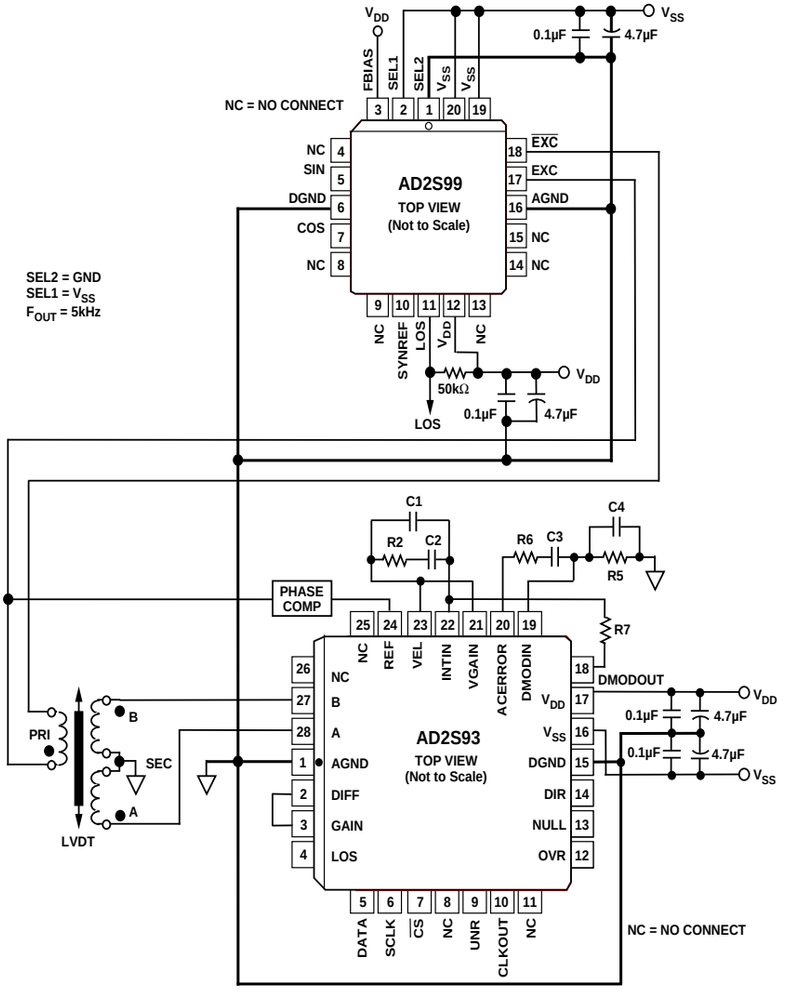


Figure 5. AD2S99 and AD2S93 Example Configuration

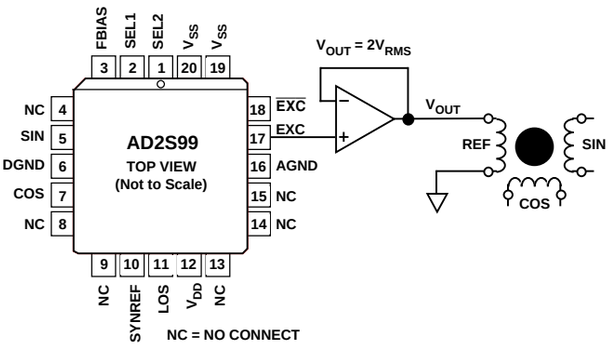


Figure 6. Sample Buffer Configuration

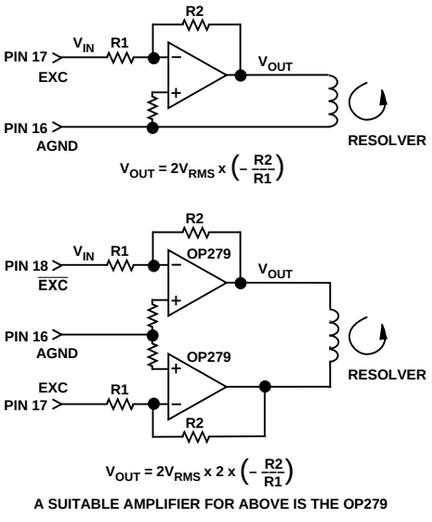


Figure 7. Sample Buffer Configurations

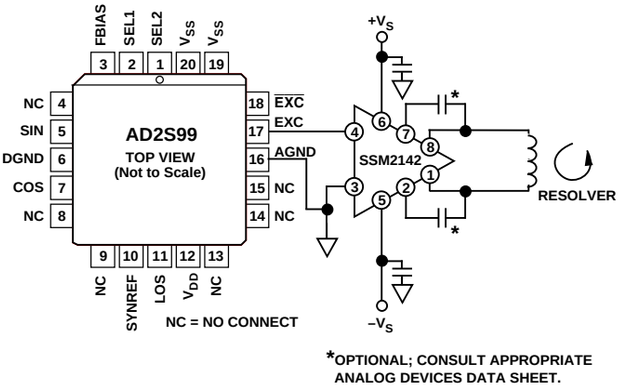
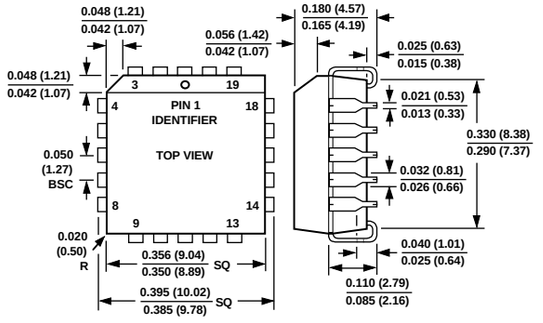


Figure 8. The SSM2142 as a Single Ended to Differential Driver

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

PLCC (P-20A)



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