HMC744LC3

v03.0514

14 GBPS, FAST RISE TIME 1:2 FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

Typical Applications

The HMC744LC3 is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 14 Gbps
- Clock Buffering up to 14 GHz

Features

Inputs Terminated Internally to 50 Ohms

Differential & Single-Ended Operation

Propagation Delay: 120 ps

Fast Rise and Fall Times: 22 / 20 ps

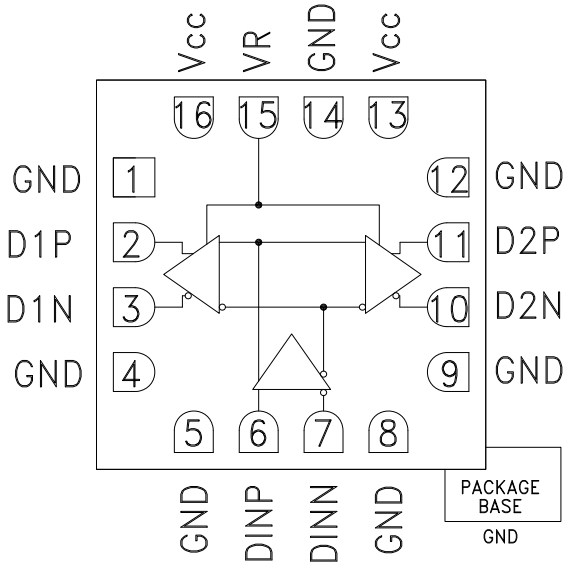
Programmable Differential
Output Voltage Swing: 600 - 1100 mV

Low Power Consumption: 287 mW typ.

Single Supply: +3.3 V

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC744LC3 is a 1:2 Fanout Buffer designed to support data transmission rates up to 14 Gbps, and clock frequencies as high as 14 GHz.

All differential inputs to the HMC744LC3 are CML and terminated on-chip with 50 Ohms to the positive supply, Vcc, and may be AC or DC coupled. The differential CML outputs are source terminated to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm Vcc-terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to ground. The HMC744LC3 also features an output level control pin, VR, which allows for loss compensation or signal-level optimization. the HMC744LC3 operates from a single 3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vcc = 3.3 V, VR = 3.3 V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		3.0	3.3	3.6	V
Power Supply Current			87		mA
Maximum Data Rate			14		Gbps
Maximum Clock Rate			14		GHz
Input Voltage Range		Vcc - 1.5		Vcc + 0.5	V
Input Differential Range		0.1		2	Vp-p
Input Return Loss	Frequency <14 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			3.29		V
Output Low Voltage			2.74		V
Output Rise / Fall Time	Single-Ended, 20% - 80%		22 / 20		ps

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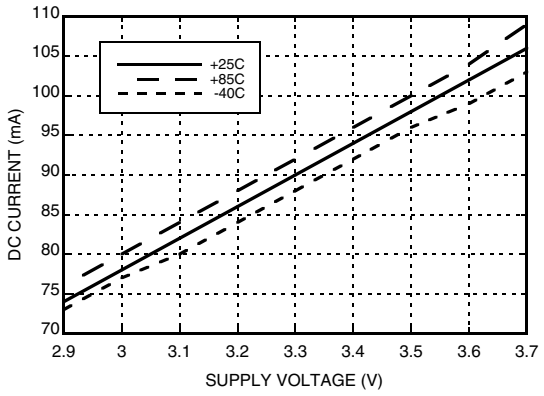
Electrical Specifications (continued)

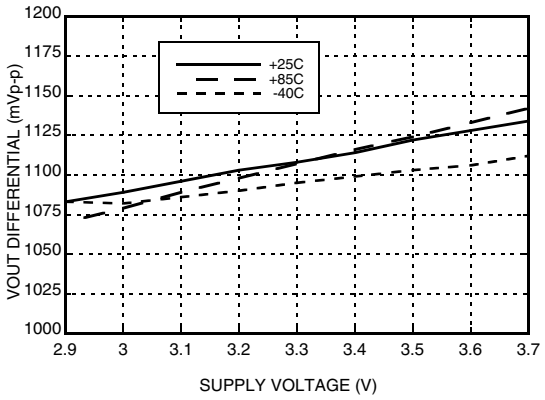
Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <13 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter J_R	rms			0.2	ps rms
Deterministic Jitter, J_D	δ - δ, 2^{15}-1 PRBS input [1]		2	6	ps
Propagation Delay, td			120		ps
D1 to D2 Data Skew, t_{SKEW}			<2		ps
VR Pin Current	VR = 3.3 V		2		mA
VR Pin Current	VR = 3.7 V			3.5	mA

[1] Deterministic jitter measured at 13 GHz with a 300 mVp-p, 2^{15}-1 PRBS input sequence.

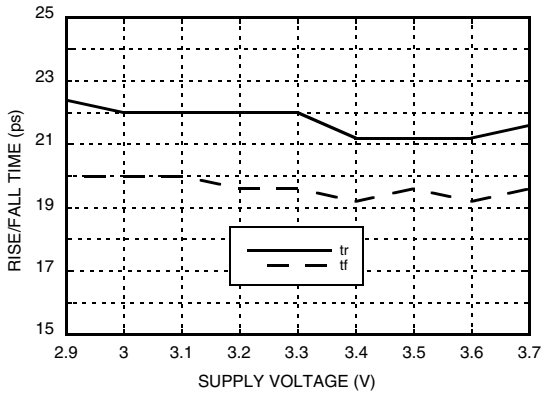
DC Current vs. Supply Voltage [1][2]



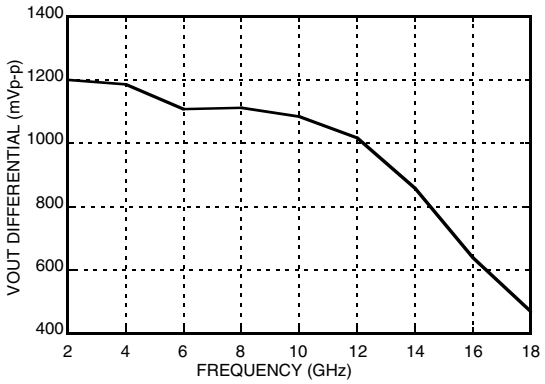
Output Differential Voltage vs. Supply Voltage [1][2]



Rise / Fall Time vs. Supply Voltage [1][2]



Output Differential Voltage vs. Frequency [1][3]



[1] VR = 3.3 V [2] Frequency = 13 GHz [3] Vcc = 3.3 V

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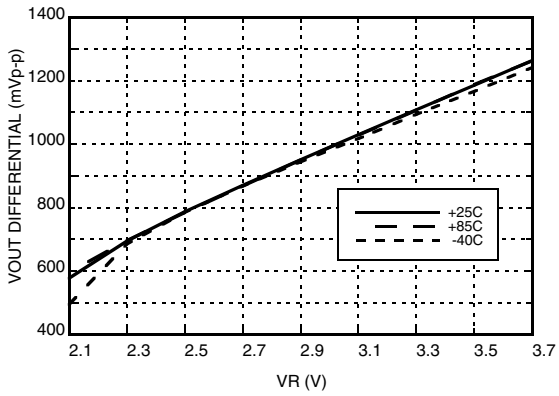
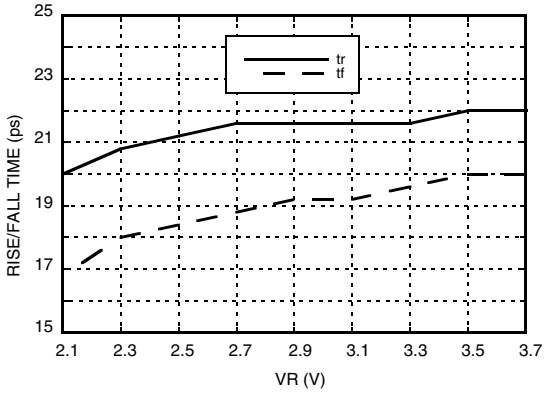
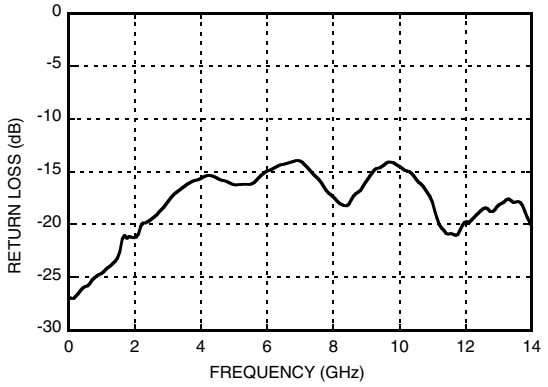
Output Differential Voltage vs. VR [1][2]



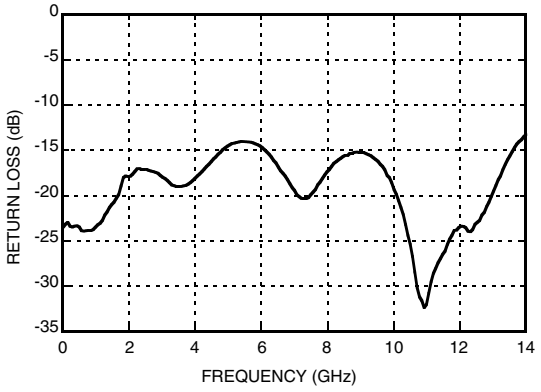
Rise / Fall Time vs. VR [1][2]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] Vcc = 3.3 V [2] Frequency = 13 GHz

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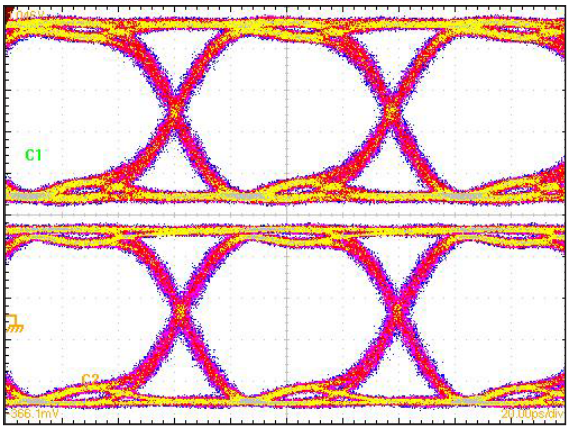
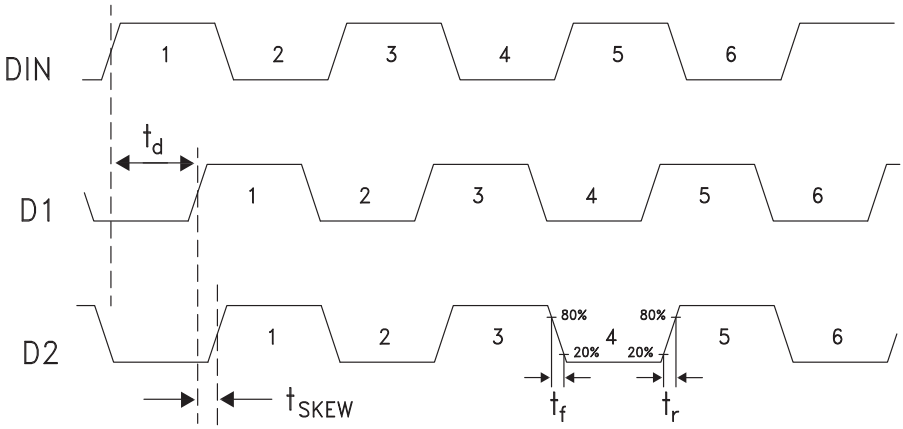
Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 13 Gbps PN code. Both output channels shown.
Device is AC coupled to scope

Timing Diagram



Truth Table

Input	Outputs	
DIN	D1	D2
L	L	L
H	H	H
Notes: DIN = DINP - DINN D1 = D1P - D1N D2 = D2P - D2N	H - Positive differential voltage L - Negative differential voltage	

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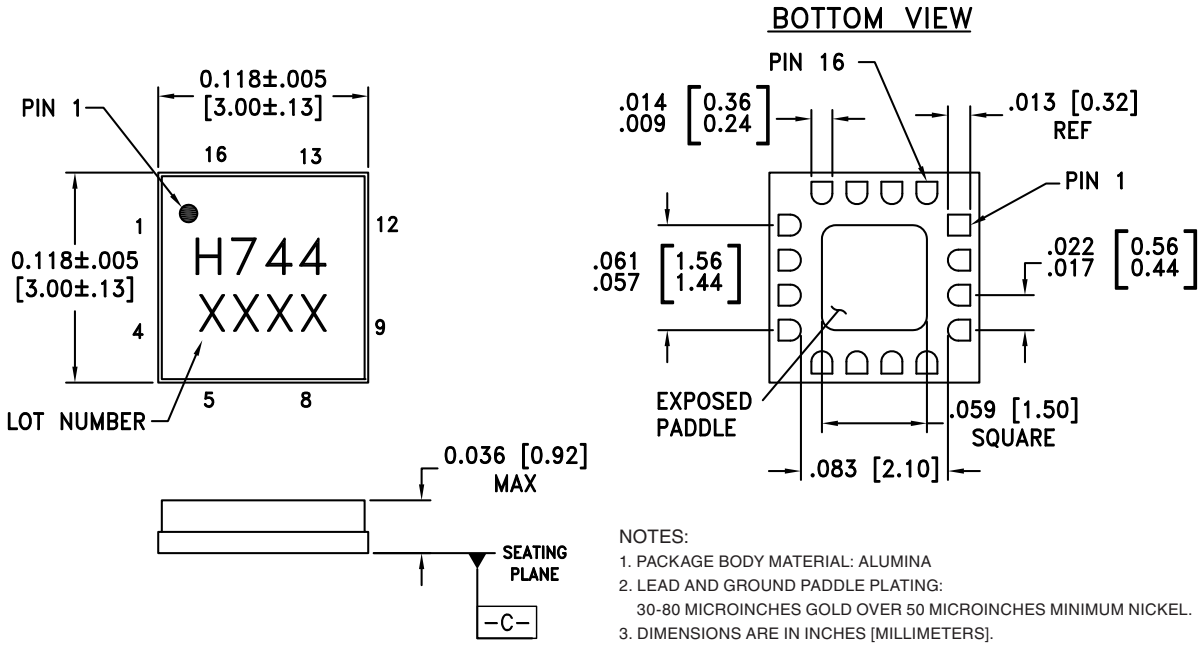
Absolute Maximum Ratings

Power Supply Voltage (Vcc)	Vcc -0.5 V to +3.75 V
Input Signals	Vcc -2.0 V to Vcc +0.5 V
Output Signals	Vcc -1.5 V to Vcc +0.5 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC744LC3	Alumina, White	Gold over Nickel	MSL3 [1]	H744 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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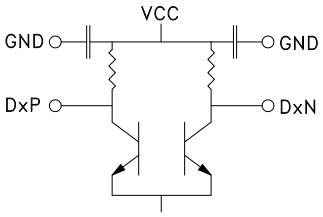
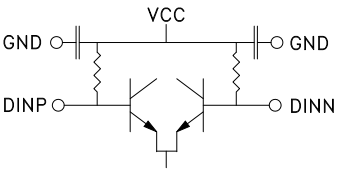
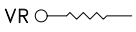
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3 10, 11	D1P, D1N D2N, D2P	Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply.	
6, 7	DINP, DINN	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
13, 16	Vcc	Positive Supply	
14, Package Base	GND	Supply Ground	
15	VR	Output level control. Output level may be adjusted by applying a voltage to VR per “Output Differential vs. VR” plot.	

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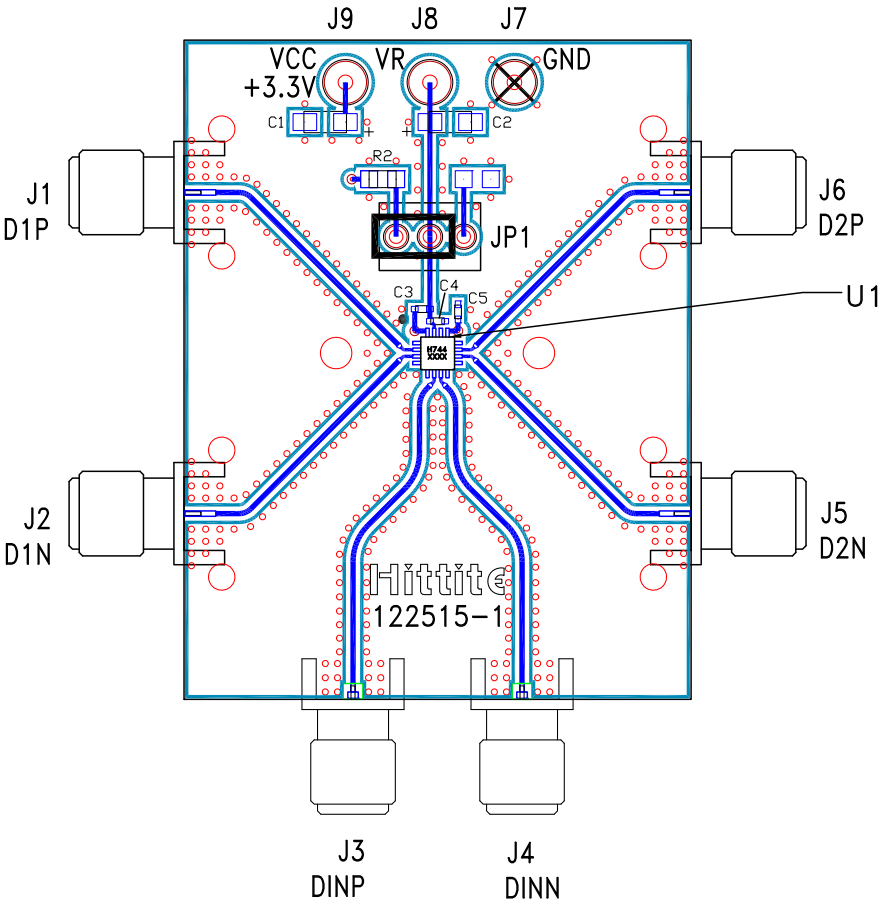
Evaluation PCB



List of Materials for Evaluation PCB 122517 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J9	DC Pin
JP1	Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF Capacitor, 0402 Pkg.
R2	10 Ohm Resistor, 0603 Pkg.
U1	HMC744LC3 High Speed Logic, Fanout Buffer
PCB [2]	122515 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to Vcc for normal operation.

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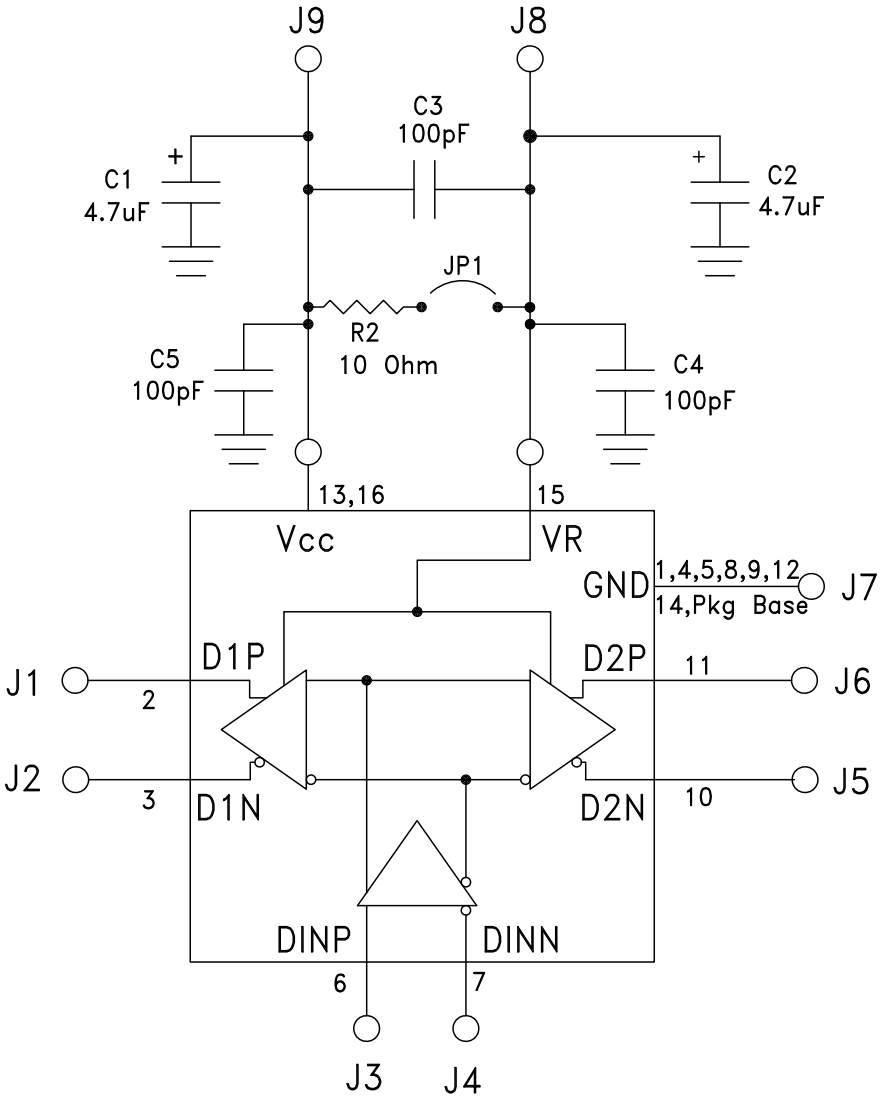
Application Circuit



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