10-Bit, 125 MSPS High Performance TxDAC® D/A Converter

AD9750

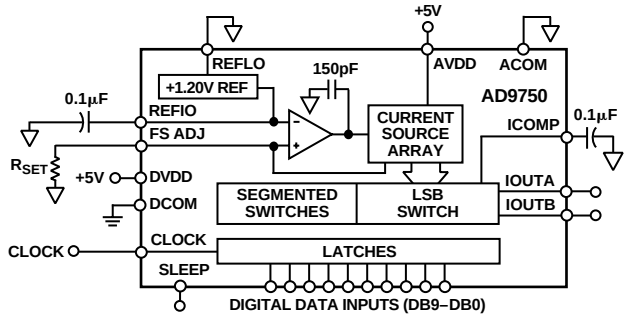
FEATURES

High Performance Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
10-Bit Resolution
Excellent Spurious Free Dynamic Range Performance
SFDR to Nyquist @ 5 MHz Output: 76 dBc
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 190 mW @ 5 V
Power-Down Mode: 20 mW @ 5 V
On-Chip 1.20 V Reference
CMOS-Compatible +2.7 V to +5.5 V Digital Interface
Packages: 28-Lead SOIC and TSSOP
Edge-Triggered Latches

APPLICATIONS

Wideband Communication Transmit Channel:
Direct IF
Basestations
Wireless Local Loop
Digital Radio Link
Direct Digital Synthesis (DDS)
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9750 is a 10-bit resolution, wideband, second generation member of the TxDAC series of high performance, low power CMOS digital-to-analog-converters (DACs). The TxDAC family, which consists of pin compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, thus providing an upward or downward component selection path based on performance, resolution and cost. The AD9750 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9750's flexible single-supply operating range of 4.5 V to 5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 65 mW, without a significant degradation in performance, by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to apprixmatley 20 mW.

The AD9750 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support +2.7 V and +5 V CMOS logic families.

The AD9750 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance.

Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25 V.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The AD9750 can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier, which provides a wide (>10:1) adjustment span, allows the AD9750 full-scale current to be adjusted over a 2 mA to 20 mA range while maintaining excellent dynamic performance. Thus, the AD9750 may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The AD9750 is available in 28-lead SOIC and TSSOP packages. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD9750 is a member of the wideband TxDAC high performance product family that provides an upward or downward component selection path based on resolution (8 to 14 bits), performance and cost. The entire family of TxDACs is available in industry standard pinouts.
2. Manufactured on a CMOS process, the AD9750 uses a proprietary switching technique that enhances dynamic performance beyond that previously attainable by higher power/cost bipolar or BiCMOS devices.
3. On-chip, edge-triggered input CMOS latches interface to +2.7 V to +5 V CMOS logic families. The AD9750 can support update rates up to 125 MSPS.
4. A flexible single-supply operating range of +4.5 V to +5.5 V, and a wide full-scale current adjustment span of 2 mA to 20 mA, allows the AD9750 to operate at reduced power levels.
5. The current output(s) of the AD9750 can be easily configured for various single-ended or differential circuit topologies.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
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AD9750–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	10			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)	–1.0	±0.1	+1.0	LSB
Differential Nonlinearity (DNL)	–0.5	±0.1	+0.5	LSB
ANALOG OUTPUT				
Offset Error	–0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	–2	±0.5	+2	% of FSR
Gain Error (With Internal Reference)	–5	±1.5	+5	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	4.5	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})[4]		33	39	mA
Digital Supply Current (I_{DVDD})[5]		5.0	7	mA
Supply Current Sleep Mode (I_{AVDD})[6]		4.0	8	mA
Power Dissipation[5] (5 V, I_{OUTFS} = 20 mA)		190	230	mW
Power Supply Rejection Ratio[7]—AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio[7]—DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at IOUTA, driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.
[3]Use an external buffer amplifier to drive any external load.
[4]Requires +5 V supply.
[5]Measured at f_{CLOCK} = 50 MSPS and I_{OUT} = static full scale (20 mA).
[6]Logic level for SLEEP pin must be referenced to AVDD. Min V_{IH} = 3.5 V.
[7]±5% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	125			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output				
T_A = +25°C	71	82		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.51 MHz		79		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz		76		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 20.2 MHz		60		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 2.51 MHz		78		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.04 MHz		77		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 20.2 MHz		69		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 40.4 MHz		63		dBc
Spurious-Free Dynamic Range within a Window				
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz	80	87		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		86		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		86		dBc
Total Harmonic Distortion				
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz				
T_A = +25°C		–80		dBc
f_{CLOCK} = 50 MHz; f_{OUT} = 2.00 MHz		–76		dBc
f_{CLOCK} = 100 MHz; f_{OUT} = 2.00 MHz		–76		dBc

NOTES

[1]Measured single ended into 50 Ω load.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V[1]	3.5	5		V
Logic "1" Voltage @ DVDD = +3 V	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V[1]		0	1.3	V
Logic "0" Voltage @ DVDD = +3 V		0	0.9	V
Logic "1" Current	–10		+10	μA
Logic "0" Current	–10		+10	μA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	3.5			ns

NOTES
[1]When DVDD = +5 V, and Logic 1 voltage ≈3.5 V and Logic 0 voltage ≈1.3 V, IVDD can increase by up to 10 mA depending on f_{CLOCK}.
Specifications subject to change without notice.

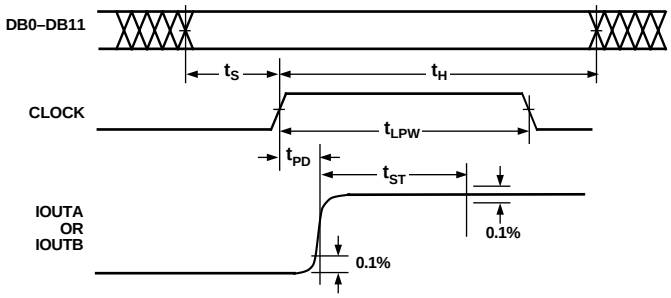


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+6.5	V
DVDD	DCOM	–0.3	+6.5	V
ACOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
CLOCK, SLEEP	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	–1.0	AVDD + 0.3	V
ICOMP	ACOM	–0.3	AVDD + 0.3	V
REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
REFLO	ACOM	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Ranges	Package Descriptions	Package Options*
AD9750AR	–40°C to +85°C	28-Lead 300 Mil SOIC	R-28
AD9750ARU	–40°C to +85°C	28-Lead TSSOP	RU-28
AD9750-EB		Evaluation Board	

*R = Small Outline IC; RU = Thin Shrink Small Outline Package.

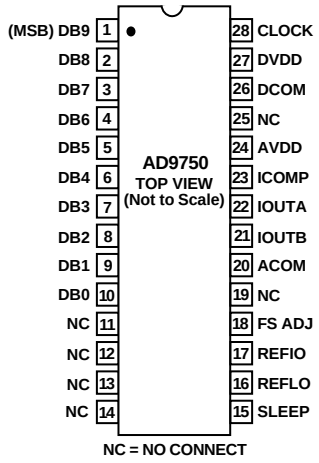
THERMAL CHARACTERISTICS

Thermal Resistance
28-Lead 300 Mil SOIC
θ_{JA} = 71.4°C/W
θ_{JC} = 23°C/W
28-Lead TSSOP
θ_{JA} = 97.9°C/W
θ_{JC} = 14.0°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9750 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DB9	Most Significant Data Bit (MSB).
2–9	DB8–DB1	Data Bits 1–8.
10	DB0	Least Significant Data Bit (LSB).
11–14, 19, 25	NC	No Internal Connection.
15	SLEEP	Power-Down Control Input. Active High. Contains active pull-down circuit, thus may be left unterminated if not used.
16	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., Tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., Tie REFLO to ACOM). Requires 0.1 µF capacitor to ACOM when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust.
20	ACOM	Analog Common.
21	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
23	ICOMP	Internal Bias Node for Switch Driver Circuitry. Decouple to ACOM with 0.1 µF capacitor.
24	AVDD	Analog Supply Voltage (+4.5 V to +5.5 V).
26	DCOM	Digital Common.
27	DVDD	Digital Supply Voltage (+2.7 V to +5.5 V).
28	CLOCK	Clock Input. Data latched on positive edge of clock.

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
The spurious-free dynamic range for an output containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

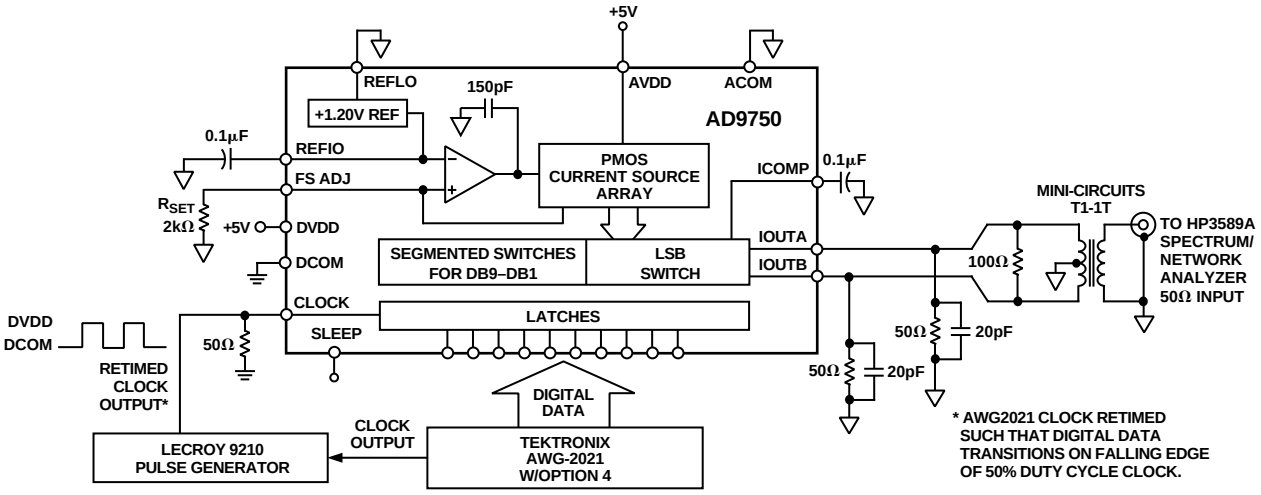


Figure 2. Basic AC Characterization Test Set-Up

Typical AC Characterization Curves @ +5 V Supplies

(AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, T_A = +25°C, SFDR up to Nyquist, unless otherwise noted)

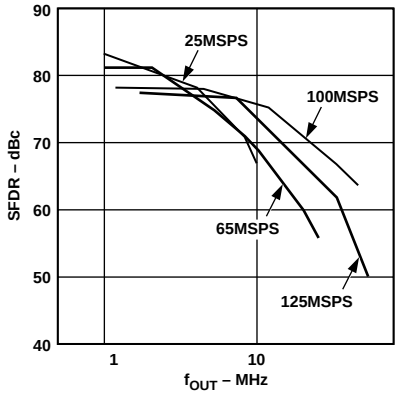


Figure 3. SFDR vs. f_{OUT} @ 0 dBFS

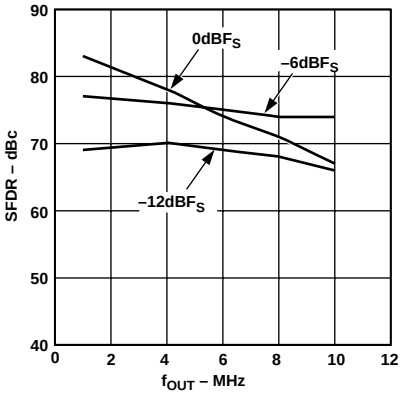


Figure 4. SFDR vs. f_{OUT} @ 25 MSPS

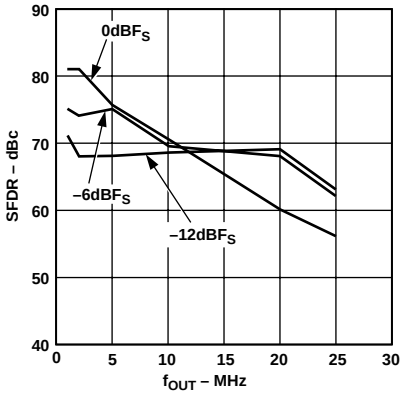


Figure 5. SFDR vs. f_{OUT} @ 65 MSPS

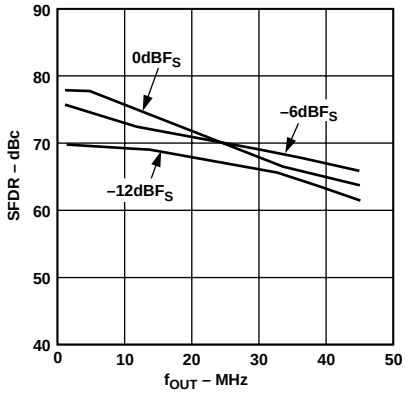


Figure 6. SFDR vs. f_{OUT} @ 100 MSPS

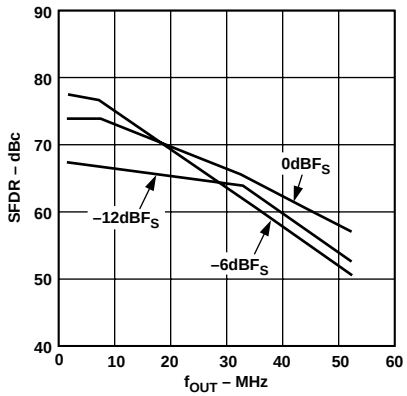


Figure 7. SFDR vs. f_{OUT} @125 MSPS

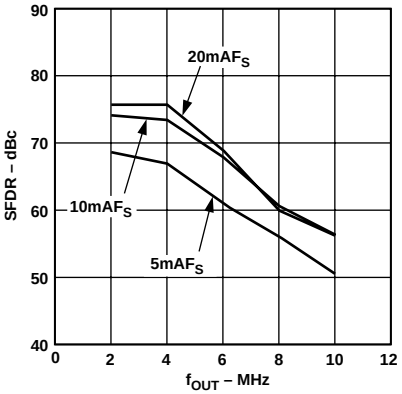


Figure 8. SFDR vs. f_{OUT} and I_{OUTFS} @ 25 MSPS and 0 dBFS

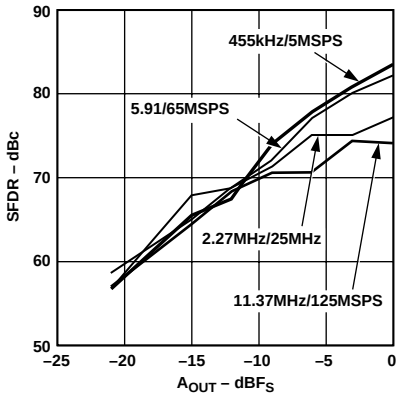


Figure 9. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/11$

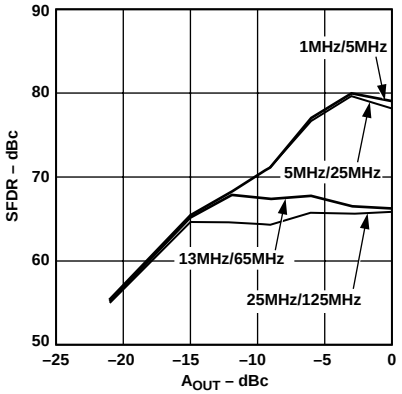


Figure 10. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

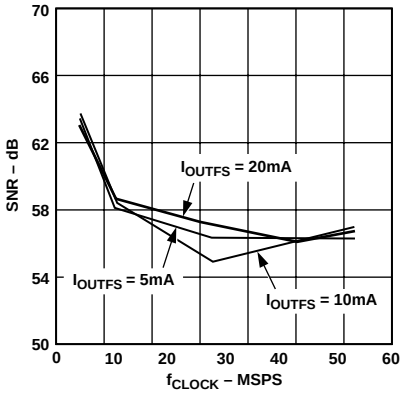


Figure 11. SNR vs. f_{CLOCK} and I_{OUTFS} @ f_{OUT} = 2 MHz and 0 dBFS

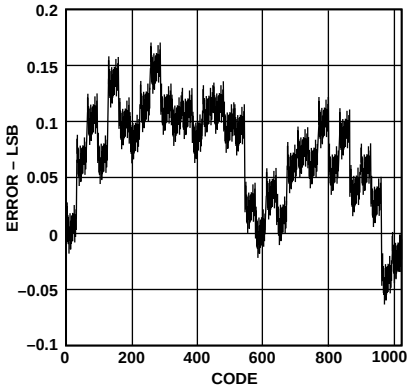


Figure 12. Typical INL

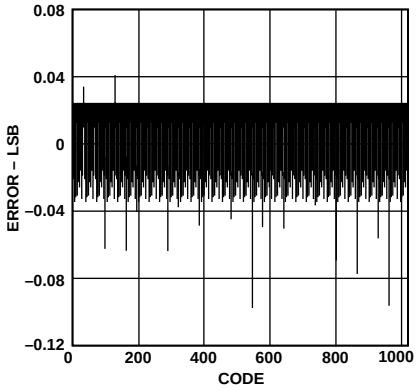


Figure 13. Typical DNL

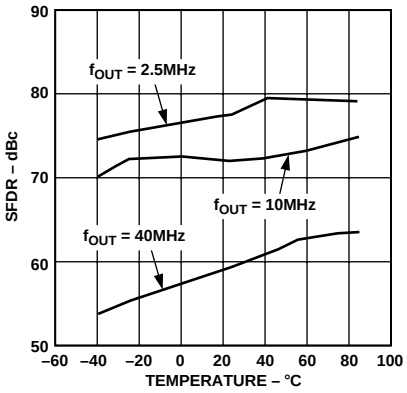


Figure 14. SFDR vs. Temperature @ 125 MSPS, 0 dBFS

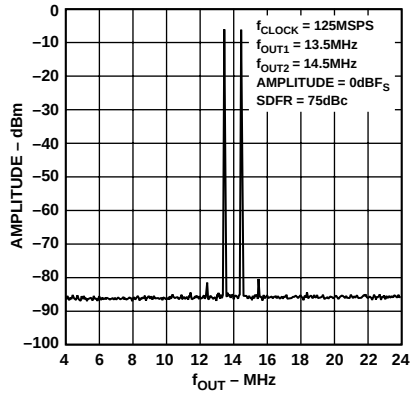


Figure 15. Two-Tone SFDR

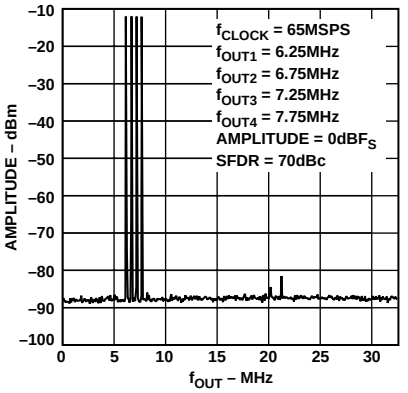


Figure 16. Four-Tone SFDR

FUNCTIONAL DESCRIPTION

Figure 17 shows a simplified block diagram of the AD9750. The AD9750 consists of a large PMOS current source array that is capable of providing up to 20 mA of total current. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSB is a binary weighted fractions of the middle-bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9750 have separate power supply inputs (i.e., AVDD and DVDD). The digital section, which is capable of operating up to a 125 MSPS clock rate and over a +2.7 V to +5.5 V operating range, consists of edge-triggered latches and segment decoding logic circuitry. The analog section, which can operate over a +4.5 V to +5.5 V range, includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is thirty-two times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9750 provides complementary current outputs, IOUTA and IOUTB. IOUTA will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 1023) while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB is a function of both the input code and I_{OUTFS} and can be expressed as:

$$IOUTA = (DAC\ CODE/1024) \times I_{OUTFS} \quad (1)$$

$$IOUTB = (1023 - DAC\ CODE)/1024 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 1023 (i.e., Decimal Representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where $I_{REF} = V_{REFIO}/R_{SET}$ (4)

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, R_{LOAD}, which are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by IOUTA or IOUTB as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply :

$$V_{OUTA} = IOUTA \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = IOUTB \times R_{LOAD} \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, V_{DIFF}, appearing across IOUTA and IOUTB is:

$$V_{DIFF} = (IOUTA - IOUTB) \times R_{LOAD} \quad (7)$$

Substituting the values of IOUTA, IOUTB, and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 1023)/1024\} \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9750 differentially. First, the differential operation will help cancel common-mode error sources associated with IOUTA and IOUTB such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9750 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

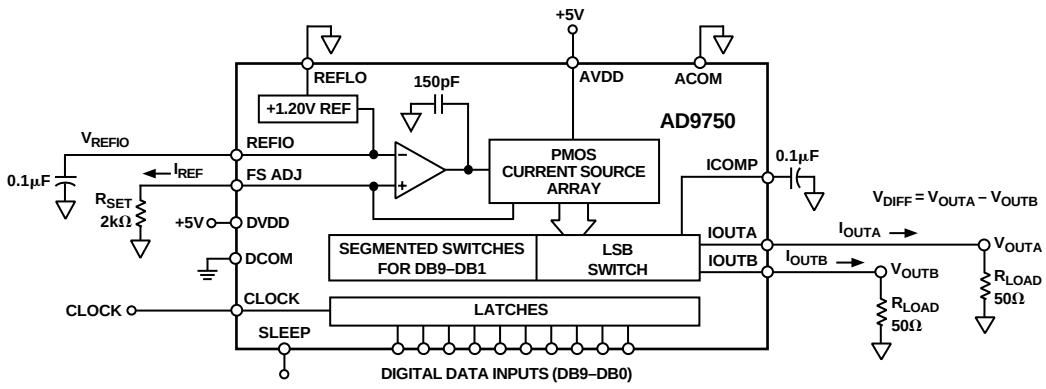


Figure 17. Functional Block Diagram

REFERENCE OPERATION

The AD9750 contains an internal 1.20 V bandgap reference that can easily be disabled and overridden by an external reference. REFIO serves as either an *input* or *output* depending on whether the internal or an external reference is selected. If REFLO is tied to ACOM, as shown in Figure 18, the internal reference is activated and REFIO provides a 1.20 V output. In this case, the internal reference *must* be compensated externally with a ceramic chip capacitor of 0.1 µF or greater from REFIO to REFLO. Also, REFIO should be buffered with an external amplifier having an input bias current less than 100 nA if any additional loading is required.

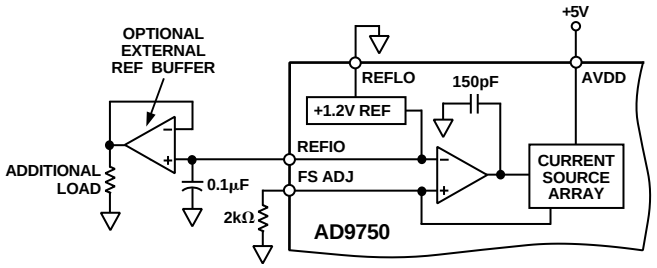


Figure 18. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external reference may then be applied to REFIO as shown in Figure 19. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1 MΩ) of REFIO minimizes any loading of the external reference.

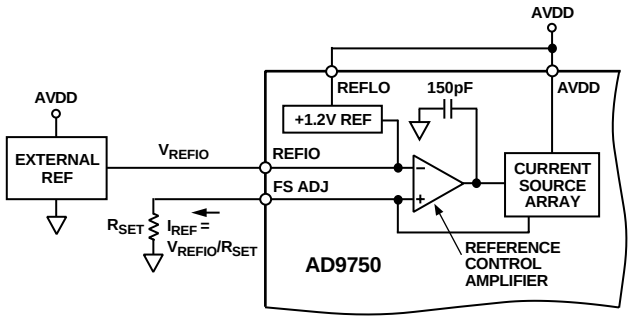


Figure 19. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9750 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter as shown in Figure 19, such that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied over to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting IREF between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9750, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 0.5 MHz. The output of the control amplifier is internally compensated via a 150 pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Since the –3 dB bandwidth corresponds to the dominant pole, and hence the time constant, the settling time of the control amplifier to a stepped reference input response can be approximated. In this case, the time constant can be approximated to be 320 ns.

There are two methods in which I_{REF} can be varied for a fixed R_{SET}. The first method is suitable for a single-supply system in which the internal reference is disabled, and the common-mode voltage of REFIO is varied over its compliance range of 1.25 V to 0.10 V. REFIO can be driven by a single-supply amplifier or DAC, thus allowing I_{REF} to be varied for a fixed R_{SET}. Since the input impedance of REFIO is approximately 1 MΩ, a simple, low cost R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 20 using the AD7524 and an external 1.2 V reference, the AD1580.

The second method may be used in a dual-supply system in which the common-mode voltage of REFIO is fixed and I_{REF} is varied by an external voltage, V_{GC}, applied to R_{SET} via an amplifier. An example of this method is shown in Figure 21, in which the internal reference is used to set the common-mode voltage of the control amplifier to 1.20 V. The external voltage, V_{GC}, is referenced to ACOM and should not exceed 1.2 V. The value of R_{SET} is such that I_{REFMAX} and I_{REFMIN} do not exceed 62.5 µA

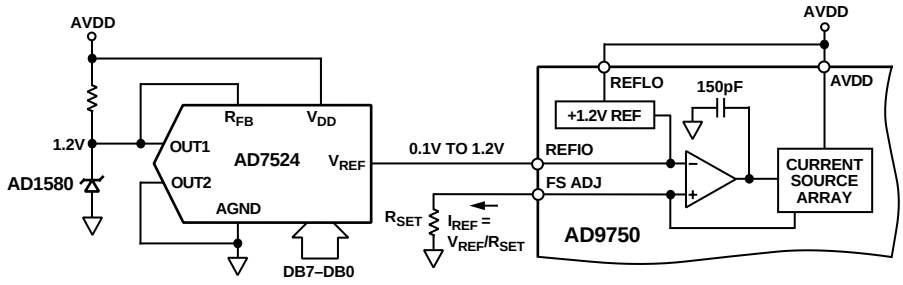


Figure 20. Single-Supply Gain Control Circuit

and 625 μA, respectively. The associated equations in Figure 21 can be used to determine the value of R_{SET}.

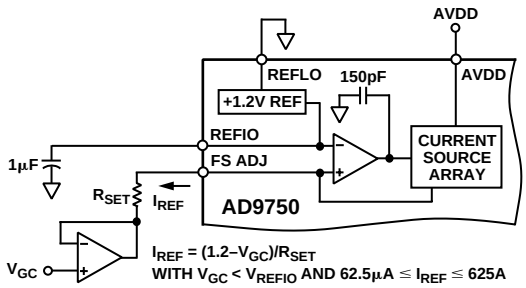


Figure 21. Dual-Supply Gain Control Circuit

ANALOG OUTPUTS

The AD9750 produces two complementary current outputs, IOUTA and IOUTB, which may be configured for single-end or differential operation. IOUTA and IOUTB can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration.

Figure 22 shows the equivalent analog output circuit of the AD9750 consisting of a parallel combination of PMOS differential current switches associated with each segmented current source. The output impedance of IOUTA and IOUTB is determined by the equivalent parallel combination of the PMOS switches and is typically 100 kΩ in parallel with 5 pF. Due to the nature of a PMOS device, the output impedance is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) and, to a lesser extent, the analog supply voltage, AVDD, and full-scale current, I_{OUTFS}. Although the output impedance's signal dependency can be a source of dc nonlinearity and ac linearity (i.e., distortion), its effects can be limited if certain precautions are noted.

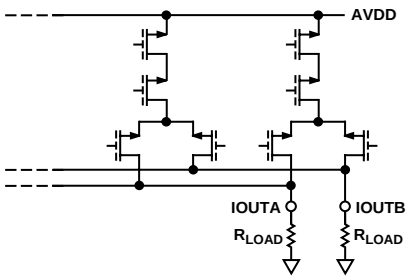


Figure 22. Equivalent Analog Output

IOUTA and IOUTB also have a negative and positive voltage compliance range. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9750. The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. Operation beyond the positive compliance range will induce clipping of the output signal which severely degrades the AD9750's linearity and distortion performance.

For applications requiring the optimum dc linearity, IOUTA and/or IOUTB should be maintained at a virtual ground via an I-V op amp configuration. Maintaining IOUTA and/or IOUTB at a virtual ground keeps the output impedance of the AD9750 fixed, significantly reducing its effect on linearity. However, it does not necessarily lead to the optimum distortion performance due to limitations of the I-V op amp. Note that the INL/DNL specifications for the AD9750 are measured in this manner using IOUTA. In addition, these dc linearity specifications remain virtually unaffected over the specified power supply range of 4.5 V to 5.5 V.

Operating the AD9750 with reduced voltage output swings at IOUTA and IOUTB in a differential or single-ended output configuration reduces the signal dependency of its output impedance thus enhancing distortion performance. Although the voltage compliance range of IOUTA and IOUTB extends from –1.0 V to +1.25 V, optimum distortion performance is achieved when the maximum full-scale signal at IOUTA and IOUTB does not exceed approximately 0.5 V. A properly selected transformer with a grounded center-tap will allow the AD9750 to provide the required power and voltage levels to different loads while maintaining reduced voltage swings at IOUTA and IOUTB. DC-coupled applications requiring a differential or single-ended output configuration should size R_{LOAD} accordingly. Refer to Applying the AD9750 section for examples of various output configurations.

The most significant improvement in the AD9750's distortion and noise performance is realized using a differential output configuration. The common-mode error sources of both IOUTA and IOUTB can be substantially reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the reconstructed wave-form's frequency content increases and/or its amplitude decreases.

The distortion and noise performance of the AD9750 is also slightly dependent on the analog and digital supply as well as the full-scale current setting, I_{OUTFS}. Operating the analog supply at 5.0 V ensures maximum headroom for its internal PMOS current sources and differential switches leading to improved distortion performance. Although I_{OUTFS} can be set between 2 mA and 20 mA, selecting an I_{OUTFS} of 20 mA will provide the best distortion and noise performance also shown in Figure 8. The noise performance of the AD9750 is affected by the digital supply (DVDD), output frequency, and increases with increasing clock rate as shown in Figure 11. Operating the AD9750 with low voltage logic levels between 3 V and 3.3 V will slightly reduce the amount of on-chip digital noise.

In summary, the AD9750 achieves the optimum distortion and noise performance under the following conditions:

(1) Differential Operation.
(2) Positive voltage swing at IOUTA and IOUTB limited to +0.5 V.
(3) I_{OUTFS} set to 20 mA.
(4) Analog Supply (AVDD) set at 5.0 V.
(5) Digital Supply (DVDD) set at 3.0 V to 3.3 V with appropriate logic levels.

Note that the ac performance of the AD9750 is characterized under the above mentioned operating conditions.

DIGITAL INPUTS

The AD9750's digital input consists of 10 data input pins and a clock input pin. The 10-bit parallel data inputs follow standard positive binary coding where DB9 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). IOUTA produces a full-scale output current when all data bits are at Logic 1. IOUTB produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. The DAC output is updated following the rising edge of the clock as shown in Figure 1 and is designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met; although the location of these transition edges may affect digital feedthrough and distortion performance. *Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.*

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$ set to approximately half the digital positive supply (DVDD) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9750 is capable of operating over a digital supply range of 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers $V_{OH(MAX)}$. A DVDD of 3 V to 3.3 V will typically ensure proper compatibility with most TTL logic families. Figure 23 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar with the exception that it contains an active pull-down circuit, thus ensuring that the AD9750 remains enabled if this input is left disconnected.

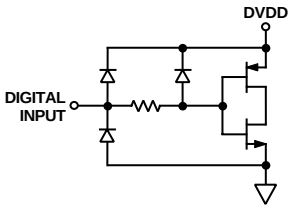


Figure 23. Equivalent Digital Input

Since the AD9750 is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the AD9750 as well as its required min/max input logic level thresholds. Typically, the selection of the slowest logic family that satisfies the above conditions will result in the lowest data feedthrough and noise.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9750 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs. Also, operating the AD9750 with reduced logic swings and a corresponding digital supply (DVDD) will also reduce data feedthrough.

The external clock driver circuitry should provide the AD9750 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

Note, the clock input could also be driven via a sine wave, which is centered around the digital threshold (i.e., DVDD/2), and meets the min/max logic threshold. This will typically result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Also, at higher sampling rates, the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and subsequently cut into the required data setup and hold times.

INPUT CLOCK/DATA TIMING RELATIONSHIP

SNR in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9750 is positive edge triggered, and so exhibits SNR sensitivity when the data transition is close to this edge. In general, the goal when applying the AD9750 is to make the data transitions shortly after the rising edge. This becomes more important as the sample rate increases. Figure 24 shows the relationship of SNR to clock placement with different sample rates and different frequencies out. Note that at the lower sample rates, much more tolerance is allowed in clock placement, while at higher rates, much more care must be taken.

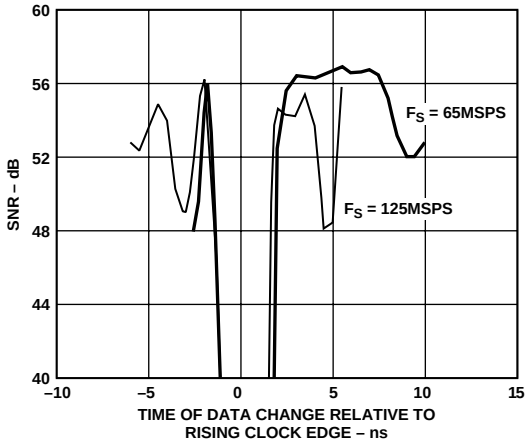


Figure 24. SNR vs. Clock Placement 2 f_{OUT} = 10 MHz

SLEEP MODE OPERATION

The AD9750 has a power-down function which turns off the output current and reduces the supply current to less than 8.5 mA over the specified supply range of 2.7 V to 5.5 V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures the AD9750 remains enabled if this input is left disconnected. The AD9750 takes less than 50 ns to power down and approximately 5 µs to power back up.

POWER DISSIPATION

The power dissipation, P_D, of the AD9750 is dependent on several factors which include: (1) AVDD and DVDD, the power supply voltages; (2) I_{OUTFS}, the full-scale current output; (3) f_{CLOCK}, the update rate; (4) and the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS} as shown in Figure 25 and is insensitive to f_{CLOCK}.

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figures 26 and 27 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 5 V and DVDD = 3 V, respectively. Note, how I_{DVDD} is reduced by more than a factor of 2 when DVDD is reduced from 5 V to 3 V.

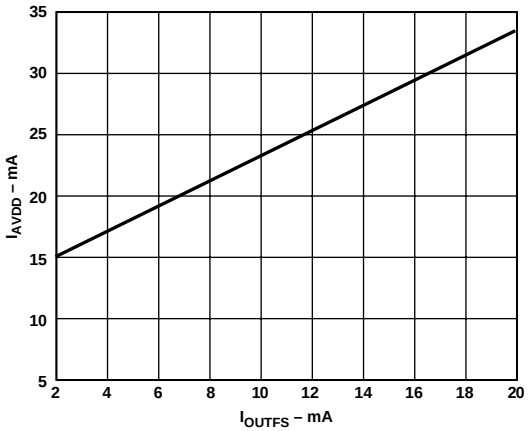


Figure 25. I_{AVDD} vs. I_{OUTFS}

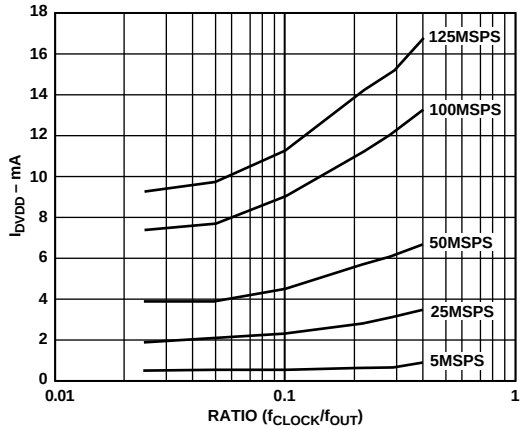


Figure 26. I_{DVDD} vs. Ratio @ DVDD = 5 V

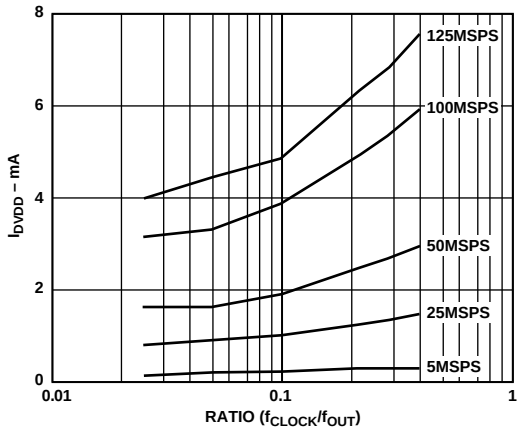


Figure 27. I_{DVDD} vs. Ratio @ DVDD = 3 V

APPLYING THE AD9750

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9750. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if IOUTA and/or IOUTB is connected to an appropriately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter thus converting IOUTA or IOUTB into a negative unipolar voltage. This configuration provides the best dc linearity since IOUTA or IOUTB is maintained at a virtual ground. Note, IOUTA provides slightly better performance than IOUTB.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 28. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

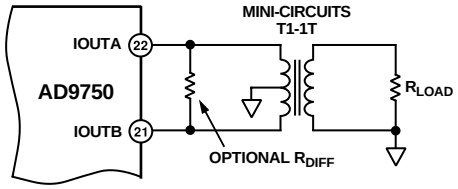


Figure 28. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both IOUTA and IOUTB. The complementary voltages appearing at IOUTA and IOUTB (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9750. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination which results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL USING AN OP AMP

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 29. The AD9750 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

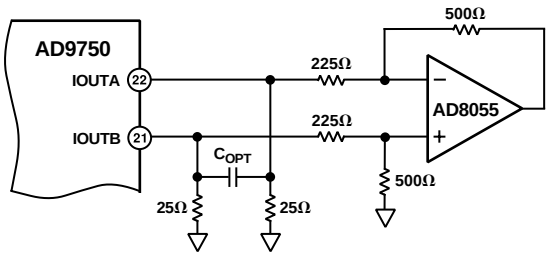


Figure 29. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ±1.0 V. A high speed amplifier such as the AD8055 or AD8057 capable of preserving the differential performance of the AD9750 while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 30 provides the necessary level-shifting required in a single supply system. In this case, AVDD which is the positive analog supply for both the AD9750 and the op amp is also used to level-shift the differential output of the AD9750 to midsupply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.

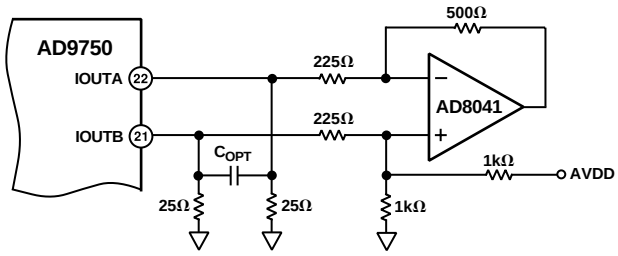


Figure 30. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 31 shows the AD9750 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the ANALOG OUTPUT section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

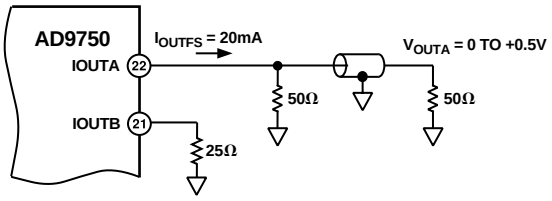


Figure 31. 0 V to +0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 32 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9750 output current. U1 maintains IOUTA (or IOUTB) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the ANALOG OUTPUT section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

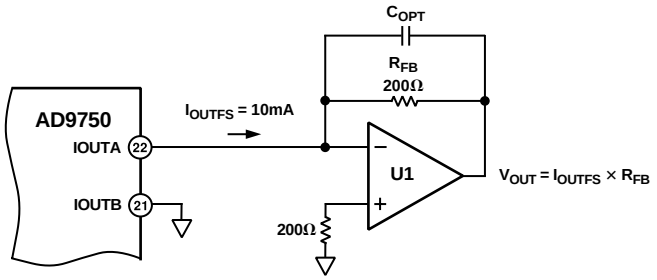


Figure 32. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION

Many applications seek high speed and high performance under less than ideal operating conditions. In these circuits, the implementation and construction of the printed circuit board design are as important as the circuit design. To ensure optimum performance, proper RF techniques must be used for device selection, placement and routing as well as power supply bypassing and grounding. Figures 39–44 illustrate the recommended printed circuit board ground, power and signal plane layouts which are implemented on the AD9750 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution (i.e., AVDD, DVDD). This is referred to as Power Supply Rejection Ratio (PSRR). For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full-scale current, I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise will occur over the spectrum from tens of kHz to several MHz. PSRR vs. frequency of the AD9750 AVDD supply, over this frequency range, is given in Figure 33.

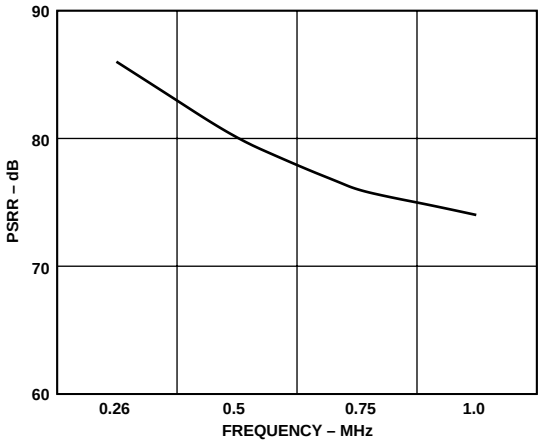


Figure 33. Power Supply Rejection Ratio of AD9750

Note that the units in Figure 33 are given in units of (amps out)/(volts in). Noise on the analog power supply has the effect of modulating the internal switches, and therefore the output current. The voltage noise on the dc power will be added in a nonlinear manner to the desired I_{OUT}. Due to the relatively different sizes of these switches, PSRR is very code-dependent. This can produce a mixing effect which can modulate low frequency power supply noise to higher frequencies. Worst case PSRR for either one of the differential DAC outputs will occur when the full-scale current is directed towards that output. As a result, the PSRR measurement in Figure 33 represents a worst case condition in which the digital inputs remain static and the full-scale output current of 20 mA is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV rms of noise and, for simplicity sake (i.e., ignore harmonics), all of this noise is concentrated at 250 kHz. To calculate how much of this undesired noise will appear as current noise superimposed on the DAC's full-scale current, I_{OUTFS}, one must determine the PSRR in dB using Figure 33 at 250 kHz. To calculate the PSRR for a given R_{LOAD}, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 33 by the scaling factor $20 \times \text{Log}(R_{LOAD})$. For instance, if R_{LOAD} is 50 Ω, the PSRR is reduced by 34 dB (i.e., PSRR of the DAC at 1 MHz, which is 74 dB in Figure 33 becomes 40 dB V_{OUT}/V_{IN}).

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9750 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close as physically as possible.

For those applications that require a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 34. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

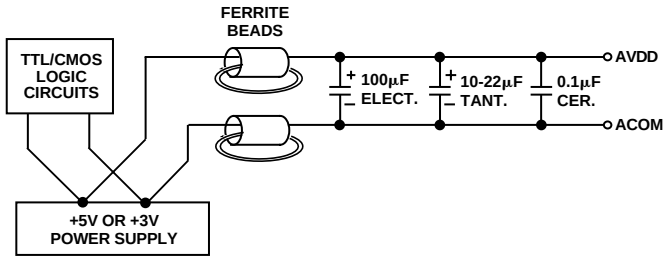


Figure 34. Differential LC Filter for Single +5 V or +3 V Applications

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the AD9750. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as providing some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistor should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed signal printed circuit boards, refer to Analog Devices' application notes AN-280 and AN-333.

APPLICATIONS

Using the AD9750 for Quadrature Amplitude Modulation (QAM)

QAM is one of the most widely used digital modulation schemes in digital communication systems. This modulation technique can be found in FDM as well as spreadspectrum (i.e., CDMA) based systems. A QAM signal is a carrier frequency that is modulated in both amplitude (i.e., AM modulation) and phase (i.e., PM modulation). It can be generated by independently modulating two carriers of identical frequency but with a 90° phase difference. This results in an in-phase (I) carrier component and a quadrature (Q) carrier component at a 90° phase shift with respect to the I component. The I and Q components are then summed to provide a QAM signal at the specified carrier frequency.

A common and traditional implementation of a QAM modulator is shown in Figure 35. The modulation is performed in the analog domain in which two DACs are used to generate the baseband I and Q components, respectively. Each component is then typically applied to a Nyquist filter before being applied to a quadrature mixer. The matching Nyquist filters shape and limit each component's spectral envelope while minimizing intersymbol interference. The DAC is typically updated at the QAM symbol rate or possibly a multiple of it if an interpolating filter precedes the DAC. The use of an interpolating filter typically eases the implementation and complexity of the analog filter, which can be a significant contributor to mismatches in gain and phase between the two baseband channels. A quadrature mixer modulates the I and Q components with in-phase and quadrature phase carrier frequency and then sums the two outputs to provide the QAM signal.

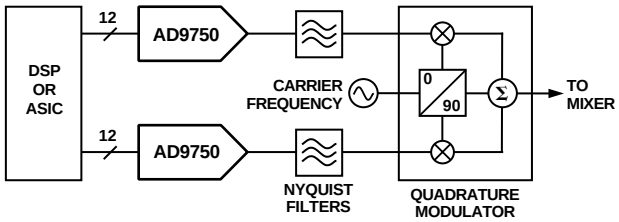


Figure 35. Typical Analog QAM Architecture

In this implementation, it is much more difficult to maintain proper gain and phase matching between the I and Q channels. The circuit implementation shown in Figure 36 helps improve upon the matching and temperature stability characteristics between the I and Q channels, as well as showing a path for upconversion using the AD8346 quadrature modulator. Using a single voltage reference derived from U1 to set the gain for both the I and Q channels will improve the gain matching and stability. R_{CAL} can be used to compensate for any mismatch in gain between the two channels. This mismatch may be attributed to the mismatch between R_{SET1} and R_{SET2}, effective load resistance of each channel, and/or the voltage offset of the control amplifier in each DAC. The differential voltage outputs of U1 and U2 are fed into the respective differential inputs of the AD8346 via matching networks.

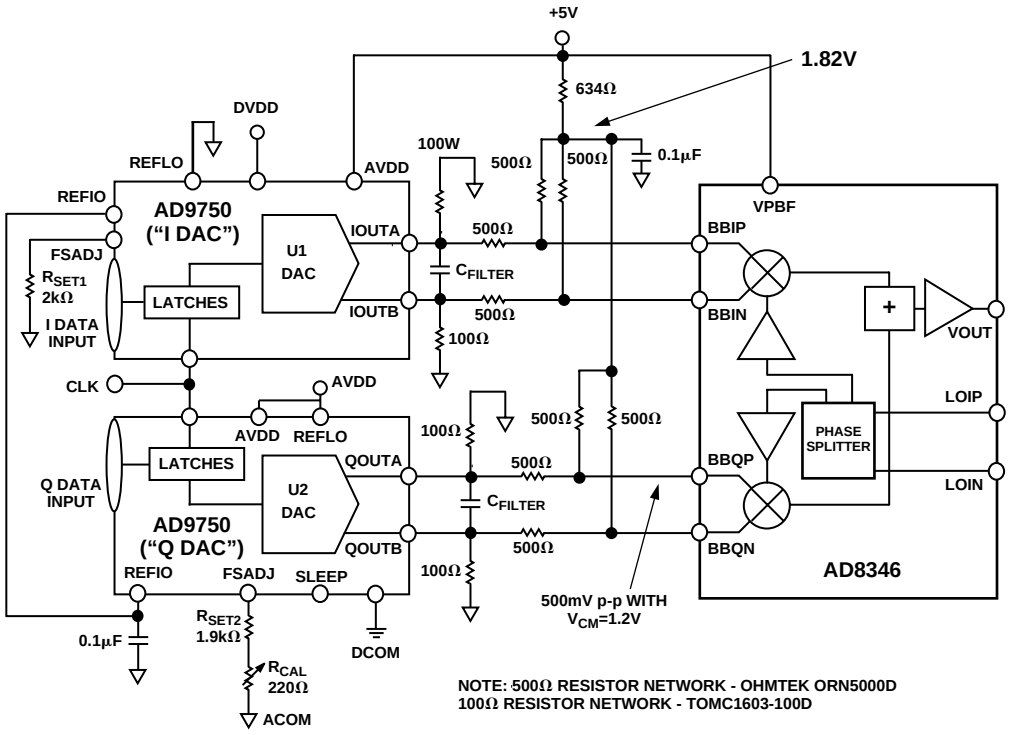


Figure 36. Baseband QAM Implementation Using Two AD9750s

It is also possible to generate a QAM signal completely in the digital domain via a DSP or ASIC, in which case only a single DAC of sufficient resolution and performance is required to reconstruct the QAM signal. Also available from several vendors are Digital ASICs which implement other digital modulation schemes such as PSK and FSK. This digital implementation has the benefit of generating perfectly matched I and Q components in terms of gain and phase, which is essential in maintaining optimum performance in a communication system. In this implementation, the reconstruction DAC must be operating at a sufficiently high clock rate to accommodate the highest specified QAM carrier frequency. Figure 37 shows a block diagram of such an implementation using the AD9750.

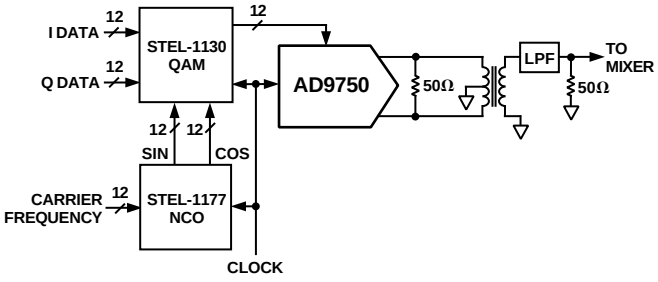


Figure 37. Digital QAM Architecture

AD9750 EVALUATION BOARD

General Description

The AD9750-EB is an evaluation board for the AD9750 10-bit D/A converter. Careful attention to layout and circuit design combined with a prototyping area allow the user to easily and effectively evaluate the AD9750 in any application where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9750 in various configurations. Possible output configurations include transformer coupled, resistor terminated, inverting/noninverting and differential amplifier outputs. The digital inputs are designed to be driven directly from various word generators, with the on-board option to add a resistor network for proper load termination. Provisions are also made to operate the AD9750 with either the internal or external reference, or to exercise the power-down feature.

Refer to the application note AN-420 for a thorough description and operating instructions for the AD9750 evaluation board.

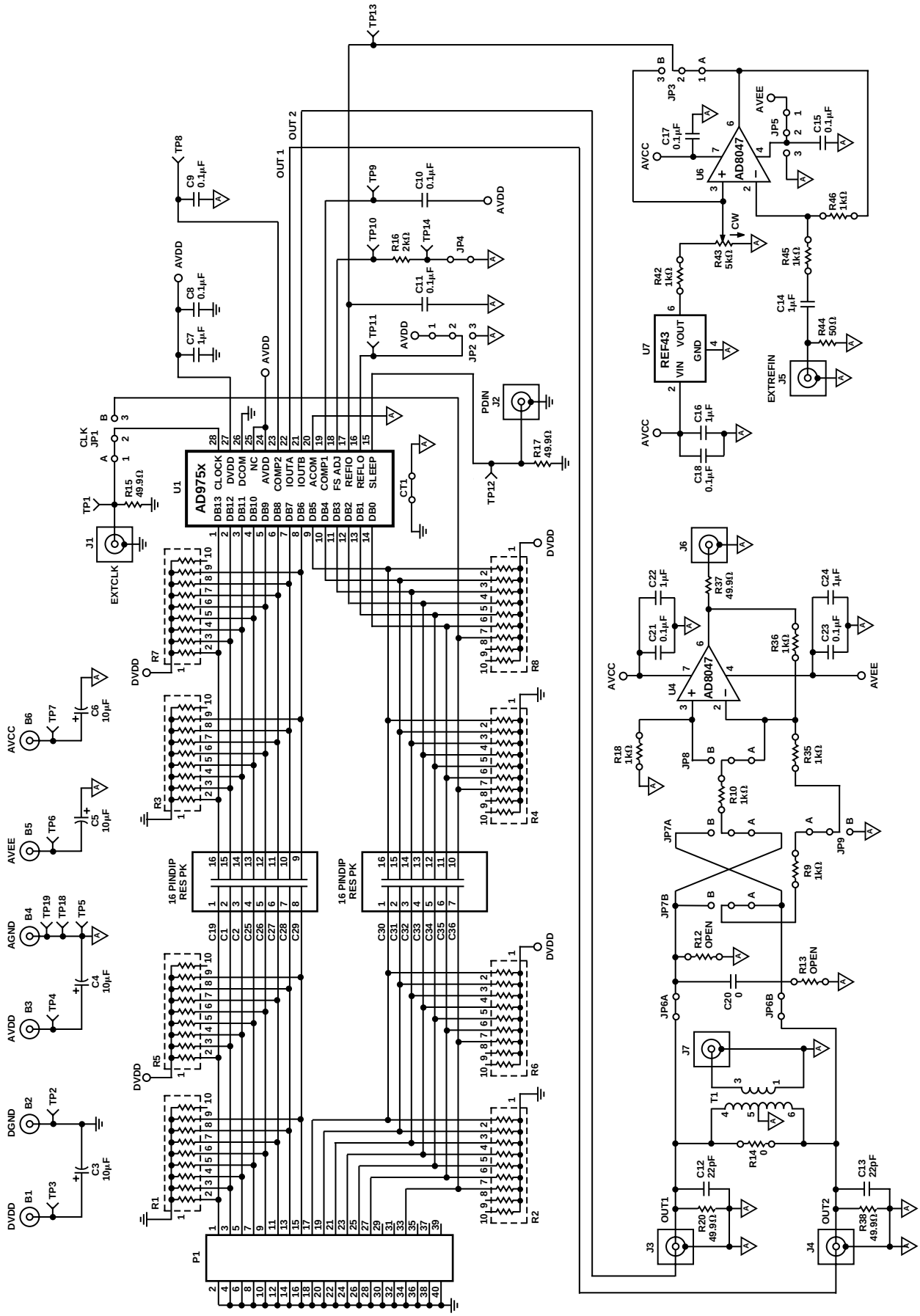


Figure 38. Evaluation Board Schematic

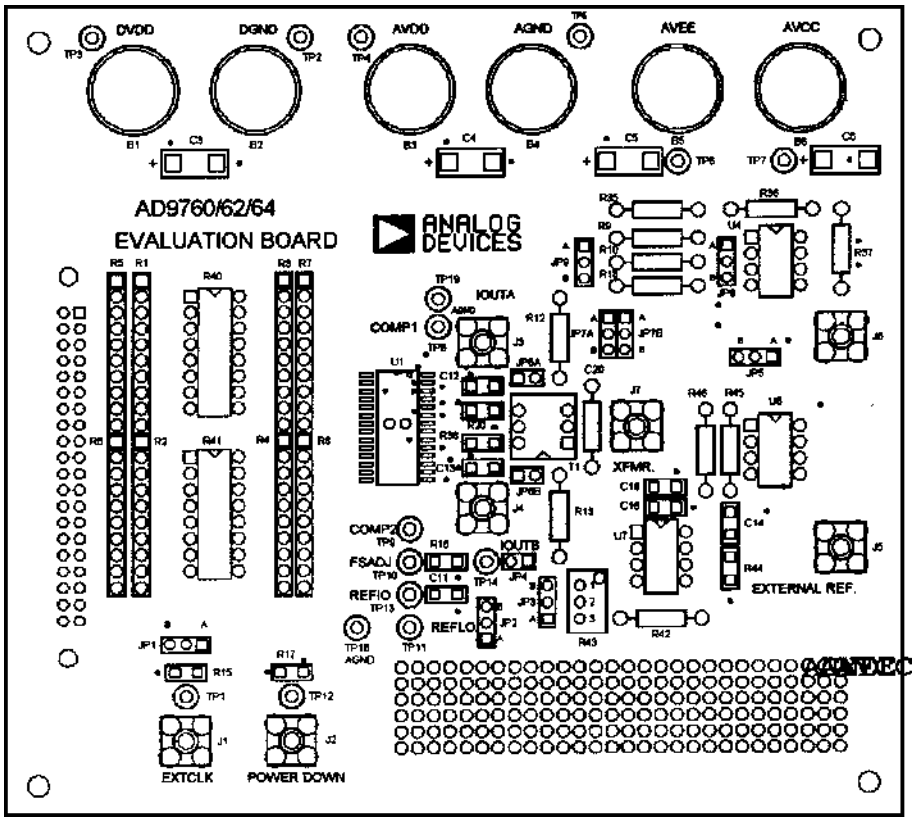


Figure 39. Silkscreen Layer—Top

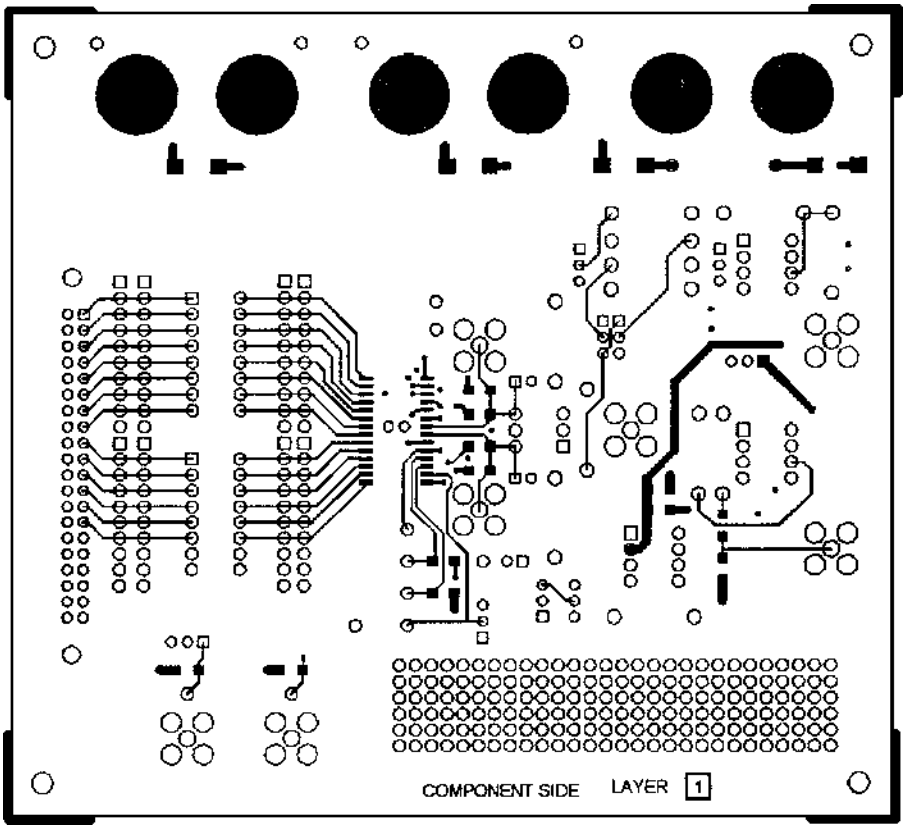


Figure 40. Component Side PCB Layout (Layer 1)

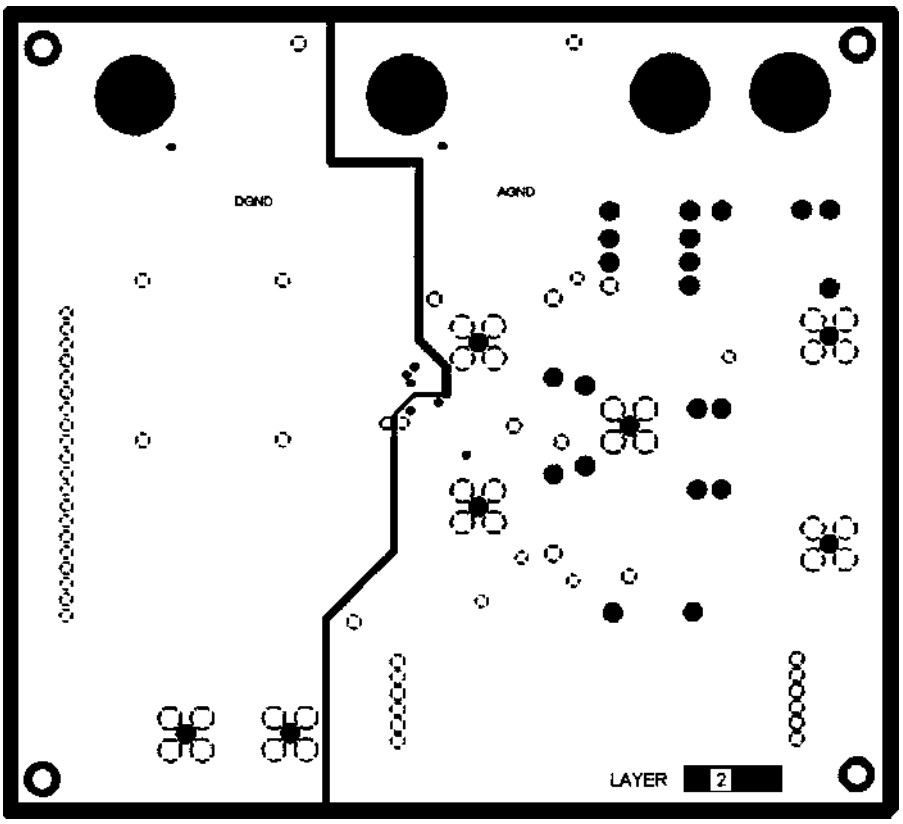


Figure 41. Ground Plane PCB Layout (Layer 2)

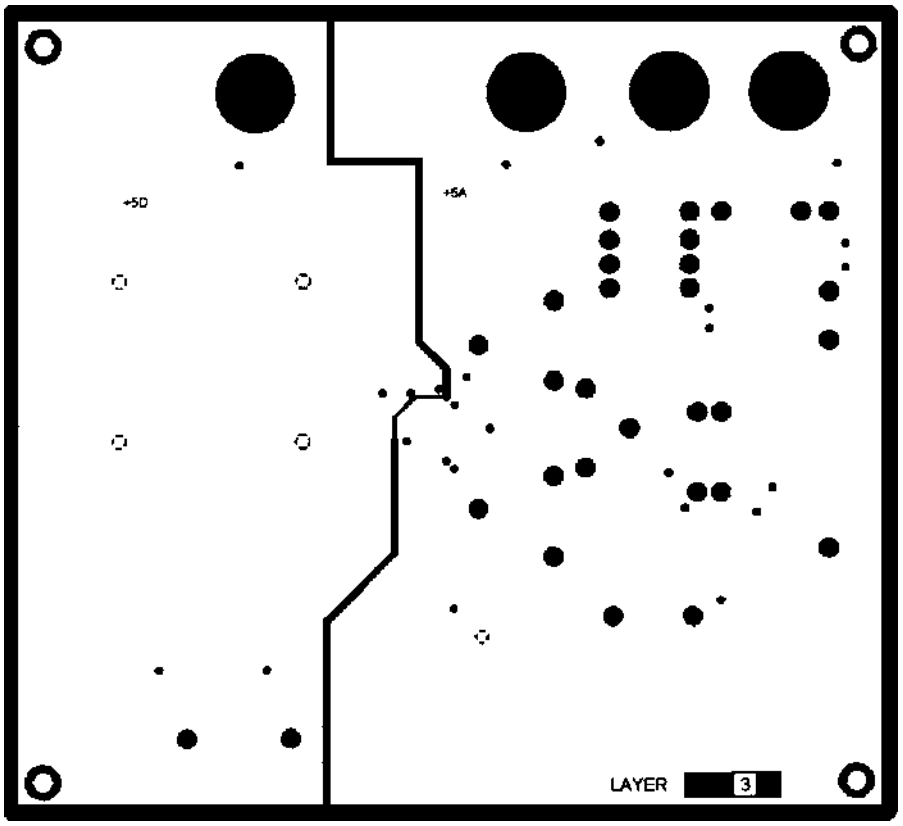


Figure 42. Power Plane PCB Layout (Layer 3)

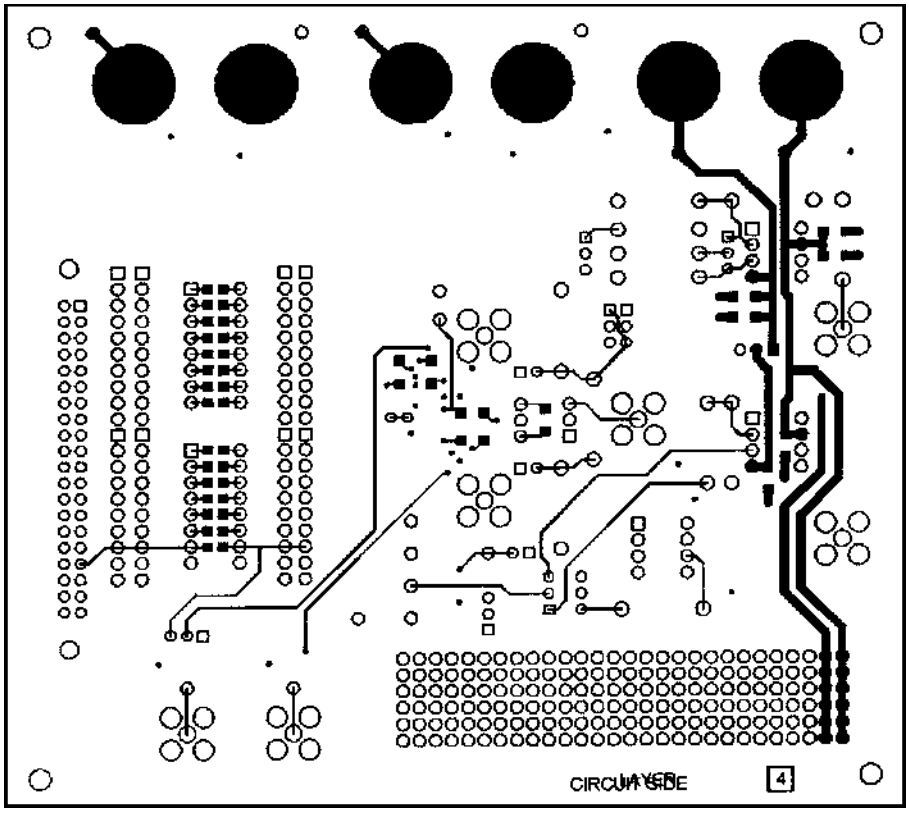


Figure 43. Solder Side PCB Layout (Layer 4)

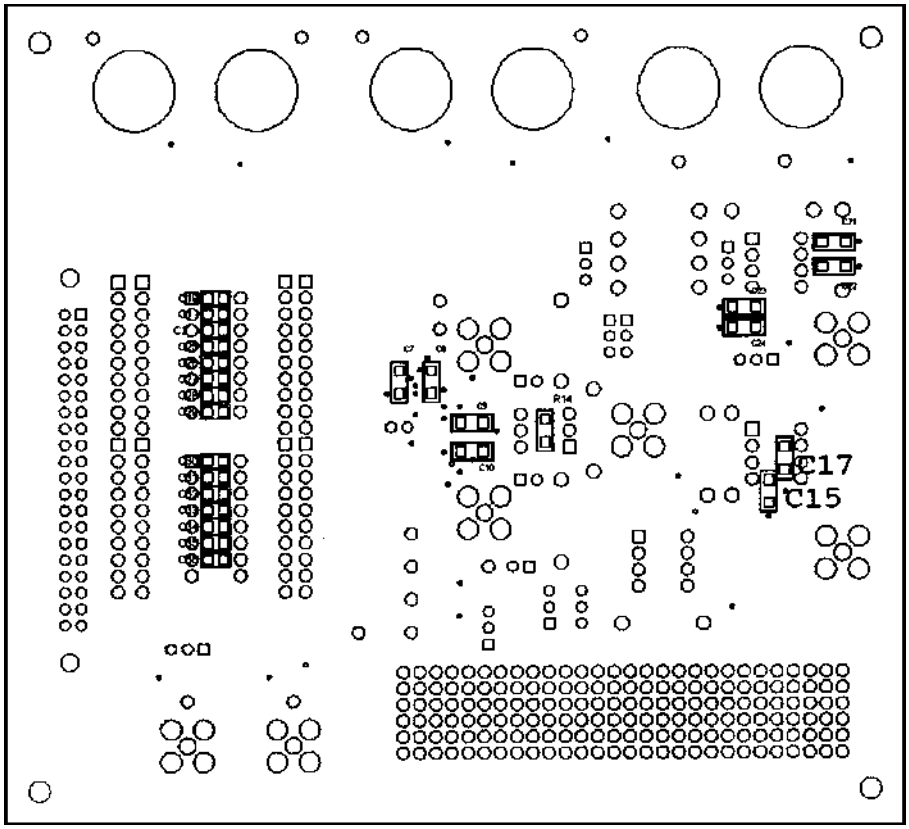
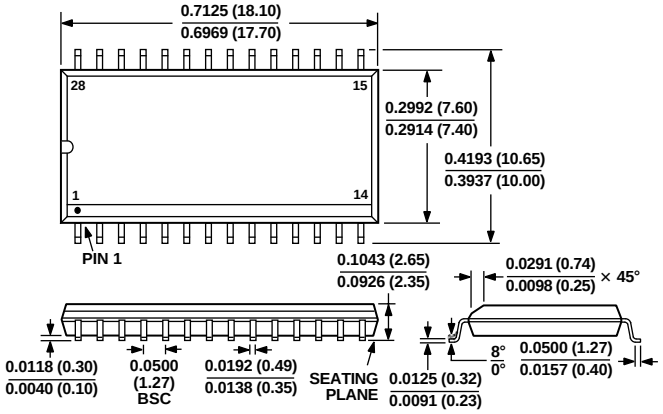


Figure 44. Silkscreen Layer—Bottom

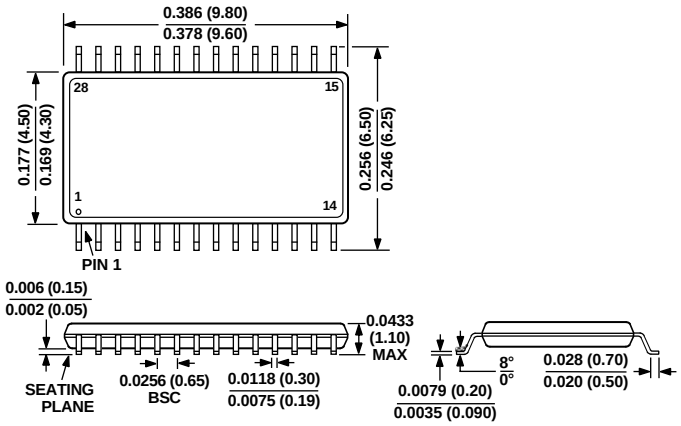
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead, 300 Mil SOIC
(R-28)



28-Lead TSSOP
(RU-28)



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