Operational Amplifiers / Comparators

Full Swing Low Voltage Operation CMOS Operational Amplifiers

BU7261G, BU7261SG, BU7295HFV, BU7295SHFV, BU7262F/FVM/NUX, BU7262SF/FVM/NUX, BU7264F, BU7264SF, BU7241G, BU7241SG, BU7275HFV, BU7275SHFV, BU7242F/FVM/NUX, BU7242S F/FVM/NUX, BU7244F, BU7244SF

No.10049EAT22

●Description

Low Voltage CMOS Op-Amp integrates one or two or four independent output full swing Op-Amps and phase compensation capacitors on a single chip. Especially, this series is operable with low voltage, low supply current and low input bias current.

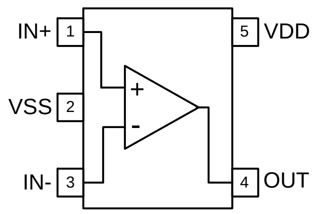
・Input-Output Full Swing : BU7261 (BU7261S) family, BU7241 (BU7241S) family,
BU7295 (BU7295S) family, BU7275 (BU7275S) family,
BU7262 (BU7262S) family, BU7242 (BU7242S) family,
BU7264 (BU7264S) family, BU7244 (BU7244S) family,

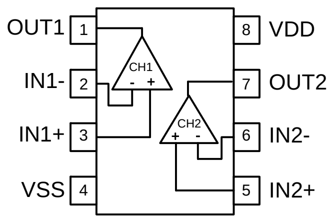
●Features

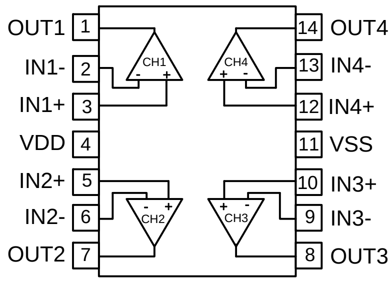
1) Operable with low voltage
   +1.8[V] ~ +5.5[V] (single supply):
   BU7261/BU7241 family BU7262/BU7242 family
   BU7264/BU7244 family BU7295/BU7275 family
2) Operable input-Output full swing
3) High slew rate (BU7261 family, BU7262 family)
   (BU7295 family, BU7264 family)
4) Internal phase compensation
5) Wide temperature range
   -40[℃] ~ +85[℃]
   (BU7261G, BU7262 family, BU7264F, BU7295HFV)
   (BU7241G, BU7242 family, BU7244F, BU7275HFV)
   -40[℃] ~ +105[℃]
   (BU7261SG, BU7262S family, BU7264SF, BU7295SHFV)
   (BU7241SG, BU7242S family, BU7244SF, BU7275SHFV)
6) High large signal voltage gain
7) Low supply current
   (BU7241 family, BU7242 family)
   (BU7275 family, BU7244 family)
8) Low input bias current 1[pA](Typ.)
9) Internal ESD protection
   Human body model (HBM)±4000[V](Typ.)

- Input-Output Full Swing
  - High speed
    - Single
      - BU7261G (BU7261SG: Operation guaranteed up to 105℃)
      - BU7295HFV (BU7295SHFV: Operation guaranteed up to 105℃)
    - Dual
      - BU7262F/FVM/NUX (BU7262S F/FVM/NUX: Operation guaranteed up to 105℃)
    - Quad
      - BU7264F (BU7264SF: Operation guaranteed up to 105℃)
  - Low power
    - Single
      - BU7241G (BU7241SG: Operation guaranteed up to 105℃)
      - BU7275HFV (BU7275SHFV: Operation guaranteed up to 105℃)
    - Dual
      - BU7242F/FVM/NUX (BU7242S F/FVM/NUX: Operation guaranteed up to 105℃)
    - Quad
      - BU7244F (BU7244SF: Operation guaranteed up to 105℃)

●Pin Assignments







SSOP5 HVSOF5 SOP8 MSOP8 VSON008X2030 SOP14

Input type	Package					
	SSOP5	HVSOF5	SOP8	VSON008X2030	MSOP8	SOP14
Input-output Full Swing	BU7261G BU7261SG BU7241G BU7241SG	BU7275HFV BU7275SHFV BU7295HFV BU7295SHFV	BU7262F BU7262SF BU7242F BU7242SF	BU7262NUX BU7262SNUX BU7242NUX BU7242SNUX	BU7262FVM BU7262SFVM BU7242FVM BU7242SFVM	BU7264F BU7264SF BU7244F BU7244SF

●Absolute maximum rating (Ta=25[℃])

Parameter	Symbol	Ratings		
		BU7261G, BU7241G, BU7262F/FVM/NUX BU7242F/FVM/NUX BU7264F, BU7244F BU7295HFV, BU7275HFV	BU7261SG, BU7241SG, BU7262SF/FVM/NUX BU7242SF/FVM/NUX BU7264SF, BU7244SF BU7295SHFV, BU7275SHFV	Unit
Supply Voltage	VDD-VSS	+7		V
Differential Input Voltage(*1)	Vid	VDD－VSS		V
Input Common-mode Voltage Range	Vicm	(VSS-0.3)(VDD+0.3)		V
Operating Temperature	Topr	-40 ~ +85	-40 ~ +105	℃
Storage Temperature	Tstg	-55 ~ +125		℃
Maximum Junction Temperature	Tjmax	+125		℃

Note: Absolute maximum rating item indicates the condition which must not be exceeded.
Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more than VSS.

●Electrical characteristics

○BU7261 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7261G, BU7261SG			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*2)(*3)	Vio	25℃	–	1	9	mV	VDD=1.8 ~ 5.5[V], VOUT=VDD/2
		Full range	–	–	10		
Input Offset Current (*2)	Iio	25℃	–	1	–	pA	–
Input Bias Current (*2)	Ib	25℃	–	1	–	pA	–
Supply Current (*3)	IDD	25℃	–	250	550	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	–	–	600		
High Level Output Voltage	VOH	25℃	VDD-0.1	–	–	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	–	–	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	95	–	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	–	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	–	dB	–
Power Supply Rejection Ratio	PSRR	25℃	60	80	–	dB	–
Output Source Current (*4)	IOH	25℃	4	10	–	mA	VDD-0.4[V]
Output Sink Current (*4)	IOL	25℃	5	12	–	mA	VSS+0.4[V]
Slew Rate	SR	25℃	–	1.1	–	V/μs	CL=25[pF]
Gain Band width	FT	25℃	–	2	–	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	–	50	–	°	CL=25[pF], AV=40[dB]

(*2) Absolute value
(*3) Full range: BU7261: Ta=-40[℃] ~ +85[℃] BU7261S: Ta=-40[℃] ~ +105[℃]
(*4) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7262 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7262F/FVM/NUX BU7262S F/FVM/NUX			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*5)(*6)	Vio	25℃	—	1	9	mV	VDD=1.8 ~ 5.5[V] VOUT=VDD/2
		Full range	—	—	10		
Input Offset Current (*5)	Iio	25℃	—	1	—	pA	—
Input Bias Current (*5)	Ib	25℃	—	1	—	pA	—
Supply Current (*6)	IDD	25℃	—	550	1100	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	—	—	1200		
High Level Output Voltage	VOH	25℃	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	95	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	—	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25℃	60	80	—	dB	—
Output Source Current (*7)	IOH	25℃	4	10	—	mA	VDD-0.4[V]
Output Sink Current (*7)	IOL	25℃	5	12	—	mA	VSS+0.4[V]
Slew Rate	SR	25℃	—	1.1	—	V/μs	CL=25[pF]
Gain Band width	FT	25℃	—	2	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	—	50	—	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	—	0.05	—	%	VOUT=0.8[Vp-p], f=1[kHz]
Channel Separation	CS	25℃	—	100	—	dB	AV=40[dB]

(*5) Absolute value
(*6) Full range: BU7262: Ta=-40[℃] ~ +85[℃] BU7262S: Ta=-40[℃] ~ +105[℃]
(*7) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7264 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7264F BU7264SF Min.	Typ.	Max.	Unit	Condition
Input Offset Voltage (*8)(*9)	Vio	25℃	－	1	9	mV	VDD=1.8 ~ 5.5[V] VOUT=VDD/2
		Full range	－	-	10		
Input Offset Current (*8)	Iio	25℃	－	1	－	pA	－
Input Bias Current (*8)	Ib	25℃	－	1	－	pA	－
Supply Current (*9)	IDD	25℃	－	1100	2300	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	－	－	2800		
High Level Output Voltage	VOH	25℃	VDD-0.1	－	－	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	－	－	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	95	－	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	－	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	－	dB	－
Power Supply Rejection Ratio	PSRR	25℃	60	80	－	dB	－
Output Source Current (*10)	IOH	25℃	4	10	－	mA	VDD-0.4[V]
Output Sink Current (*10)	IOL	25℃	5	12	－	mA	VSS+0.4[V]
Slew Rate	SR	25℃	－	1.1	－	V/μs	CL=25[pF]
Gain Band width	FT	25℃	－	2	－	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	－	50	－	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	－	0.05	－	%	VOUT=0.8[Vp-p], f=1[kHz]
Channel Separation	CS	25℃	－	100	－	dB	AV=40[dB]

(*8) Absolute value
(*9) Full range: BU7264: Ta=-40[℃] ~ +85[℃] BU7264S: Ta=-40[℃] ~ +105[℃]
(*10) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7295 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7295HFV BU7295SHFV			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*11)	Vio	25℃	—	1	6	mV	—
Input Offset Current (*11)	Iio	25℃	—	1	—	pA	—
Input Bias Current (*11)	Ib	25℃	—	1	—	pA	—
Supply Current (*12)	IDD	25℃	—	150	300	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	—	—	400		
High Level Output Voltage	VOH	25℃	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	60	95	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	—	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25℃	60	80	—	dB	—
Output Source Current (*13)	IOH	25℃	4	8	—	mA	VDD-0.4[V]
Output Sink Current (*13)	IOL	25℃	9	18	—	mA	VSS+0.4[V]
Slew Rate	SR	25℃	—	1.0	—	V/μs	CL=25[pF]
Gain Band width	FT	25℃	—	1.0	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	—	60	—	°	CL=25[pF], AV=40[dB]

(*11) Absolute value
(*12) Full range: BU7295: Ta=-40[℃] ~ +85[℃] BU7295S: Ta=-40[℃] ~ +105[℃]
(*13) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7241 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7241G, BU7241SG Min.	Typ.	Max.	Unit	Condition
Input Offset Voltage (*14)(*15)	Vio	25℃	―	1	9	mV	VDD=1.8 ~ 5.5[V] VOUT=VDD/2
		Full range	―	―	10		
Input Offset Current (*14)	Iio	25℃	―	1	―	pA	―
Input Offset Current (*14)	Ib	25℃	―	1	―	pA	―
Supply Current (*15)	IDD	25℃	―	70	150	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	―	―	250		
High Level Output Voltage	VOH	25℃	VDD-0.1	―	―	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	―	―	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	95	―	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	―	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	―	dB	―
Power Supply Rejection Ratio	PSRR	25℃	60	80	―	dB	―
Output Source Current (*16)	IOH	25℃	4	10	―	mA	VDD-0.4[V]
Output Sink Current (*16)	IOL	25℃	5	12	―	mA	VSS+0.4[V]
Slew Rate	SR	25℃	―	0.4	―	V/μs	CL=25[pF]
Gain Band width	FT	25℃	―	0.9	―	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	―	50	―	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	―	0.05	―	%	VOUT=0.8[Vp-p], f=1[kHz]

(*14) Absolute value
(*15) Full range: BU7241: Ta=-40[℃] ~ +85[℃] BU7241S: Ta=-40[℃] ~ +105[℃]
(*16) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7242 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7242F/FVM/NUX BU7242S F/FVM/NUX Min.	Typ.	Max.	Unit	Condition
Input Offset Voltage (*17) (*18)	Vio	25℃	−	1	9	mV	VDD=1.8 ~ 5.5[V] VOUT=VDD/2
		Full range	−	−	10		
Input Offset Current (*17)	Iio	25℃	−	1	−	pA	−
Input Bias Current (*17)	Ib	25℃	−	1	−	pA	−
Supply Current (*18)	IDD	25℃	−	180	360	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	−	−	600		
High Level Output Voltage	VOH	25℃	VDD-0.1	−	−	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	−	−	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	95	−	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	−	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	−	dB	−
Power Supply Rejection Ratio	PSRR	25℃	60	80	−	dB	−
Output Source Current (*19)	IOH	25℃	4	10	−	mA	VDD-0.4[V]
Output Sink Current (*19)	IOL	25℃	5	12	−	mA	VSS+0.4[V]
Slew Rate	SR	25℃	−	0.4	−	V/μs	CL=25[pF]
Gain Band width	FT	25℃	−	0.9	−	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	−	50	−	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	−	0.05	−	%	VOUT=0.8[Vp-p], f=1[kHz]
Channel Separation	CS	25℃	−	100	−	dB	AV=40[dB]

(*17) Absolute value
(*18) Full range: BU7242: Ta=-40[℃] ~ +85[℃] BU7242S: Ta=-40[℃] ~ +105[℃]
(*19) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7244 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7244F BU7244SF				
			Min.	Typ.	Max.		
Input Offset Voltage (*20) (*21)	Vio	25℃	—	1	9	mV	VDD=1.8 ~ 5.5[V] VOUT=VDD/2
		Full range	—	—	10		
Input Offset Current (*20)	Iio	25℃	—	1	—	pA	—
Input Bias Current (*20)	Ib	25℃	—	1	—	pA	—
Supply Current (*21)	IDD	25℃	—	360	750	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	—	—	1200		
High Level Output Voltage	VOH	25℃	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	95	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	—	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25℃	60	80	—	dB	—
Output Source Current (*22)	IOH	25℃	4	10	—	mA	VDD-0.4[V]
Output Sink Current (*22)	IOL	25℃	5	12	—	mA	VSS+0.4[V]
Slew Rate	SR	25℃	—	0.4	—	V/μs	CL=25[pF]
Gain Band width	FT	25℃	—	0.9	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	—	50	—	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	—	0.05	—	%	VOUT=0.8[Vp-p], f=1[kHz]
Channel Separation	CS	25℃	—	100	—	dB	AV=40[dB]

(*20) Absolute value
(*21) Full range: BU7244: Ta=-40[℃] ~ +85[℃] BU7244S: Ta=-40[℃] ~ +105[℃]
(*22) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7275 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7275HFV BU7275SHFV			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*23)	Vio	25℃	–	1	6	mV	–
Input Offset Current (*23)	Iio	25℃	–	1	–	pA	–
Input Bias Current (*23)	Ib	25℃	–	1	–	pA	–
Supply Current (*24)	IDD	25℃	–	40	80	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	–	–	130		
High Level Output Voltage	VOH	25℃	VDD-0.1	–	–	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	–	–	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	60	95	–	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	–	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	–	dB	–
Power Supply Rejection Ratio	PSRR	25℃	60	80	–	dB	–
Output Source Current (*25)	IOH	25℃	4	8	–	mA	VDD-0.4[V]
Output Sink Current (*25)	IOL	25℃	9	18	–	mA	VSS+0.4[V]
Slew Rate	SR	25℃	–	0.3	–	V/μs	CL=25[pF]
Gain Band width	FT	25℃	–	0.6	–	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	–	60	–	°	CL=25[pF], AV=40[dB]

(*23) Absolute value
(*24) Full range: BU7275: Ta=-40[℃] ~ +85[℃] BU7275S: Ta=-40[℃] ~ +105[℃]
(*25) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

●Reference Data (BU7261 family)

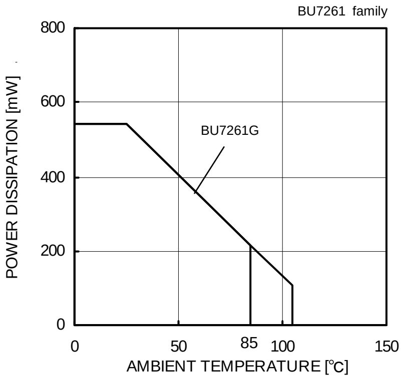


Fig.1

Derating curve

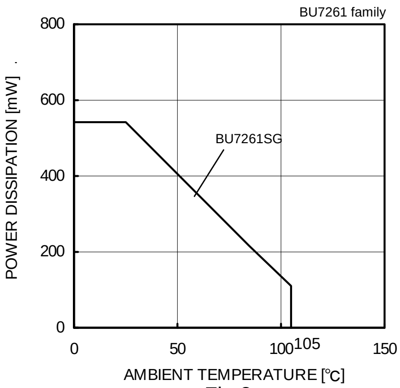


Fig.2

Derating curve

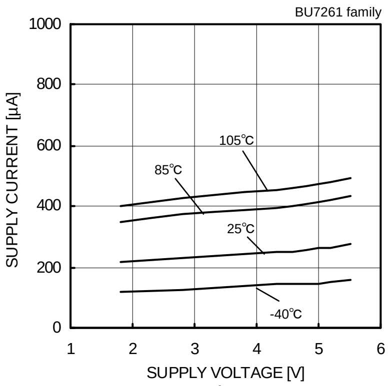


Fig.3

Supply Current – Supply Voltage

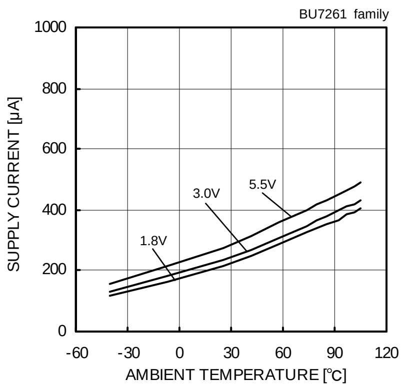


Fig.4

Supply Current – Ambient Temperature

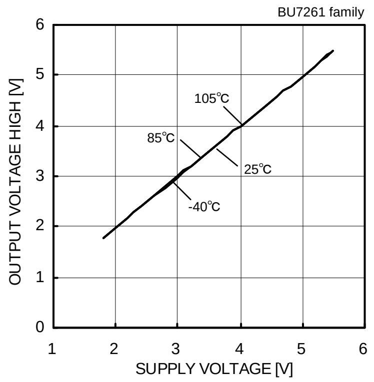


Fig.5

Output Voltage High – Supply Voltage
(RL=10[kΩ])

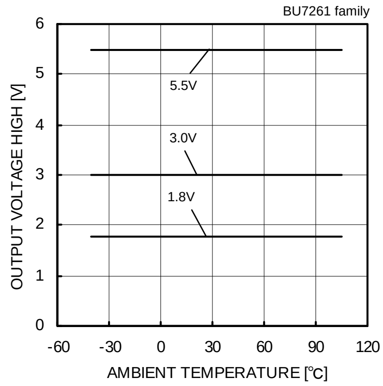


Fig.6

Output Voltage High – Ambient Temperature
(RL=10[kΩ])

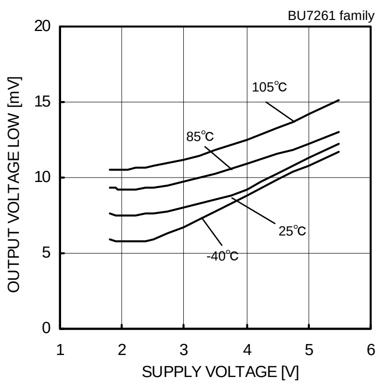


Fig.7
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

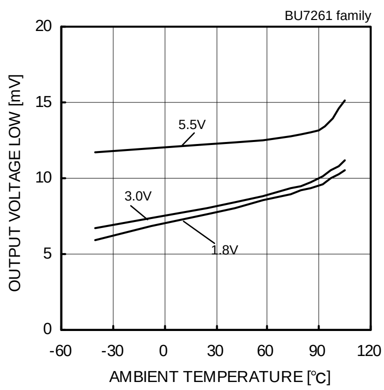


Fig.8
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

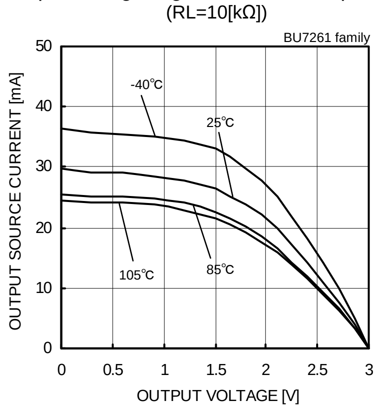


Fig.9
Output Source Current – Output Voltage
(VDD=3[V])

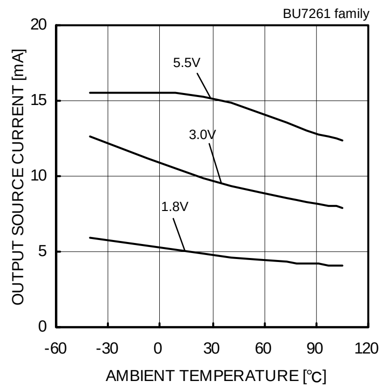


Fig.10

Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

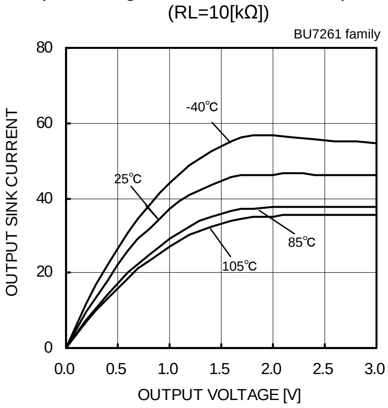


Fig.11

Output Sink Current – Output Voltage
(VDD=3[V])

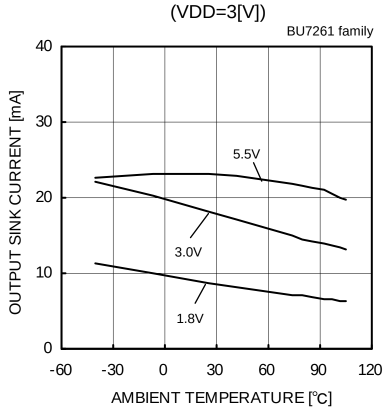


Fig.12

Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above data is ability value of sample, it is not guaranteed. BU7261G: -40[℃] ~ +85[℃]　BU7261SG: -40[℃] ~ +105[℃]

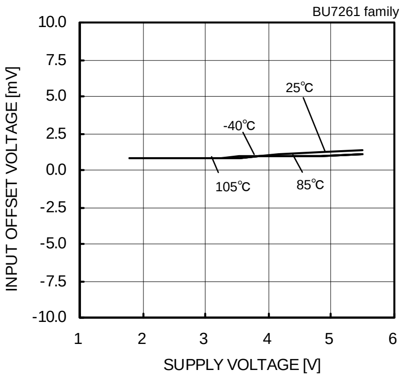


Fig.13
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

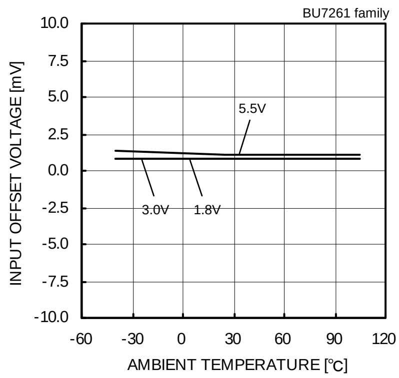


Fig.14
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

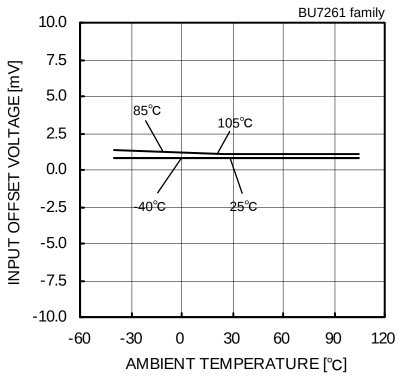


Fig.15
Input Offset Voltage – Ambient Temperature
(VDD=3[V])

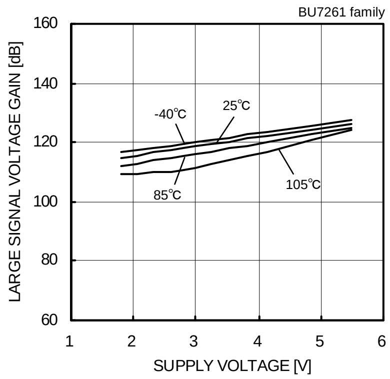


Fig.16
Large Signal Voltage Gain
– Supply Voltage

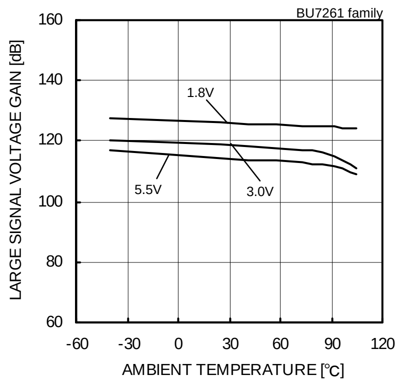


Fig.17
Large Signal Voltage Gain
– Ambient Temperature

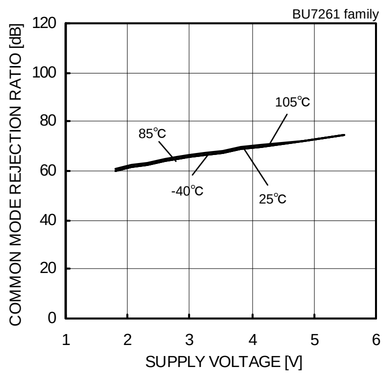


Fig.18
Common Mode Rejection Ratio
– Supply Voltage

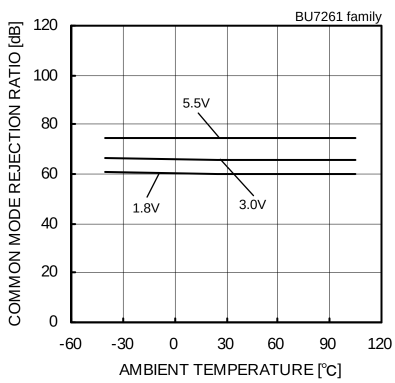


Fig.19
Common Mode Rejection Ratio
– Ambient Temperature

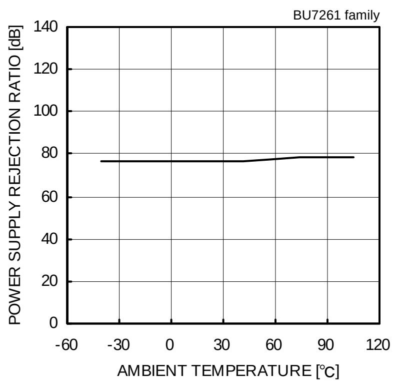


Fig.20
Power Supply Rejection Ratio
– Ambient Temperature

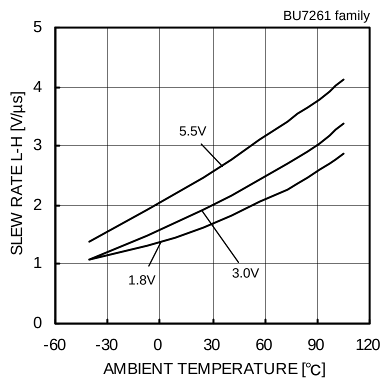


Fig.21
Slew Rate L-H – Ambient Temperature

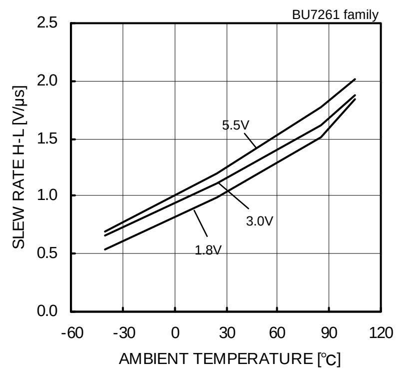


Fig.22
Slew Rate H-L – Ambient Temperature

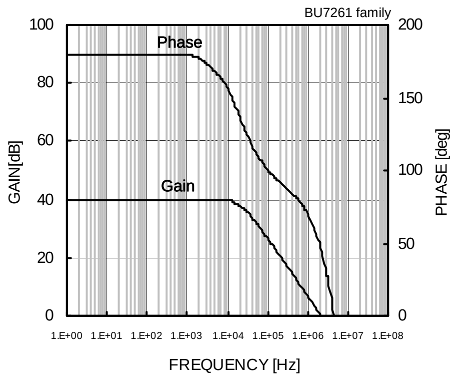


Fig.23
Voltage Gain – Frequency

(*) The above data is ability value of sample, it is not guaranteed. BU7261G: -40[℃] ~ +85[℃] BU7261SG: -40[℃] ~ +105[℃]

●Reference Data (BU7262 family)

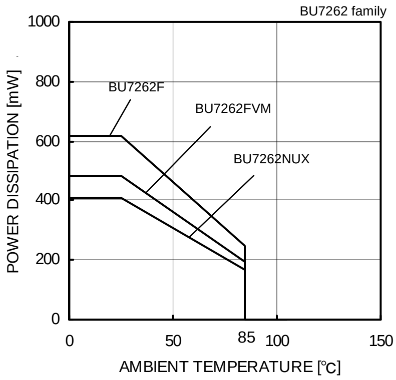


Fig.24

Derating curve

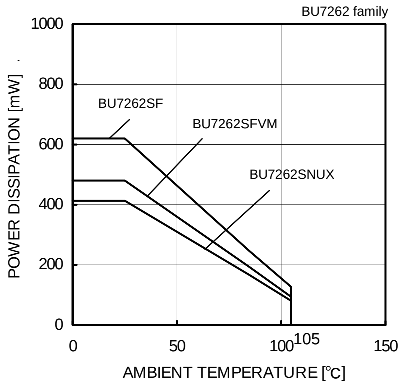


Fig.25

Derating curve

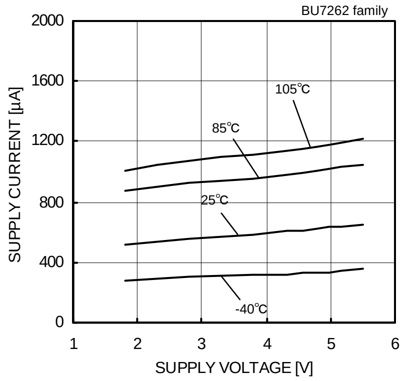


Fig.26

Supply Current – Supply Voltage

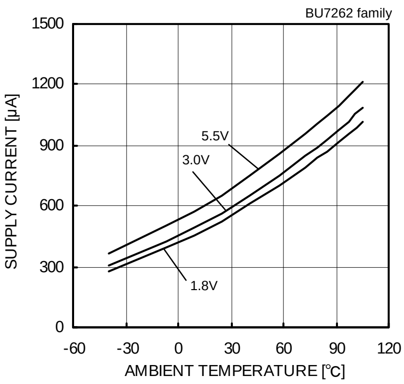


Fig.27

Supply Current – Ambient Temperature

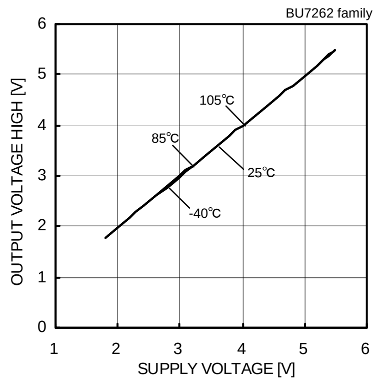


Fig.28

Output Voltage High – Supply Voltage

(RL=10[kΩ])

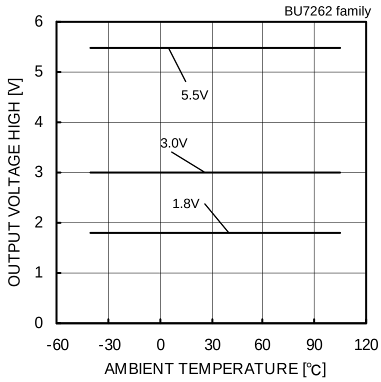


Fig.29

Output Voltage High – Ambient Temperature

(RL=10[kΩ])

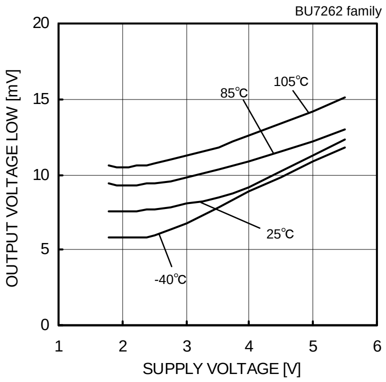


Fig.30

Output Voltage Low – Supply Voltage

(RL=10[kΩ])

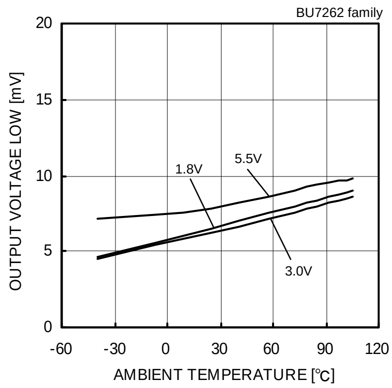


Fig.31

Output Voltage Low – Ambient Temperature

(RL=10[kΩ])

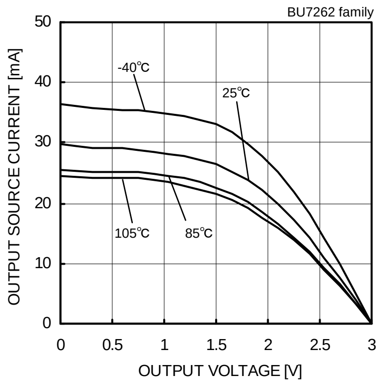


Fig.32

Output Source Current – Output Voltage

(VDD=3.0[V])

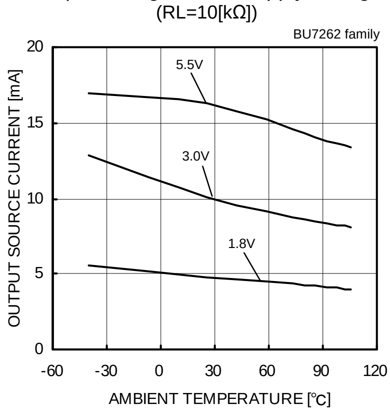


Fig.33

Output Source Current – Ambient Temperature

(VOUT=VDD-0.4[V])

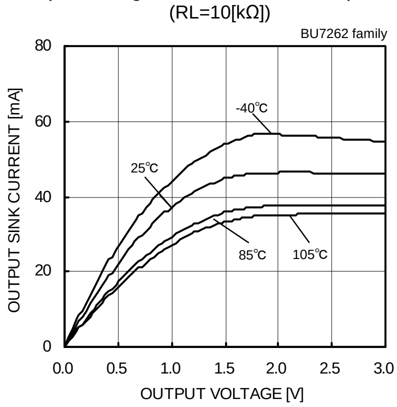


Fig.34

Output Sink Current – Output Voltage

(VDD=3[V])

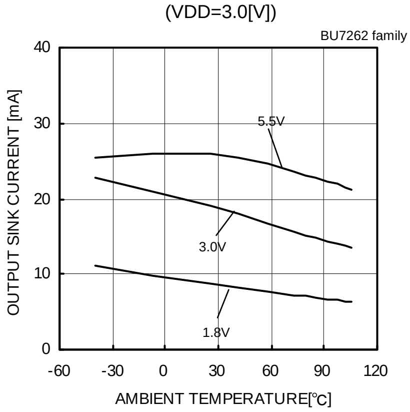


Fig.35

Output Sink Current – Ambient Temperature

(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7262F/FVM/NUX: -40[℃] ~ +85[℃] BU7262S F/FVM/NUX: -40[℃] ~ +105[℃]

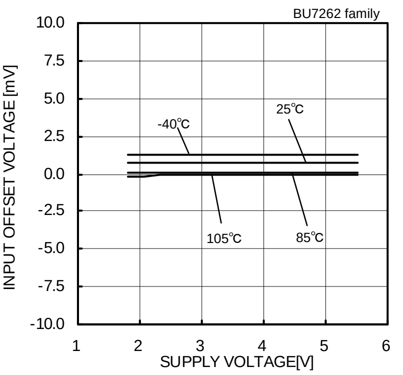


Fig.36
Input Offset Voltage – Supply Voltage
(Vicm=VDD,VOUT=1.5[V])

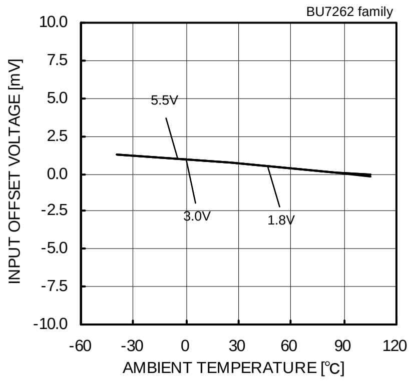


Fig.37
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

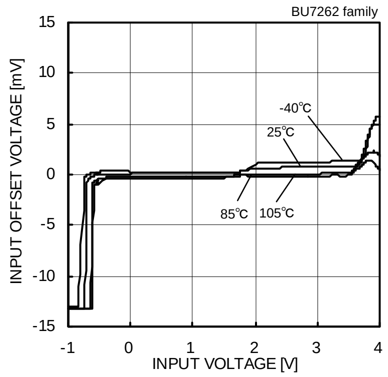


Fig.38
Input Offset Voltage – Input Voltage
(VDD=3[V])

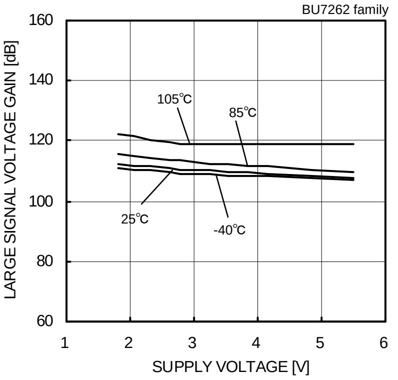


Fig.39
Large Signal Voltage Gain
– Supply Voltage

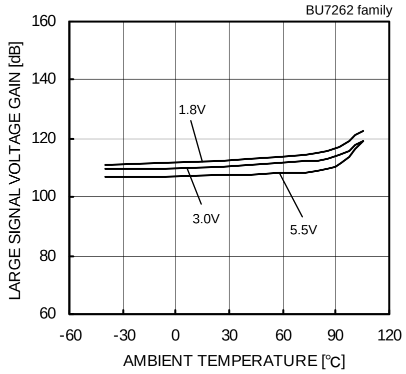


Fig.40
Large Signal Voltage Gain
– Ambient Temperature

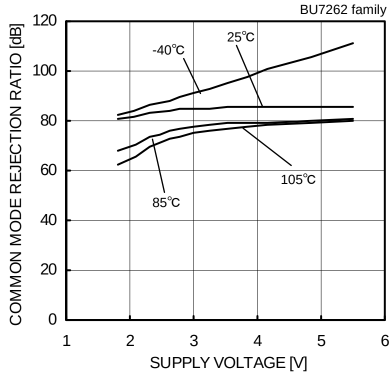


Fig.41
Common Mode Rejection Ratio
– Supply Voltage

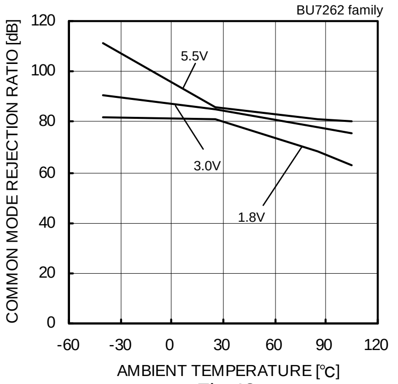


Fig.42
Common Mode Rejection Ratio
– Ambient Temperature

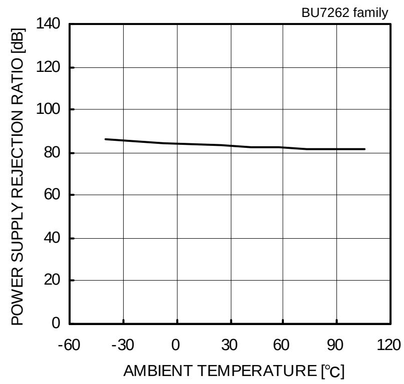


Fig.43
Power Supply Rejection Ratio
– Ambient Temperature

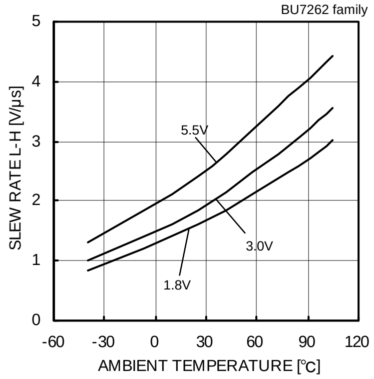


Fig.44
Slew Rate L-H – Ambient Temperature

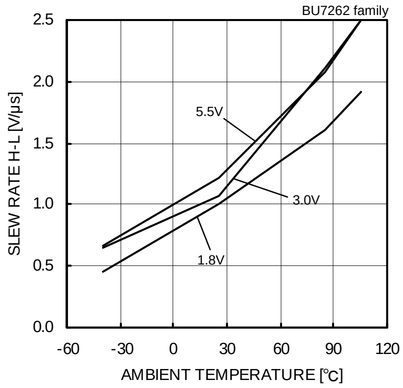


Fig.45
Slew Rate H-L – Ambient Temperature

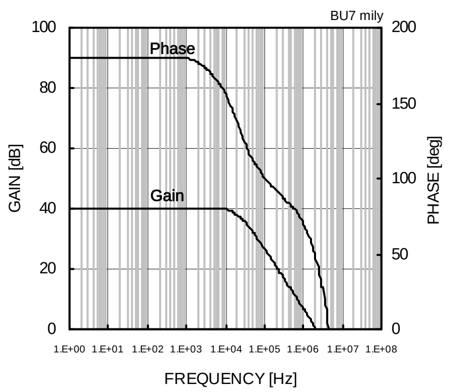


Fig.46
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7262F/FVM/NUX: -40[℃] ~ +85[℃] BU7262S F/FVM/NUX: -40[℃] ~ +105[℃]

●Reference Data (BU7264 family)

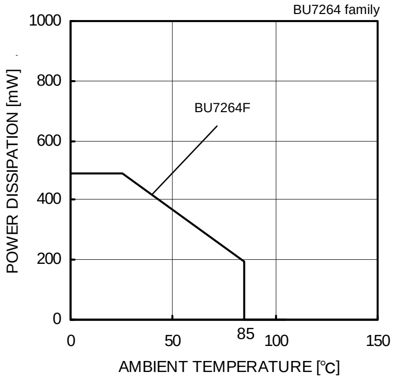


Fig.47
Derating curve

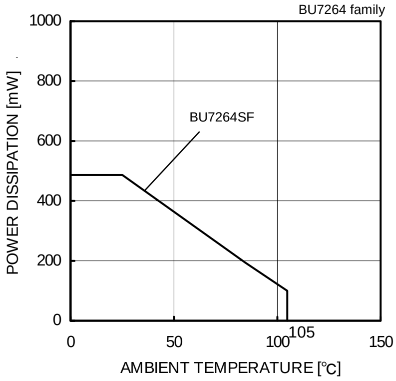


Fig.48
Derating curve

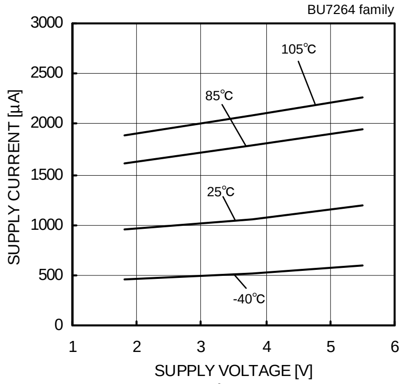


Fig.49
Supply Current – Supply Voltage

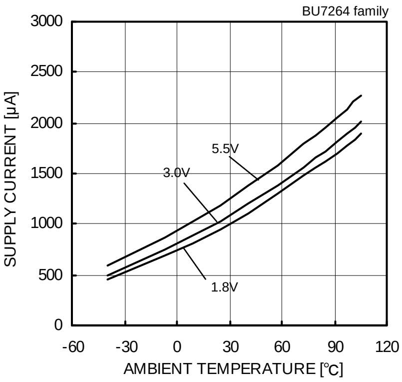


Fig.50
Supply Current – Ambient Temperature

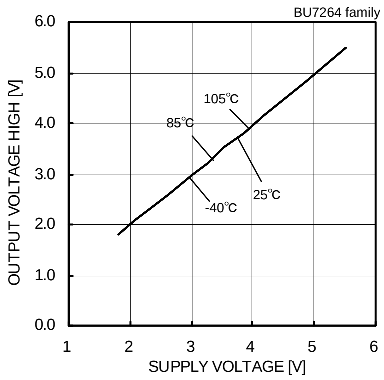


Fig.51
Output Voltage High – Supply Voltage
(RL=10[kΩ])

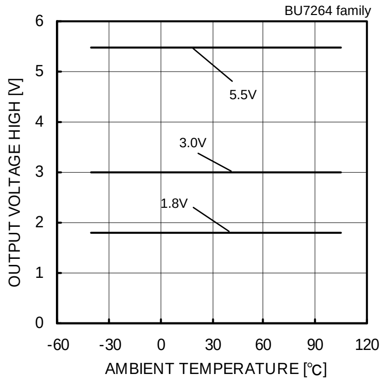


Fig.52
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

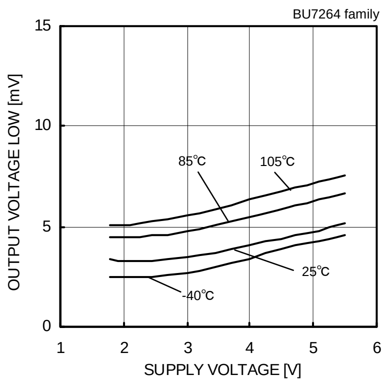


Fig.53
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

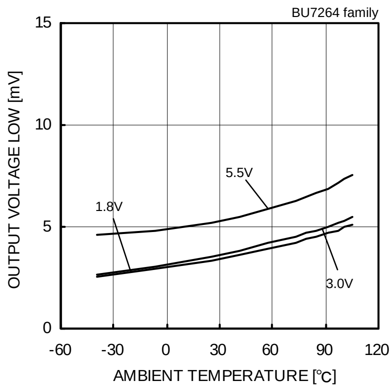


Fig.54
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

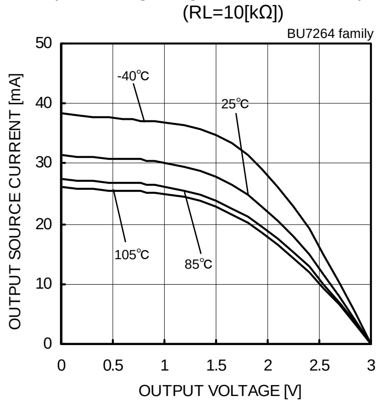


Fig.55
Output Source Current – Output Voltage
(VDD=3[V])

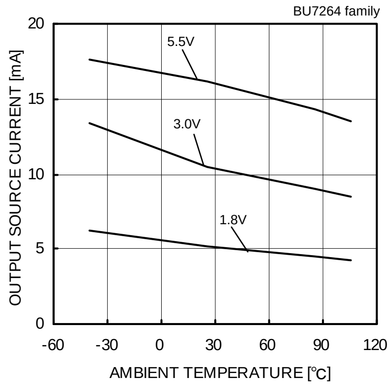


Fig.56
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

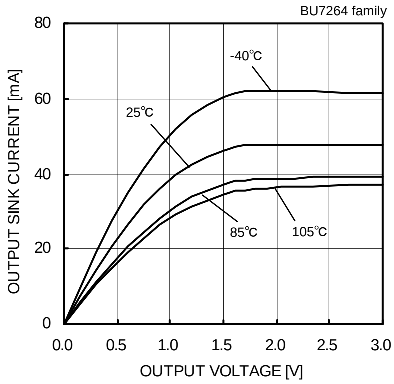


Fig.57
Output Sink Current – Output Voltage
(VDD=3[V])

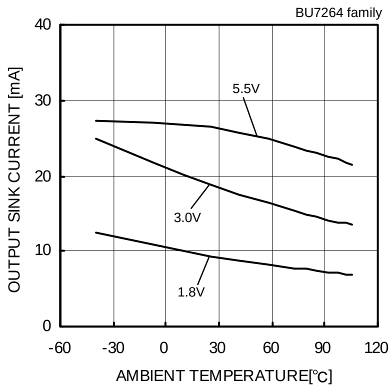


Fig.58
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7264F: -40[℃] ~ +85[℃] BU7264SF: -40[℃] ~ +105[℃]

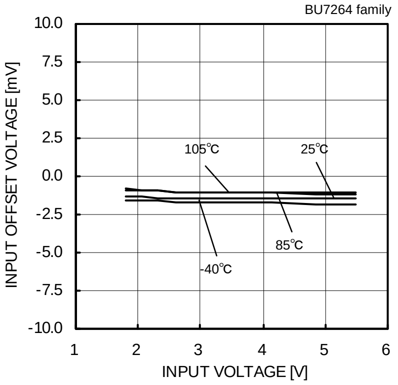


Fig.59

Input Offset Voltage – Supply Voltage
(Vicm=VDD,VOUT=1.5[V])

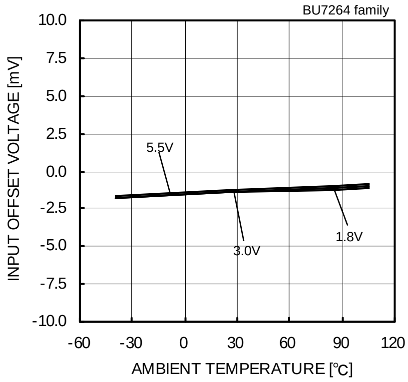


Fig.60

Input Offset Voltage – Ambient Temperature
(Vicm=VDD,VOUT=1.5[V])

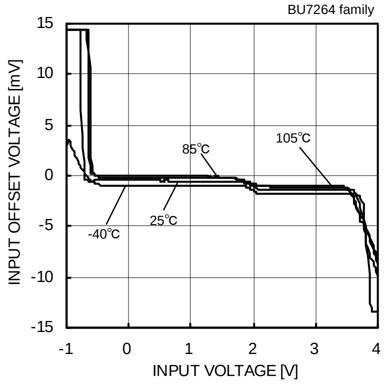


Fig.61

Input Offset Voltage – Input Voltage
(VDD=3[V])

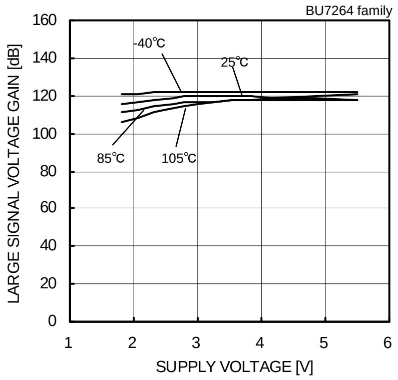


Fig.62

Large Signal Voltage Gain
– Supply Voltage

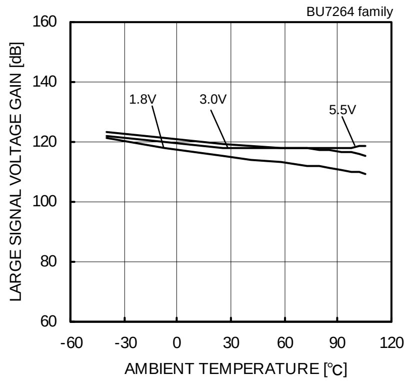


Fig.63

Large Signal Voltage Gain
– Ambient Temperature

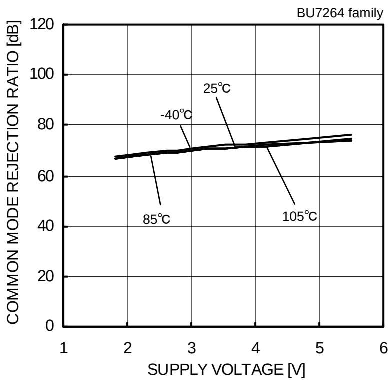


Fig.64

Common Mode Rejection Ratio
– Supply Voltage

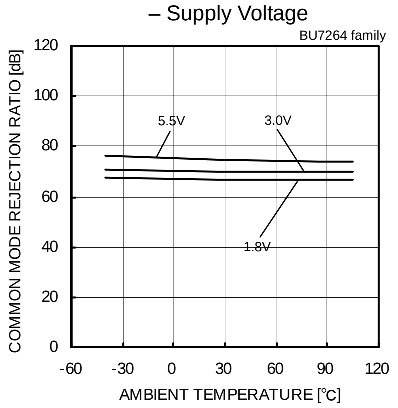


Fig.65

Common Mode Rejection Ratio
– Ambient Temperature

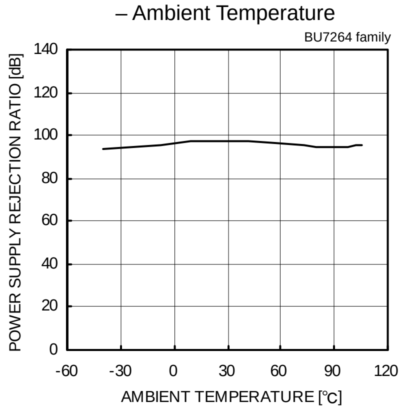


Fig.66

Power Supply Rejection Ratio
– Ambient Temperature

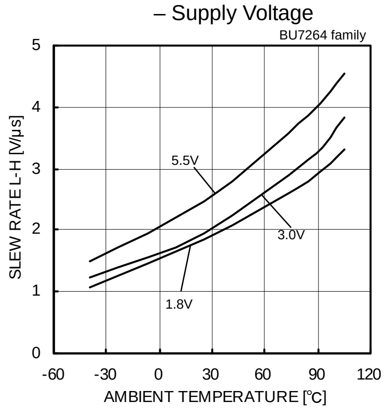


Fig.67

Slew Rate L-H – Ambient Temperature

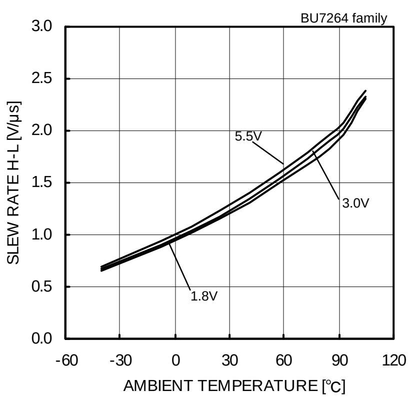


Fig.68

Slew Rate H-L – Ambient Temperature

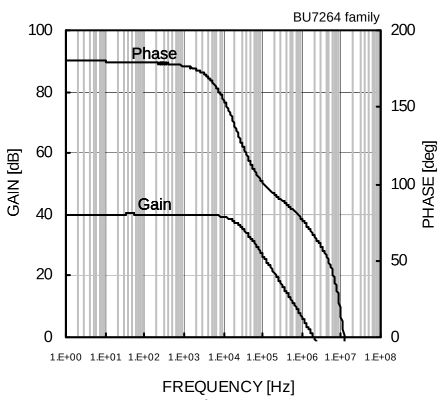


Fig.69

Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7264F: -40[℃] ~ +85[℃] BU7264SF: -40[℃] ~ +105[℃]

●Reference Data (BU7295 family)

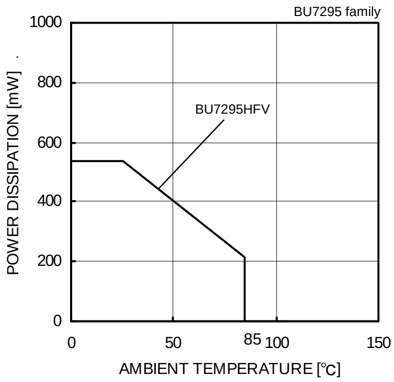


Fig.70

Derating curve

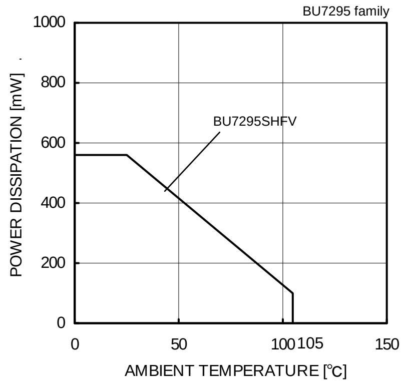


Fig.71

Derating curve

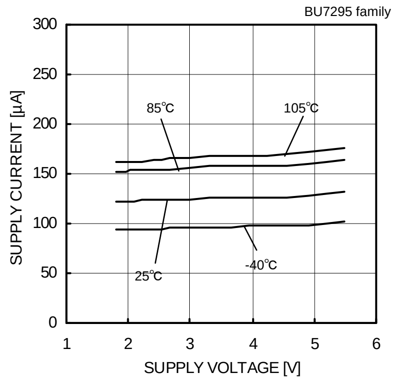


Fig.72

Supply Current – Supply Voltage

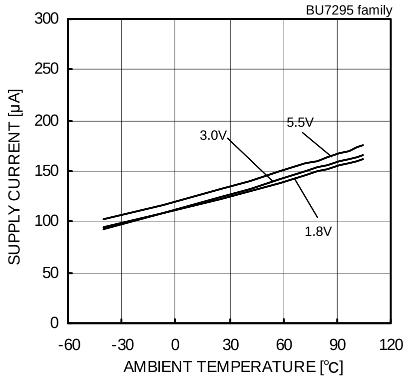


Fig.73

Supply Current – Ambient Temperature

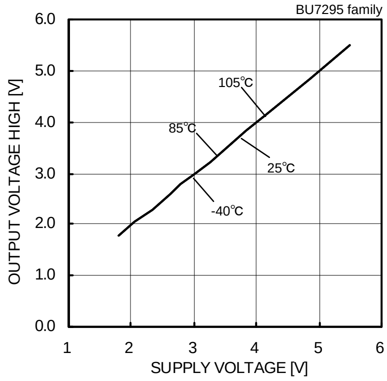


Fig.74

Output Voltage High – Supply Voltage

(RL=10[kΩ])

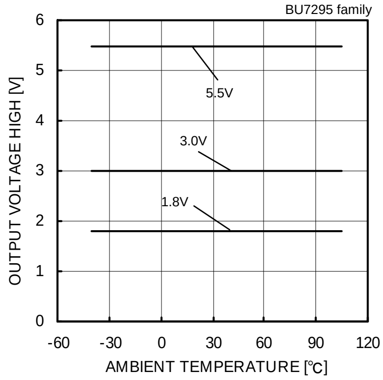


Fig.75

Output Voltage High – Ambient Temperature

(RL=10[kΩ])

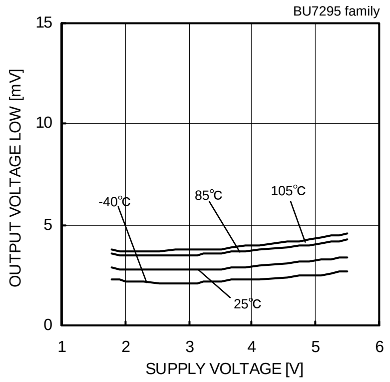


Fig.76

Output Voltage Low – Supply Voltage

(RL=10[kΩ])

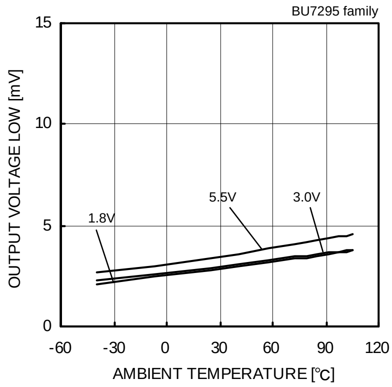


Fig.77

Output Voltage Low – Ambient Temperature

(RL=10[kΩ])

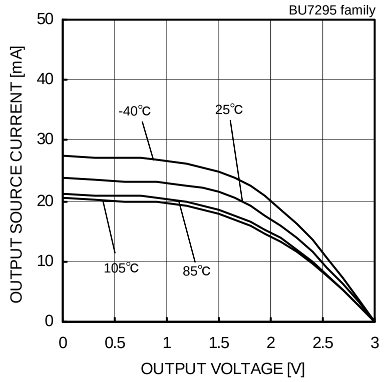


Fig.78

Output Source Current – Output Voltage

(VDD=3[V])

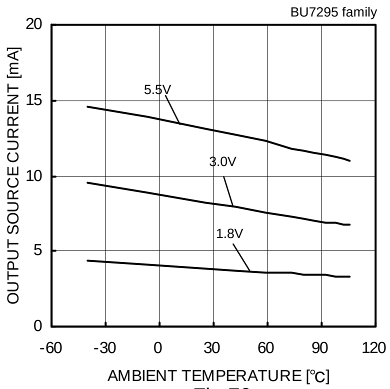


Fig.79

Output Source Current – Ambient Temperature

(VOUT=VDD-0.4[V])

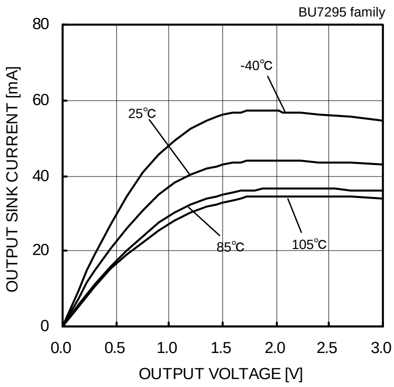


Fig.80

Output Sink Current – Output Voltage

(VDD=3[V])

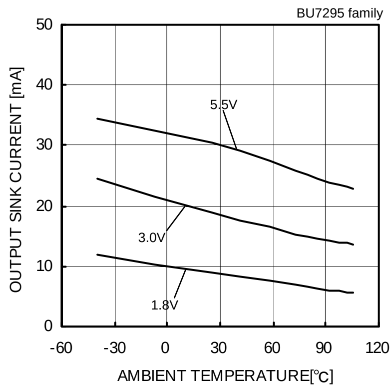


Fig.81

Output Sink Current – Ambient Temperature

(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7295HFV: -40[℃] ~ +85[℃] BU7295SHFV: -40[℃] ~ +105[℃]

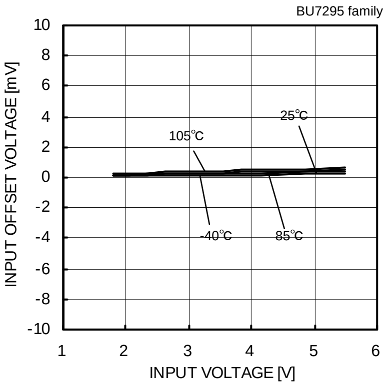


Fig.82
Input Offset Voltage – Supply Voltage
(Vicm=VDD,VOUT=1.5[V])

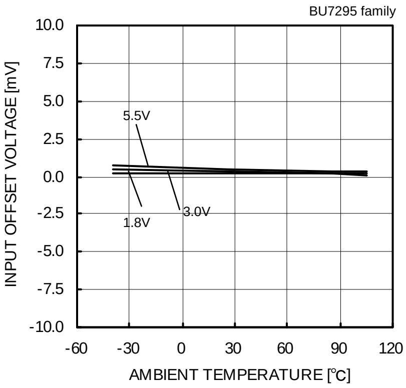


Fig.83
Input Offset Voltage – Ambient Temperature
(Vicm=VDD,VOUT=1.5[V])

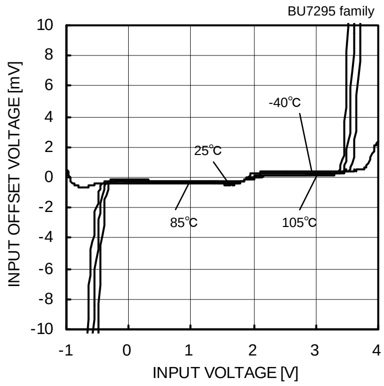


Fig.84
Input Offset Voltage – Input Voltage
(VDD=3[V])

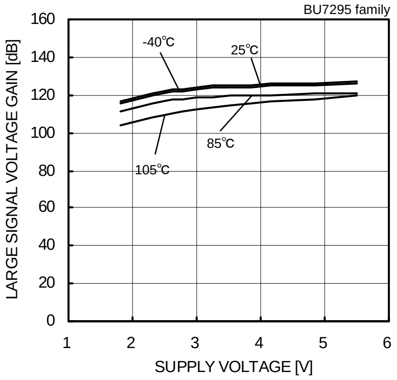


Fig.85
Large Signal Voltage Gain
– Supply Voltage

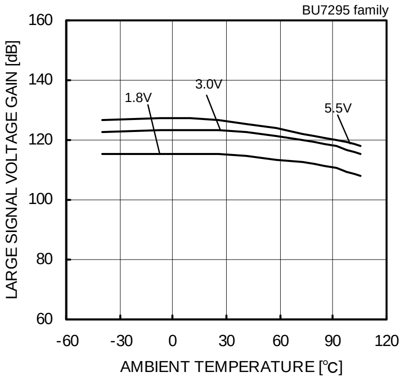


Fig.86
Large Signal Voltage Gain
– Ambient Temperature

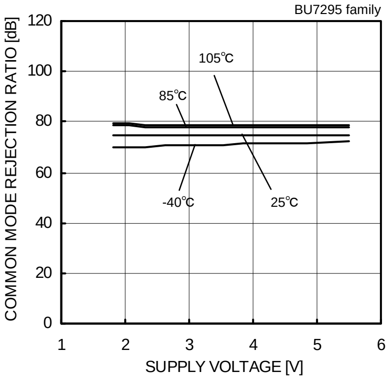


Fig.87
Common Mode Rejection Ratio
– Supply Voltage

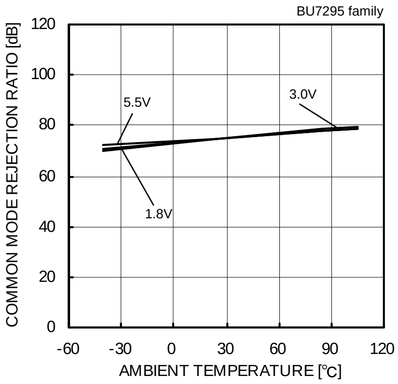


Fig.88
Common Mode Rejection Ratio
– Ambient Temperature

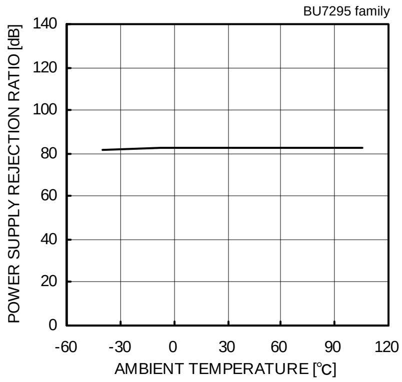


Fig.89
Power Supply Rejection Ratio
– Ambient Temperature

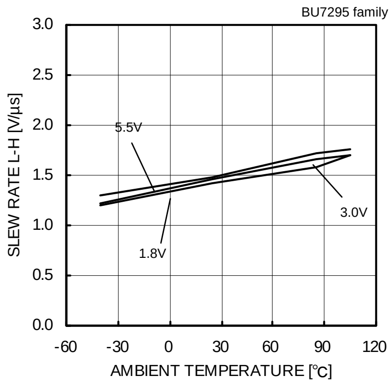


Fig.90
Slew Rate L-H – Ambient Temperature

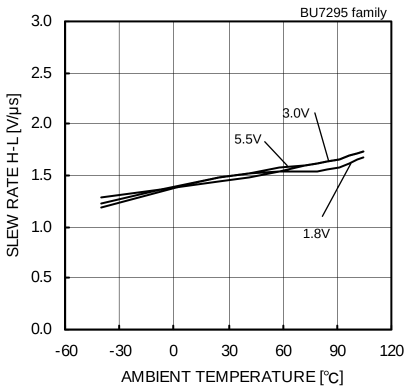


Fig.91

Slew Rate H-L – Ambient Temperature

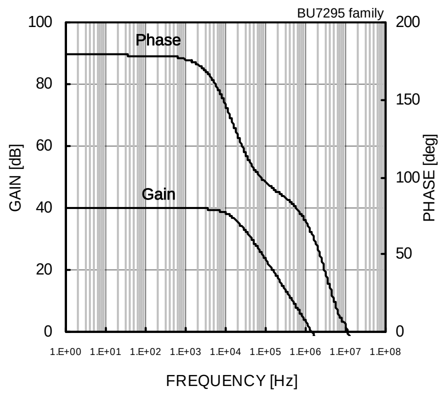


Fig.92

Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7295HFV: -40[℃] ~ +85[℃] BU7295SHFV: -40[℃] ~ +105[℃]

●Reference Data (BU7241 family)

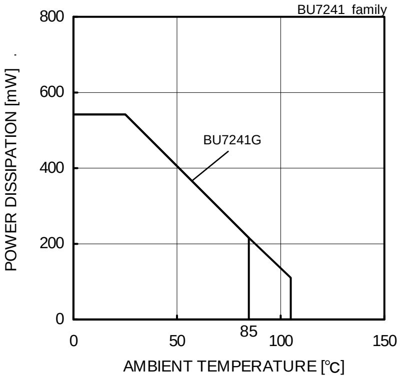


Fig.93
Derating curve

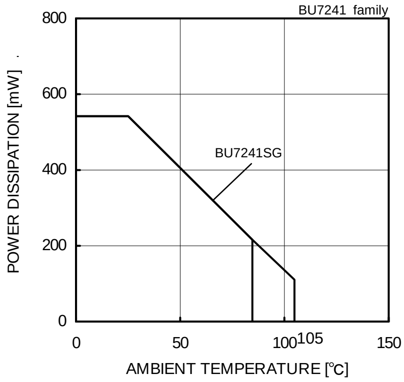


Fig.94
Derating curve

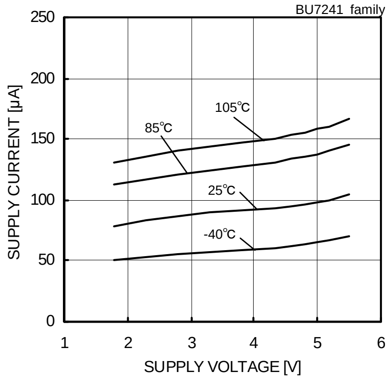


Fig.95
Supply Current – Supply Voltage

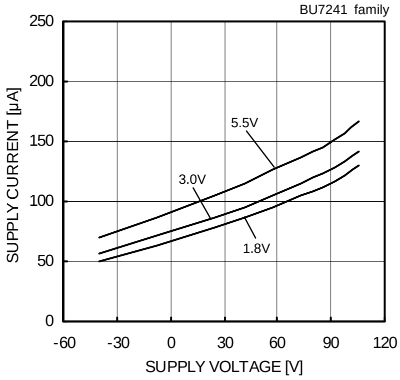


Fig.96
Supply Current – Ambient Temperature

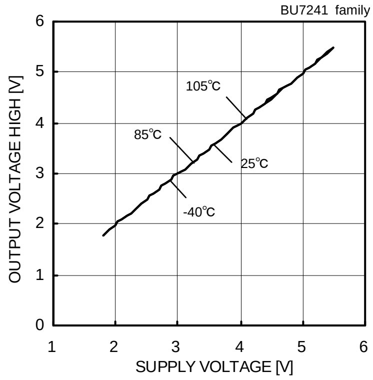


Fig.97
Output Voltage High – Supply Voltage
(RL=10[kΩ])

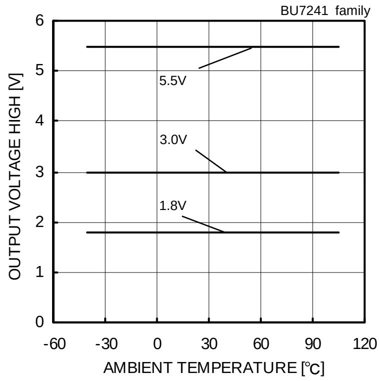


Fig.98
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

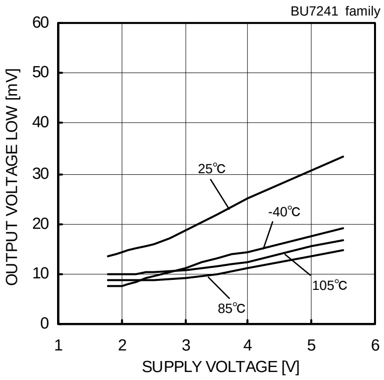


Fig.99
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

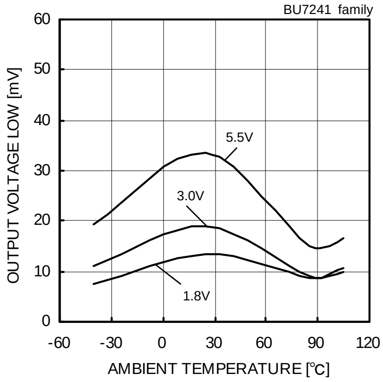


Fig.100
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

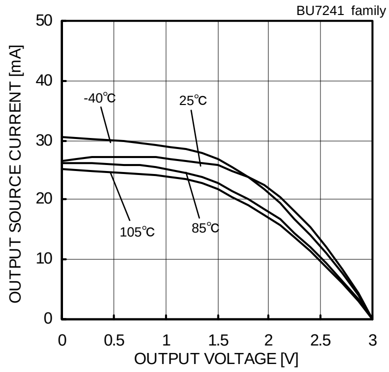


Fig.101
Output Source Current – Output Voltage
(VDD=3[V])

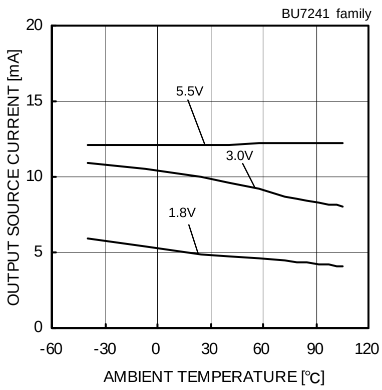


Fig.102
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

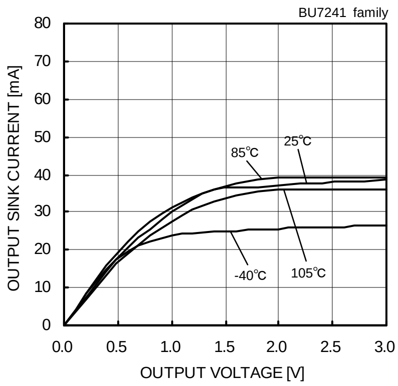


Fig.103
Output Sink Current – Output Voltage
(VDD=3[V])

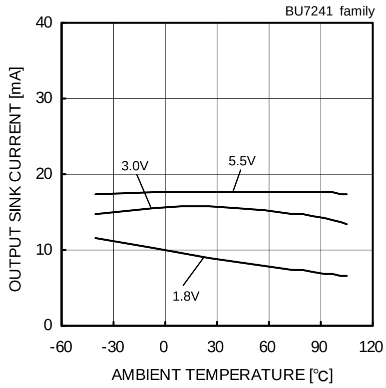


Fig.104
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7241G: -40[℃] ~ +85[℃] BU7241SG: -40[℃] ~ +105[℃]

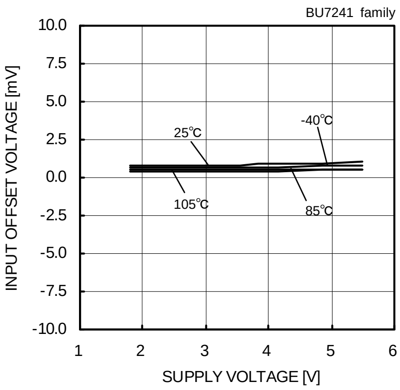


Fig.105
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

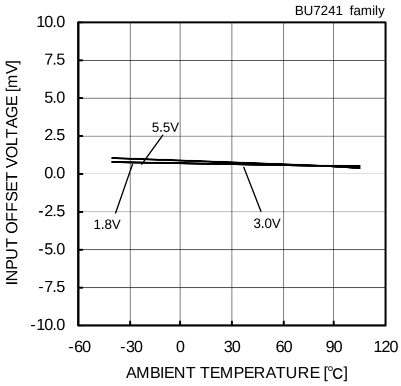


Fig.106
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

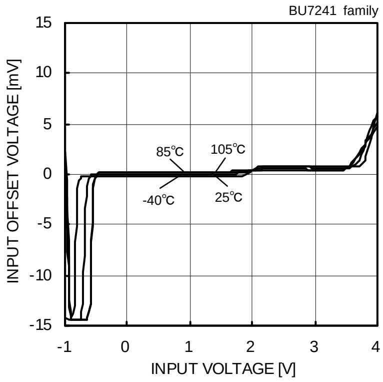


Fig.107
Input Offset Voltage – Input Voltage
(VDD=3[V])

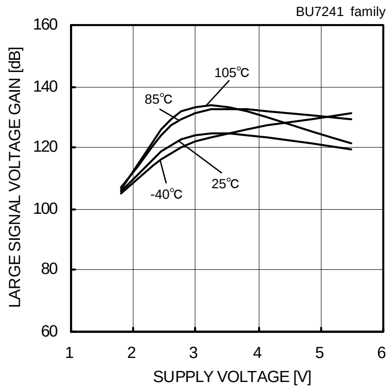


Fig.108
Large Signal Voltage Gain
– Supply Voltage

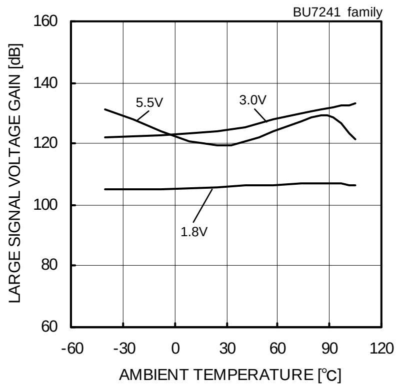


Fig.109
Large Signal Voltage Gain
– Ambient Temperature

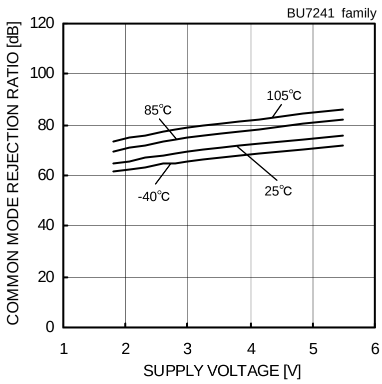


Fig.110
Common Mode Rejection Ratio
– Supply Voltage

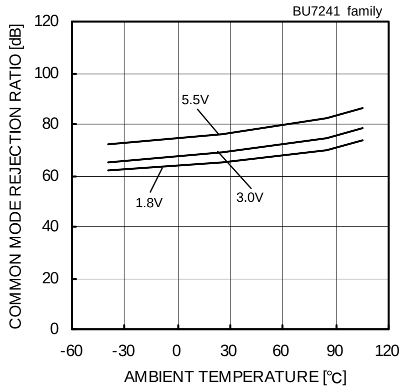


Fig.111
Common Mode Rejection Ratio
– Ambient Temperature

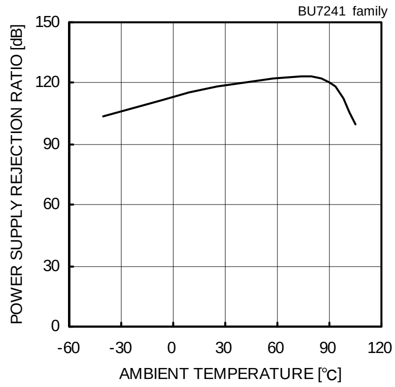


Fig.112
Power Supply Rejection Ratio
– Ambient Temperature

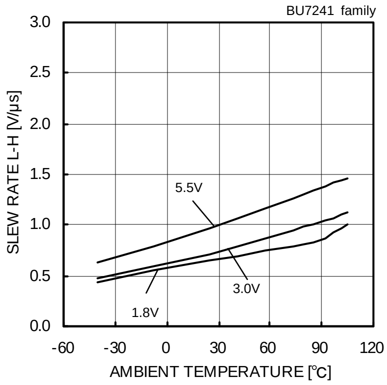


Fig.113
Slew Rate L-H – Ambient Temperature

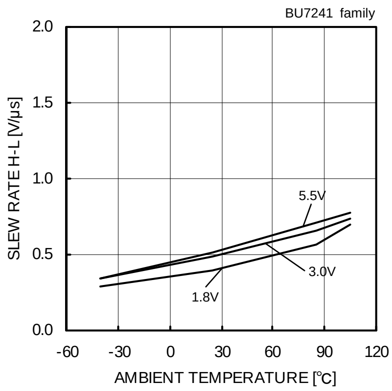


Fig.114
Slew Rate H-L – Ambient Temperature

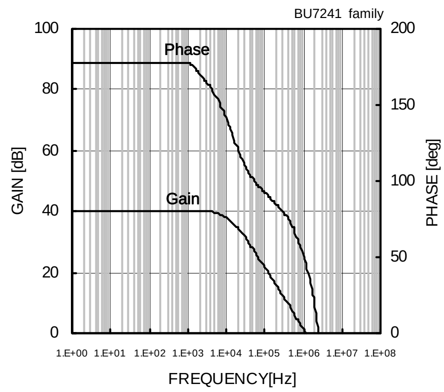


Fig.115
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7241G: -40[℃] ~ +85[℃] BU7241SG: -40[℃] ~ +105[℃]

●Reference Data (BU7242 family)

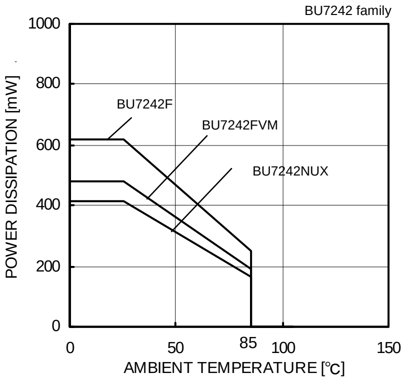


Fig.116

Derating curve

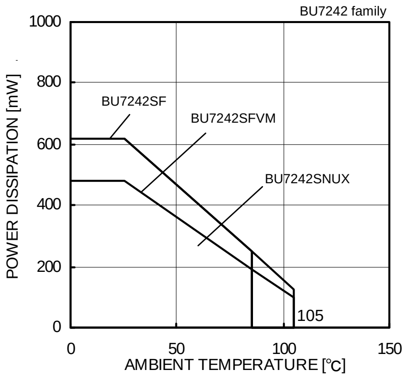


Fig.117

Derating curve

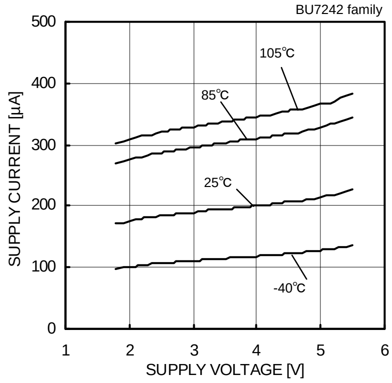


Fig.118

Supply Current – Supply Voltage

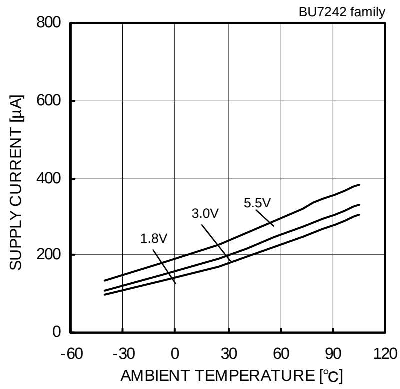


Fig.119

Supply Current – Ambient Temperature

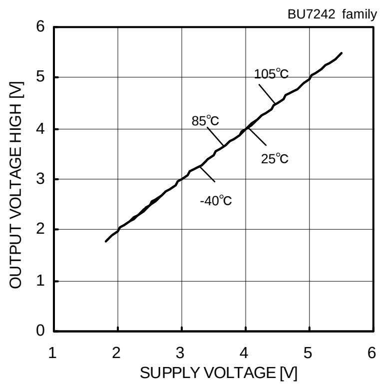


Fig.120

Output Voltage High – Supply Voltage
(RL=10[kΩ])

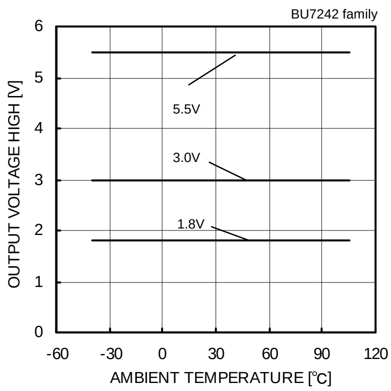


Fig.121

Output Voltage High – Ambient Temperature
(RL=10[kΩ])

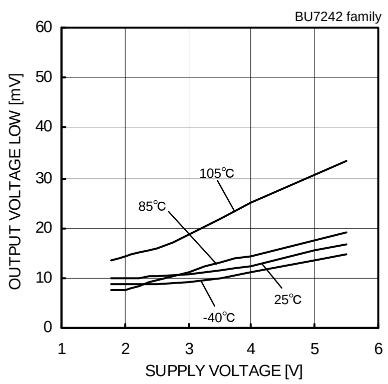


Fig.122

Output Voltage Low – Supply Voltage
(RL=10[kΩ])

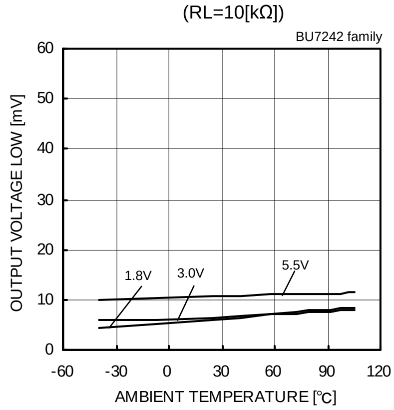


Fig.123

Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

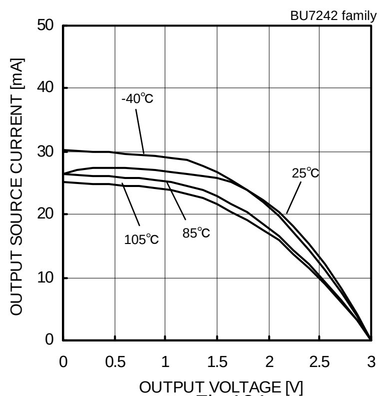


Fig.124

Output Source Current – Output Voltage
(VDD=3[V])

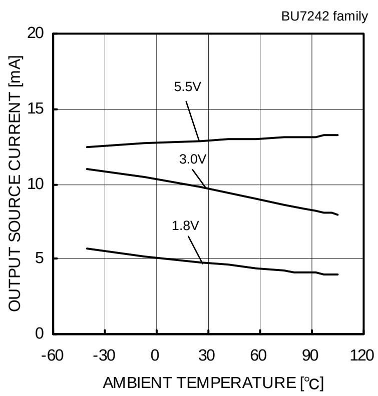


Fig.125

Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

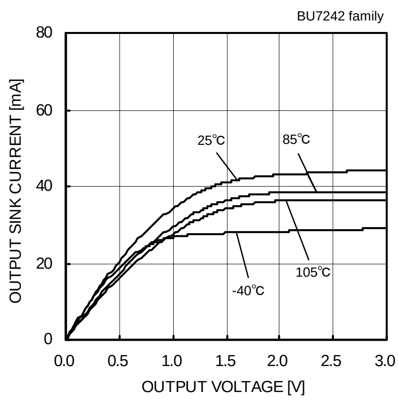


Fig.126

Output Sink Current – Output Voltage
(VDD=3[V])

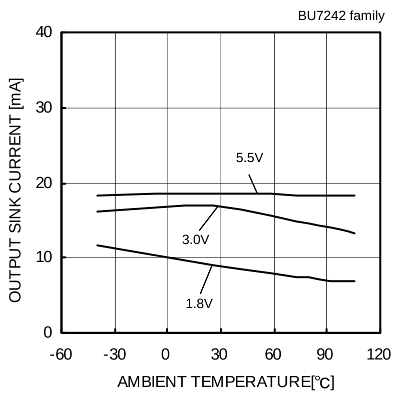


Fig.127

Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7242F/FVM/NUX: -40[℃] ~ +85[℃] BU7242S F/FVM/NUX: -40[℃] ~ +105[℃]

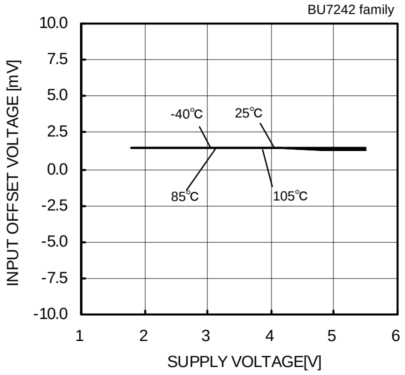


Fig.128
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

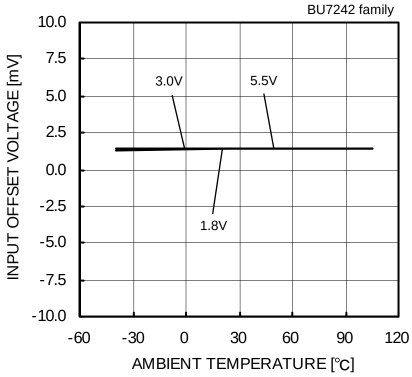


Fig.129
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

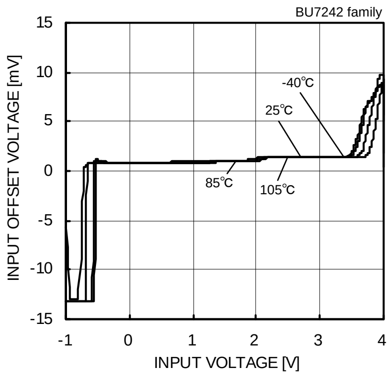


Fig.130
Input Offset Voltage – Input Voltage
(VDD=3[V])

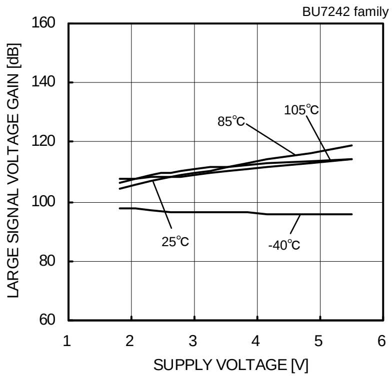


Fig.131
Large Signal Voltage Gain
– Supply Voltage

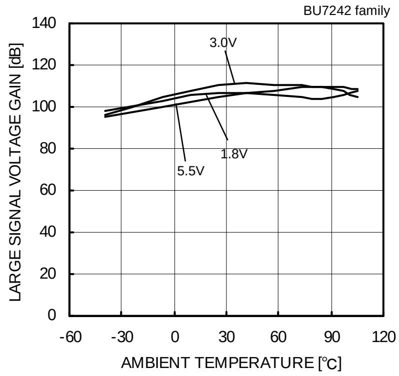


Fig.132
Large Signal Voltage Gain
– Ambient Temperature

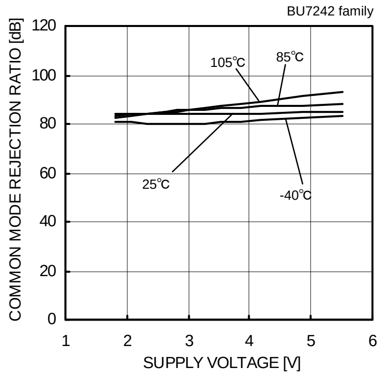


Fig.133
Common Mode Rejection Ratio
– Supply Voltage

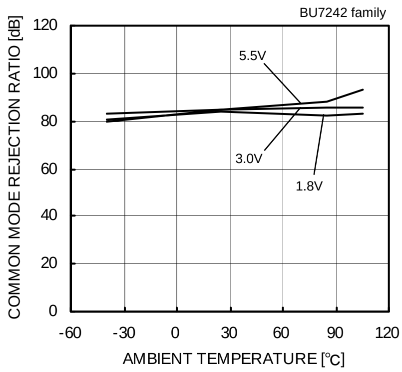


Fig.134
Common Mode Rejection Ratio
– Ambient Temperature

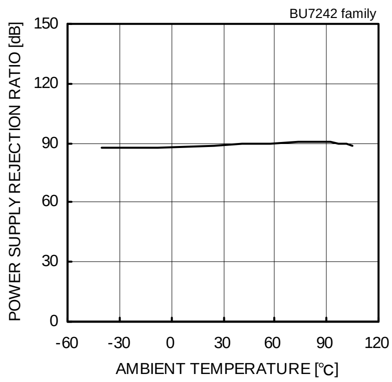


Fig.135
Power Supply Rejection Ratio
– Ambient Temperature

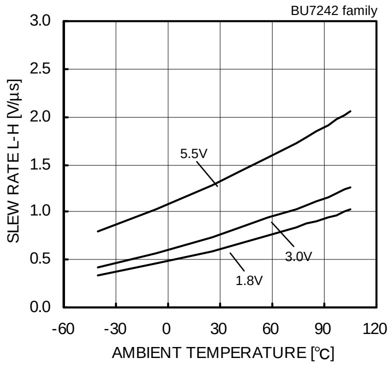


Fig.136
Slew Rate L-H – Ambient Temperature

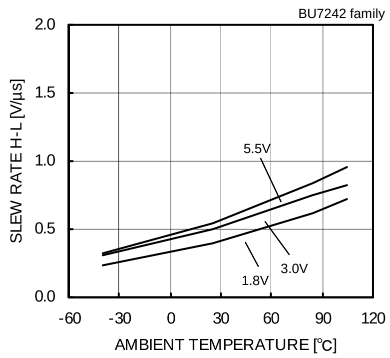


Fig.137
Slew Rate H-L – Ambient Temperature

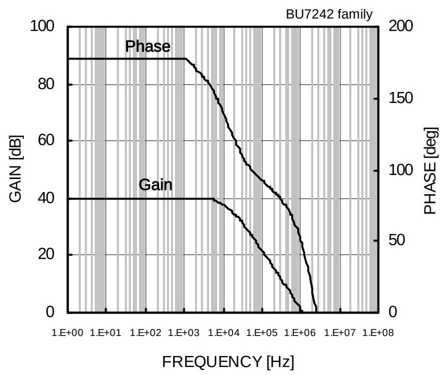


Fig.138
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7242F/FVM/NUX: -40[℃] ~ +85[℃] BU7242S F/FVM/NUX: -40[℃] ~ +105[℃]

●Reference Data (BU7244 family)

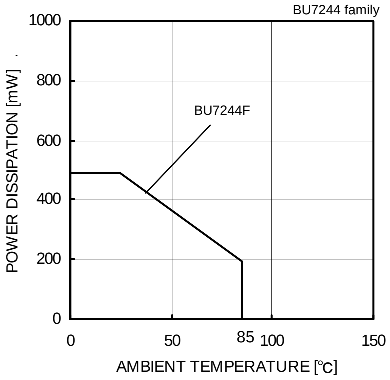


Fig.139
Derating curve

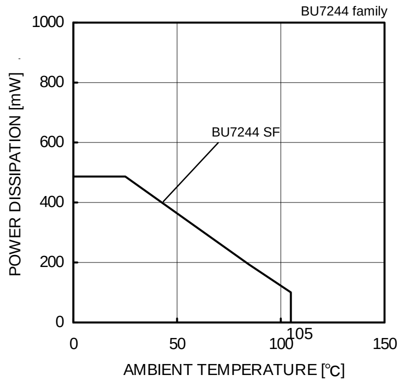


Fig.140
Derating curve

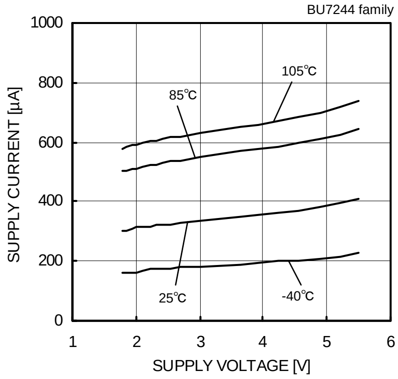


Fig.141
Supply Current – Supply Voltage

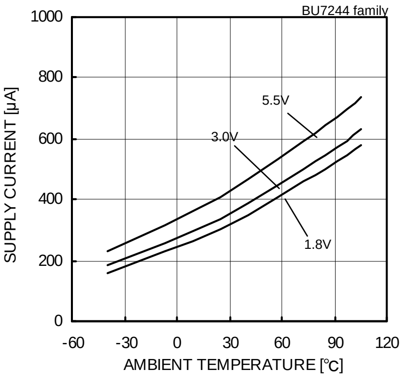


Fig.142
Supply Current – Supply Voltage

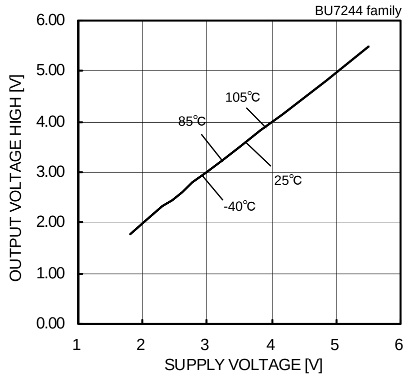


Fig.143
Output Voltage High – Supply Voltage
(RL=10[kΩ])

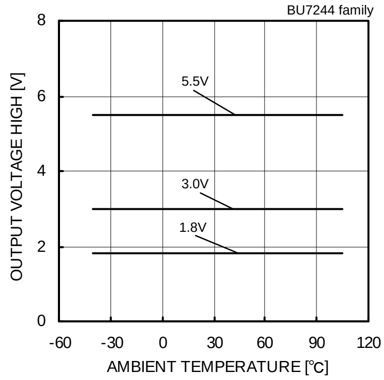


Fig.144
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

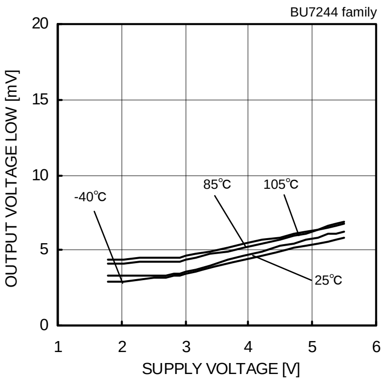


Fig.145
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

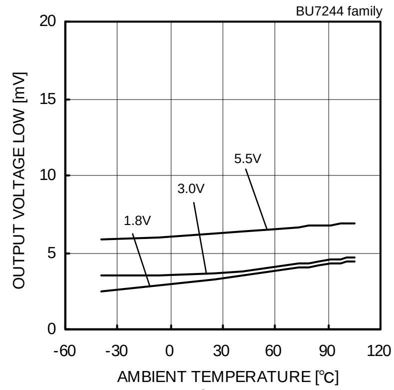


Fig.146
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

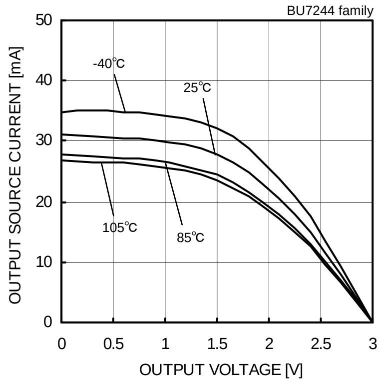


Fig.147
Output Source Current – Output Voltage
(VDD=3[V])

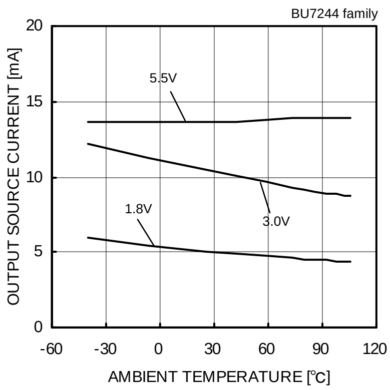


Fig.148
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

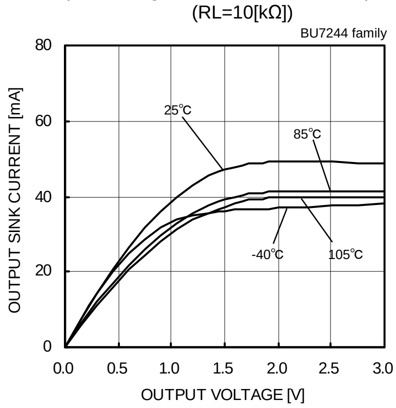


Fig.149
Output Sink Current – Output Voltage
(VDD=3[V])

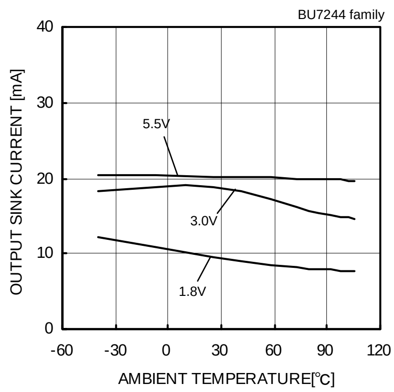


Fig.150
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7244F: -40[℃] ~ +85[℃] BU7244SF: -40[℃] ~ +105[℃]

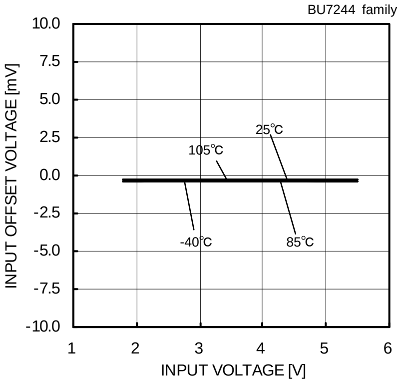


Fig.151

Input Offset Voltage – Supply Voltage
(Vicm=VDD,VOUT=1.5[V])

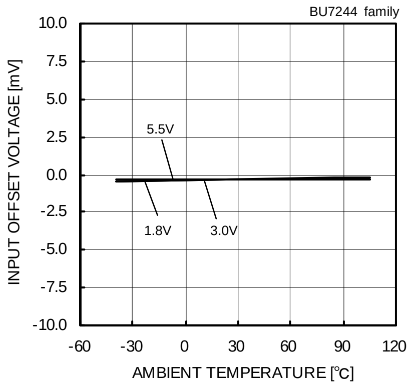


Fig.152

Input Offset Voltage – Ambient Temperature
(Vicm=VDD,VOUT=1.5[V])

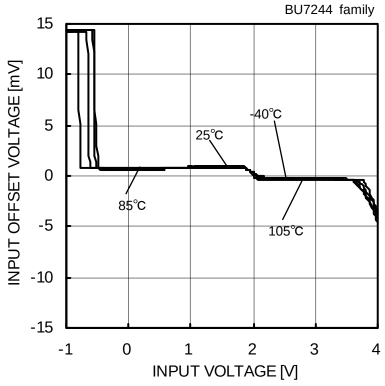


Fig.153

Input Offset Voltage – Input Voltage
(VDD=3[V])

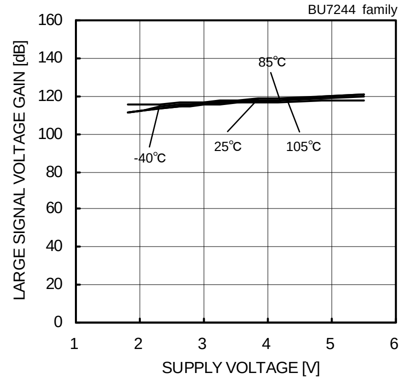


Fig.154

Large Signal Voltage Gain
– Supply Voltage

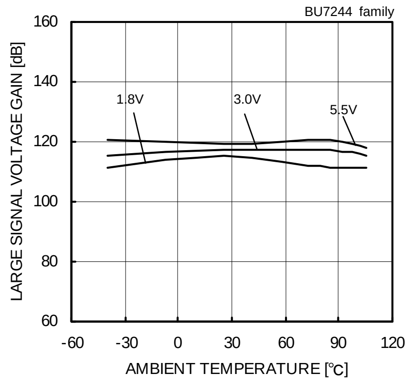


Fig.155

Large Signal Voltage Gain
– Ambient Temperature

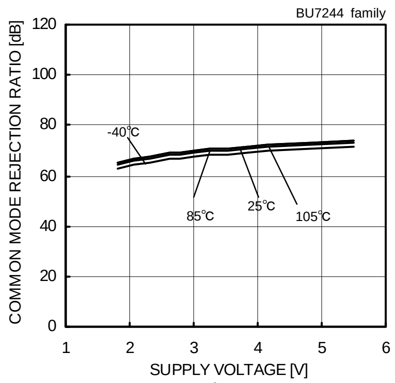


Fig.156

Common Mode Rejection Ratio
– Supply Voltage

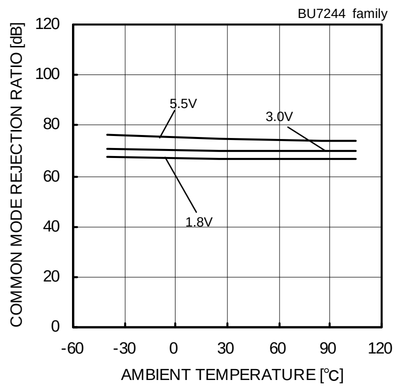


Fig.157

Common Mode Rejection Ratio
– Ambient Temperature

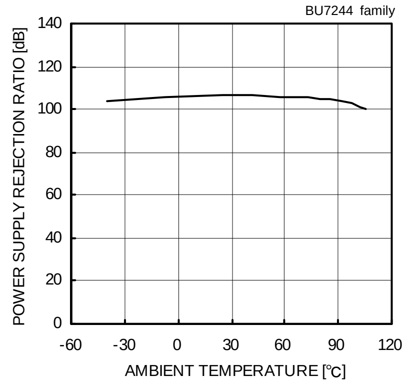


Fig.158

Power Supply Rejection Ratio
– Ambient Temperature

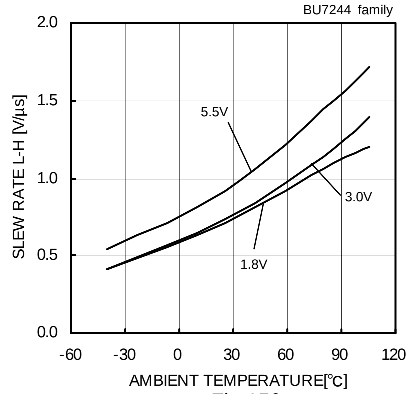


Fig.159

Slew Rate L-H – Ambient Temperature

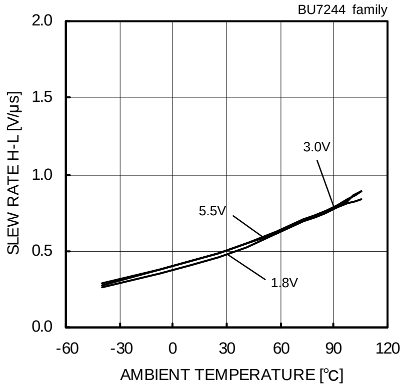


Fig.160

Slew Rate H-L – Ambient Temperature

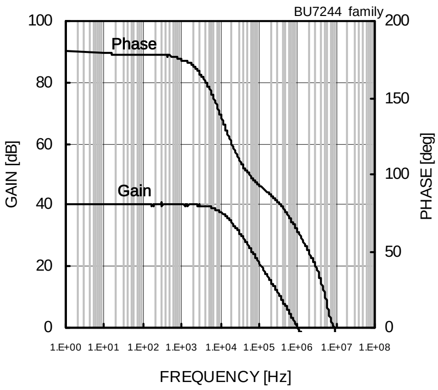


Fig.161

Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7244F: -40[℃] ~ +85[℃] BU7244SF: -40[℃] ~ +105[℃]

●Reference Data (BU7275 family)

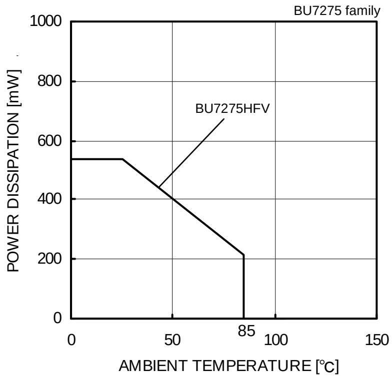


Fig.162
Derating curve

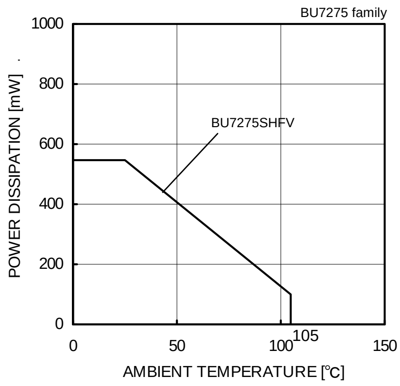


Fig.163
Derating curve

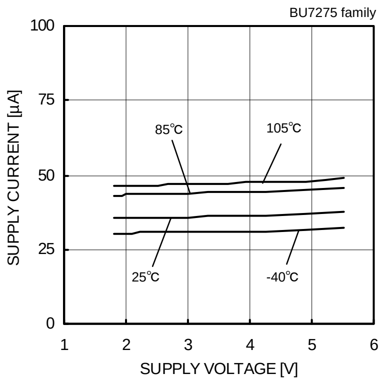


Fig.164
Supply Current – Supply Voltage

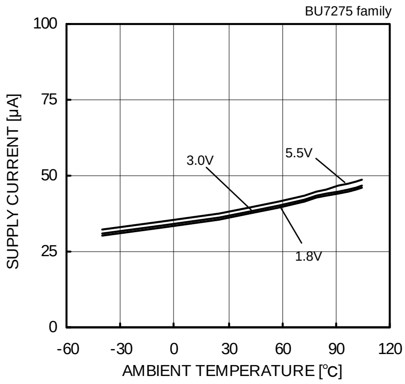


Fig.165
Supply Current – Supply Voltage

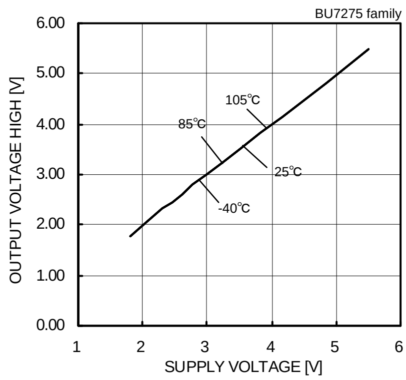


Fig.166
Output Voltage High – Supply Voltage
(RL=10[kΩ])

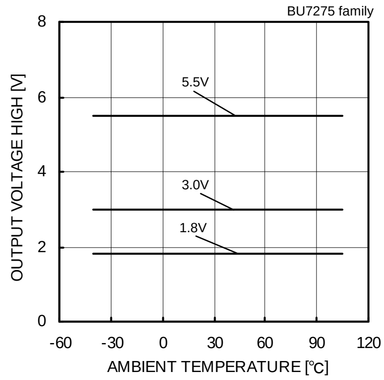


Fig.167
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

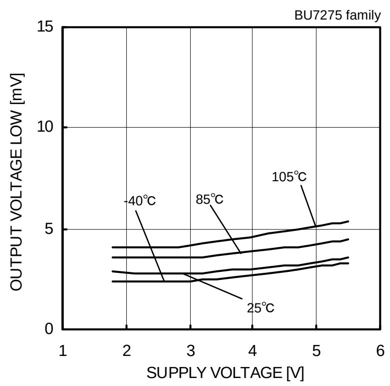


Fig.168
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

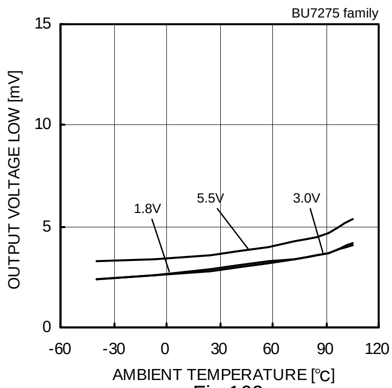


Fig.169
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

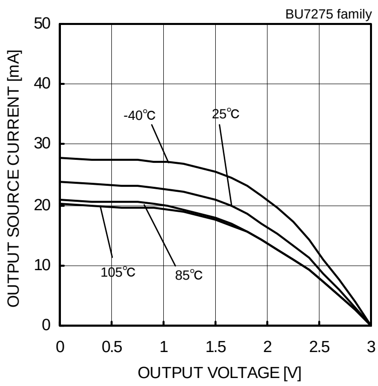


Fig.170
Output Source Current – Output Voltage
(VDD=3 [V])

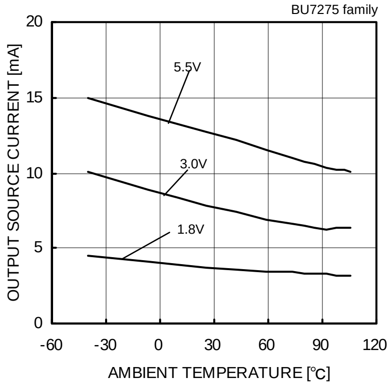


Fig.171
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

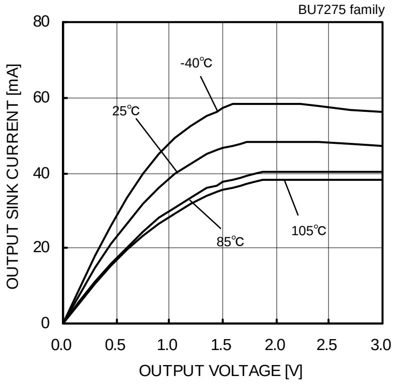


Fig.172
Output Sink Current – Output Voltage
(VDD=3[V])

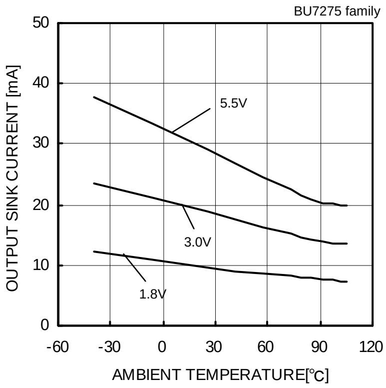


Fig.173
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7275 HFV: -40[℃] ~ +85[℃] BU7275S HFV: -40[℃] ~ +105[℃]

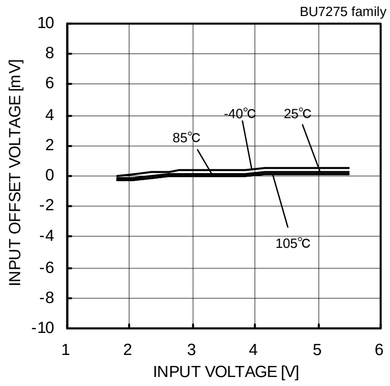


Fig.174
Input Offset Voltage – Supply Voltage
(Vicm=VDD,VOUT=1.5[V])

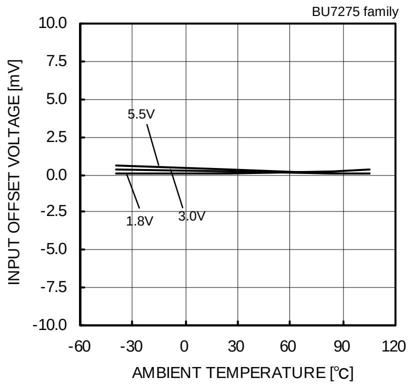


Fig.175
Input Offset Voltage – Ambient Temperature
(Vicm=VDD,VOUT=1.5[V])

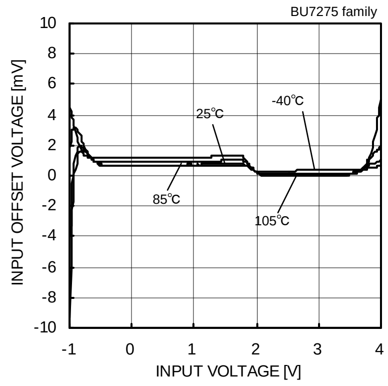


Fig.176
Input Offset Voltage – Input Voltage
(VDD=3[V])

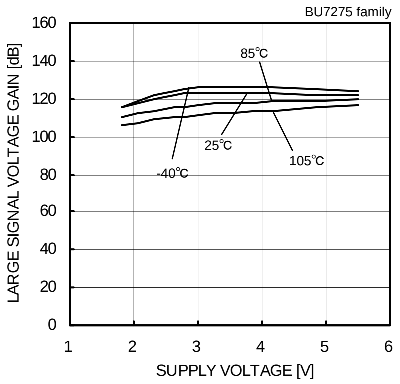


Fig.177
Large Signal Voltage Gain
– Supply Voltage

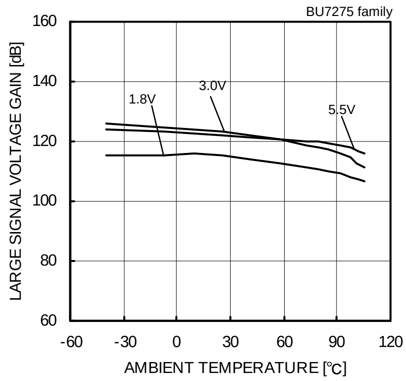


Fig.178
Large Signal Voltage Gain
– Ambient Temperature

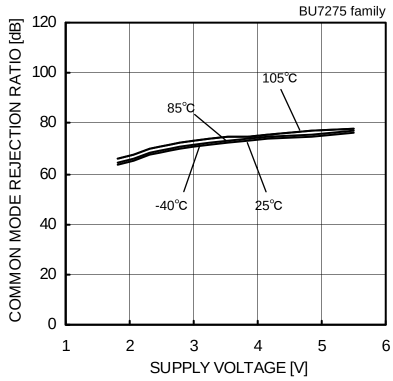


Fig.179
Common Mode Rejection Ratio
– Supply Voltage

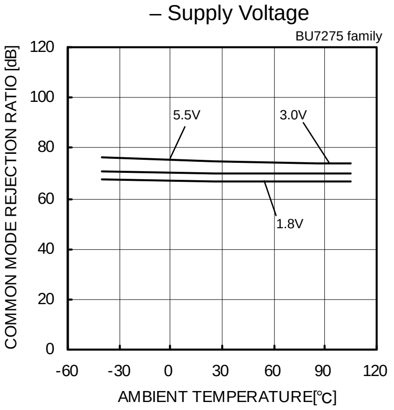


Fig.180
Common Mode Rejection Ratio
– Ambient Temperature

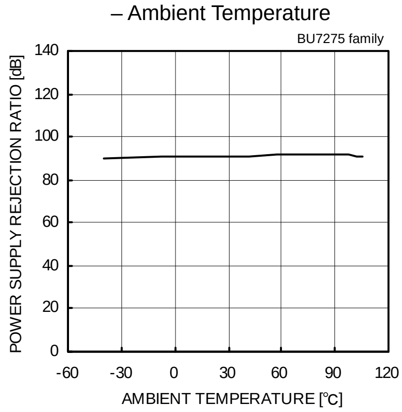


Fig.181
Power Supply Rejection Ratio
– Ambient Temperature

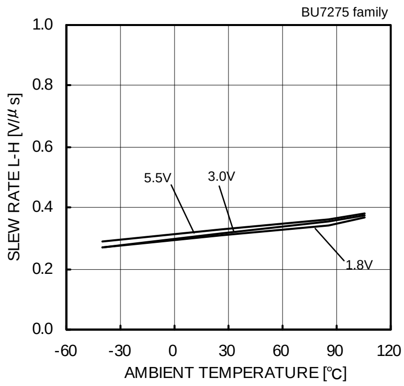


Fig.182
Slew Rate L-H – Ambient Temperature

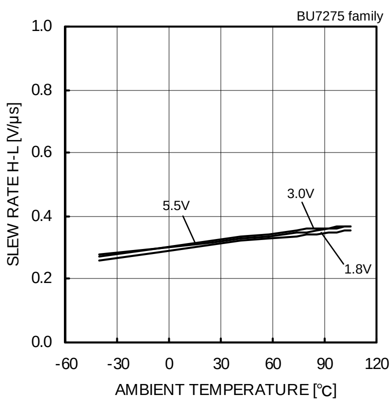


Fig.183
Slew Rate H-L – Ambient Temperature

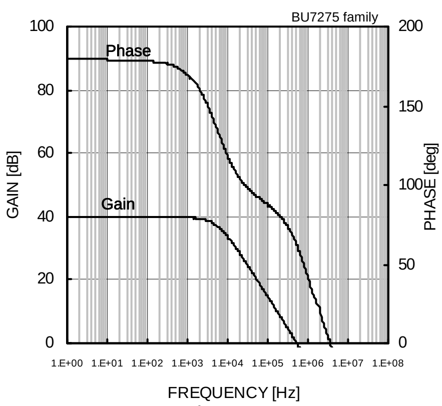


Fig.184
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7275HFV: -40[℃] ~ +85[℃] BU7275SHFV: -40[℃] ~ +105[℃]

●Test circuit 1 NULL method

VDD, VSS, EK, Vicm Unit: [V]

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation
Input Offset Voltage	VF1	ON	ON	OFF	3	0	-1.5	3	1
Large Signal Voltage Gain	VF2	ON	ON	ON	3	0	-0.5	1.5	2
	VF3						-2.5		
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF4	ON	ON	OFF	3	0	-1.5	0	3
	VF5							3	
Power Supply Rejection Ratio	VF6	ON	ON	OFF	1.8	0	-0.9	0	4
	VF7				5.5				

－Calculation－

1. Input Offset Voltage (Vio)

$$Vio = \frac{|VF1|}{1+Rf/Rs} \quad [V]$$

2. Large Signal Voltage Gain (Av)

$$Av = 20Log \frac{2\times(1+Rf/Rs)}{|VF2-VF3|} \quad [dB]$$

3. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20Log \frac{1.8\times(1+Rf/Rs)}{|VF4-VF5|} \quad [dB]$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20Log \frac{3.7\times(1+Rf/Rs)}{|VF6-VF7|} \quad [dB]$$

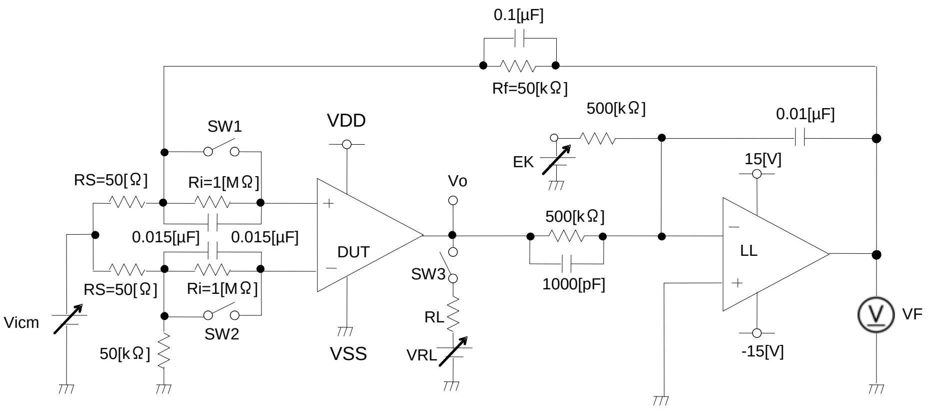


Fig.185 Test circuit 1 (one channel only)

●Test circuit2 switch condition

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage RL=10 [kΩ]	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Maximum Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

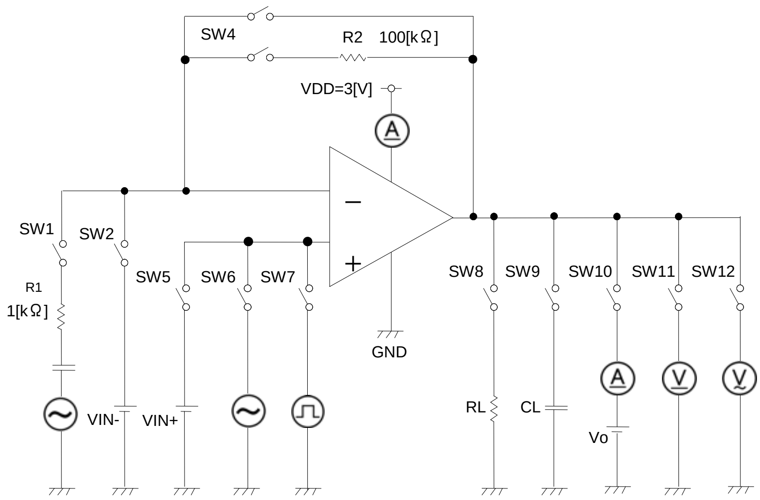


Fig.186 Test circuit 2

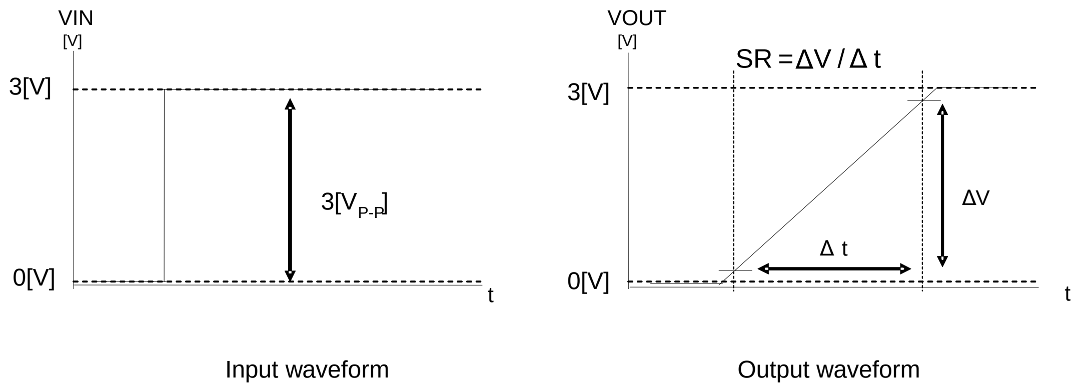
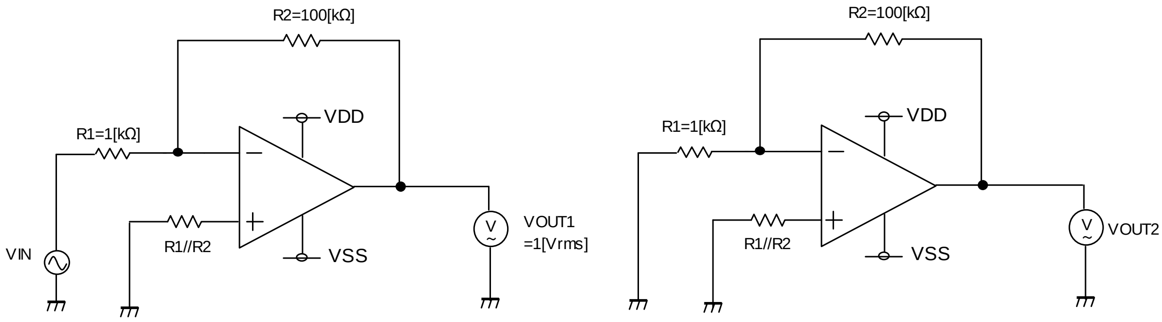


Fig.187. Slew rate input output wave

●Test circuit 3 Channel separation



$$CS=20\log\frac{100\times VOUT1}{VOUT2}$$

Fig.188 Test circuit 3

●Schematic diagram

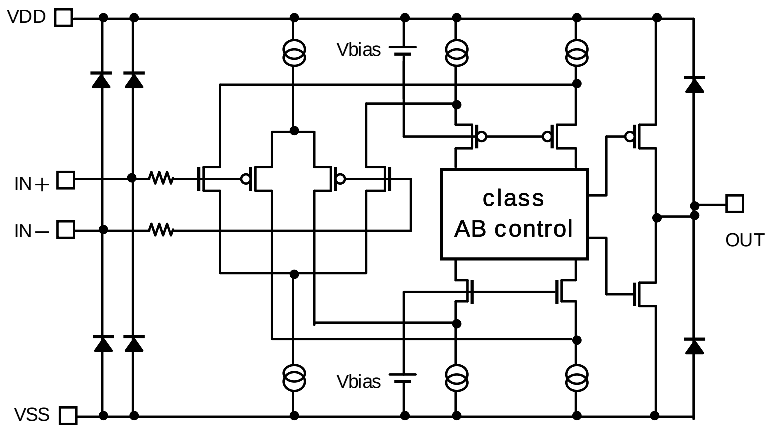


Fig.189 Simplified schematic

●Examples of circuit

○Voltage follower

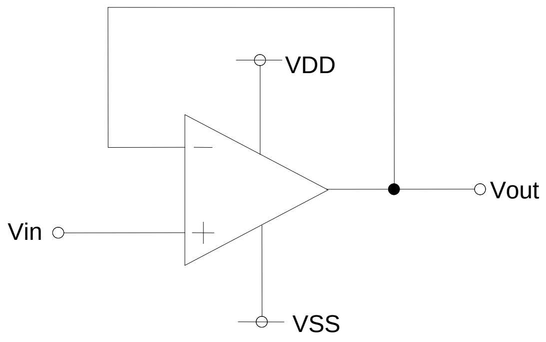


Fig. 190 Voltage follower circuit

Voltage gain is 0 [dB].
This circuit controls output voltage (Vout) equal input voltage (Vin), and keeps Vout with stable because of high input impedance and low output impedance.
Vout is shown next formula.

Vout=Vin

○Inverting amplifier

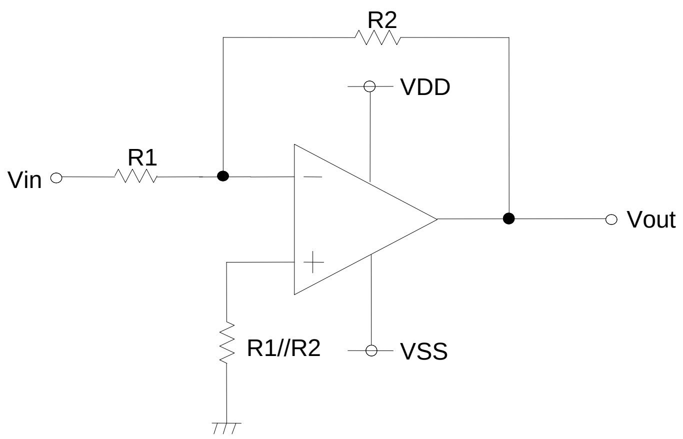


Fig. 191 Inverting amplifier circuit

For inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase reversed voltage is outputted.
Vout is shown next formula.

Vout=-(R2/R1)・Vin

Input impedance is R1.

○Non-inverting amplifier

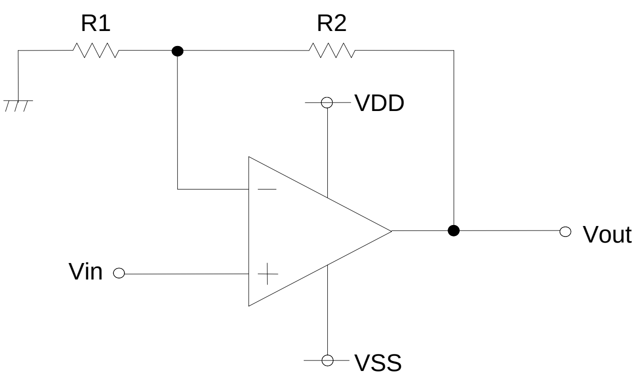


Fig. 192 Non-inverting amplifier circuit

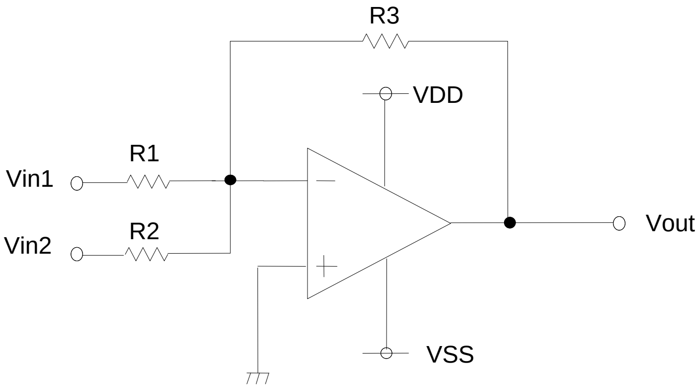
For non-inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase is same with Vin.
Vout is shown next formula.

Vout=(1+R2/R1)・Vin

This circuit realizes high input impedance because Input impedance is operational amplifier's input Impedance.

●Examples of circuit

○Adder circuit



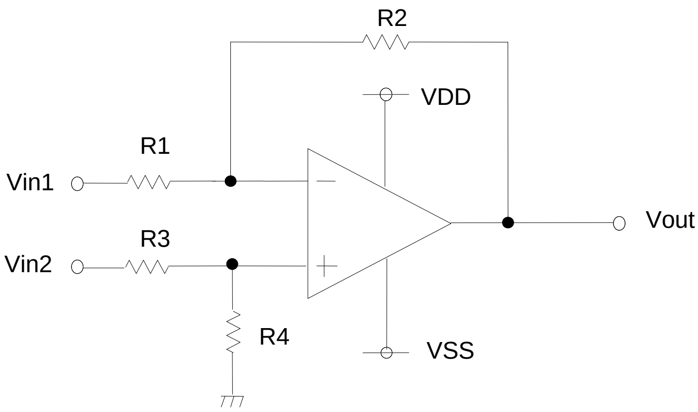
Adder circuit output the voltage that added up Input voltage. A phase of the output voltage turns over, because non-inverting circuit is used.
Vout is shown next formula.

Vout = -R3(Vin1/R1+Vin2/R2)

When three input voltage is as above, it connects with input through resistance like R1 and R2.

Fig. 193 Adder circuit

○Differential amplifier



Differential amplifier output the voltage that amplified a difference of input voltage.
In the case of R1=R3=Ra, R2=R4=Rb
Vout is shown next formula.

Vout = -Rb/Ra(Vin1-Vin2)

Fig. 194 Differential amplifier

●Description of electrical characteristics

Described here are the terms of electric characteristics used in this technical note. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of dharacteristics.

1.1 Power supply voltage (VDD/VSS)
Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminalwithout deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)
Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (Vicm)
Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normalOperation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (Pd)
Indicates the power that can be consumed by specified mounted board at the ambient temperature 25℃(normal temperature).
As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2. Electrical characteristics item

2.1 Input offset voltage (Vio)
Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 [V].

2.2 Input offset current (Iio)
Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current (Ib)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Circuit current (IDD)
Indicates the IC current that flows under specified conditions and no-load steady status.

2.5 High level output voltage / Low level output voltage (VOM)
Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into high-level output voltage and low-level output voltage. High-level output voltage indicates the upper limit of output voltage. Low-level output voltage indicates the lower limit.

2.6 Large signal voltage gain (AV)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage fluctuation) / (Input offset fluctuation)

2.7 Input common-mode voltage range (Vicm)
Indicates the input voltage range where IC operates normally.

2.8 Common-mode rejection ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
CMRR =(Change of Input common-mode voltage)/(Input offset fluctuation)

2.9 Power supply rejection ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
PSRR=(Change of power supply voltage)/(Input offset fluctuation)

2.10 Channel separation (CS)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.11 Slew rate (SR)
Indicates the time fluctuation ratio of voltage output when step input signal is applied.

2.12 Unity gain frequency (ft)
Indicates a frequency where the voltage gain of Op-Amp is 1.

2.13 Total harmonic distortion + Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

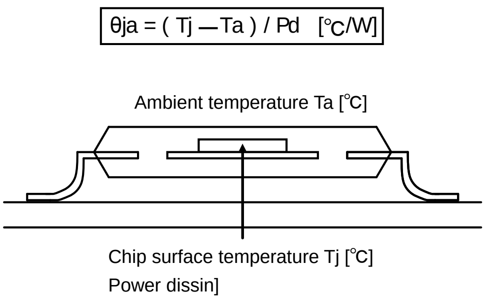
2.14 Input referred noise voltage (Vn)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

●Derating curve

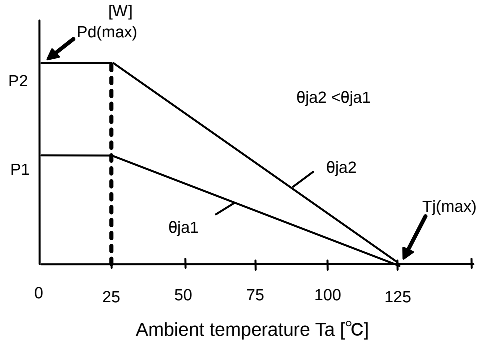
Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature).IC is heated when it consumed power, and the temperature of IC ship becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θj-a[℃/W]. The temperature of IC inside the package can be estimated by this thermal resistance. Fig.195 (a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below :

$$\theta ja = (Tj - Ta) / Pd \quad [℃/W] \quad \cdots\cdots \quad (\mathrm{I})$$

Derating curve in Fig.195(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig196(c) ~ (h) show a derating curve for an example of low voltage full swing CMOS Op-Amp.

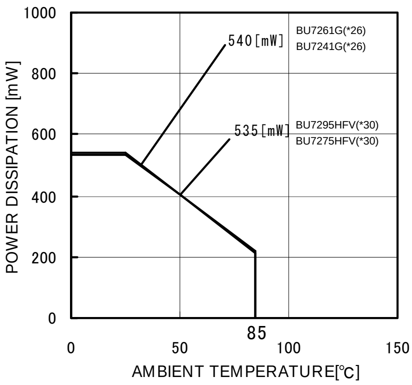


(a)Thermal resistance

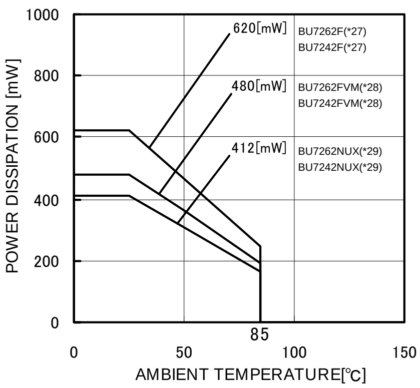


(b) Derating curve

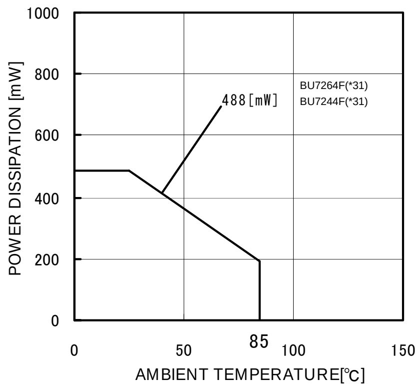
Fig. 195 Thermal resistance and derating



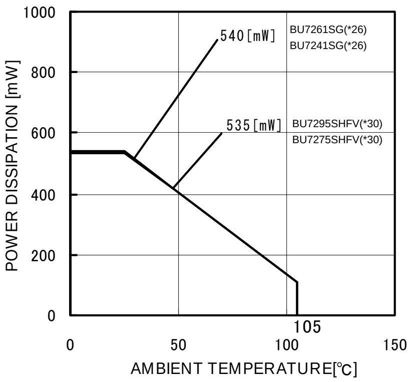
(c) BU7261G BU7241G BU7275HFV BU7295HFV



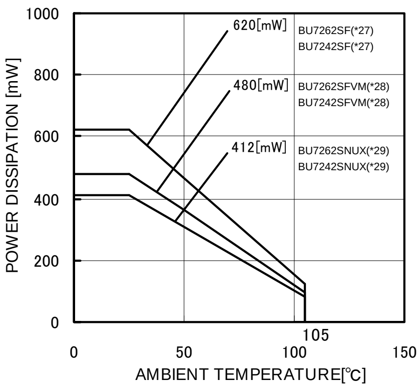
(d) BU7262F/FVM/NUX BU7242F/FVM/NUX



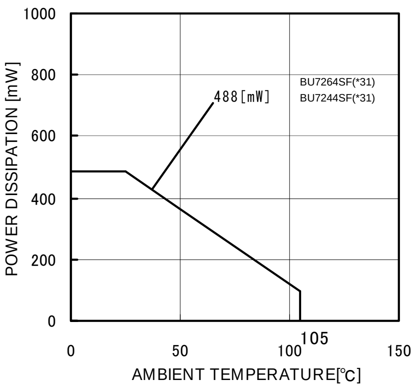
(e) BU7264F BU7244F



(f) BU7261SG BU7241SG BU7275SHFV BU7295SHFV



(g) BU7262S F/FVM/NUX BU7242S F/FVM/NUX



(h) BU7264SF BU7244SF

(*26)	(*27)	(*28)	(*29)	(*30)	(*31)	Unit
5.4	6.2	4.8	4.12	5.35	4.88	[mW/℃]

When using the unit above Ta=25[℃], subtract the value above per degree[℃]. Permissible dissipation is the value.
when FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm] (cooper foil area below 3[%]) is mounted.

Fig. 196 Derating Curve

●Notes for use

1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.

2) Applied voltage to the input terminal
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage VDD + 0.3[V].
Then, regardless of power supply voltage, VSS-0.3[V] can be applied to input terminals without deterioration or destruction of its characteristics.

3) Operating power supply (split power supply/single power supply)
The voltage comparator operates if a given level of voltage is applied between VDD and VSS.
Therefore, the operational amplifier can be operated under single power supply or split power supply.

4) Power dissipation (pd)
If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC. For example, reduction of current capability. Take consideration of the effective power dissipation and thermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.

5) Short circuits between pins and incorrect mounting
Short circuits between pins and incorrect mounting when mounting the IC on a printed circuits board, take notice of the direction and positioning of the IC.
If IC is mounted erroneously, It may be damaged. Also, when a foreign object is inserted between output, between output and VDD terminal or VSS terminal which causes short circuit, the IC may be damaged.

6) Using under strong electromagnetic field
Be careful when using the IC under strong electromagnetic field because it may malfunction.

7) Usage of IC
When stress is applied to the IC through warp of the printed circuit board, The characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.

8) Testing IC on the set board
When testing IC on the set board, in cases where the capacitor is connected to the low impedance, make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress.
When removing IC from the set board, it is essential to cut supply voltage. As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.

9) The IC destruction caused by capacitive load
The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor.When IC is used as a operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor, the output capacitor must be kept below 0.1[μF] in order to prevent the damage mentioned above.

10) Decupling capacitor
Insert the decupling capacitance between VDD and VSS, for stable operation of operational amplifier.

11) Latch up
Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise

12) Decupling capacitor
Insert the decupling capacitance between VDD and VSS, for stable operation of operational amplifier.

●Ordering part number

B	U		7	2	6	2	S		F	V	M	-	T	R

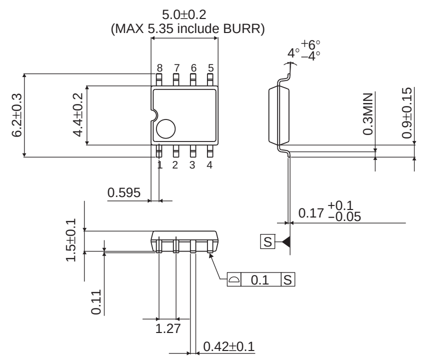
Part No.

Part No.
・7261 7261S ・7264 7264S
・7241 7241S ・7244 7244S
・7262 7262S ・7295 7295S
・7242 7242S ・7275 7275S

Package
G : SSOP5
F : SOP8, SOP14
FVM : MSOP8
NUX : VSON008X2030
HFV : HVSOF5

Packaging and forming specification
E2: Embossed tape and reel
(SOP8/SOP14)
TR: Embossed tape and reel
(SSOP5/MSOP8/VSON008X2030/HVSOF5)

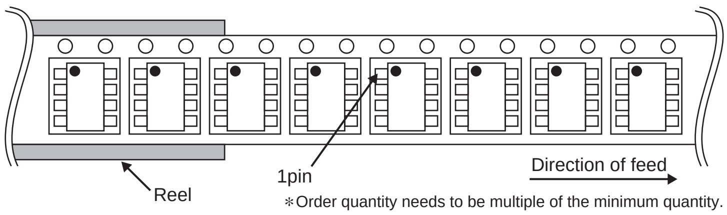
SOP8



(Unit : mm)

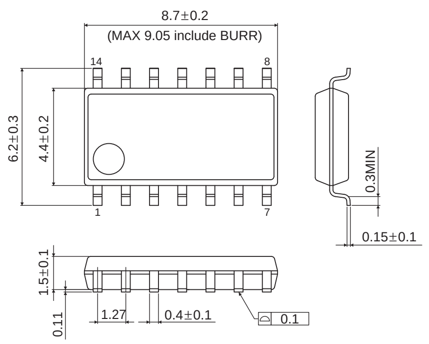
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

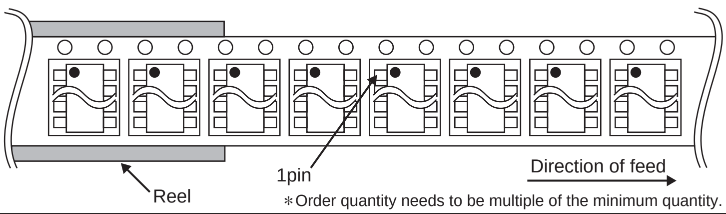
SOP14



(Unit : mm)

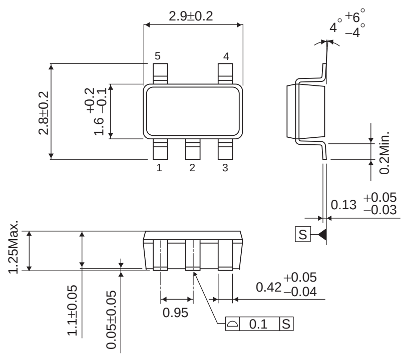
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

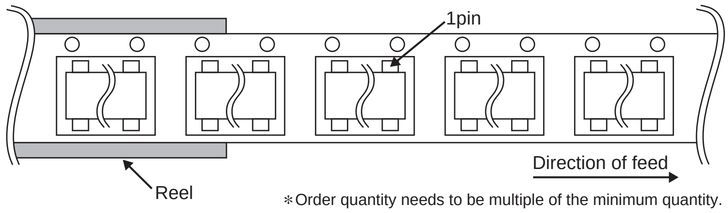
SSOP5



(Unit : mm)

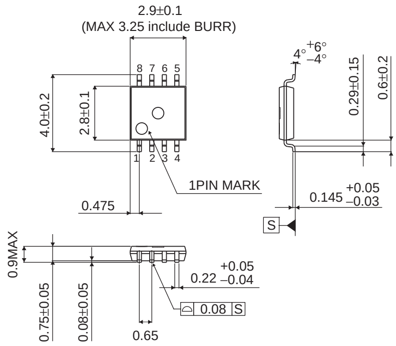
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

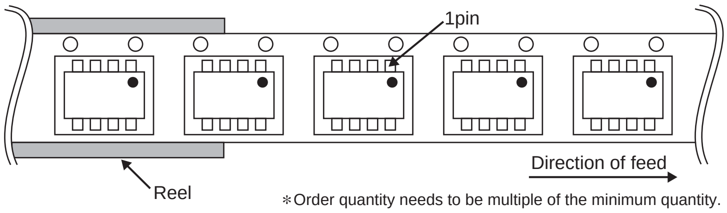
MSOP8



(Unit : mm)

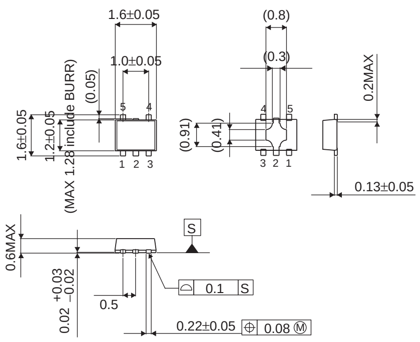
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

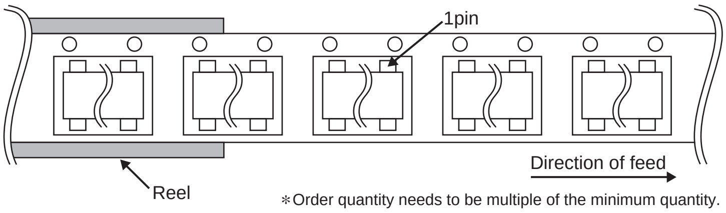
HVSOF5



(Unit : mm)

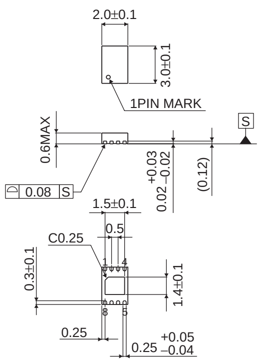
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

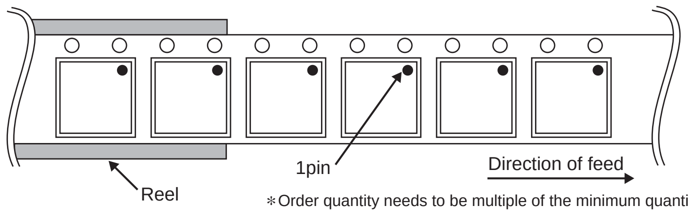
VSON008X2030



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/