

## Product Summary

$BV_{DSS}$	$R_{DS(ON)}$ max	$I_D$ max $T_C = +25^\circ C$
80V	17m $\Omega$ @ $V_{GS} = 10V$	44A
	22m $\Omega$ @ $V_{GS} = 4.5V$	38A

## Features

- Low  $R_{DS(ON)}$  – ensures on state losses are minimized
- High Conversion Efficiency
- Low Input Capacitance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

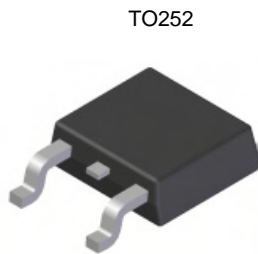
## Description and Applications

This MOSFET is designed to minimize the on-state resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

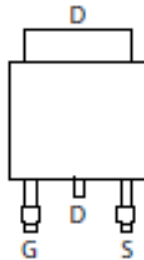
- Synchronous Rectifier
- Backlighting
- Power Management Functions
- DC-DC Converters

## Mechanical Data

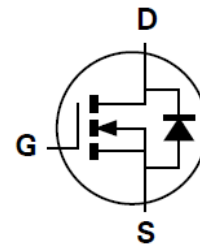
- Case: TO252
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.33 grams (Approximate)



Top View



Pin Out Top View



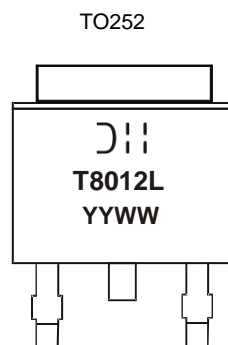
Equivalent Circuit

## Ordering Information (Note 4)

Part Number	Case	Packaging
DMT8012LK3-13	TO252	2,500/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



= Manufacturer's Marking  
 T8012L = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Last Digit of Year (ex: 14 = 2014)  
 WW = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	80	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 10V	I <sub>D</sub>	T <sub>C</sub> = +25°C	44
		T <sub>C</sub> = +100°C	28
Maximum Continuous Body Diode Forward Current (Note 5)	I <sub>S</sub>	3	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	60	A
Avalanche Current, L=0.1mH	I <sub>AS</sub>	11.6	A
Avalanche Energy, L=0.1mH	E <sub>AS</sub>	10.2	mJ

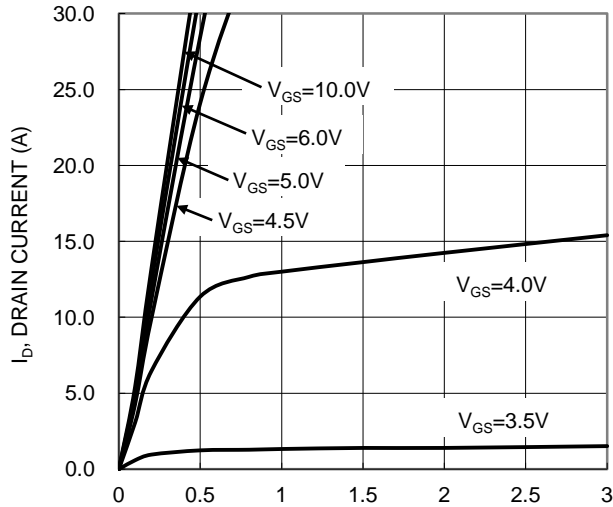
**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	2.7	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	47	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	50	W
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	2.5	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

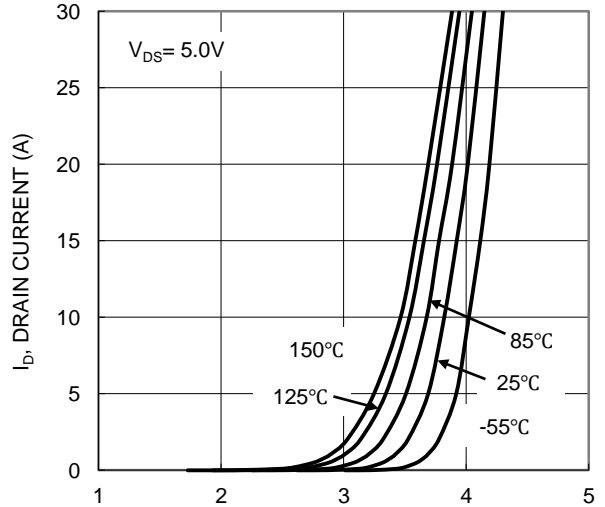
**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	80	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	-	-	1	µA	V <sub>DS</sub> = 64V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1	-	3	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	12	17	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A
		-	18.2	22		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6A
Diode Forward Voltage	V <sub>SD</sub>	-	0.9	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 25A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	-	1,949	-	pF	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V, f = 1MHz
Output Capacitance	C <sub>oss</sub>	-	177	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	10	-		
Gate Resistance	R <sub>g</sub>	-	0.7	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	-	15	-	nC	V <sub>DS</sub> = 40V, I <sub>D</sub> = 12A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	-	34	-		
Gate-Source Charge	Q <sub>gs</sub>	-	6	-		
Gate-Drain Charge	Q <sub>gd</sub>	-	4.5	-		
Turn-On Delay Time	t <sub>D(ON)</sub>	-	4.9	-	ns	V <sub>DD</sub> = 40V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A, R <sub>G</sub> = 1.6Ω
Turn-On Rise Time	t <sub>R</sub>	-	3.8	-		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	-	16.5	-		
Turn-Off Fall Time	t <sub>F</sub>	-	3.5	-		
Body Diode Reverse Recovery Time	t <sub>RR</sub>	-	30.2	-	ns	I <sub>F</sub> = 12A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	-	34.6	-	nC	

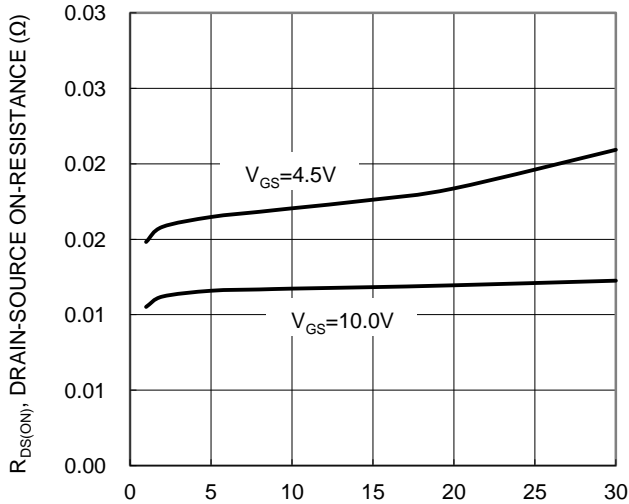
- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.
  - Device mounted on infinite heat sink and measured by thermal couple attached on bottom heat sink of package.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to product testing.



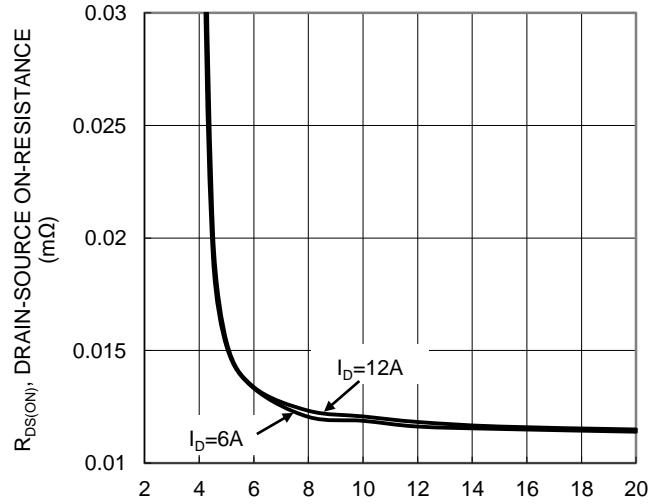
$V_{DS}$ , DRAIN-SOURCE VOLTAGE (V)  
Figure 1. Typical Output Characteristic



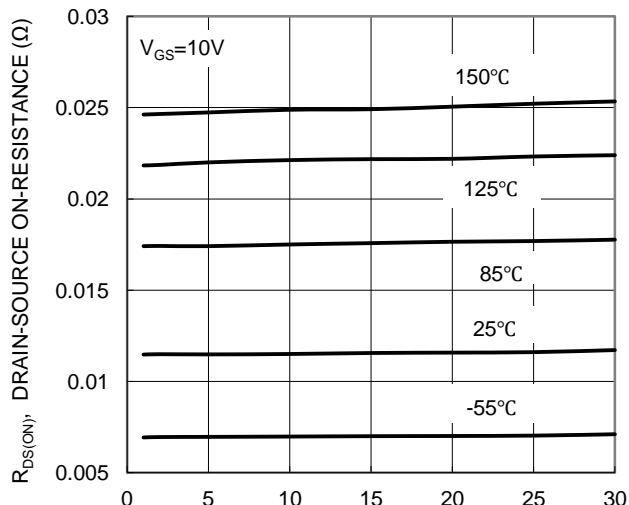
$V_{GS}$ , GATE-SOURCE VOLTAGE (V)  
Figure 2. Typical Transfer Characteristic



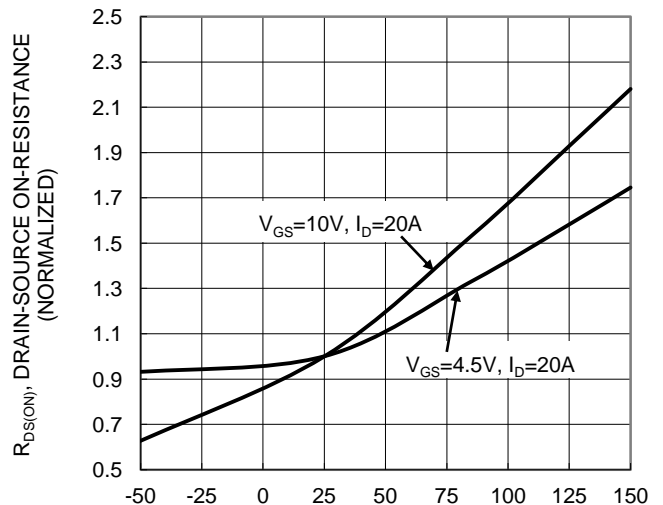
$I_D$ , DRAIN-SOURCE CURRENT (A)  
Figure 3. Typical On-Resistance vs Drain Current and Gate Voltage



$V_{GS}$ , GATE-SOURCE VOLTAGE (V)  
Figure 4. Typical Transfer Characteristic



$I_D$ , DRAIN CURRENT (A)  
Figure 5. Typical On-Resistance vs Drain Current and Temperature



$T_J$ , JUNCTION TEMPERATURE ( $^{\circ}C$ )  
Figure 6. On-Resistance Variation with Temperature

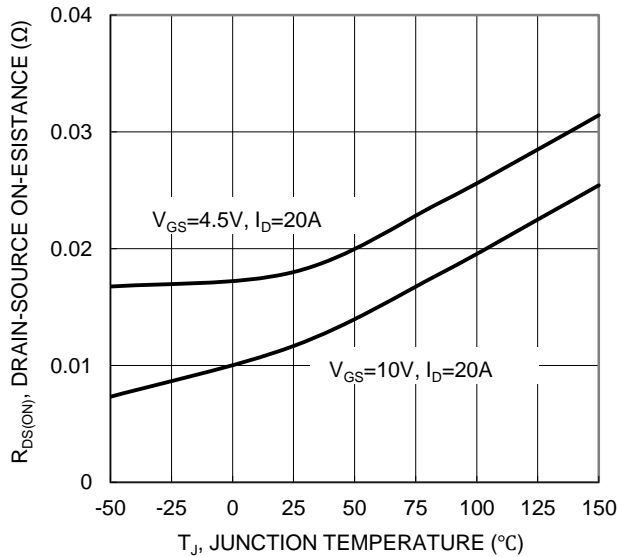


Figure 7. On-Resistance Variation with Temperature

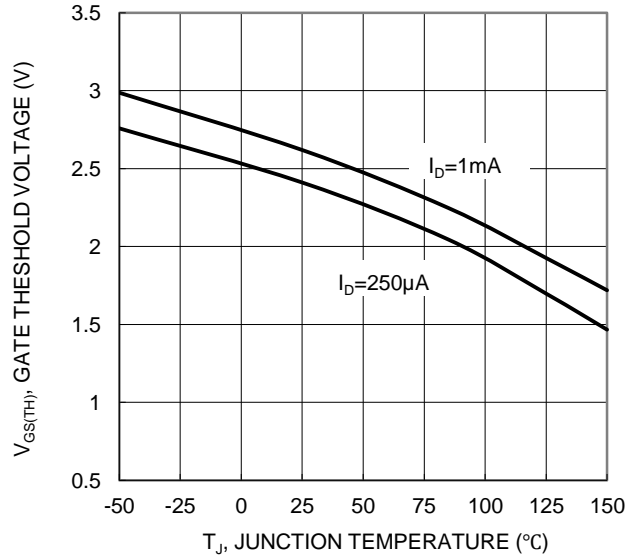


Figure 8. Gate Threshold Variation vs Temperature

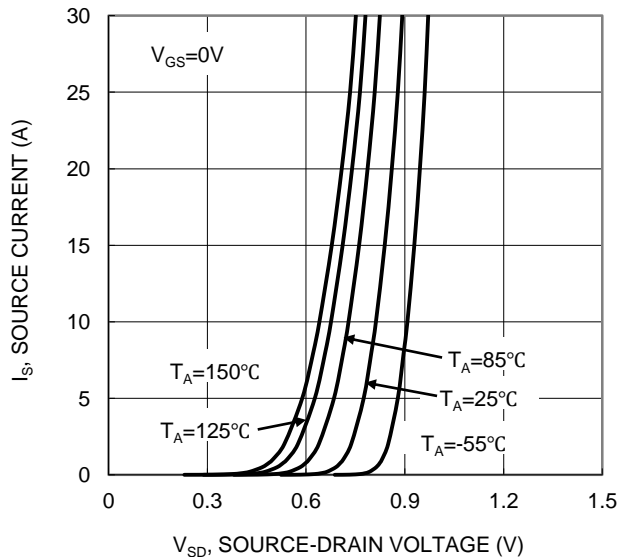


Figure 9. Diode Forward Voltage vs Current

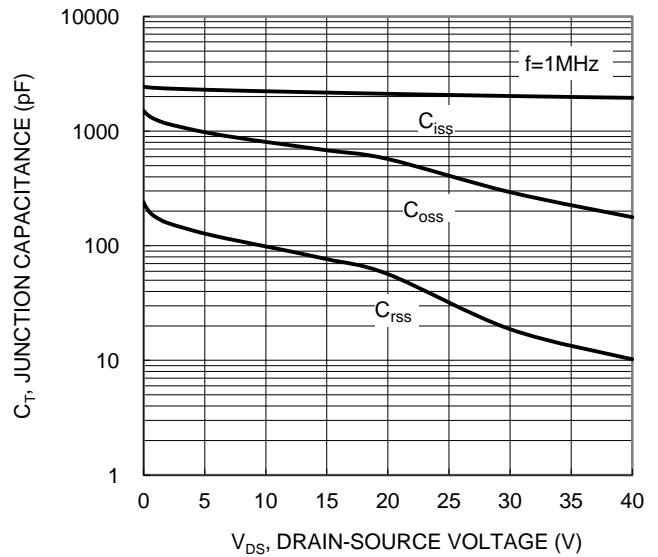


Figure 10. Typical Junction Capacitance

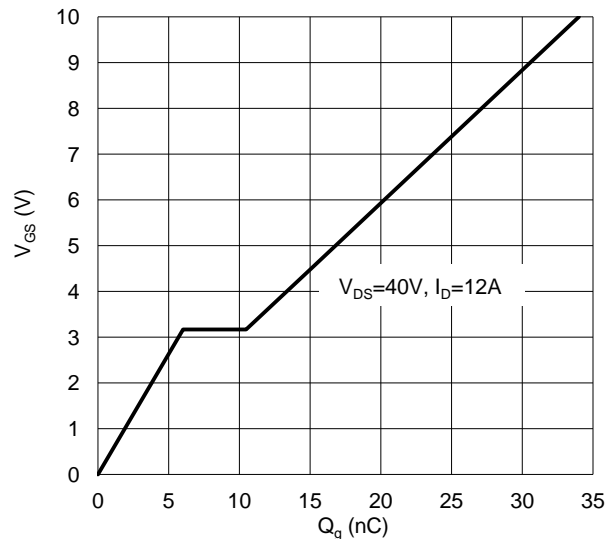


Figure 11. Gate Charge

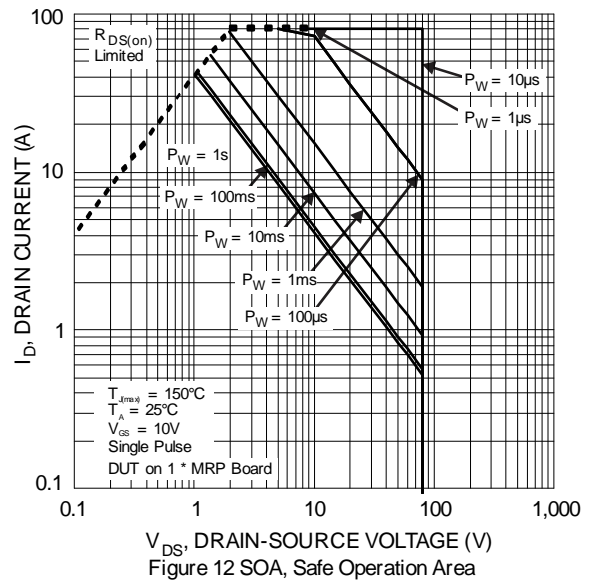


Figure 12 SOA, Safe Operation Area

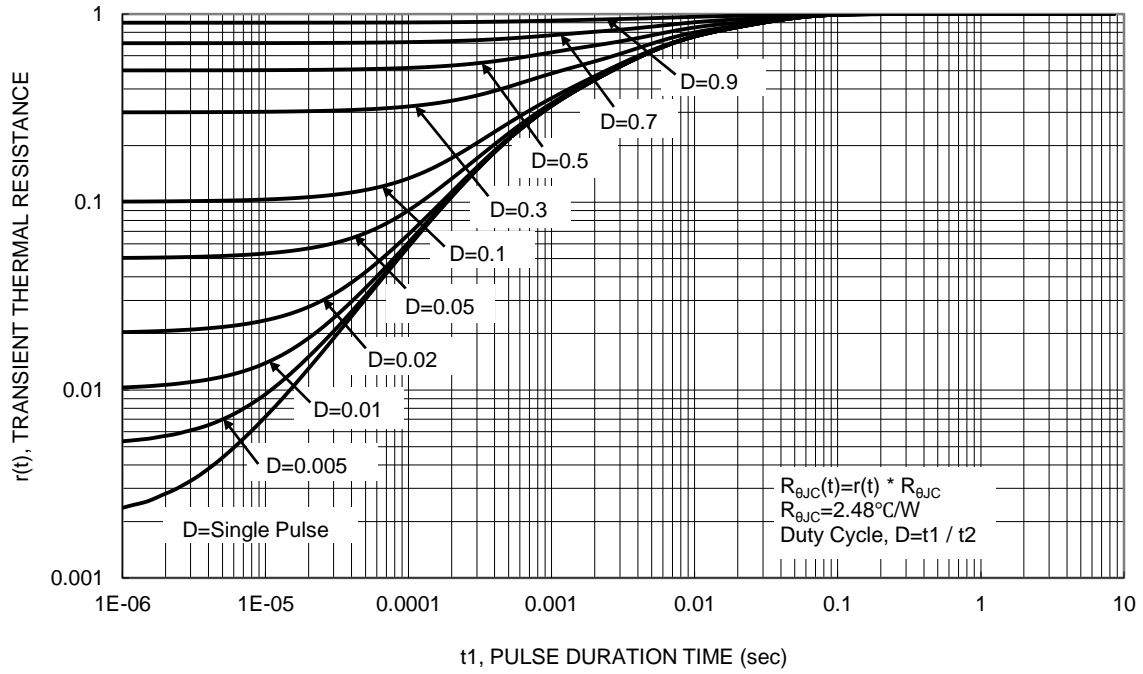
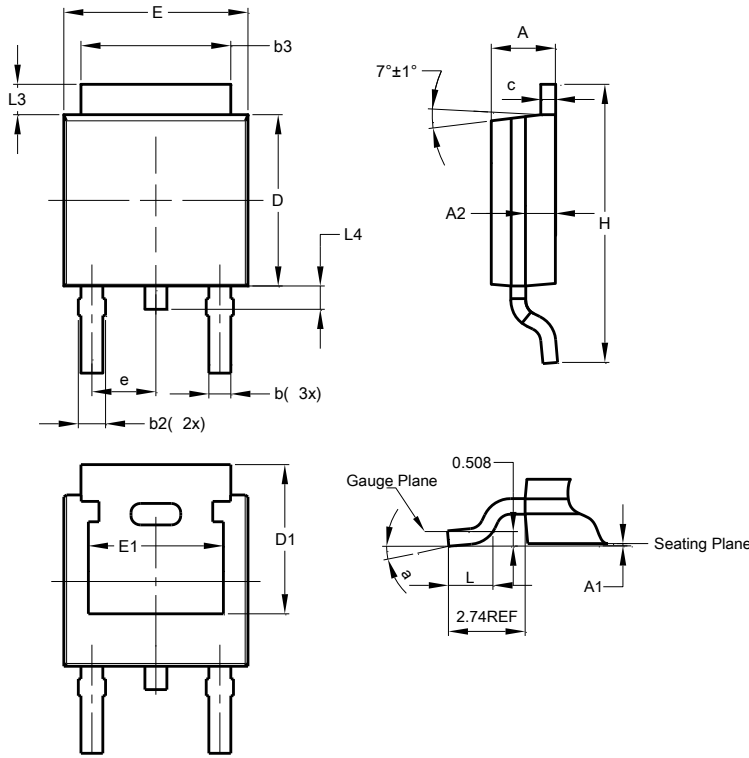


Figure 13. Transient Thermal Resistance

**Package Outline Dimensions**

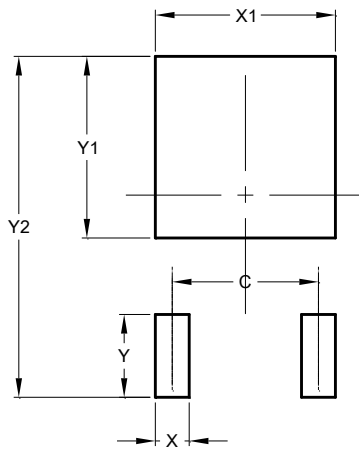
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



TO252 (DPAK)			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700

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