

### Key Features

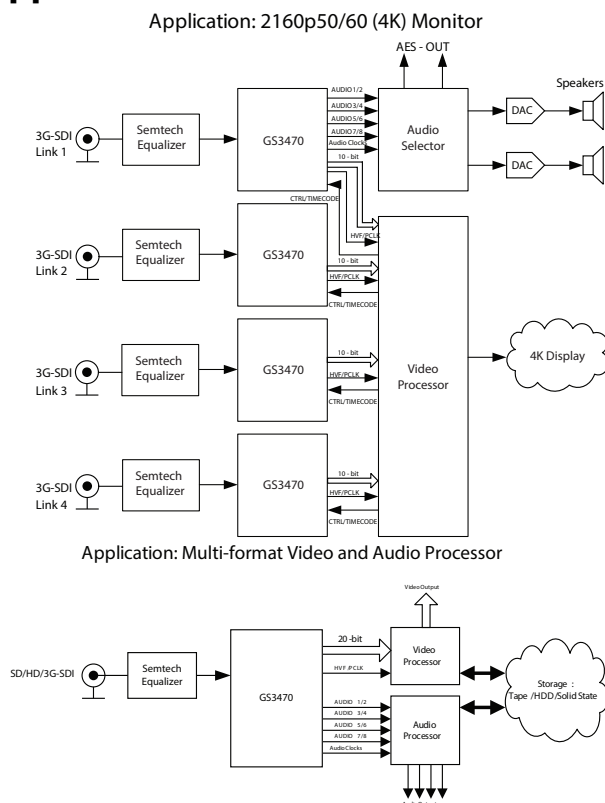
- Operation at 2.970Gb/s, 2.970/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s, and 270Mb/s
- Supports SMPTE ST 425 (Level A and Level B), SMPTE ST 424, SMPTE 292, SMPTE ST 259-C, and DVB-ASI
- 2K and Multi-link UHD support
- Configurable Power-down modes
- Integrated Retimer
- Serial digital reclocked or non-reclocked loop-through output
- Integrated audio de-embedder for 8 channels of 48kHz audio and audio clock generation
- Ancillary data extraction
- Parallel data bus selectable as either 20-bit or 10-bit, SDR or DDR rate
- Comprehensive error detection and correction features
- Dual serial digital input buffer with 2x2 MUX
- Serial Loopback independently configurable to select either input
  - ♦ Performance optimized for 270Mb/s, 1.485Gb/s, and 2.97Gb/s.
- Dual/Quad Link 3G-SDI support with multiple GS3470 devices
- Output H, V, F, or CEA 861 timing signals
- GSPI host interface
- +1.2V digital core power supply, +1.2V and +1.8V analog power supplies, and selectable +1.8V or +2.5V I/O power supply
- -20°C to +85°C operating temperature range
- Low power operation — typically 220mW
- Small 9mm x 9mm 100-ball BGA package (0.80mm Ball Pitch)
- Pb-free, Halogen-free, and RoHS/ WEEE-compliant package

### Applications

SDI Interfaces for:

- Monitors
- DVRs
- Video Switchers
- Editing Systems
- Cameras
- Medical Imaging
- Aviation, Military, and Vehicular video systems

### LED Wall and Digital Signage Applications



The GS3470 is a multi-rate SDI Receiver which includes complete SMPTE processing. The SMPTE processing features can be bypassed to support signals with other coding schemes. Multi-link UHD can be supported when multiple GS3470 devices are used.

The device features a dual input buffer with a 2x2 MUX. The 2x2 MUX can select between either input for de-serialization and can route either of the two inputs to the serial loopback independently (relocked or non-relocked). In addition, the integrated Retimer with an internal VCO provides a wide Input Jitter Tolerance (IJT).

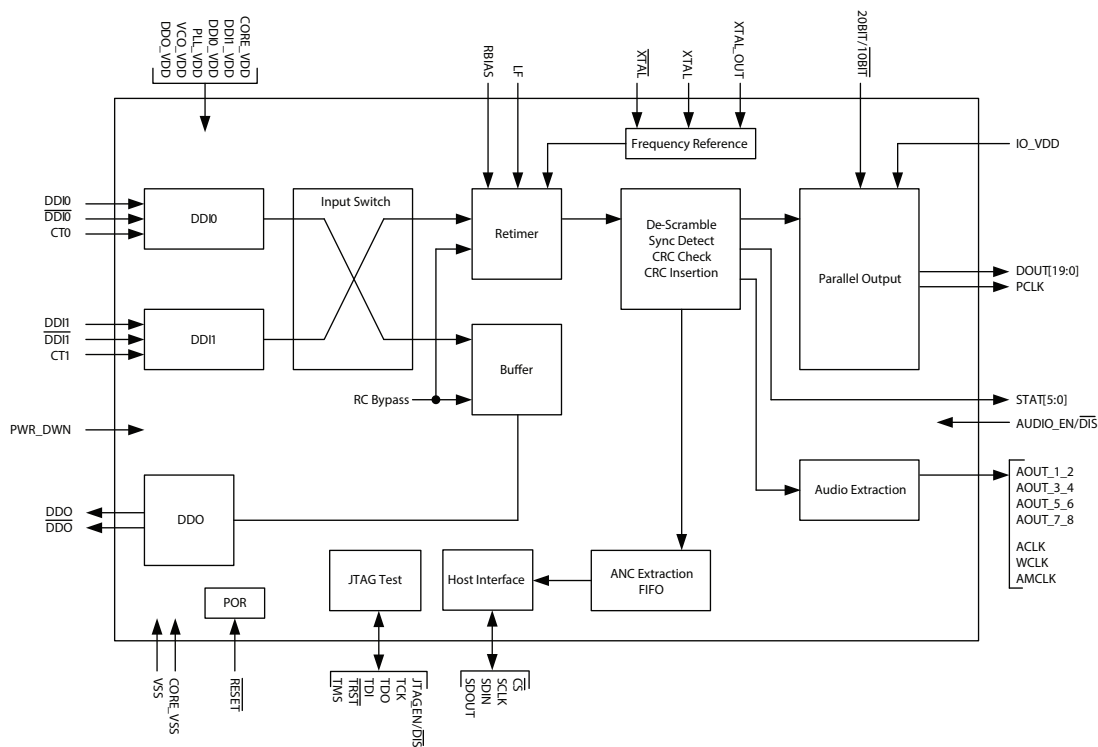
Configurable Power-down modes are available and allows for increased flexibility. Each Power-down mode enables power savings to a varying degree by selectively enabling or disabling key features. Some of the options available in

Power-down mode are CSR access, PCLK, retimed DDO loop-through output, and non-retimed DDO loop-through output. Enabling or disabling each of these options will offer power consumption levels to suit the application's requirements.

The device has three other basic modes of operation which include:

- SMPTE mode
- DVB-ASI mode
- Data-Through mode

The GS3470 includes an audio de-embedder and audio clocks are internally generated. Up to eight channels (two audio groups) of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272-C and SMPTE ST 299.



## GS3470 Functional Block Diagram

## Revision History

| Version | ECO    | Date           | Changes and/or Modifications                                                                                                                                                                                                                    |
|---------|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8       | 038819 | September 2017 | Updated to latest corporate template.                                                                                                                                                                                                           |
| 7       | 038315 | September 2017 | Updated several register and parameter names throughout <a href="#">Section 4</a> . Updated <a href="#">Figure 4-1</a> , <a href="#">Figure 6-1</a> .                                                                                           |
| 6       | 037007 | May 2017       | Updated <a href="#">Table 2-2</a> , <a href="#">Table 2-3</a> , <a href="#">Table 2-4</a> , <a href="#">Table 4-27</a> , <a href="#">Table 5-8</a> .<br>Changed all instances of DBUS to DOUT, and VSS/VEE to A_GND.                            |
| 5       | 035144 | March 2017     | Added <a href="#">Figure 4-25</a> through <a href="#">Figure 4-30</a> .<br>Updated <a href="#">Section 4.16.1</a> .<br>Updated <a href="#">Table 2-2</a> , <a href="#">Table 2-3</a> , <a href="#">Table 2-4</a> , <a href="#">Table 4-27</a> . |
| 4       | 033598 | October 2016   | Updated data sheet to reflect GS3471 modifications.                                                                                                                                                                                             |
| 3       | 029850 | March 2016     | Updates to <a href="#">1.1 Pin Assignment</a> and <a href="#">2.2 Recommended Operating Conditions</a> .                                                                                                                                        |
| 2       | 029341 | February 2016  | Initial release changes.                                                                                                                                                                                                                        |
| 1       | 028179 | October 2015   | Initial release changes.                                                                                                                                                                                                                        |
| 0       | 020778 | July 2014      | New document.                                                                                                                                                                                                                                   |

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# 1. Pin Out

## 1.1 Pin Assignment

Figure 1-1: Pin Assignment

|   | 1                        | 2        | 3            | 4        | 5                         | 6                        | 7                        | 8        | 9        | 10     |
|---|--------------------------|----------|--------------|----------|---------------------------|--------------------------|--------------------------|----------|----------|--------|
| A | $\overline{\text{DDI0}}$ | DDI0     | CT0          | RBIAS    | XTAL                      | $\overline{\text{XTAL}}$ | RSVD                     | PCLK     | DOUT18   | DOUT17 |
| B | DDI0_VDD                 | DDI0_VDD | RSVD         | RSVD     | STAT0                     | STAT1                    | IO_VDD                   | DOUT19   | DOUT16   | DOUT15 |
| C | PLL_VDD                  | PLL_VDD  | LF           | VCO_VDD  | STAT2                     | STAT3                    | CORE_GND                 | DOUT12   | DOUT14   | DOUT13 |
| D | DDI1_VDD                 | PLL_VDD  | A_GND        | VCO_VDD  | STAT4                     | STAT5                    | $\overline{\text{TRST}}$ | TDI      | CORE_GND | IO_VDD |
| E | CT1                      | DDI1_VDD | A_GND        | CORE_GND | CORE_VDD                  | CORE_VDD                 | TDO                      | TCK      | DOUT10   | DOUT11 |
| F | DDI1                     | A_GND    | A_GND        | CORE_GND | CORE_GND                  | CORE_VDD                 | TMS                      | SDIN     | DOUT8    | DOUT9  |
| G | $\overline{\text{DDI1}}$ | A_GND    | A_GND        | CORE_GND | CORE_GND                  | CORE_VDD                 | SDOUT                    | SCLK     | CORE_GND | IO_VDD |
| H | NC                       | NC       | JTAG_EN/DIS  | WCLK     | $\overline{\text{RESET}}$ | BIT20/BIT10              | $\overline{\text{CS}}$   | CORE_GND | DOUT6    | DOUT7  |
| J | DDO_VDD                  | DDO_VDD  | PWR_DWN      | AOUT_1_2 | ACLK                      | AOUT_5_6                 | CORE_GND                 | DOUT1    | DOUT4    | DOUT5  |
| K | $\overline{\text{DDO}}$  | DDO      | AUDIO_EN/DIS | AOUT_3_4 | AMCLK                     | AOUT_7_8                 | IO_VDD                   | DOUT0    | DOUT2    | DOUT3  |

## 1.2 Pin Descriptions

Table 1-1: Pin Descriptions

| Pin Number       | Name                                                               | Type         | Description                                                                                                                                                                                                                                                                                                                              |
|------------------|--------------------------------------------------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1, A2<br>G1, F1 | $\overline{\text{DDI0}}$ , DDI0<br>$\overline{\text{DDI1}}$ , DDI1 | SDI Input    | Serial digital differential input. It is possible to DC-couple to upstream Semtech devices supporting 1.2V outputs. Additionally, devices with 1.8 and 2.5V outputs are supported through a 4.7 $\mu$ F capacitor in series with the $\overline{\text{DDI}}$ /DDI input. Connect unused inputs to DDI_VDD through 1k $\Omega$ resistors. |
| A4               | RBIAS                                                              | Analog Input | External resistor for the bias circuit. Connect to ground through 777 $\Omega$ resistor.                                                                                                                                                                                                                                                 |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number                                                                             | Name                           | Type         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------------------------------------------------------------------------------|--------------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A5, A6                                                                                 | XTAL, $\overline{\text{XTAL}}$ | Analog Input | Input connection for 27MHz crystal. When a reference clock input is used on $\overline{\text{XTAL}}$ , do not connect XTAL.                                                                                                                                                                                                                                                                                                                                                                          |
| A8                                                                                     | PCLK                           | Output       | Parallel data bus clock.<br>Please refer to the Output Logic parameters in <a href="#">Table 2-3: DC Electrical Characteristics</a> for logic level threshold and compatibility.<br>Please refer to <a href="#">Table 4-5: GS3470 Output Data Formats</a> for PCLK output rates.                                                                                                                                                                                                                     |
| A7, B3, B4                                                                             | RSVD                           | —            | These pins are reserved, do not connect.                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| B7, D10, G10, K7                                                                       | IO_VDD                         | Power        | Power connection for digital I/O. Connect to 1.8V or 2.5V DC digital.                                                                                                                                                                                                                                                                                                                                                                                                                                |
| B8, A9, A10, B9, B10, C9, C10, C8, E10, E9, F10, F9, H10, H9, J10, J9, K10, K9, J8, K8 | DOUT[19:0]                     | Output       | Parallel data bus.<br>Please refer to the Output Logic parameters in <a href="#">Table 2-3: DC Electrical Characteristics</a> for logic level threshold and compatibility.                                                                                                                                                                                                                                                                                                                           |
|                                                                                        |                                |              | 20-bit mode<br>20BIT_10BIT = HIGH<br><br>SMPTE mode<br>( $\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB_ASI = LOW):<br>DOUT[19:10] — Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate<br>DOUT[9:0] — Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate<br><br>Data-Through mode<br>( $\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = LOW):<br>Data output                                                                                 |
|                                                                                        |                                |              | 10-bit mode<br>20BIT_10BIT = LOW<br>(DOUT[19:10])<br><br>SMPTE mode<br>( $\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB_ASI = LOW):<br>Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate<br><br>DVB-ASI mode<br>( $\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = HIGH):<br>8/10bit decoded DVB-ASI data for SD data rates<br><br>Data-Through mode<br>( $\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = LOW):<br>Data output |
|                                                                                        |                                |              | <b>Note 1:</b> When in 10-bit mode, DOUT[9:0] are set to 0.<br><b>Note 2:</b> When in 10-bit mode, leave unused output pins unconnected.                                                                                                                                                                                                                                                                                                                                                             |
| C1, C2, D2                                                                             | PLL_VDD                        | Power        | Power pins for the Retimer PLL. Connect to 1.2V DC analog.                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number                             | Name                     | Type                                    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------------------------------|--------------------------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C3                                     | LF                       | Analog Input                            | Loop Filter component connection. Connect as per <a href="#">Typical Application Circuit</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| C4, D4                                 | VCO_VDD                  | Power                                   | Power pin for the VCO. Connect to RC filter as per <a href="#">Typical Application Circuit</a> . Connect to a 1.2V $\pm 5\%$ analog supply through a $24\Omega \pm 1\%$ resistor. Additionally, connect to ground through a 10 $\mu$ F capacitor.                                                                                                                                                                                                                                                                                          |
| C7, D9, E4, F4, F5, G4, G5, G9, J7, H8 | CORE_GND                 | Power                                   | Ground pins for digital circuitry. Connect to digital ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| D3, E3, F2, F3, G2, G3                 | A_GND                    | Power                                   | Ground pins for analog circuitry. Connect to analog ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| D1, E2<br>B1, B2                       | DDI1_VDD<br>DDIO_VDD     | Power                                   | Power pins for SDI buffer. Connect to 1.2V DC analog.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| D6, D5, C6,<br>C5, B6, B5              | STAT[5:0]                | Digital Output                          | Multi-function status outputs. See <a href="#">Section 4.11</a> for more details on assigning signals to STAT pins.<br>Please refer to the Output Logic parameters in <a href="#">Table 2-3: DC Electrical Characteristics</a> for logic level threshold and compatibility.<br>Each of the STAT[5:0] pins can be configured individually to output one of the following signals.<br>See <a href="#">Table 4-7: Output Signals Available on Programmable Multi-Function Pins</a> for Status Signal Selection Codes and Default Output Pins. |
| D7                                     | $\overline{\text{TRST}}$ | Digital Input,<br>Internal<br>Pull-down | JTAG interface reset. Digital active-low reset input. Used to reset the JTAG test sequence.<br>When LOW, the JTAG test sequence is reset.<br>When HIGH, normal operation of the JTAG test sequence resumes.                                                                                                                                                                                                                                                                                                                                |
| D8                                     | TDI                      | Digital Input,<br>Internal Pull-up      | JTAG interface Test Data Input. Serial instructions and data are received on this pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| E1, A3                                 | CT[1:0]                  | Analog Input                            | Decoupling for internal SDI termination resistors. Connect as per <a href="#">Typical Application Circuit</a> . When an input is not used, its corresponding CT pin can be left unconnected.                                                                                                                                                                                                                                                                                                                                               |
| E5, E6, F6, G6                         | CORE_VDD                 | Power                                   | Power connection for device core. Connect to 1.2V DC digital.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| E7                                     | TDO                      | Digital Output                          | JTAG interface Test Data Output. TDO is the serial output for test instructions and data.                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| E8                                     | TCK                      | Digital Input                           | JTAG interface Test Clock input. The test clock input provides the clock for the test logic of this device.                                                                                                                                                                                                                                                                                                                                                                                                                                |
| F7                                     | TMS                      | Digital Input,<br>Internal Pull-up      | JTAG interface Test Mode Select input. This signal is decoded by the internal TAP controller to control test operations.                                                                                                                                                                                                                                                                                                                                                                                                                   |
| F8                                     | SDIN                     | Digital Input                           | Serial Digital Data Input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. When GSPI is not used, SDIN should be tied HIGH or LOW to minimize noise.                                                                                                                                                                                                                                                                                                                                                            |
| G7                                     | SDOUT                    | Digital Output                          | Serial Digital Data Output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-high output. When GSPI is not used, leave unconnected.                                                                                                                                                                                                                                                                                                                                                                       |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number              | Name                                            | Type                                 | Description                                                                                                                                                                                                                                               |
|-------------------------|-------------------------------------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G8                      | SCLK                                            | Digital Input                        | Serial Data Clock input. Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. When GSPI is not used, SCLK should be tied HIGH or LOW to minimize noise.                                                     |
| H1, H2                  | NC                                              | —                                    | No connect. Pins are not connected internally.                                                                                                                                                                                                            |
| H3                      | JTAG_EN/ $\overline{\text{DIS}}$                | Digital Input,<br>Internal Pull-down | JTAG interface reset. Digital active-high to enable JTAG communications.<br>When HIGH, JTAG operational mode is enabled.<br>When LOW, JTAG operational mode is disabled.                                                                                  |
| H4                      | WCLK                                            | Output                               | 48kHz word clock for audio. When not used, leave unconnected.                                                                                                                                                                                             |
| H5                      | $\overline{\text{RESET}}$                       | Digital Input,<br>Internal Pull-up   | Device reset signal.<br>When LOW, the device will be set to default conditions.                                                                                                                                                                           |
| H6                      | BIT20/ $\overline{\text{BIT10}}$                | Digital Input,<br>Internal Pull-up   | Control signal input.<br>Used to select the output bus width.<br>HIGH = 20-bit, LOW = 10-bit.<br>Please refer to the Input Logic parameters in <a href="#">Table 2-3: DC Electrical Characteristics</a> for logic level threshold and compatibility.      |
| H7                      | $\overline{\text{CS}}$                          | Digital Input                        | Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-low input. When GSPI is not used, connect $\overline{\text{CS}}$ to IO_VDD.                                                                          |
| J1, J2                  | DDO_VDD                                         | Power                                | Power pin for the serial digital output 50Ω buffer. Connect to 1.2V or 1.8V DC analog.                                                                                                                                                                    |
| J3                      | PWR_DWN                                         | Digital Input,<br>Internal Pull-down | When HIGH, places the device in a power-down state.                                                                                                                                                                                                       |
| J4,<br>K4,<br>J6,<br>K6 | AOUT_1_2,<br>AOUT_3_4,<br>AOUT_5_6,<br>AOUT_7_8 | Output                               | Serial Audio Outputs. When not in use, leave unconnected.                                                                                                                                                                                                 |
| J5                      | ACLK                                            | Output                               | 64fs sample clock for audio. When not in use, leave unconnected.                                                                                                                                                                                          |
| K1, K2                  | $\overline{\text{DDO}}$ , DDO                   | Digital Output                       | Differential serial digital outputs. It is possible to DC-couple to downstream Semtech devices supporting 2.5V inputs. When not in use, leave unconnected.                                                                                                |
| K3                      | AUDIO_EN/ $\overline{\text{DIS}}$               | Digital Input,<br>Internal Pull-up   | Control signal input.<br>When HIGH, enables audio extraction. When LOW, disables audio extraction.<br>Please refer to the Input Logic parameters in <a href="#">Table 2-3: DC Electrical Characteristics</a> for logic level threshold and compatibility. |
| K5                      | AMCLK                                           | Output                               | Oversampled master clock for audio (128fs, 256fs, 512fs selectable). When not in use, leave unconnected.                                                                                                                                                  |

## 2. Electrical Characteristics

### 2.1 Absolute Maximum Ratings

**Table 2-1: Absolute Maximum Ratings**

| Parameter                                               | Value                  |
|---------------------------------------------------------|------------------------|
| Supply Voltage, Digital Core (CORE_VDD)                 | -0.3V to +1.5V         |
| Supply Voltage, Digital I/O (IO_VDD)                    | -0.3V to +2.8V         |
| Supply Voltage, Analog 1.2V (PLL_VDD, VCO_VDD, DDI_VDD) | -0.3V to +1.5V         |
| Supply Voltage, Analog 1.8V (DDO_VDD)                   | -0.3V to +2.0V         |
| Input Voltage Range (Digital Inputs)                    | -0.3V to IO_VDD + 0.3V |
| Ambient Operating Temperature (T <sub>A</sub> )         | -20°C to +85°C         |
| Storage Temperature (T <sub>STG</sub> )                 | -50°C to +125°C        |
| Peak Reflow Temperature (JEDEC J-STD-020C)              | 260°C                  |
| ESD Sensitivity, HBM (JESD22-A114)                      | 3kV                    |

**Note:** Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

### 2.2 Recommended Operating Conditions

**Table 2-2: Recommended Operating Conditions**

| Parameter                            | Symbol                | Conditions | Min  | Typ | Max  | Units |
|--------------------------------------|-----------------------|------------|------|-----|------|-------|
| Operating Temperature Range, Ambient | T <sub>A</sub>        | —          | -20  | —   | +85  | °C    |
| Supply Voltage, Digital Core         | CORE_VDD              | —          | 1.14 | 1.2 | 1.26 | V     |
| Supply Voltage, Digital I/O          | IO_VDD                | 1.8V mode  | 1.71 | 1.8 | 1.89 | V     |
|                                      |                       | 2.5V mode  | 2.38 | 2.5 | 2.63 | V     |
| Supply Voltage, PLL                  | PLL_VDD               | —          | 1.14 | 1.2 | 1.26 | V     |
| Supply Voltage, VCO                  | VCO_VDD               | —          | 1.14 | 1.2 | 1.26 | V     |
| Supply Voltage, Serial Digital Input | DDI0_VDD,<br>DDI1_VDD | —          | 1.14 | 1.2 | 1.26 | V     |
| Supply Voltage, CD Buffer            | DDO_VDD               | 1.2V mode  | 1.14 | 1.2 | 1.26 | V     |
|                                      |                       | 1.8V mode  | 1.71 | 1.8 | 1.89 | V     |
| Serial Input Data Rate               | —                     | —          | 270  | —   | 2970 | Mb/s  |

## 2.3 DC Electrical Characteristics

**Table 2-3: DC Electrical Characteristics**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                                                                | Symbol            | Conditions               | Min  | Typ  | Max  | Units | Notes |
|--------------------------------------------------------------------------|-------------------|--------------------------|------|------|------|-------|-------|
| <b>System</b>                                                            |                   |                          |      |      |      |       |       |
| DDI0_VDD,<br>DDI1_VDD Supply<br>Current                                  | I <sub>DDI</sub>  | 1.2V                     | 0.01 | 0.02 | 0.03 | mA    | —     |
| IO_VDD Supply<br>Current                                                 | I <sub>IO</sub>   | 1.8V                     | 7.4  | 9.2  | 10.8 | mA    | —     |
|                                                                          |                   | 2.5V                     | 12.3 | 12.5 | 12.8 | mA    | —     |
| DDO_VDD Supply<br>Current                                                | I <sub>DDO</sub>  | 1.2V                     | 7.4  | 9.1  | 10.7 | mA    | —     |
|                                                                          |                   | 1.8V                     | 7.4  | 9.1  | 10.7 | mA    | —     |
| VCO_VDD Supply<br>Current                                                | I <sub>VCO</sub>  | 1.2V                     | 7.0  | 7.8  | 9.4  | mA    | —     |
| PLL_VDD Supply<br>Current                                                | I <sub>PLL</sub>  | 1.2V                     | 50.3 | 63.0 | 74.5 | mA    | —     |
| CORE_VDD Supply<br>Current                                               | I <sub>CORE</sub> | 1.2V                     | 17.7 | 20.3 | 22.2 | mA    | —     |
| Total Device Power<br>DDO_VDD = 1.2V<br>IO_VDD = 1.8V<br>(Audio Enabled) | P                 | 10-bit 3GA               | 160  | 191  | 227  | mW    | —     |
|                                                                          |                   | 10-bit 3GB               | 135  | 158  | 192  | mW    | —     |
|                                                                          |                   | 20-bit 3GA               | 137  | 161  | 193  | mW    | —     |
|                                                                          |                   | 20-bit 3GB               | 154  | 184  | 230  | mW    | —     |
|                                                                          |                   | 10-bit HD                | 125  | 148  | 179  | mW    | —     |
|                                                                          |                   | 20-bit HD                | 109  | 129  | 170  | mW    | —     |
|                                                                          |                   | 10/20-bit SD             | 97   | 109  | 141  | mW    | —     |
|                                                                          |                   | DVB-ASI                  | —    | 103  | —    | mW    | —     |
|                                                                          |                   | Sleep                    | 3.3  | 5    | 11.3 | mW    | —     |
|                                                                          |                   | Standby with DDO Retimed | 82   | 105  | 121  | mW    | —     |
| Total Device Power<br>DDO_VDD = 1.8V<br>IO_VDD = 2.5V<br>(Audio Enabled) | P                 | 10-bit 3GA               | 275  | 287  | 300  | mW    | —     |
|                                                                          |                   | 10-bit 3GB               | 224  | 230  | 237  | mW    | —     |
|                                                                          |                   | 20-bit 3GA               | 219  | 228  | 241  | mW    | —     |
|                                                                          |                   | 20-bit 3GB               | 276  | 286  | 325  | mW    | —     |
|                                                                          |                   | 10-bit HD                | 211  | 218  | 221  | mW    | —     |
|                                                                          |                   | 20-bit HD                | 165  | 174  | 209  | mW    | —     |
|                                                                          |                   | 10/20-bit SD             | 125  | 132  | 164  | mW    | —     |
|                                                                          |                   | DVB-ASI                  | —    | 121  | —    | mW    | —     |
|                                                                          |                   | Sleep                    | 7.1  | 10.1 | 16.9 | mW    | —     |
|                                                                          |                   | Standby with DDO Retimed | 108  | 127  | 163  | mW    | —     |

**Table 2-3: DC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                         | Symbol          | Conditions                            | Min          | Typ                             | Max          | Units | Notes |
|-----------------------------------|-----------------|---------------------------------------|--------------|---------------------------------|--------------|-------|-------|
| Digital I/O                       |                 |                                       |              |                                 |              |       |       |
| Input Logic LOW                   | V <sub>IL</sub> | 2.5V or 1.8V operation                | —            | —                               | 0.3 x IO_VDD | V     | —     |
| Input Logic HIGH                  | V <sub>IH</sub> | 2.5V or 1.8V operation                | 0.7 x IO_VDD | —                               | —            | V     | —     |
| Output Logic LOW                  | V <sub>OL</sub> | I <sub>OL</sub> = 8mA, 1.8V operation | —            | —                               | 0.41         | V     | —     |
|                                   |                 | I <sub>OL</sub> = 8mA, 2.5V operation | —            | —                               | 0.29         | V     | —     |
| Output Logic HIGH                 | V <sub>OH</sub> | I <sub>OL</sub> = 8mA, 1.8V operation | 1.49         | —                               | —            | V     | —     |
|                                   |                 | I <sub>OL</sub> = 8mA, 2.5V operation | 2.27         | —                               | —            | V     | —     |
| Serial Input                      |                 |                                       |              |                                 |              |       |       |
| Serial Input Common Mode Voltage  | —               | AC or DC-coupled                      | 0.90         | 0.96                            | 1.06         | V     | —     |
| Serial Output                     |                 |                                       |              |                                 |              |       |       |
| Serial Output Common Mode Voltage | —               | 50Ω load                              | —            | DDO_VDD - V <sub>swing</sub> /2 | —            | V     | 1     |

**Note:**

1. Serial output swing limited when using  $DDO\_VDD = 1.2V$ .

## 2.4 AC Electrical Characteristics

**Table 2-4: AC Electrical Characteristics**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                                                          | Symbol             | Conditions              | Min | Typ                            | Max | Units | Notes |
|--------------------------------------------------------------------|--------------------|-------------------------|-----|--------------------------------|-----|-------|-------|
| <b>System</b>                                                      |                    |                         |     |                                |     |       |       |
| Device Latency:<br>AUDIO_EN = 1,<br>SMPTE mode,<br>IOPROC_EN = 1   | —                  | 3G (Level A)            | 65  | 67                             | 69  | PCLK  | —     |
|                                                                    |                    | 3G (Level B)            | 141 | 144                            | 147 | PCLK  | —     |
|                                                                    |                    | HD                      | 65  | 67                             | 69  | PCLK  | —     |
|                                                                    |                    | SD                      | 37  | 39                             | 41  | PCLK  | —     |
| Device Latency:<br>AUDIO_EN = 0,<br>SMPTE mode,<br>IOPROC_EN = 1   | —                  | 3G (Level A)            | 28  | 30                             | 32  | PCLK  | —     |
|                                                                    |                    | 3G (Level B)            | 63  | 65                             | 67  | PCLK  | —     |
|                                                                    |                    | HD                      | 25  | 27                             | 29  | PCLK  | —     |
|                                                                    |                    | SD                      | 25  | 27                             | 29  | PCLK  | —     |
| Device Latency:<br>AUDIO_EN = 0,<br>SMPTE mode,<br>IOPROC_EN = 0   | —                  | 3G (Level A)            | 20  | 22                             | 24  | PCLK  | —     |
|                                                                    |                    | 3G (Level B)            | 47  | 50                             | 53  | PCLK  | —     |
|                                                                    |                    | HD                      | 21  | 23                             | 25  | PCLK  | —     |
|                                                                    |                    | SD                      | 19  | 21                             | 23  | PCLK  | —     |
| Device Latency:<br>AUDIO_EN = 0,<br>SMPTE bypass,<br>IOPROC_EN = 0 | —                  | 3G (Level A)            | 11  | 13                             | 15  | PCLK  | —     |
|                                                                    |                    | 3G (Level B)            | 11  | 13                             | 15  | PCLK  | —     |
|                                                                    |                    | HD                      | 11  | 13                             | 15  | PCLK  | —     |
|                                                                    |                    | SD                      | 11  | 13                             | 15  | PCLK  | —     |
| Device Latency: DVB-ASI                                            | —                  | —                       | 12  | 14                             | 16  | PCLK  | —     |
| Reset Time                                                         | t <sub>reset</sub> | —                       | 1   | —                              | —   | ms    | —     |
| <b>Parallel Output</b>                                             |                    |                         |     |                                |     |       |       |
| Parallel Clock Frequency                                           | f <sub>PCLK</sub>  | 3G/ HD (10-bit)         | —   | 148.5<br>or<br>148.5/<br>1.001 | —   | MHz   | —     |
|                                                                    |                    | HD (20-bit), 10-bit DDR | —   | 74.25<br>or<br>74.25/<br>1.001 | —   | MHz   | —     |
|                                                                    |                    | SD (20-bit), 10-bit DDR | —   | 13.5                           | —   | MHz   | —     |
|                                                                    |                    | SD (10-bit)             | —   | 27                             | —   | MHz   | —     |

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                    | Symbol                             | Conditions | Min  | Typ | Max | Units | Notes |
|------------------------------|------------------------------------|------------|------|-----|-----|-------|-------|
| Parallel Clock Duty Cycle    | DC <sub>PCLK</sub>                 | —          | —    | 50  | —   | %     | —     |
| Output Data Hold Time (1.8V) | 6pF C <sub>load</sub>              | SPI        | 1.5  | —   | —   | ns    | —     |
|                              |                                    | AUDIO      | 1.5  | —   | —   | ns    | —     |
|                              | 3G 10-bit<br>6pF C <sub>load</sub> | DOUT       | 0.3  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 0.3  | —   | —   | ns    | —     |
|                              | 3G 20-bit<br>6pF C <sub>load</sub> | DOUT       | 0.5  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 0.5  | —   | —   | ns    | —     |
|                              | HD 10-bit<br>6pF C <sub>load</sub> | DOUT       | 1.5  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 1.5  | —   | —   | ns    | —     |
|                              | HD 20-bit<br>6pF C <sub>load</sub> | DOUT       | 5.0  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 5.0  | —   | —   | ns    | —     |
|                              | SD 10-bit<br>6pF C <sub>load</sub> | DOUT       | 15.0 | —   | —   | ns    | —     |
|                              |                                    | STAT       | 15.0 | —   | —   | ns    | —     |
|                              | SD 20-bit<br>6pF C <sub>load</sub> | DOUT       | 30.0 | —   | —   | ns    | —     |
|                              |                                    | STAT       | 30.0 | —   | —   | ns    | —     |
| Output Data Hold Time (2.5V) | 6pF C <sub>load</sub>              | SPI        | 1.5  | —   | —   | ns    | —     |
|                              |                                    | AUDIO      | 1.5  | —   | —   | ns    | —     |
|                              | 3G 10-bit<br>6pF C <sub>load</sub> | DOUT       | 0.3  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 0.3  | —   | —   | ns    | —     |
|                              | 3G 20-bit<br>6pF C <sub>load</sub> | DOUT       | 0.5  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 0.5  | —   | —   | ns    | —     |
|                              | HD 10-bit<br>6pF C <sub>load</sub> | DOUT       | 1.5  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 1.5  | —   | —   | ns    | —     |
|                              | HD 20-bit<br>6pF C <sub>load</sub> | DOUT       | 4.0  | —   | —   | ns    | —     |
|                              |                                    | STAT       | 4.0  | —   | —   | ns    | —     |
|                              | SD 10-bit<br>6pF C <sub>load</sub> | DOUT       | 15.0 | —   | —   | ns    | —     |
|                              |                                    | STAT       | 15.0 | —   | —   | ns    | —     |
|                              | SD 20-bit<br>6pF C <sub>load</sub> | DOUT       | 30.0 | —   | —   | ns    | —     |
|                              |                                    | STAT       | 30.0 | —   | —   | ns    | —     |

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                         | Symbol    | Conditions                   | Min   | Typ | Max  | Units | Notes |
|-----------------------------------|-----------|------------------------------|-------|-----|------|-------|-------|
| Output Data Delay Time (1.8V)     | $t_{od}$  | 15pF $C_{load}$              | SPI   | —   | 28.0 | ns    | —     |
|                                   |           |                              | AUDIO | —   | 10.0 | ns    | —     |
|                                   |           | 3G 10-bit<br>15pF $C_{load}$ | DOUT  | —   | 2.4  | ns    | —     |
|                                   |           |                              | STAT  | —   | 2.8  | ns    | —     |
|                                   |           | 3G 20-bit<br>15pF $C_{load}$ | DOUT  | —   | 6.0  | ns    | —     |
|                                   |           |                              | STAT  | —   | 6.3  | ns    | —     |
|                                   |           | HD 10-bit<br>15pF $C_{load}$ | DOUT  | —   | 4.0  | ns    | —     |
|                                   |           |                              | STAT  | —   | 4.2  | ns    | —     |
|                                   |           | HD 20-bit<br>15pF $C_{load}$ | DOUT  | —   | 14.2 | ns    | —     |
|                                   |           |                              | STAT  | —   | 14.4 | ns    | —     |
|                                   |           | SD 10-bit<br>15pF $C_{load}$ | DOUT  | —   | 21.0 | ns    | —     |
|                                   |           |                              | STAT  | —   | 21.0 | ns    | —     |
|                                   |           | SD 20-bit<br>15pF $C_{load}$ | DOUT  | —   | 40.0 | ns    | —     |
|                                   |           |                              | STAT  | —   | 40.0 | ns    | —     |
| Output Data Delay Time (2.5V)     | $t_{od}$  | 15pF $C_{load}$              | SPI   | —   | 28.0 | ns    | —     |
|                                   |           |                              | AUDIO | —   | 10.0 | ns    | —     |
|                                   |           | 3G 10-bit<br>15pF $C_{load}$ | DOUT  | —   | 2.3  | ns    | —     |
|                                   |           |                              | STAT  | —   | 2.8  | ns    | —     |
|                                   |           | 3G 20-bit<br>15pF $C_{load}$ | DOUT  | —   | 6.0  | ns    | —     |
|                                   |           |                              | STAT  | —   | 6.3  | ns    | —     |
|                                   |           | HD 10-bit<br>15pF $C_{load}$ | DOUT  | —   | 3.8  | ns    | —     |
|                                   |           |                              | STAT  | —   | 4.2  | ns    | —     |
|                                   |           | HD 20-bit<br>15pF $C_{load}$ | DOUT  | —   | 13.0 | ns    | —     |
|                                   |           |                              | STAT  | —   | 13.5 | ns    | —     |
|                                   |           | SD 10-bit<br>15pF $C_{load}$ | DOUT  | —   | 21.0 | ns    | —     |
|                                   |           |                              | STAT  | —   | 21.0 | ns    | —     |
|                                   |           | SD 20-bit<br>15pF $C_{load}$ | DOUT  | —   | 40.0 | ns    | —     |
|                                   |           |                              | STAT  | —   | 40.0 | ns    | —     |
| Output Data Rise/Fall Time (1.8V) | $t_r/t_f$ | 6pF $C_{load}$               | STAT  | —   | 3.1  | ns    | —     |
|                                   |           |                              | DOUT  | —   | 3.1  | ns    | —     |
|                                   |           |                              | AUDIO | —   | 3.3  | ns    | —     |

**Table 2-4: AC Electrical Characteristics (Continued)**

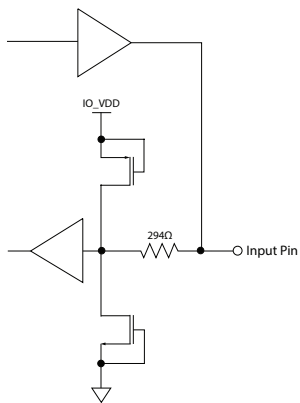
Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                              | Symbol           | Conditions                                 | Min   | Typ  | Max  | Units             | Notes |   |
|----------------------------------------|------------------|--------------------------------------------|-------|------|------|-------------------|-------|---|
| Output Data Rise/Fall Time (2.5V)      | $t_r/t_f$        | 6pF $C_{load}$                             | STAT  | —    | —    | 2.1               | ns    | — |
|                                        |                  |                                            | DOUT  | —    | —    | 2.1               | ns    | — |
|                                        |                  |                                            | AUDIO | —    | —    | 2.2               | ns    | — |
| Serial Digital Input                   |                  |                                            |       |      |      |                   |       |   |
| Serial Input Data Rate                 | $DR_{SDI}$       | —                                          | 0.27  | —    | 2.97 | Gb/s              | —     |   |
| Serial Input Swing                     | $\Delta V_{DDI}$ | Differential with 100Ω load                | 200   | 400  | 1000 | mV <sub>ppd</sub> | —     |   |
| Serial Input Jitter Tolerance          | SIJT             | Nominal loop bandwidth<br>Square wave mod. | 0.8   | —    | —    | UI                | —     |   |
| Serial Digital Output                  |                  |                                            |       |      |      |                   |       |   |
| Serial Output Data Rate                | $DR_{DDO}$       | —                                          | 0.27  | —    | 2.97 | Gb/s              | —     |   |
| Serial Output Swing                    | $\Delta V_{DDO}$ | Differential with 100Ω load                | 200   | 400  | 1000 | mV <sub>ppd</sub> | 2     |   |
| Serial Output Rise Time<br>20% ~ 80%   | $t_{rDDO}$       | —                                          | —     | 112  | 135  | ps                | —     |   |
| Serial Output Fall Time<br>20% ~ 80%   | $t_{fDDO}$       | —                                          | —     | 114  | 135  | ps                | —     |   |
| Rise/ Fall Mismatch                    |                  | —                                          | —     | 2    | 8    | ps                | —     |   |
| Serial Output Intrinsic Jitter         | $t_{OJ}$         | 3G PRBS                                    | 0.05  | 0.06 | 0.08 | UI                | 3     |   |
|                                        |                  | HD PRBS                                    | 0.03  | 0.04 | 0.05 | UI                | 3     |   |
|                                        |                  | SD PRBS                                    | 0.01  | 0.02 | 0.03 | UI                | 3     |   |
| Serial Output Duty Cycle<br>Distortion | $DCD_{SDD}$      | 3G                                         | 3     | 5    | 10   | ps                | —     |   |
|                                        |                  | HD                                         | 1     | 5    | 7    | ps                | —     |   |
|                                        |                  | SD                                         | 1     | 2    | 5    | ps                | —     |   |
| Asynchronous Lock Time                 | —                | —                                          | —     | —    | 750  | μs                | —     |   |
| Lock Time from Power-up                | —                | After 20 minutes<br>at -20°C               | —     | 725  | —    | ms                | —     |   |

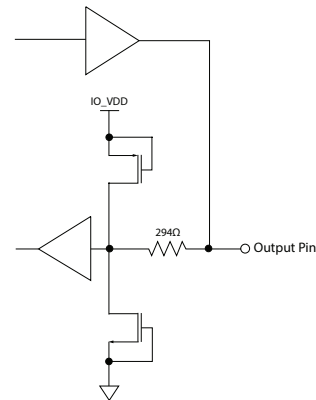
**Notes:**

1. Serial output swing limited when using DDO\_VDD = 1.2V
2. Serial output swing can be adjusted through GSPI.
3. Retiming enabled.

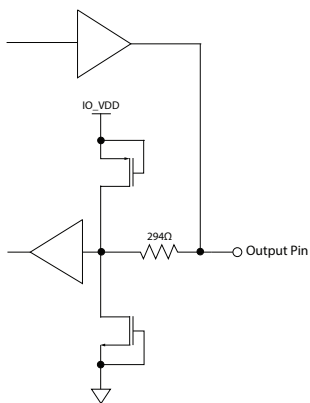
### 3. Input/Output Circuits



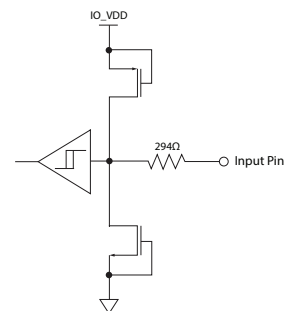
**Figure 3-1: Bidirectional Digital Input/Output Pin Configured as an Input (SDIN, CS, SCLK)**



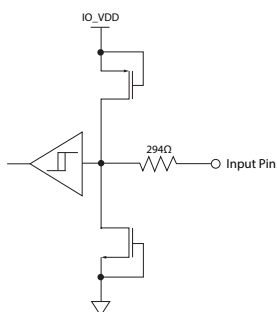
**Figure 3-2: Bidirectional Digital Input/Output Pin Configured as an Output (AMCLK, TDO, SDOUT, WCLK, AOUT\_1\_2, AOUT\_3\_4, AOUT\_5\_6, AOUT\_7\_8, ACLK)**



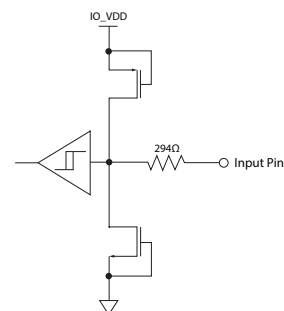
**Figure 3-3: Bidirectional Digital Input/Output Pin Configured as an Output with Programmable Drive Strength (DOUT[19:0], PCLK, STAT[5:0])**



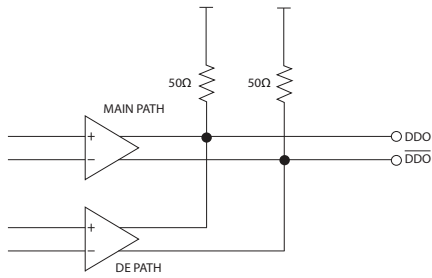
**Figure 3-4: Digital Input with Schmitt Trigger and 100kΩ Internal Pull-Up (AUDIO\_EN/DIS, TDI, TMS, RESET, BIT20/BIT10)**



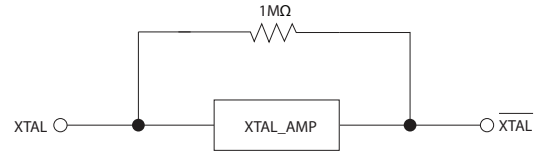
**Figure 3-5: Digital Input with Schmitt Trigger and 100kΩ Internal Pull-Down (TRST, JTAG\_EN/DIS, PWR\_DWN)**



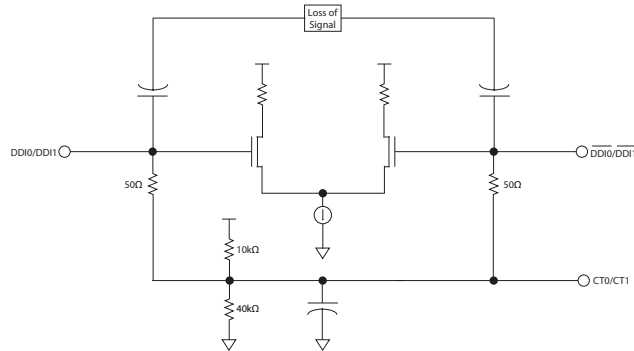
**Figure 3-6: Digital Input with Schmitt Trigger (TCK)**



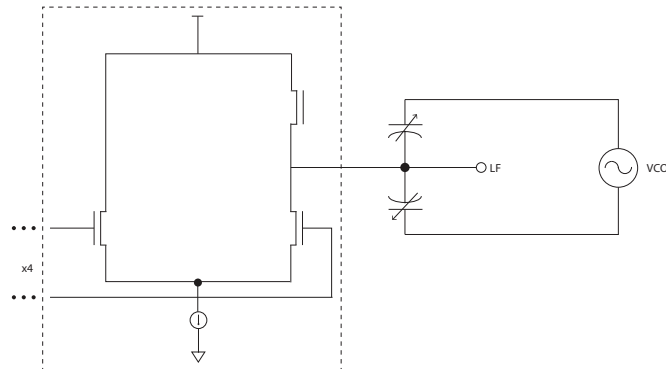
**Figure 3-7: DDO/DDO**



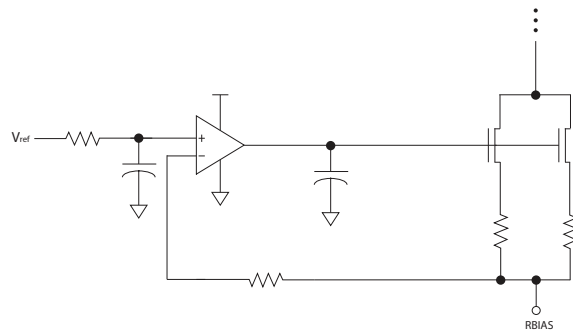
**Figure 3-8: XTAL/XTAL**



**Figure 3-9: DDI0/DDI0, DDI1/DDI1, CT[1:0]**



**Figure 3-10: LF**



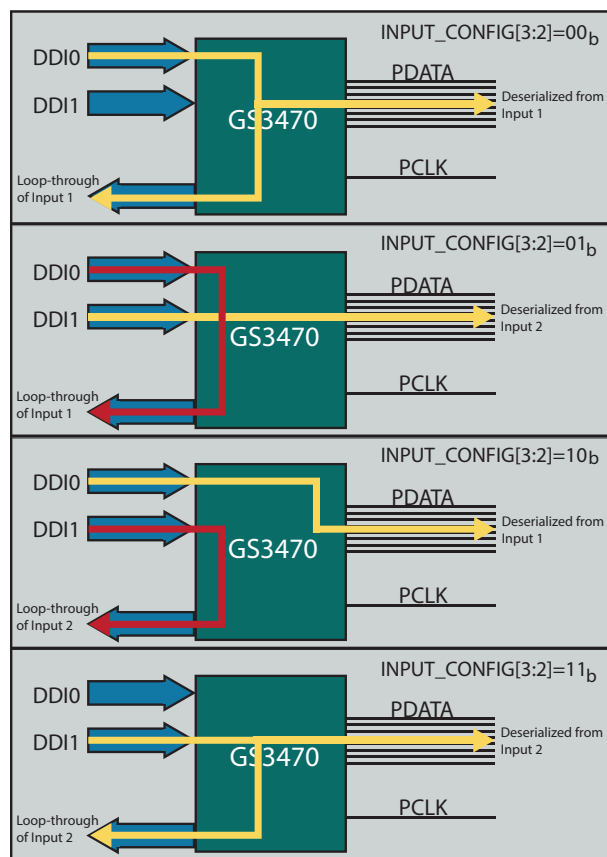
**Figure 3-11: RBIAS**

## 4. Detailed Description

### 4.1 Functional Overview

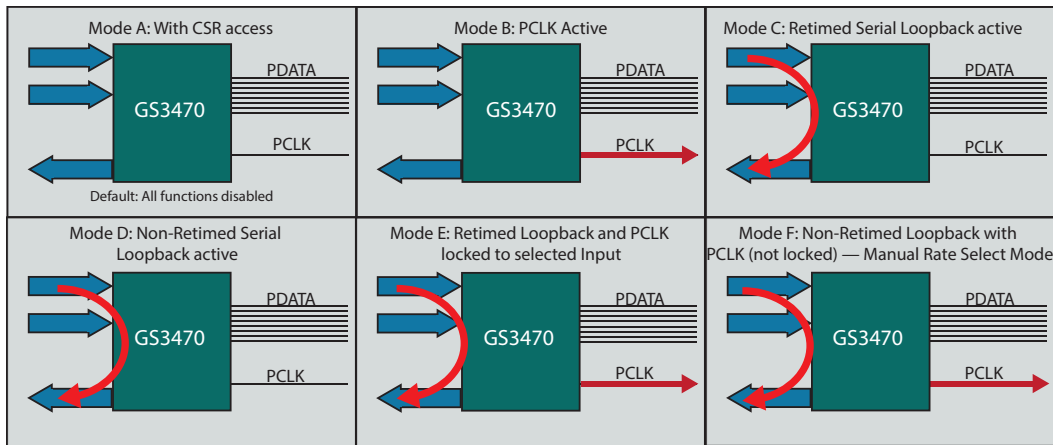
The GS3470 includes a dual serial digital input buffer with 2x2 MUX, an integrated retimer, serial data loop through output, robust serial-to-parallel conversion, integrated SMPTE video processing, and additional processing functions such as audio extraction, ancillary data extraction, EDH support, and DVB-ASI decoding.

The serial digital input buffer with 2x2 MUX offers a lot of flexibility for use in default and various Power-down modes. From Figure 4-1 below, the top two blocks shown represent input select with loopback, while the bottom two allow input select with separate loopback select.



**Figure 4-1: Flexible Input Loopback**

Expanded and configurable Power-down modes offer increased flexibility by selectively enabling or disabling key features (such as CSR access, PCLK, retimed DDO loop-through output, and non-retimed DDO loop-through output). Figure 4-2 show the various Power-down modes.



**Figure 4-2: Flexible Power Down Modes**

The device has three other primary modes of operation which include SMPTE mode, DVB-ASI mode, and Data-Through mode. In SMPTE mode, when receiving a SMPTE compliant SDI input, the GS3470 performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities. The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. Packet detection and error handling features are also offered. All processing features are optional, and may be individually enabled or disabled through register programming. In DVB-ASI mode, sync word detection, alignment, and 8/10bit decoding is applied to the received data stream. While in Data-Through mode, all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

The GS3470 includes an audio de-embedder and audio clocks are internally generated. Up to eight channels (two audio groups) of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272-C and SMPTE ST 299. The output audio formats supported by the device include AES/EBU and I<sup>2</sup>S. A variety of audio processing features are provided to ease implementation.

## 4.2 Device Power-Up

The GS3470 is designed to operate in a multi-voltage environment which allows any power-up sequence to be used. Supply pins can all be powered up in any order.

### 4.2.1 Power-Down Mode

The *PWR\_DWN* pin reduces power to a minimum by disabling various device features. When the *PWR\_DWN* pin is de-asserted, the device returns to its previous operating condition within 1 second, without requiring input from the host interface. There are several power-down options which can be configured through GSPI prior to the device going into power-down. Table 4-1 provides a summary of the supported power-down options by accessing the **POWER\_DOWN** register.

**Table 4-1: Power-down Mode**

| Power-down Mode                                                                                                       | CSR Access | DDO Loop-through Mode   | PCLK Mode     |
|-----------------------------------------------------------------------------------------------------------------------|------------|-------------------------|---------------|
| <b>Power-down</b><br>PD_PCLK_ENABLE = 0<br>SERIAL_LOOPBACK_EN = 0<br>PD_CSR_ACCESS = 0<br>RC_BYP = X                  | No         | DDO Disabled            | PCLK Disabled |
| <b>Power-down with CSR Access</b><br>PD_PCLK_ENABLE = 0<br>SERIAL_LOOPBACK_EN = 0<br>PD_CSR_ACCESS = 1<br>RC_BYP = X  | Yes        | DDO Disabled            | PCLK Disabled |
| <b>Power-down with PCLK</b><br>PD_PCLK_ENABLE = 1<br>SERIAL_LOOPBACK_EN = 0<br>PD_CSR_ACCESS = X<br>RC_BYP = X        | Yes        | DDO Disabled            | PCLK Enabled  |
| <b>Power-down with DDO</b><br>PD_PCLK_ENABLE = 0<br>SERIAL_LOOPBACK_EN = 1<br>PD_CSR_ACCESS = X<br>RC_BYP = 1         | No         | DDO Enabled Non-retimed | PCLK Disabled |
| <b>Power-down with DDO retimed</b><br>PD_PCLK_ENABLE = 0<br>SERIAL_LOOPBACK_EN = 1<br>PD_CSR_ACCESS = X<br>RC_BYP = 0 | Yes        | DDO Enabled Retimed     | PCLK Disabled |

**Table 4-1: Power-down Mode**

| Power-down Mode                                                                 | CSR Access | DDO Loop-through Mode      | PCLK Mode    |
|---------------------------------------------------------------------------------|------------|----------------------------|--------------|
| <b>Power-down with DDO/PCLK</b>                                                 |            |                            |              |
| PD_PCLK_ENABLE = 1<br>SERIAL_LOOPBACK_EN = 1<br>PD_CSR_ACCESS = X<br>RC_BYP = 1 | Yes        | DDO Enabled<br>Non-retimed | PCLK Enabled |
| <b>Power-down with DDO/PCLK retimed</b>                                         |            |                            |              |
| PD_PCLK_ENABLE = 1<br>SERIAL_LOOPBACK_EN = 1<br>PD_CSR_ACCESS = X<br>RC_BYP = 0 | Yes        | DDO Enabled<br>Retimed     | PCLK Enabled |

**Table 4-2: Status Output Support in Power Down Modes**

| Mode                                  | Rate Detect                                     | Carrier Detect     | Lock                                    | All Other Status Outputs |
|---------------------------------------|-------------------------------------------------|--------------------|-----------------------------------------|--------------------------|
| Sleep                                 | N/A                                             | N/A                | N/A                                     | N/A                      |
| Sleep with DDO not retimed            | N/A                                             | N/A                | N/A                                     | N/A                      |
| Standby with DDO retimed              | Available in automatic or manual modes          | Analog detect only | Locked status available on STAT outputs | N/A                      |
| Standby with PCLK                     | Available in manual mode only, rate must be set | Analog detect only | N/A                                     | N/A                      |
| Standby with PCLK and DDO retimed     | Available in automatic or manual modes          | Analog detect only | Locked status available on STAT outputs | N/A                      |
| Standby with PCLK and DDO not retimed | Available in manual mode only, rate must be set | Analog detect only | N/A                                     | N/A                      |
| Standby with CSR access               | N/A                                             | Analog detect only | N/A                                     | N/A                      |

## 4.2.2 Device Reset

**Note:** On power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the  $\overline{RESET}$  signal LOW for a minimum of  $t_{reset} = 1\text{ ms}$  after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs are driven to a high-impedance state, with the exception of  $SDOUT$ .  $SDOUT$  continues normal operation during reset.

GSPI access is restored 10 clock cycles after  $\overline{RESET}$  is de-asserted.

All output buffers (including the  $PCLK$  output), are set to high-impedance in Reset mode ( $\overline{RESET} = \text{LOW}$ ).

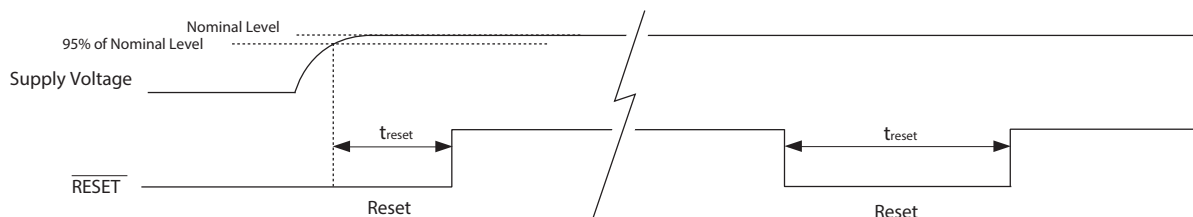


Figure 4-3: Reset Pulse

## 4.3 Modes of Operation

### 4.3.1 Auto and Manual Mode

The lock detection algorithm is a continuous process, beginning at device power-up or after a system reset. It continues until the device is powered down or held in reset.

The device first determines if a valid serial digital input signal has been presented to the device. If no valid serial data stream has been detected, the serial data into the device is considered invalid, and the LOCKED signal is LOW.

Once a valid input signal has been detected, the device attempts to detect the presence of either TRS words or DVB-ASI sync words.

By default, the device powers up in Auto mode (the **AUTO\_** $\overline{MAN}$  bit in the host interface is set HIGH). In this mode, the device operating frequency toggles between 3G, HD, and SD rates as it attempts to lock to the incoming data rate. As it searches through rates,  $PCLK$  output cycles through 148.5MHz, 74.25MHz, 27MHz, and 13.5MHz. The  $PCLK$  output pin can be set to be high-impedance when not locked through GSPI.

When the device is operating in Manual mode (**AUTO\_** $\overline{MAN}$  bit in the host interface register is LOW), the operating frequency needs to be set through the **RATE\_SEL\_TOP** bits in the host interface. **RATE\_SEL\_TOP[0]** =  $SD/\overline{HD}$  and **RATE\_SEL\_TOP[1]** =  $3G/\overline{HD}$ .

**Note:** The  $SD/\overline{HD}$  bit takes precedence over the  $3G/\overline{HD}$  bit, so if the  $SD/\overline{HD}$  bit is HIGH, the  $3G/\overline{HD}$  bit is ignored.

---

## 4.3.2 Low Latency Video Path

The GS3470 has a low latency mode of operation for audio and ancillary data extraction.

Audio can be extracted without incurring any associated delay if the error correction feature and audio packet delete feature are not required. The device will automatically select low latency mode if the **ALL\_DEL** CSR bit is set LOW (SD) or **ALL\_DEL** CSR bit is set LOW and **ECC\_OFF** CSR bit is set HIGH (HD/3G). This means that in low latency mode for audio, ECC errors in the HD/3G audio data packets will not be corrected and no audio packets will be deleted from the data stream after extraction. If either of these features are desired, then a delay will be incurred through the audio extraction blocks. To maintain consistent delay independent of selected features, the **LOW\_LATENCY\_BYPASS** bit must be set HIGH.

Ancillary data will automatically be extracted without incurring any associated delay if the **ANC\_DATA\_DEL** CSR bit is set LOW.

## 4.3.3 SMPTE and SMPTE Bypass Mode

The GS3470 has the ability to run either in SMPTE mode or SMPTE Bypass mode.

In SMPTE mode (**SMPTE\_BYPASS** = HIGH), the timing signal generator becomes operational, video signals error detection and SMPTE processing functions are available, and the retimer PLL locks to valid SMPTE video.

In SMPTE Bypass mode (**SMPTE\_BYPASS** = LOW), the GS3470 operates either in DVB-ASI mode or Data-Through mode. When operating in SMPTE Bypass mode, none of the SMPTE detection and processing functions are available.

### 4.3.3.1 Descrambling and Word Alignment

The GS3470 performs NRZI (Non Return to Zero Invert) to NRZ (Non Return to Zero) decoding and data descrambling according to SMPTE ST 424/SMPTE ST 292/SMPTE ST 259-C and word aligns the data to TRS sync words.

When operating in Manual mode (**AUTO\_MAN** = LOW), the device only carries out SMPTE decoding, descrambling, and word alignment, when the **SMPTE\_BYPASS** bit is set HIGH and the DVB\_ASI bit is set LOW.

When operating in Auto mode (**AUTO\_MAN** = HIGH), the GS3470 carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

TRS ID word detection is a continuous process. The device remains in SMPTE mode until TRS ID words fail to be detected.

**Note 1:** Both 8-bit and 10-bit TRS headers are identified by the device.

**Note 2:** In 3G Level B mode, the device only supports Data Stream 1 and Data Stream 2 having the same bit width (i.e. both data streams contain 8-bit data, or both data streams contain 10-bit data). If the bit widths between the two data streams are different, the GS3470 cannot word align the input stream. When **SMPTE\_BYPASS** is HIGH and the device is set to Auto mode, it will continuously try to lock.

---

### 4.3.4 DVB-ASI Mode

When in DVB-ASI mode ( $\overline{\text{SMPTE\_BYPASS}}$  = LOW and DVB\_ASI = HIGH), the retimer PLL locks to a DVB-ASI stream. In DVB-ASI mode, the parallel outputs are configured appropriately as described in [4.9.3 Parallel Output in DVB-ASI Mode](#). None of the SMPTE detection and processing functions are available in this mode.

## 4.4 Digital Differential Input (DDI/ $\overline{\text{DDI}}$ )

The GS3470 can accept two serial digital inputs compliant with SMPTE ST 424, SMPTE 292, and SMPTE ST 259-C— however, only one of the input serial data streams can be retimed. The GS3470 contains a 100 $\Omega$  differential input buffer which can be DC-coupled to Semtech equalizers, but only if equalizer output stage is connected to 1.2V. Otherwise must be AC coupled.

See [Figure 4-1](#) for a visualization of the Flex Input Loopback.

**INPUT\_CONFIG[3:2]** allows for selection of DDI0 or DDI1 into the parallel retimed output and DDO path.

**LOS\_CTRL[8]** register contains the LOS\_AFE\_SEL bit, which allows for selection of DDI0 or DDI1 for LOS sensing.

## 4.5 Serial Digital Loop-Through Output

The GS3470 contains a differential serial digital output buffer. This output provides an active loop-through of the input signal. It can be a reclocked or non-reclocked version of the input used for processing or a non-reclocked version of the other input. Moreover, selection of the loop-through output is independent of the selection of the signal going into the de-serializer block.

[Table 4-3](#) provides a summary of all the options available for the serial digital output.

The DDO,  $\overline{\text{DDO}}$  differential signal is capable of driving a Semtech Cable Driver through at least 150mm of 100 $\Omega$  differential FR4 trace, such that the Cable Driver output conforms to the relevant SMPTE specification for the data rate, with the exception of the jitter specifications.

The output can be DC-coupled into Semtech Cable Drivers that support 1.2V, 1.8V and 2.5V inputs.

The output buffer may be disabled to achieve power savings. This can be done using the **SERIAL\_LOOPBACK\_EN** bit through the GSPI interface.

**Table 4-3: Serial Digital Output**

| SERIAL_LOOPBACK_EN | RC_BYP | DDO/ $\overline{\text{DDO}}$ |
|--------------------|--------|------------------------------|
| 0                  | X      | Disabled                     |
| 1                  | 0      | Re-timed                     |
| 1                  | 1      | Buffered (not Re-timed)      |

## 4.6 Serial Digital Retimer

The retimer operates at three frequencies: 2.97Gb/s, 1.485Gb/s, and 270Mb/s.

**Note:** The  $\text{SD}/\overline{\text{HD}}$  bit takes precedence over the  $3\text{G}/\overline{\text{HD}}$  bit, so if the  $\text{SD}/\overline{\text{HD}}$  bit is HIGH, the  $3\text{G}/\overline{\text{HD}}$  bit is ignored.

The retimer can automatically determine the supported rate based on the input signal, or the rate can be set manually. For more detail on these modes, please refer to [Section 4.3.1](#).

## 4.7 External Crystal/Reference Clock

The GS3470 requires an external 27MHz reference clock for correct operation. This reference clock is generated by connecting a crystal to the  $\text{XTAL}$  and  $\overline{\text{XTAL}}$  pins of the device. Refer to [Typical Application Circuit](#).

A crystal with a maximum frequency variation of  $\pm 100\text{ppm}$  and a maximum equivalent resistance of  $50\Omega$  should be selected. The external crystal is used in the frequency acquisition process. It has no impact on the output jitter performance of the device when the device is locked to incoming data.

Alternately, a 27MHz external clock source can be connected to the  $\overline{\text{XTAL}}$  pin of the device. It is recommended to DC-couple the reference clock input and to ensure the reference clock does not exceed 1.2V.

## 4.8 Lock Detect

The LOCKED output signal is set HIGH by the Lock Detect block under the following conditions:

**Table 4-4: Lock Detect Conditions**

| Mode of Operation | Mode Setting                                                           | Condition for Locked                        |
|-------------------|------------------------------------------------------------------------|---------------------------------------------|
| SMPTE Mode        | $\text{SMPTE\_BYPASS} = \text{HIGH}$<br>$\text{DVB\_ASI} = \text{LOW}$ | Retimer PLL is locked to valid SMPTE video. |

**Table 4-4: Lock Detect Conditions (Continued)**

| Mode of Operation | Mode Setting                                                                      | Condition for Locked                       |
|-------------------|-----------------------------------------------------------------------------------|--------------------------------------------|
| DVB-ASI Mode      | $\overline{\text{SMPTE\_BYPASS}} = \text{LOW}$<br>$\text{DVB\_ASI} = \text{HIGH}$ | Retimer PLL is locked to a DVB-ASI stream. |
| Data-Through Mode | $\overline{\text{SMPTE\_BYPASS}} = \text{LOW}$<br>$\text{DVB\_ASI} = \text{LOW}$  | Retimer PLL is locked.                     |

The LOCKED output signal is available by default on the *STAT3* output pin, but can be programmed to be output through any one of the six programmable multi-functional pins of the device, *STAT[5:0]*.

**Note:** In Power-down mode with **RC\_BYP** disabled, the PLL unlocks. However, the LOCKED signal retains whatever state it previously held. For instance, if before power-down assertion the LOCKED signal is HIGH, during power-down it will remain HIGH regardless of the status of the PLL.

## 4.9 Parallel Data Outputs

A 20-bit parallel bus is available which can be configured in 10-bit or 20-bit mode. The parallel data outputs are aligned to the rising edge of the PCLK.

### 4.9.1 Parallel Data Bus Output Levels

The parallel data bus supports 1.8V or 2.5V (LVTTTL and LVCMOS levels) supplied at the *IO\_VDD* pins.

### 4.9.2 Parallel Output in SMPTE Mode

When the device is operating in SMPTE mode ( $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$ ), data is output in either multiplexed or demultiplexed form depending on the setting of the *20BIT\_10BIT* pin or **PIN\_CSR\_SELECT** register (877<sub>h</sub>).

When operating in 20-bit mode (*20BIT\_10BIT* = HIGH), the output data is demultiplexed Luma (*DOUT[19:10]*) and Chroma (*DOUT[9:0]*) data for SD and HD data rates. For 3G data rate, Data Stream 1 is output on the *DOUT[19:10]* pins and Data Stream 2 is output on the *DOUT[9:0]* pins.

When operating in 10-bit mode (*20BIT\_10BIT* = LOW), the output data format is multiplexed Luma and Chroma data. In this mode, the data is presented on the *DOUT[19:10]* pins, with *DOUT[9:0]* being forced LOW. For SD/ HD data rates, the clock is either at the 10-bit word rate or at half of this rate (DDR mode). For 3G data rates, the clock is always at half the 10-bit word rate (DDR mode).

### 4.9.3 Parallel Output in DVB-ASI Mode

The DVB-ASI mode of the GS3470 is enabled when the **SMPTE\_BYPASS** bit is LOW and the **DVB\_ASI** bit is HIGH.

The extracted 8-bit data is presented on *DOUT[17:10]* such that  $DOUT[17:10] = HOUT \sim AOUT$ , where *AOUT* is the least significant bit of the decoded transport stream data.

In addition, the *DOUT19* and *DOUT18* pins are configured as DVB-ASI status signals *WORDERR* and *SYNCOUT* respectively.

*SYNCOUT* is HIGH whenever a K28.5 sync character is output from the device.

*WORDERR* is HIGH whenever the device has detected a running disparity error or illegal code word.

*DOUT[9:0]* is forced LOW, when the GS3470 is operating in DVB-ASI mode.

The clock is either at the 10-bit word rate or at half of this rate (DDR mode).

### 4.9.4 Parallel Output in Data-Through Mode

This mode is enabled when the **SMPTE\_BYPASS** and **DVB\_ASI** bits are LOW.

In this mode, data is passed to the output bus without any decoding, descrambling, or word-alignment.

GSPI can be used to set the output data width to either 10-bit or 20-bit, adjust the drive strength of the outputs and enable DDR mode.

The output data width (10-bit or 20-bit) can also be controlled through the *20BIT\_10BIT* pin.

### 4.9.5 Parallel Output Data Format Clock/PCLK Settings

The PCLK output frequency of the GS3470 is determined by the output data format.

Table 4-5 lists the output signal formats according to the external selection pins for the GS3470.

**Table 4-5: GS3470 Output Data Formats**

| Pin/CSR Bit Settings |              |              |                     |                |                      | Output Data Format | PCLK Rate               |
|----------------------|--------------|--------------|---------------------|----------------|----------------------|--------------------|-------------------------|
| <i>20BIT_10BIT</i>   | <i>SD/HD</i> | <i>3G/HD</i> | <i>SMPTE_BYPASS</i> | <i>DVB-ASI</i> | <i>SD_HD_DDR_SEL</i> |                    |                         |
| HIGH                 | LOW          | HIGH         | HIGH                | LOW            | LOW                  | 20-bit 3G format   | 148.5 or 148.5/1.001MHz |
| HIGH                 | LOW          | HIGH         | LOW                 | LOW            | LOW                  | 20-bit data output | 148.5 or 148.5/1.001MHz |
| HIGH                 | LOW          | LOW          | HIGH                | LOW            | LOW                  | 20-bit HD format   | 74.25 or 74.25/1.001MHz |

**Table 4-5: GS3470 Output Data Formats (Continued)**

| Pin/CSR Bit Settings |       |       |                 |         |                   | Output Data Format                  | PCLK Rate                  |
|----------------------|-------|-------|-----------------|---------|-------------------|-------------------------------------|----------------------------|
| 20BIT/<br>10BIT      | SD/HD | 3G/HD | SMPTE<br>BYPASS | DVB-ASI | SD_HD_<br>DDR_SEL |                                     |                            |
| HIGH                 | LOW   | LOW   | LOW             | LOW     | LOW               | 20-bit data output                  | 74.25 or<br>74.25/1.001MHz |
| HIGH                 | HIGH  | X     | HIGH            | LOW     | LOW               | 20-bit SD format                    | 13.5MHz                    |
| HIGH                 | HIGH  | X     | LOW             | LOW     | LOW               | 20-bit data output                  | 13.5MHz                    |
| LOW                  | LOW   | HIGH  | HIGH            | LOW     | X                 | 10-bit multiplexed 3G<br>DDR format | 148.5 or<br>148.5/1.001MHz |
| LOW                  | LOW   | HIGH  | LOW             | LOW     | X                 | 10-bit data output<br>DDR format    | 148.5 or<br>148.5/1.001MHz |
| LOW                  | LOW   | LOW   | HIGH            | LOW     | LOW               | 10-bit multiplexed HD<br>format     | 148.5 or<br>148.5/1.001MHz |
| LOW                  | LOW   | LOW   | LOW             | LOW     | LOW               | 10-bit data output                  | 148.5 or<br>148.5/1.001MHz |
| LOW                  | LOW   | LOW   | HIGH            | LOW     | HIGH              | 10-bit multiplexed HD<br>DDR format | 74.25 or<br>74.25/1.001MHz |
| LOW                  | LOW   | LOW   | LOW             | LOW     | HIGH              | 10-bit data DDR<br>format           | 74.25 or<br>74.25/1.001MHz |
| LOW                  | HIGH  | X     | HIGH            | LOW     | LOW               | 10-bit multiplexed SD<br>format     | 27MHz                      |
| LOW                  | HIGH  | X     | LOW             | LOW     | LOW               | 10-bit data output                  | 27MHz                      |
| LOW                  | HIGH  | X     | LOW             | HIGH    | LOW               | 10-bit ASI output                   | 27MHz                      |
| LOW                  | HIGH  | X     | HIGH            | LOW     | HIGH              | 10-bit multiplexed SD<br>DDR format | 13.5MHz                    |
| LOW                  | HIGH  | X     | LOW             | LOW     | HIGH              | 10-bit data output<br>DDR format    | 13.5MHz                    |
| LOW                  | HIGH  | X     | LOW             | HIGH    | HIGH              | 10-bit ASI output DDR<br>format     | 13.5MHz                    |

#### 4.9.5.1 Delay Line

The GS3470 has the ability to shift the Setup/Hold window on the receive interface, by using an on-chip delay line to shift the phase of PCLK with respect to the data bus. The timing of the PCLK output, relative to the data, can be adjusted through the host interface registers. Each data rate has its own 5-bit delay line offset setting as well as a PCLK invert option.

The delay adjustment range is defined in [Table 4-6](#). The PCLK output can be delayed by up to 0.5UI using the rate dependent **PCLK\_DELAY\_XX** parameters and it can be advanced by 0.5UI by using the **PCLK\_INVERT\_XX** parameters.

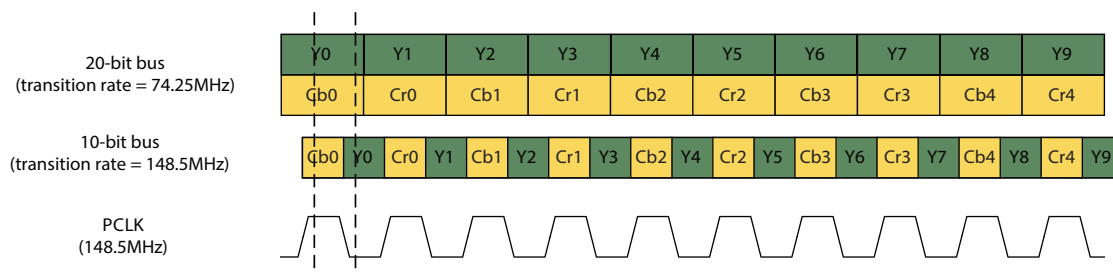
**Table 4-6: Delay Adjustment Range**

| Data Rate | Delay Line Control Parameter | Delay Range (UI) |
|-----------|------------------------------|------------------|
| SD        | PCLK_DELAY_SD[14:10]         | 0.1              |
| HD        | PCLK_DELAY_HD[9:5]           | 0.5              |
| 3G        | PCLK_DELAY_3G[4:0]           | 0.5              |

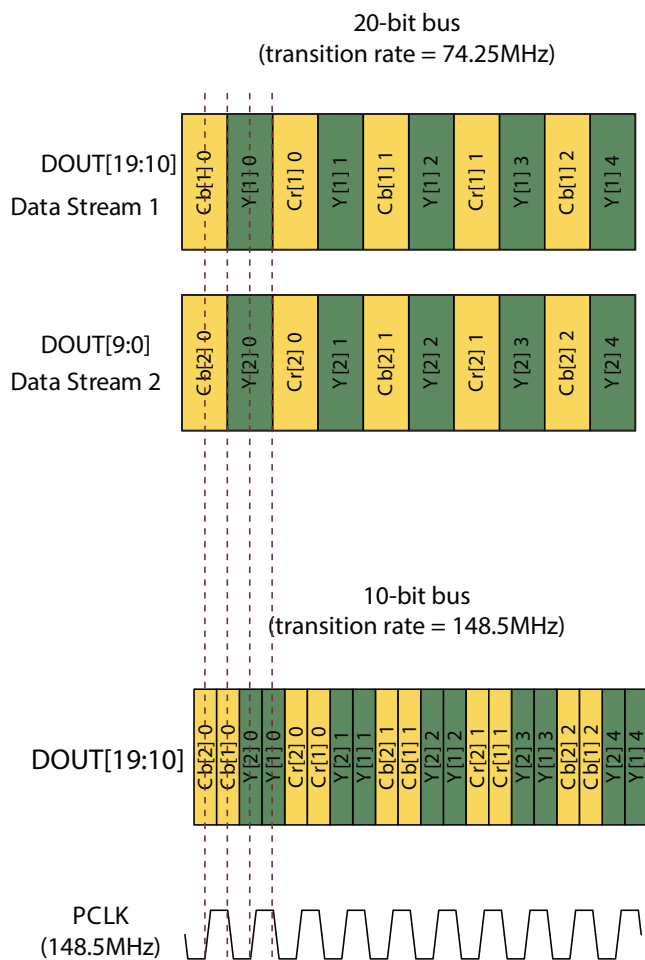
## 4.9.6 DDR Parallel Clock Timing

The GS3470 has the ability to transmit 10-bit parallel video data with a DDR (Dual Data Rate) pixel clock over a single-ended interface.

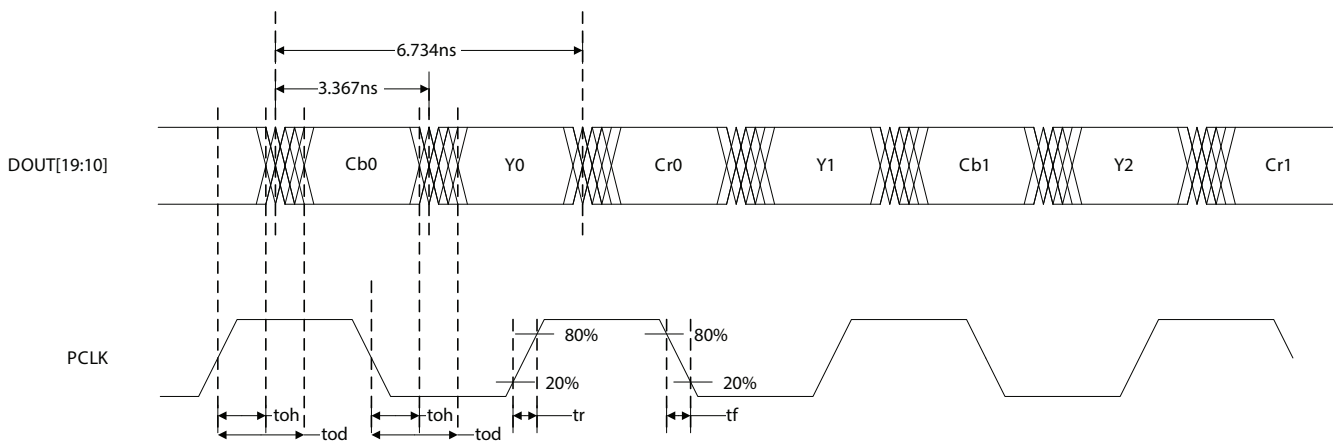
The default DDR timing is configured such that a rising clock edge can be used by a downstream device to clock in data from the C Stream (SD and HD) and Data Stream 2 (3G), and the falling clock edge can be used by a receiving device to clock in data from the Y Stream (SD and HD) and Data Stream 1 (3G).



**Figure 4-4: DDR Video Interface - 3G Level A**



**Figure 4-5: DDR Video Interface - 3G Level B**



**Figure 4-6: DDR Mode Timing Diagram**

**Note:** For output data hold times, please refer to [Table 2-4: AC Electrical Characteristics](#).

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## 4.10 Timing Signal Extraction

The GS3470 extracts timing information from the input data stream and provides FVH timing reference signals.

Video timing signals are only operational in SMPTE mode (**SMPTE\_BYPASS** = HIGH).

It takes one video frame to obtain full synchronization of the received video standard.

**Note:** Both 8-bit and 10-bit TRS words are identified. Once synchronization is achieved, the device continues to monitor the received TRS timing information to maintain synchronization.

### 4.10.1 Automatic Switch Line Lock Handling

The principle of switch line lock handling is that the switching of synchronous video sources will only disturb the horizontal timing and alignment, whereas the vertical timing remains in synchronization – i.e. switching between video sources of the same format. Switch line lock handling is only available in SMPTE mode.

To account for the horizontal disturbance caused by a synchronous switch, the flywheel must be re-synchronized, immediately following a switch line, as defined in the SMPTE recommended practice document RP168-2002.

The synchronous switch point is defined for all major video standards in SMPTE RP168-2002. The device automatically re-synchronizes the word alignment block and timing signal generator at the switch point, based on the detected video standard.

The switch line is defined as follows:

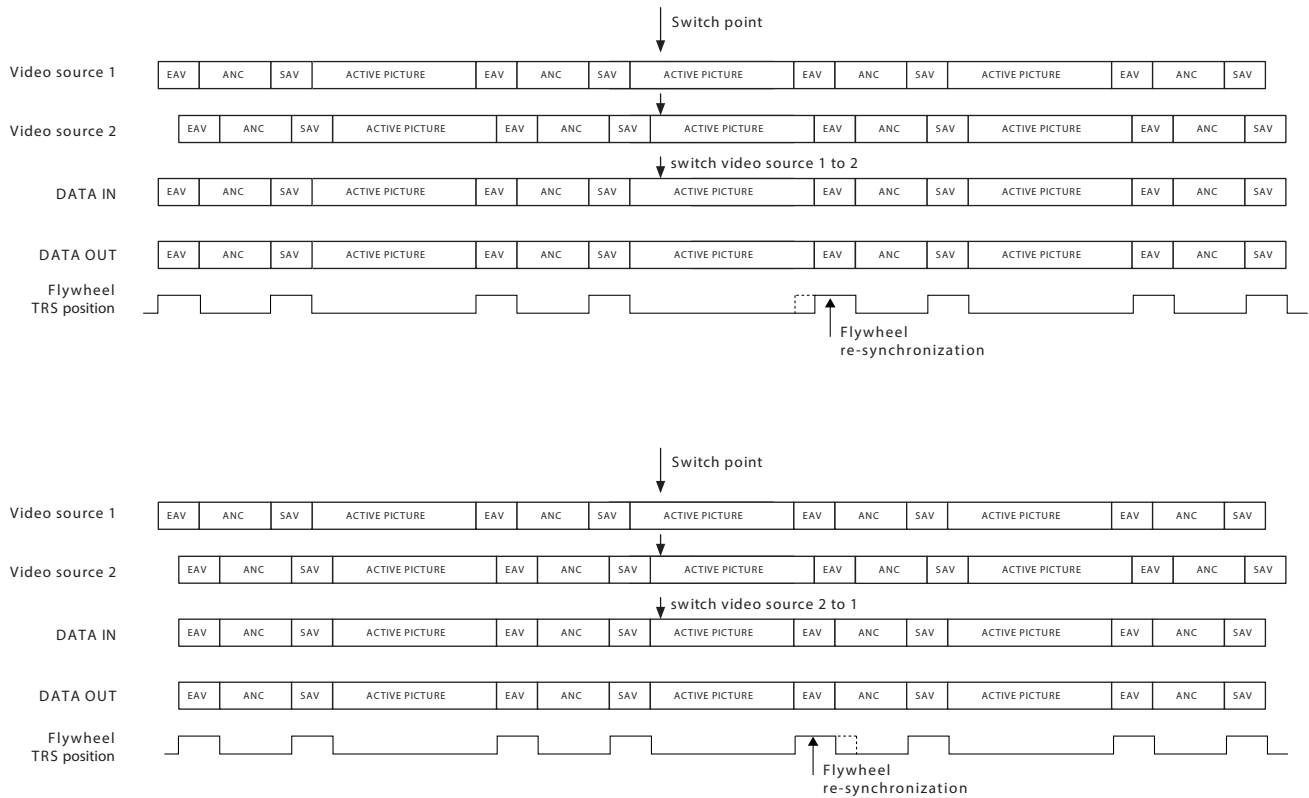
- For 525 line interlaced systems:  
resynchronization takes place at the end of lines 10 & 273
- For 525 line progressive systems:  
resynchronization takes place at the end of line 10
- For 625 line interlaced systems:  
resynchronization takes place at the end of lines 6 & 319
- For 625 line progressive systems:  
resynchronization takes place at the end of line 6
- For 750 line progressive systems:  
resynchronization takes place at the end of line 7
- For 1125 line interlaced systems:  
resynchronization takes place at the end of lines 7 & 569
- For 1125 line progressive systems:  
resynchronization takes place at the end of line 7

**Note:** Unless indicated by SMPTE ST 352 payload identifier packets, the GS3470 does not distinguish between 1125-line progressive segmented-frame (PsF) video and 1125-line interlaced video operating at 25 or 30fps. However, PsF video operating at 24fps is detected by the device.

A full list of all major video standards and switching lines can be found in SMPTE RP168-2002.

## 4.10.2 Manual Switch Line Lock Handling

The automatic switch point can be reconfigured using GSPI. The switch line is programmed by the user via the host interface. The user may program two lines, one for Field One and one for Field Two of an interlaced standard. For progressive formats, only the first number is used. If the numbers are set to zero, then the switch lines used are those defined in RP168-2002. This enables the user to force immediate lock-up on any line, if the switch point is non-standard.



**Figure 4-7: Switch Line Locking on a Non-Standard Switch Line**

## 4.11 Programmable Multi-Function Outputs

The GS3470 has 6 multi-function output pins, *STAT [5:0]*, which are programmable via the host interface register **STAT[5:0]\_CONFIG** to output one of the following signals:

**Table 4-7: Output Signals Available on Programmable Multi-Function Pins**

| Status Signal                                                        | Selection Code | Default Output Pin |
|----------------------------------------------------------------------|----------------|--------------------|
| H/HSYNC (according to TIM_861 register) <a href="#">Section 4.12</a> | 00000          | STAT0              |
| V/VSNC (according to TIM_861 register) <a href="#">Section 4.12</a>  | 00001          | STAT1              |
| F/DE (according to TIM_861 register) <a href="#">Section 4.12</a>    | 00010          | STAT2              |
| LOCKED <a href="#">Section 4.8</a>                                   | 00011          | STAT3              |
| Y/1ANC <a href="#">Section 4.17</a>                                  | 00100          | —                  |
| C/2ANC <a href="#">Section 4.17</a>                                  | 00101          | —                  |
| $\overline{\text{DATA ERROR}}$                                       | 00110          | STAT5              |
| $\overline{\text{VIDEO ERROR}}$                                      | 00111          | —                  |
| $\overline{\text{AUDIO ERROR}}$                                      | 01000          | —                  |
| EDH DETECTED                                                         | 01001          | —                  |
| $\overline{\text{CARRIER DETECT}}$                                   | 01010          | —                  |
| SD/ $\overline{\text{HD}}$                                           | 01011          | STAT4              |
| 3G/ $\overline{\text{HD}}$                                           | 01100          | —                  |
| $\overline{\text{SMPTE BYPASS}}$                                     | 11101          | —                  |
| DVB_ASI                                                              | 11110          | —                  |

**Note:** Unused digital output pins can be left unconnected.

## 4.12 H:V:F Timing Signal Extraction

The GS3470 extracts critical timing parameters from the received TRS words.

Horizontal blanking (H), Vertical blanking (V), and Field odd/even (F) timing are output on the *STAT[2:0]* pins by default.

The H signal timing can be selected through GSPI using the **H\_CONFIG** parameter. By default, the H signal timing is set to active line blanking. This can be changed to TRS based blanking by setting the **H\_CONFIG** parameter to 1.

The timing of these signals is shown in Figure 4-8 through Figure 4-13.

**Note:** Both 8-bit and 10-bit TRS words are identified by the device.



Figure 4-8: H:V:F Output Timing - 3G Level A and HD 20-bit Mode

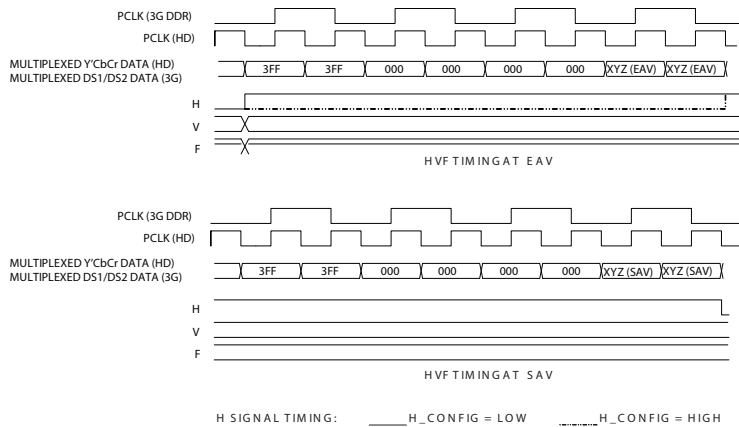


Figure 4-9: H:V:F Output Timing - 3G Level A and HD 10-bit Mode

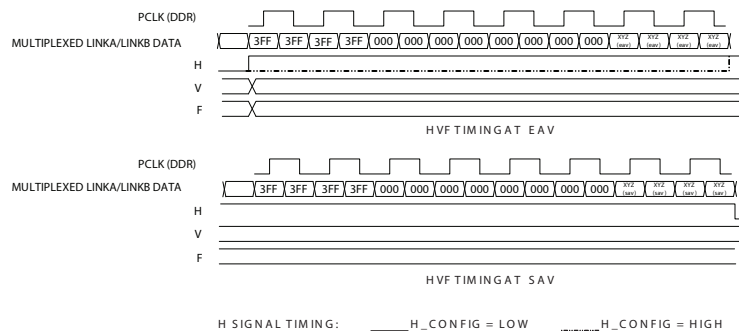
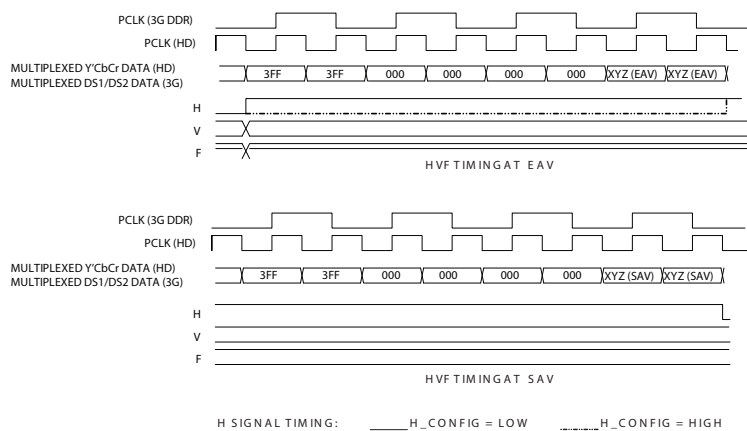
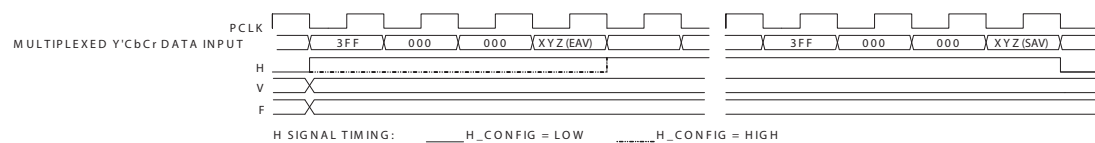


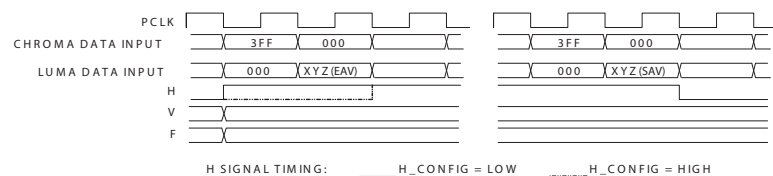
Figure 4-10: H:V:F Output Timing - 3G Level B 10-bit Mode



**Figure 4-11: H:V:F Output Timing - 3G Level B 20-bit Mode, each 10-bit Stream**



**Figure 4-12: H:V:F Output Timing - SD 10-bit Mode**



**Figure 4-13: H:V:F Output Timing - SD 20-bit Mode**

## 4.12.1 CEA-861 Timing Generation

The GS3470 is capable of generating CEA861 timing for all of the supported video formats.

**Table 4-8: Supported CEA-861 Formats**

| Format                              | CEA-861                | VD_STD[5:0]                                                                                                                                                                |
|-------------------------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 720 (1440) x 480i @ 59.94/60Hz      | 6 & 7                  | 16 <sub>hr</sub> , 17 <sub>hr</sub> , 19 <sub>hr</sub> , 1B <sub>h</sub>                                                                                                   |
| 720(1440) x 576i @ 50Hz             | 21 & 22                | 18 <sub>hr</sub> , 1A <sub>h</sub>                                                                                                                                         |
| 1280 x 720p @ 59.94/60Hz            | 4                      | 20 <sub>hr</sub> , 00 <sub>h</sub>                                                                                                                                         |
| 1280 x 720p @ 50Hz                  | 19                     | 24 <sub>hr</sub> , 04 <sub>h</sub>                                                                                                                                         |
| 1280x720p @ 29.97/30Hz              | 62                     | 27 <sub>hr</sub> , 02 <sub>h</sub>                                                                                                                                         |
| 1280x720p @ 25Hz                    | 61                     | 26 <sub>hr</sub> , 06 <sub>h</sub>                                                                                                                                         |
| 1920 x 1080i @ 59.94/60Hz           | 5                      | 2A <sub>hr</sub> , 0A <sub>h</sub>                                                                                                                                         |
| 1920 x 1080i @ 50Hz                 | 20                     | 2C <sub>hr</sub> , 0C <sub>h</sub>                                                                                                                                         |
| 1920 x 1080p @ 29.97/30Hz           | 34 <sup>1</sup>        | 2B <sub>hr</sub> , 0B <sub>h</sub>                                                                                                                                         |
| 1920 x 1080p @ 25Hz                 | 33 <sup>2</sup>        | 2D <sub>hr</sub> , 0D <sub>h</sub>                                                                                                                                         |
| 1920 x 1080p @ 23.98/24Hz           | 32                     | 30 <sub>hr</sub> , 10 <sub>h</sub>                                                                                                                                         |
| 1920 x 1080p @ 59.94/60Hz           | 16 <sup>1</sup>        | 2B <sub>h</sub>                                                                                                                                                            |
| 1920 x 1080p @ 50Hz                 | 31 <sup>2</sup>        | 2D <sub>h</sub>                                                                                                                                                            |
| 2048x1080p @<br>30/25/24/48/50/60Hz | Undefined <sup>3</sup> | 21 <sub>hr</sub> , 22 <sub>hr</sub> , 23 <sub>hr</sub> , 37 <sub>hr</sub> , 38 <sub>hr</sub> ,<br>39 <sub>hr</sub> , 3A <sub>hr</sub> , 3B <sub>hr</sub> , 3C <sub>h</sub> |
| 2048x1080i @ 48/50/59.94/60Hz       | Undefined <sup>3</sup> | 34 <sub>hr</sub> , 35 <sub>hr</sub> , 36 <sub>h</sub>                                                                                                                      |

**Notes:**

1,2: Timing is identical for the corresponding formats

3: Derived from the standard. Timing diagram provided.

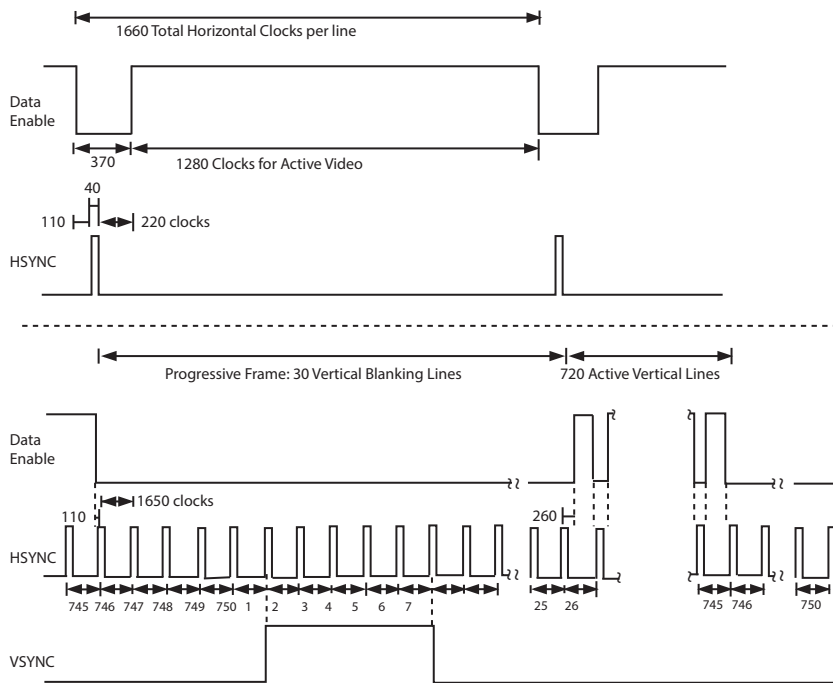
### 4.12.1.1 Vertical Timing

When CEA 861 timing is selected, the device outputs standards compliant CEA 861 timing signals as shown in the figures below, for example 240 active lines per field for SMPTE ST 125.

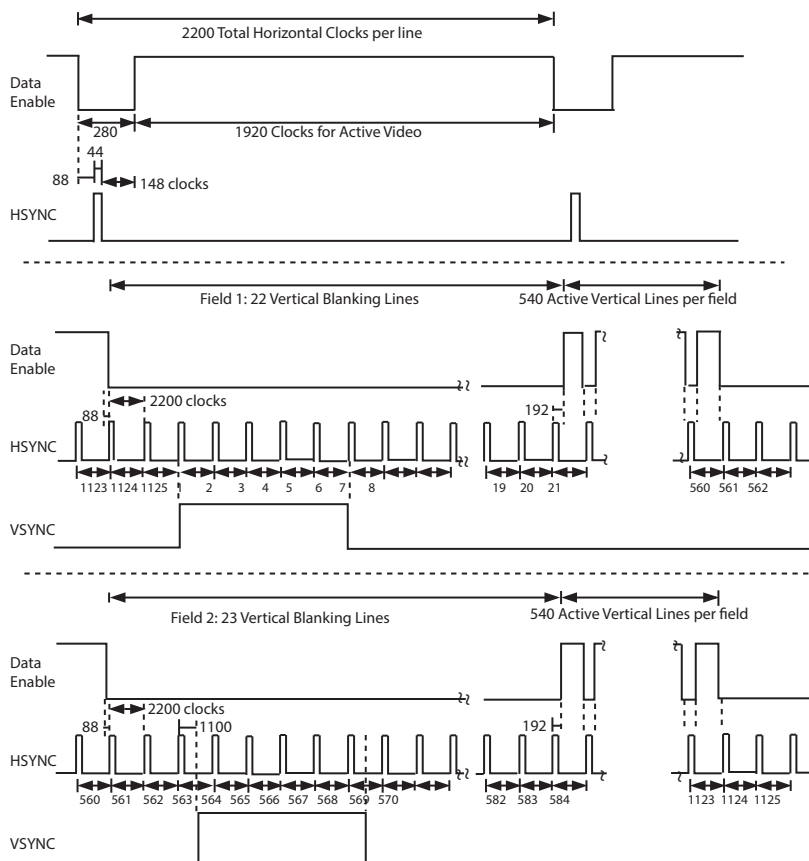
The timing of the CEA 861 timing reference signals can be found in the CEA 861 specifications.

**Table 4-9: CEA861 Timing Formats**

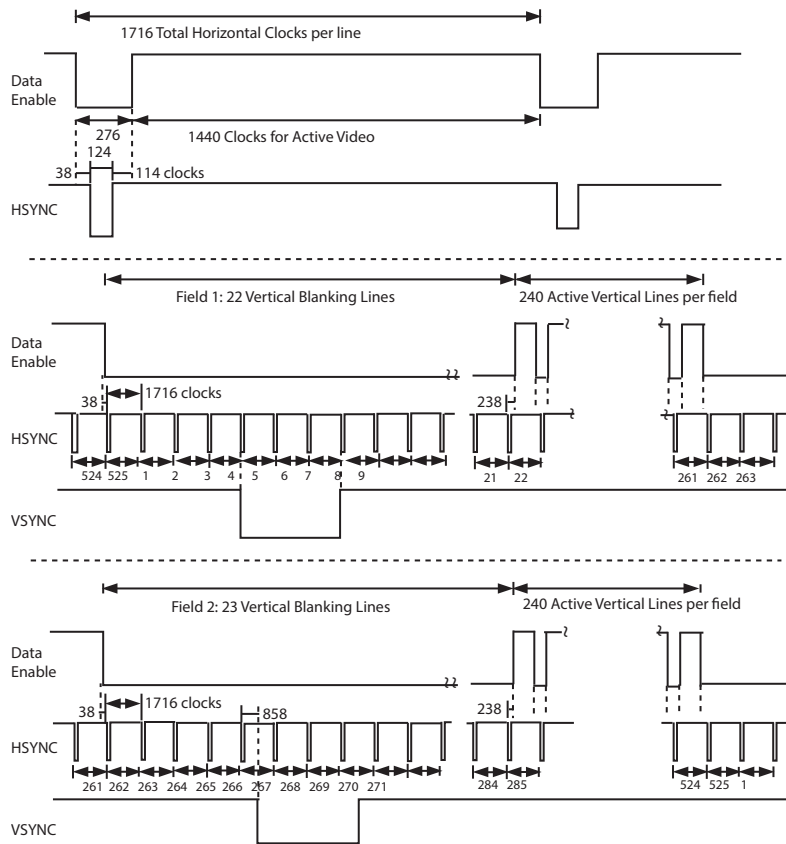
| Format    | Parameters                                      |
|-----------|-------------------------------------------------|
| 4         | H:V:DE Input Timing 1280 x720p @ 59.94/60Hz     |
| 5         | H:V:DE Input Timing 1920 x1080i @ 59.94/60Hz    |
| 6 & 7     | H:V:DE Input Timing 720(1440)x480i @ 59.94/60Hz |
| 16        | H:V:DE Input Timing 1920 x1080p @ 59.94/60Hz    |
| 19        | H:V:DE Input Timing 1280 x 720p @ 50Hz          |
| 20        | H:V:DE Input Timing 1920 x1080i @ 50Hz          |
| 21 & 22   | H:V:DE Input Timing 720 (1440) x576 @ 50Hz      |
| 31        | H:V:DE Input Timing 1920 x1080p @ 50Hz          |
| 32        | H:V:DE Input Timing 1920 x1080p @ 23.976/24Hz   |
| 33        | H:V:DE Input Timing 1920 x1080p @ 25Hz          |
| 34        | H:V:DE Input Timing 1920 x1080p @ 29.97/30Hz    |
| 61        | H:V:DE Input Timing 1280 x720p @ 25Hz           |
| 62        | H:V:DE Input Timing 1280 x720p @ 29.97/30Hz     |
| Undefined | H:V:DE Input Timing 2048x1080p @ 30/60Hz        |
| Undefined | H:V:DE Input Timing 2048x1080p @ 25/50Hz        |
| Undefined | H:V:DE Input Timing 2048x1080p @ 24/48Hz        |
| Undefined | H:V:DE Input Timing 2048x1080i @ 30/60Hz        |
| Undefined | H:V:DE Input Timing 2048x1080i @ 25/50Hz        |
| Undefined | H:V:DE Input Timing 2048x1080i @ 24/48Hz        |



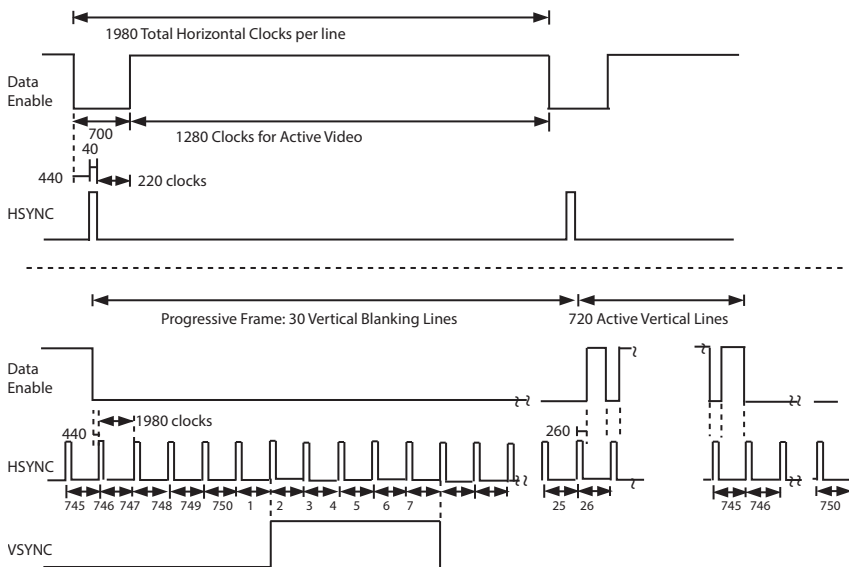
**Figure 4-14: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4)**



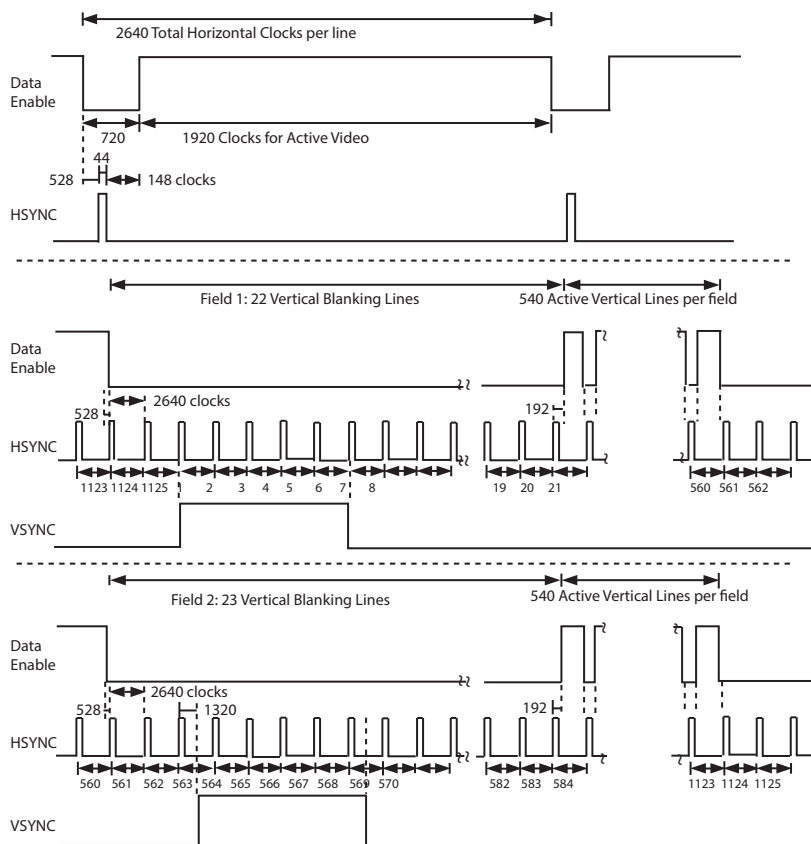
**Figure 4-15: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5)**



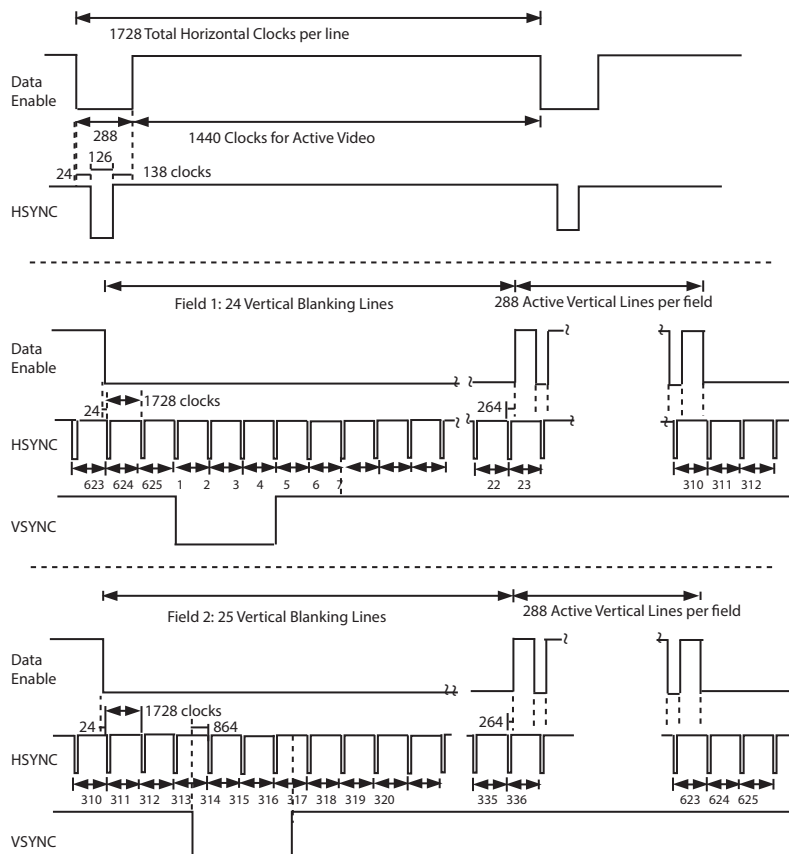
**Figure 4-16: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6 & 7)**



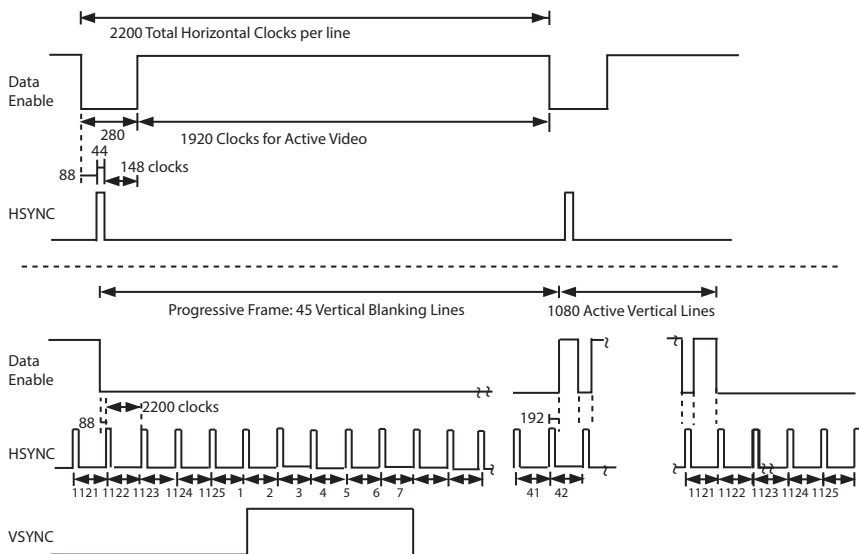
**Figure 4-17: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19)**



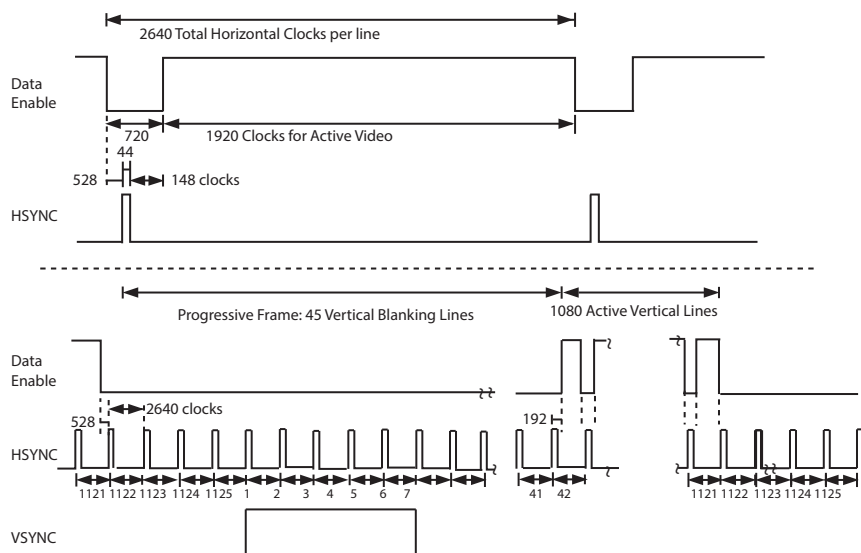
**Figure 4-18: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20)**



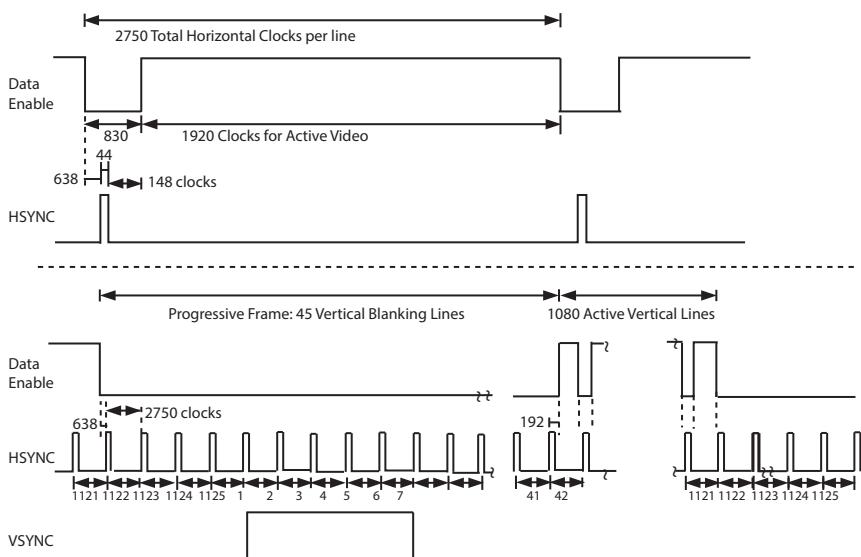
**Figure 4-19: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22)**



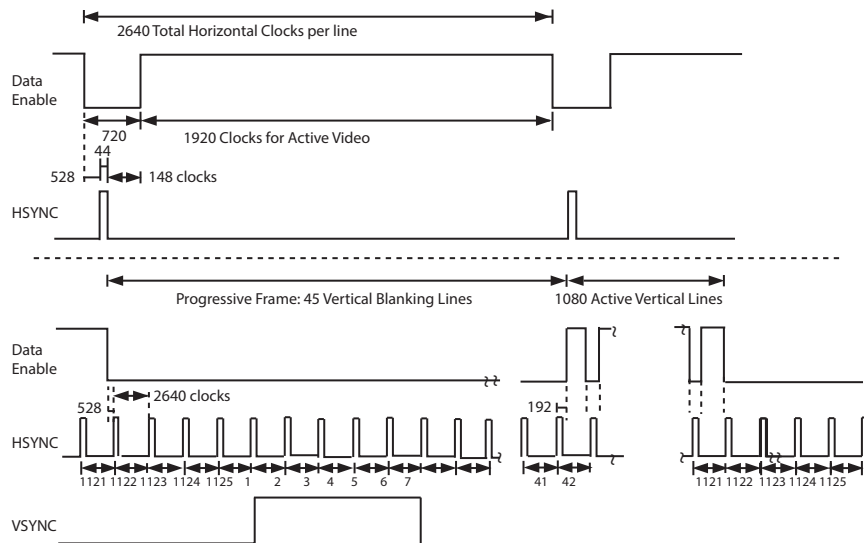
**Figure 4-20: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16)**



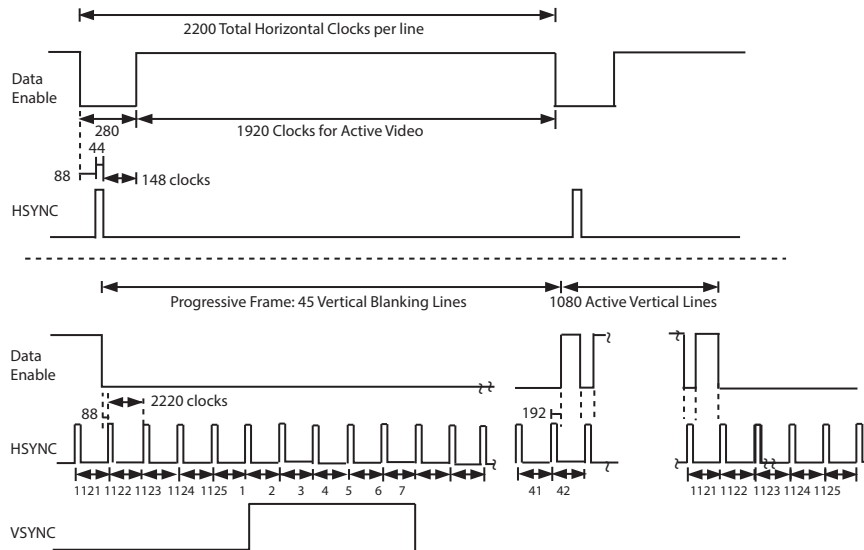
**Figure 4-21: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31)**



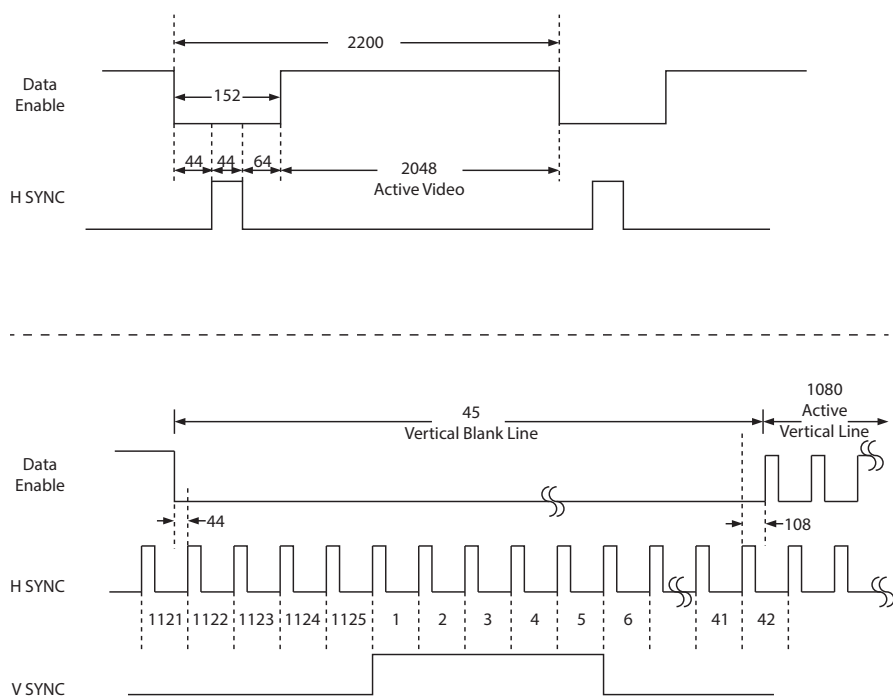
**Figure 4-22: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32)**



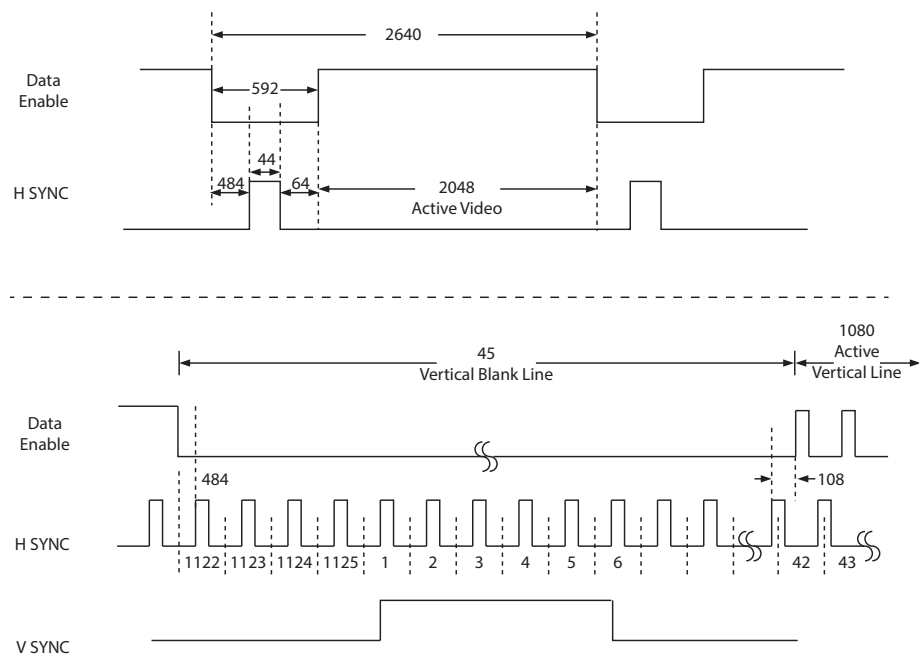
**Figure 4-23: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33)**



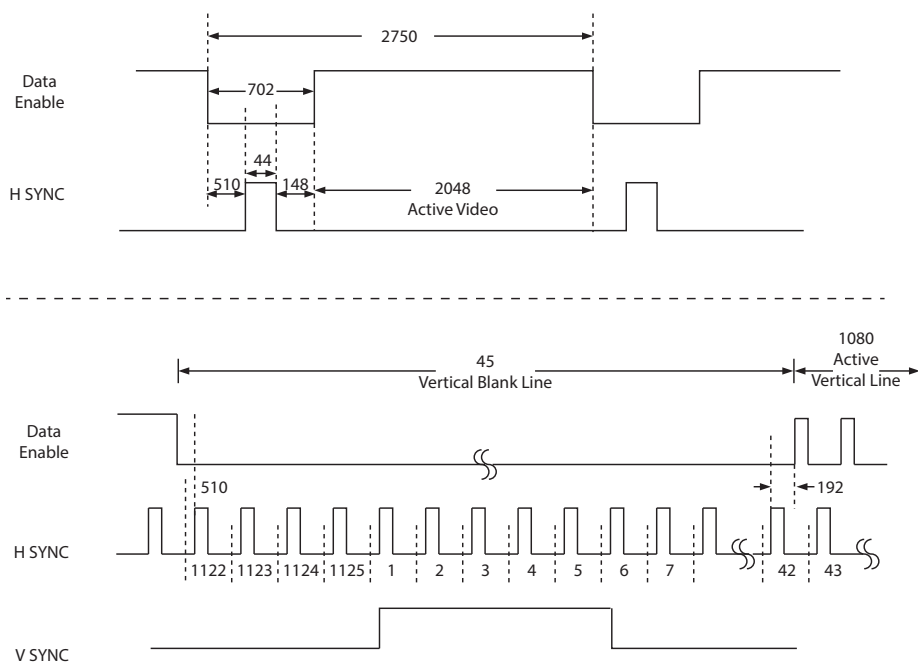
**Figure 4-24: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34)**



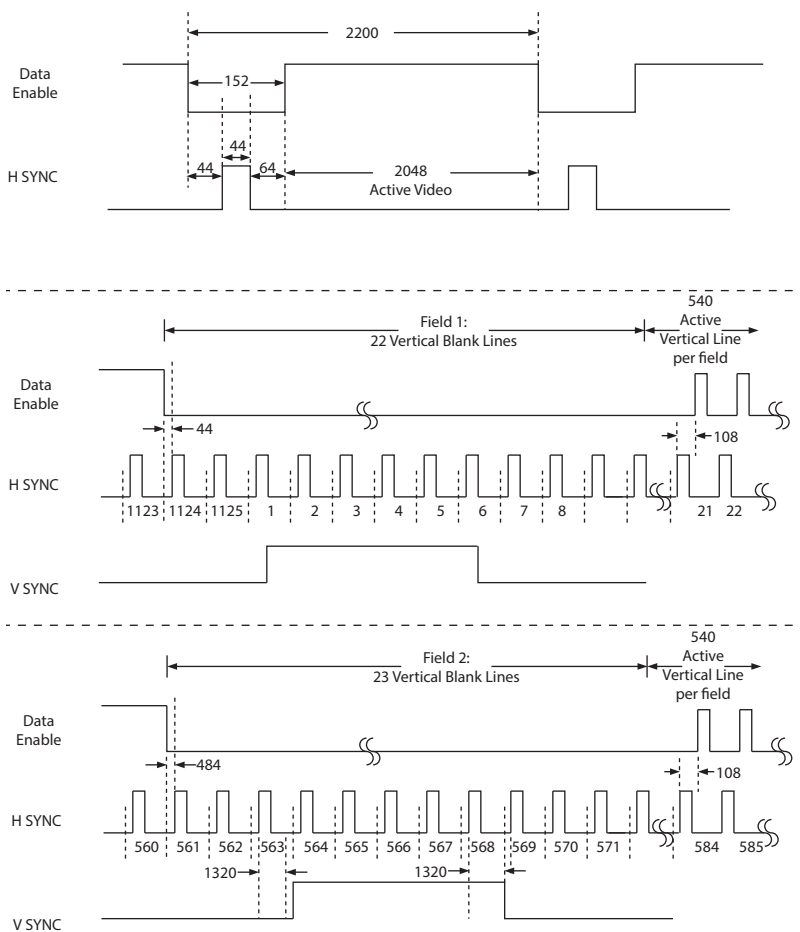
**Figure 4-25: H:V:DE Output Timing 2048 x 1080p @ 60/30**



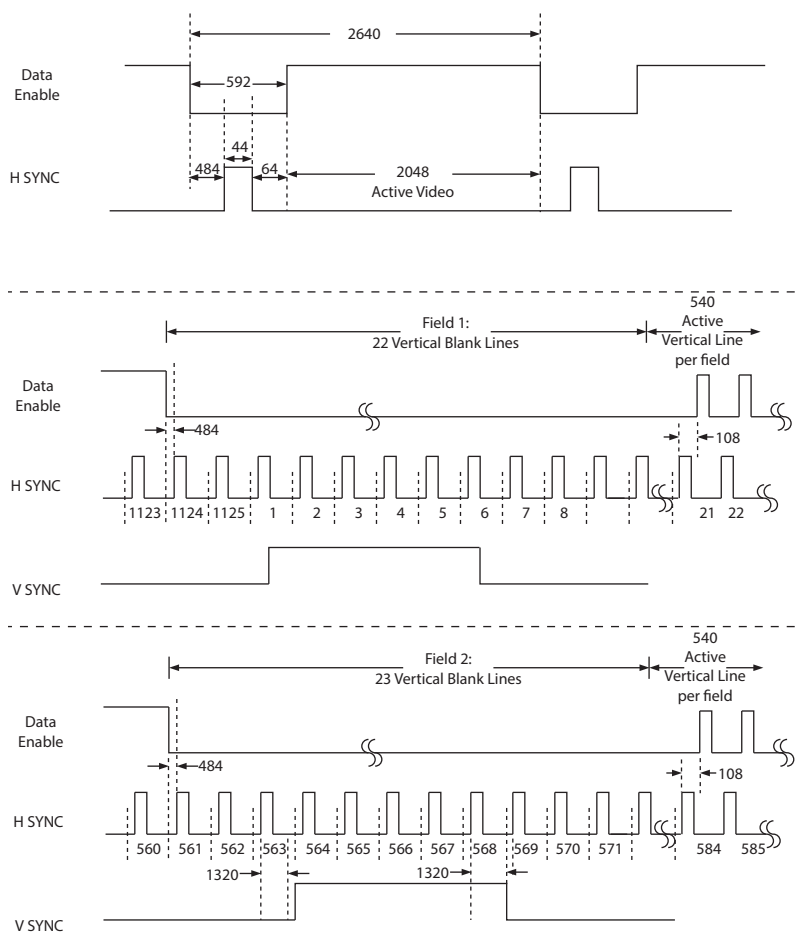
**Figure 4-26: H:V:DE Output Timing 2048 x 1080p @ 50/25**



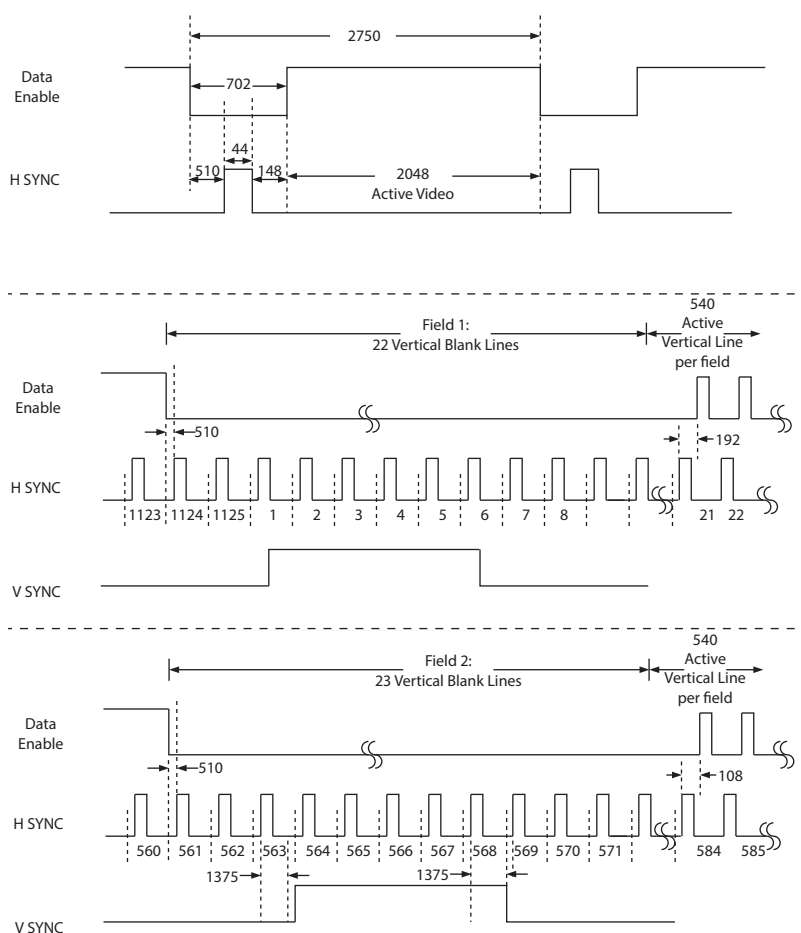
**Figure 4-27: H:V:DE Output Timing 2048 x 1080p @ 48/24**



**Figure 4-28: H:V:DE Output Timing 2048 x 1080p @ 60/30**



**Figure 4-29: H:V:DE Output Timing 2048 x 1080p @ 50/25**



**Figure 4-30: H:V:DE Output Timing 2048 x 1080p @ 48/24**

## 4.13 Automatic Video Standards Detection

The GS3470 is able to identify the received video standard. It will also indicate whether the 3G input signal is Level A or Level B. The **VID\_STD\_DS1** and **VID\_STD\_DS2** registers can be used to access this information. [Table 4-10](#) describes the 5-bit codes for the recognized video standards.

Four additional registers are provided to allow the host to read the video standard information from the device such as total words per line, active words per line, total lines per field/frame, and active lines per field/frame. This information can be accessed through the **RASTER\_STRUC\_4[1]\_DS[2:1]** registers.

The **RASTER\_STRUC\_4\_DS[2:1]** registers also contain three status bits: **STD\_LOCK\_DS[2:1]**, **INT\_PROG\_DS[2:1]**, and **M\_DS[2:1]**. The **STD\_LOCK\_DS[2:1]** bit is set HIGH whenever the timing signal generator is fully synchronized to the incoming standard, and detects it as one of the supported formats. The **INT\_PROG\_DS[2:1]** bit is set HIGH if the detected video standard is interlaced and LOW if the detected video standard is progressive. M is set HIGH if the clock frequency includes the “1000/1001” factor denoting a 23.98Hz, 29.97Hz, or 59.94Hz frame rate.

**Table 4-10: Supported Video Standard Codes**

| SMPTE Standard     | Active Video Area                        | Length of HANC Level A (Level B) | Total Lines per Frame | Length of Active Word | Total Clocks per Line | VD STD [5:0]    | SD/HD | 3G/HD |
|--------------------|------------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------|-------|-------|
| 2048-2<br>4:2:2    | 2048x1080/60 (1:1)                       | 140 (128) <sup>2</sup>           | 1125                  | 2048                  | 2200                  | 37 <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/50 (1:1)                       | 580 (568) <sup>2</sup>           | 1125                  | 2048                  | 2640                  | 38 <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/48 (1:1)                       | 690 (678) <sup>2</sup>           | 1125                  | 2048                  | 2750                  | 39 <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/30 (1:1)                       | 140 (128) <sup>2</sup>           | 1125                  | 2048                  | 2200                  | 21 <sub>h</sub> | 0     | 0     |
|                    | 2048x1080/25 (1:1)                       | 580 (568) <sup>2</sup>           | 1125                  | 2048                  | 2640                  | 22 <sub>h</sub> | 0     | 0     |
|                    | 2048x1080/24 (1:1)                       | 690 (678) <sup>2</sup>           | 1125                  | 2048                  | 2750                  | 23 <sub>h</sub> | 0     | 0     |
|                    | 2048x1080/60(2:1) or 2048x1080/30(PsF)   | 140(128) <sup>2</sup>            | 1125                  | 2048                  | 2200                  | 29 <sub>h</sub> | 0     | 0     |
|                    | 2048x1080/50(2:1) or 2048x1080/25(PsF)   | 580(568) <sup>2</sup>            | 1125                  | 2048                  | 2640                  | 32 <sub>h</sub> | 0     | 0     |
|                    | 2048x1080/48(2:1) or 2048x1080/24(PsF)   | 690(678) <sup>2</sup>            | 1125                  | 2048                  | 2750                  | 33 <sub>h</sub> | 0     | 0     |
| 2048-2<br>4:4:4    | 2048x1080/60 (2:1) or 2048x1080/30 (PsF) | —                                | 1125                  | 4096                  | 4400                  | 34 <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/50 (2:1) or 2048x1080/25 (PsF) | —                                | 1125                  | 4096                  | 5280                  | 35 <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/48 (2:1) or 2048x1080/24 (PsF) | —                                | 1125                  | 4096                  | 5500                  | 36 <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/30 (1:1)                       | 292 (280) <sup>2</sup>           | 1125                  | 4096 <sup>1</sup>     | 4400                  | 3A <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/25 (1:1)                       | 1172 (1160) <sup>2</sup>         | 1125                  | 4096 <sup>1</sup>     | 5280                  | 3B <sub>h</sub> | 0     | 1     |
|                    | 2048x1080/24 (1:1)                       | 1392 (1380) <sup>2</sup>         | 1125                  | 4096 <sup>1</sup>     | 5500                  | 3C <sub>h</sub> | 0     | 1     |
| 425M (3G)<br>4:2:2 | 1920x1080/60 (1:1)                       | 268 (256) <sup>2</sup>           | 1125                  | 1920                  | 2200                  | 2B <sub>h</sub> | 0     | 1     |
|                    | 1920x1080/50 (1:1)                       | 708 (696) <sup>2</sup>           | 1125                  | 1920                  | 2640                  | 2D <sub>h</sub> | 0     | 1     |

**Table 4-10: Supported Video Standard Codes**

| SMPTE Standard  | Active Video Area                        | Length of HANC Level A (Level B) | Total Lines per Frame | Length of Active Word | Total Clocks per Line | VD STD [5:0]    | SD/H $\overline{D}$ | 3G/H $\overline{D}$ |
|-----------------|------------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------|---------------------|---------------------|
| 425M (3G) 4:4:4 | 1920x1080/60 (2:1) or 1920x1080/30 (PsF) | 548 (536) <sup>2</sup>           | 1125                  | 3840 <sup>1</sup>     | 4400                  | 2A <sub>h</sub> | 0                   | 1                   |
|                 | 1920x1080/50 (2:1) or 1920x1080/25 (PsF) | 1428 (1416) <sup>2</sup>         | 1125                  | 3840 <sup>1</sup>     | 5280                  | 2C <sub>h</sub> | 0                   | 1                   |
|                 | 1920x1080/30 (1:1)                       | 548 (536) <sup>2</sup>           | 1125                  | 3840 <sup>1</sup>     | 4400                  | 2E <sub>h</sub> | 0                   | 1                   |
|                 | 1920x1080/25 (1:1)                       | 1428 (1416) <sup>2</sup>         | 1125                  | 3840 <sup>1</sup>     | 5280                  | 2F <sub>h</sub> | 0                   | 1                   |
|                 | 1920x1080/24 (1:1)                       | 1648 (1636) <sup>2</sup>         | 1125                  | 3840 <sup>1</sup>     | 5500                  | 30 <sub>h</sub> | 0                   | 1                   |
|                 | 1920x1080/24 (PsF)                       | 1648 (1636) <sup>2</sup>         | 1125                  | 3840 <sup>1</sup>     | 5500                  | 31 <sub>h</sub> | 0                   | 1                   |
|                 | 1280x720/60 (1:1)                        | 728 (716) <sup>2</sup>           | 750                   | 2560 <sup>1</sup>     | 3300                  | 20 <sub>h</sub> | 0                   | 1                   |
|                 | 1280x720/50 (1:1)                        | 1388 (1376) <sup>2</sup>         | 750                   | 2560 <sup>1</sup>     | 3960                  | 24 <sub>h</sub> | 0                   | 1                   |
|                 | 1280x720/30 (1:1)                        | —                                | 750                   | 2560 <sup>1</sup>     | 6600                  | 27 <sub>h</sub> | 0                   | 1                   |
|                 | 1280x720/25 (1:1)                        | 5348 (5336) <sup>2</sup>         | 750                   | 2560 <sup>1</sup>     | 7920                  | 26 <sub>h</sub> | 0                   | 1                   |
|                 | 1280x720/24 (1:1)                        | 5678 (5666) <sup>2</sup>         | 750                   | 2560 <sup>1</sup>     | 8250                  | 28 <sub>h</sub> | 0                   | 1                   |
| 260M (HD)       | 1920x1035/60(2:1)                        | 268                              | 1125                  | 1920                  | 2200                  | 15 <sub>h</sub> | 0                   | 0                   |
| 295M (HD)       | 1920x1080/50 (2:1)                       | 444                              | 1250                  | 1920                  | 2376                  | 14 <sub>h</sub> | 0                   | 0                   |
| 274M (HD)       | 1920x1080/60 (2:1) or 1920x1080/30 (PsF) | 268                              | 1125                  | 1920                  | 2200                  | 0A <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/50 (2:1) or 1920x1080/25 (PsF) | 708                              | 1125                  | 1920                  | 2640                  | 0C <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/30 (1:1)                       | 268                              | 1125                  | 1920                  | 2200                  | 0B <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/25 (1:1)                       | 708                              | 1125                  | 1920                  | 2640                  | 0D <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/24 (1:1)                       | 818                              | 1125                  | 1920                  | 2750                  | 10 <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/24 (PsF)                       | 818                              | 1125                  | 1920                  | 2750                  | 11 <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/25 (1:1) — EM                  | 324                              | 1125                  | 2304                  | 2640                  | 0E <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/25 (PsF) — EM                  | 324                              | 1125                  | 2304                  | 2640                  | 0F <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/24 (1:1) — EM                  | 338                              | 1125                  | 2400                  | 2750                  | 12 <sub>h</sub> | 0                   | 0                   |
|                 | 1920x1080/24 (PsF) — EM                  | 338                              | 1125                  | 2400                  | 2750                  | 13 <sub>h</sub> | 0                   | 0                   |

**Table 4-10: Supported Video Standard Codes**

| SMPTE Standard    | Active Video Area                            | Length of HANC Level A (Level B) | Total Lines per Frame | Length of Active Word | Total Clocks per Line | VD STD [5:0]    | SD/HD | 3G/HD |
|-------------------|----------------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------|-------|-------|
| 296M (HD)         | 1280x720/30 (1:1)                            | 2008                             | 750                   | 1280                  | 3300                  | 02 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/30 (1:1) — EM                       | 408                              | 750                   | 2880                  | 3300                  | 03 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/50 (1:1)                            | 688                              | 750                   | 1280                  | 1980                  | 04 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/50 (1:1) — EM                       | 240                              | 750                   | 1728                  | 1980                  | 05 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/25 (1:1)                            | 2668                             | 750                   | 1280                  | 3960                  | 06 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/25 (1:1) — EM                       | 492                              | 750                   | 3456                  | 3960                  | 07 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/24 (1:1)                            | 2833                             | 750                   | 1280                  | 4125                  | 08 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/24 (1:1) — EM                       | 513                              | 750                   | 3600                  | 4125                  | 09 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/60 (1:1)                            | 358                              | 750                   | 1280                  | 1650                  | 00 <sub>h</sub> | 0     | 0     |
|                   | 1280x720/60 (1:1) — EM                       | 198                              | 750                   | 1440                  | 1650                  | 01 <sub>h</sub> | 0     | 0     |
| 125M (SD)         | 1140x487/60 (2:1) (or dual link progressive) | 268                              | 525                   | 1440                  | 1716                  | 16 <sub>h</sub> | 1     | X     |
|                   | 1440x507/60 (2:1)                            | 268                              | 525                   | 1440                  | 1716                  | 17 <sub>h</sub> | 1     | X     |
|                   | 525-line 487 generic                         | —                                | 525                   | —                     | 1716                  | 19 <sub>h</sub> | 1     | X     |
|                   | 525-line 507 generic                         | —                                | 525                   | —                     | 1716                  | 1B <sub>h</sub> | 1     | X     |
| ITU-R BT.656 (SD) | 1440x576/50 (2:1) (or dual link progressive) | 280                              | —                     | 1440                  | 1728                  | 18 <sub>h</sub> | 1     | X     |
|                   | 625-line generic (EM)                        | —                                | —                     | —                     | 1728                  | 1A <sub>h</sub> | 1     | X     |
| Unknown HD        | SD/HD = 0                                    | —                                | —                     | —                     | —                     | 1D <sub>h</sub> | 0     | 0     |
| Unknown SD        | SD/HD = 1                                    | —                                | —                     | —                     | —                     | 1E <sub>h</sub> | 1     | X     |
| Unknown 3G        | SD/HD = 0                                    | —                                | —                     | —                     | —                     | 3F <sub>h</sub> | 0     | 1     |

**Notes:**

1. The 4:4:4 standards have 2 clocks per sample at the data stream level.
2. HANC space is shorter for a Level B signal because of the double TRS.

**Note:** In certain systems, due to greater ppm offsets in the crystal, the ‘M’ bit may not assert properly. In such cases, the **M\_DETECTION\_TOLERANCE\_DS[2:1]** value can be increased through GSPI.

By default (after power up or after systems reset), the four **RASTER\_STRUC\_[4:1]\_DS[2:1]**, **VD\_STD\_DS[2:1]**, **STD\_LOCK\_DS[2:1]**, and **INT\_PROG\_DS[2:1]** fields are set to zero. These fields are also cleared when the **SMPTE\_BYPASS** register is LOW.

## 4.14 Data Format Detection & Indication

In addition to detecting the video standard, the GS3470 also detects the data format. This information can be found in the **DATA\_FORMAT\_DS[2:1]** registers. Data format information is only accessible while the device is locked. By default, at power-up, after reset or while the device is not locked, the **DATA\_FORMAT\_DS[2:1]** registers are set to  $F_h$ .

**Table 4-11: Data Format Register Codes**

| YDATA_FORMAT[3:0] or<br>CDATA_FORMAT[3:0] | Data Format           | Remarks                                                                                                                                  |
|-------------------------------------------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| $0_h$ to $05_h$                           | SDTI                  | SMPTE ST 321, SMPTE ST 322,<br>SMPTE ST 326                                                                                              |
| $6_h$                                     | SDI                   | —                                                                                                                                        |
| $7_h$                                     | Reserved              | —                                                                                                                                        |
| $8_h$                                     | TDM                   | SMPTE ST 346                                                                                                                             |
| $9_h$                                     | HD-SDTI               | —                                                                                                                                        |
| $A_h$ to $E_h$                            | Reserved              | —                                                                                                                                        |
| $F_h$                                     | Non-SMPTE data format | Detected data format is not SMPTE.<br>LOCKED = LOW.<br><b>Note:</b> This Data Format register is<br>invalid in <b>SMPTE_BYPASS</b> mode. |

The data format is determined based on the presence of TRS ID words, SDTI header and TDM header.

**Note:** In SD video mode only the Y data format register contains the data, and the C register is set to  $F_h$  (undefined format).

## 4.14.1 SMPTE ST 425 Mapping - 3G Level A and Level B Formats

### 4.14.1.1 Level A Mapping

Direct image format mapping - the mapping structure used to define 1080p/50/59.94/60 4:2:2 YCbCr 10 bit data, as supported by the GS3470. See Figure 4-31.

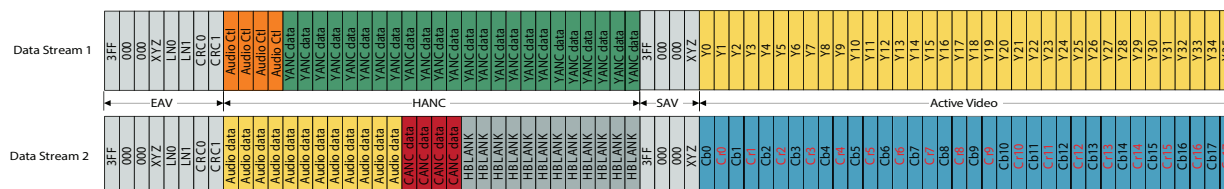


Figure 4-31: Level A Mapping

### 4.14.1.2 Level B Mapping

The 2 x 292 HD SDI interface - this can be two distinct links running at 1.5Gb/s or one 3Gb/s link formatted according to SMPTE ST 292 on two 10-bit links (Y/C interleaved). For 1080p/50/59.94/60 4:2:2 video formats, each link should be line-interleaved as per SMPTE ST 372. See Figure 4-32:

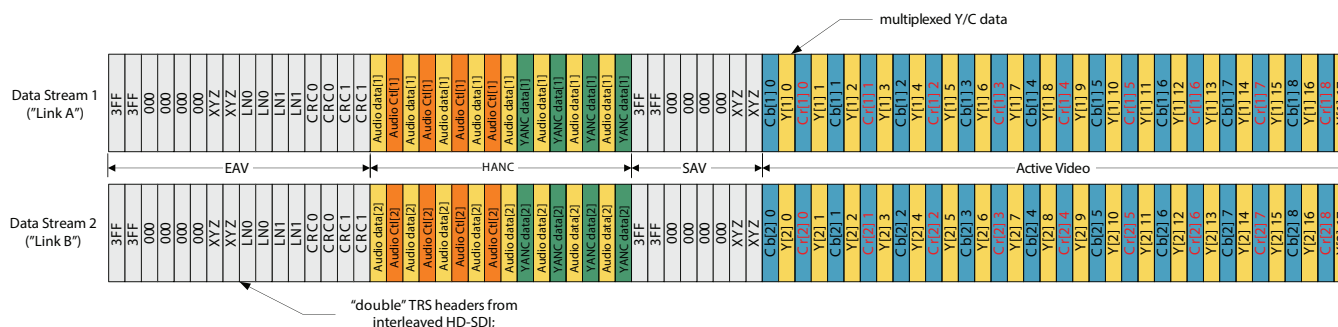


Figure 4-32: Level B Mapping

The GS3470 distinguishes between Level A and Level B mappings at 3Gb/s. When Level B data is detected, each 10-bit link is demultiplexed into its individual component streams, and most video processing features, including error detection and correction are enabled separately for Data Stream 1 and Data Stream 2 (Link A and Link B, respectively).

**Note:** Audio demultiplexing and ancillary data extraction can only be enabled for one link for 3Gb/s Level B data. Data Stream 1 or Data Stream 2 can be selected via the host interface.

---

## 4.15 EDH Detection

### 4.15.1 EDH Packet Detection (SD Only)

The GS3470 determines if EDH packets are present in the incoming video data and asserts the **EDH\_DETECT** status according to the SMPTE standard.

**EDH\_DETECT** is set HIGH when EDH packets have been detected and remains HIGH until EDH packets are no longer present. It is set LOW at the end of the vertical blanking (falling edge of V) if an EDH packet has not been detected during vertical blanking.

**EDH\_DETECT** can be programmed to be an output on the *STAT[5:0]* pins through GSPI.

### 4.15.2 EDH Flag Detection

The EDH flags for ancillary data, active picture, and full field regions are extracted from the detected EDH packets and placed in the **EDH\_FLAG\_IN** register.

When the **EDH\_FLAG\_UPDATE\_MASK** bit in the host interface is set HIGH, the GS3470 updates the Ancillary Data, Full Field, and Active Picture EDH flags according to SMPTE RP165. The updated EDH flags are available in the **EDH\_FLAG\_OUT** register. The EDH packet output from the device contains these updated flags.

Flags are provided for both fields 1 and 2. The field 1 flag data is overwritten by the field 2 flag data.

When EDH packets are not detected, the UES flags in the **EDH\_FLAG\_OUT** register are set HIGH to signify that the received signal does not support Error Detection and Handling. In addition, the **EDH\_DETECT** bit is set LOW. These flags are set regardless of the setting of the **EDH\_FLAG\_UPDATE\_MASK** bit.

**EDH\_FLAG\_OUT** and **EDH\_FLAG\_IN** may be read via the host interface at any time during the received frame except on the lines defined in SMPTE RP165, when these flags are updated.

The GS3470 indicates the CRC validity for both active picture and full field CRCs. The **AP\_CRC\_V** bit in the host interface indicates the active picture CRC validity, and the **FF\_CRC\_V** bit indicates the full field CRC validity. When **EDH\_DETECT** = LOW, these bits are cleared.

The **EDH\_FLAG\_OUT** and **EDH\_FLAG\_IN** register values remain set until overwritten by the decoded flags in the next received EDH packet. When an EDH packet is not detected during vertical blanking, the flag registers are cleared at the end of the vertical blanking period.

---

## 4.16 Video Signal Error Detection & Indication

The GS3470 includes a number of video signal error detection functions. These are provided when operating in SMPTE mode ( $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$ ).

Signal errors that can be detected include:

1. TRS errors
2. HD line based CRC errors
3. EDH errors
4. HD line number errors
5. Device lock error
6. Ancillary data checksum errors

The GS3470 has two different registers for each set of error flags, **ERROR\_STAT\_[2:1]** and **ERROR\_STAT\_[2:1]\_STICKY**. **ERROR\_STAT\_[2:1]** registers are cleared on write, when not locked, on a change of video standard, and once per frame.

**ERROR\_STAT\_[2:1]\_STICKY** registers are read only and only cleared on read and reset.

**ERROR\_MASK\_[3:1]** are also provided, allowing the user to select which error conditions are reported. Each bit of the **ERROR\_MASK** register corresponds to a unique error type. Please refer to [Table 4-12](#) for a description of the **ERROR\_MASK** register bits.

Separate interrupt enable (**INT\_ENABLE**) registers for SD and HD audio cores are also provided, allowing select error conditions to be reported. Each bit of each **ERROR\_MASK** register corresponds to a unique error type.

By default (at power-up or after system reset), all bits of the **ERROR\_MASK** registers are zero, enabling all errors to be reported. Individual error detection may be disabled by setting the corresponding bit HIGH in the mask registers.

Error conditions are indicated by a **VIDEO\_ERROR** signal and an **AUDIO\_ERROR** signal, which are available for output on the multifunction I/O output pins. The two signals are also combined into a summary **DATA\_ERROR** signal, which is also available on the multifunction I/O pins. These signals are normally HIGH, but are set LOW by the device when an error condition has been detected.

These signals are a logical 'NOR' of the appropriate error status flags stored in the **ERROR\_STAT\_[2:1]** register, which are gated by the bit settings in the **ERROR\_MASK\_[3:1]** registers. When an error status bit is HIGH and the corresponding error mask bit is LOW, the corresponding **DATA\_ERROR** signal is set LOW by the device.

All bits of the error status register, including the **LOCK\_ERR** bit, is set LOW during system reset.

[Table 4-12](#) shows the **ERROR\_STAT\_[2:1]** register.

**Table 4-12: Error Status Register and Error Mask Register**

| Video Error Status Register | Video Error Mask Register                                                 |
|-----------------------------|---------------------------------------------------------------------------|
| EAV_ERR                     | EAV_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> )    |
| SAV_ERR                     | SAV_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> )    |
| YCRC_ERR                    | YCRC_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> )   |
| CCRC_ERR                    | CCRC_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> )   |
| LNUM_ERR                    | LNUM_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> )   |
| YCS_ERR_[2:1]               | YCS_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> )    |
| CCS_ERR_[2:1]               | CCS_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> )    |
| AP_CRC_ERR                  | AP_CRC_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> ) |
| FF_CRC_ERR                  | FF_CRC_ERR_MASK (848 <sub>h</sub> , 849 <sub>h</sub> , 84A <sub>h</sub> ) |

**Note 1:** See [Section 4.19](#) for Audio Error Status.

**Note 2:** In 3G Level B mode, separate Video Error Mask registers exist for Link A and Link B.

### 4.16.1 TRS Error Detection

TRS error flags are generated by the GS3470 under the following two conditions:

1. A phase shift in received TRS timing is observed.
2. The received TRS Hamming codes are incorrect

Both SAV and EAV TRS words are checked for timing and data integrity errors.

For HD mode, only the Y channel TRS codes are checked for errors.

For 3G mode Level A signals, only Data Stream 1 TRS codes are checked for errors. For 3G Level B signals, the Y channel TRS codes of both Link A and Link B are checked for errors.

Both 8-bit and 10-bit TRS code words are checked for errors.

---

### 4.16.2 Line Based CRC Error Detection

The GS3470 calculates line based CRCs for HD and 3G video signals. CRC calculations are performed for each 10-bit channel (Y and C for HD video, DS1 and DS2 for 3G video).

If a mismatch in the calculated and received CRC values is detected for Y channel data (Data Stream 1 for 3G video), the **YCRC\_ERR** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH.

If a mismatch in the calculated and received CRC values is detected for C channel data (Data Stream 2 for 3G video), the **CCRC\_ERR** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH.

Y or C CRC errors are also generated if CRC values are not embedded.

3G Level B signals all consist of two data streams. Each data stream is a multiplex of a C channel and a Y channel. Each channel of each data stream has CRC.

For 3G Level B formats, YCRC errors are detected for both of the two Y channels, and CCRC errors are detected for both of the two C channels.

**Note:** By default, 8-bit to 10-bit TRS remapping is enabled. If an 8-bit input is used, the HD CRC check is based on the 10-bit remapped value, not the 8-bit value, so the CRC Error Flag is incorrectly asserted and should be ignored. If 8-bit to 10-bit remapping is enabled, then CRC insertion should be enabled by setting the **CRC\_INS\_DS[2:1]\_MASK** bit LOW in the **IOPROC\_1** or **IOPROC\_2** register. This ensures that the CRC values are updated.

### 4.16.3 EDH CRC Error Detection

The GS3470 also calculates Full Field (FF) and Active Picture (AP) CRC's according to SMPTE RP165 in support of Error Detection and Handling packets in SD signals.

These calculated CRC values are compared with the received CRC values.

Error flags for AP and FF CRC errors are provided and each error flag is a logical OR of field 1 and field 2 error conditions.

The **AP\_CRC\_ERR** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH when an Active Picture CRC mismatch has been detected in field 1 or 2.

The **FF\_CRC\_ERR** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH when a Full Field CRC mismatch has been detected in field 1 or 2.

EDH CRC errors are only indicated when the device is operating in SD mode and when the device has correctly received EDH packets.

### 4.16.4 HD & 3G Line Number Error Detection

If a mismatch in the calculated and received line numbers is detected, the **LNUM\_ERR** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH.

---

## 4.17 Ancillary Data Detection & Indication

The GS3470 detects ancillary data in both the vertical and horizontal ancillary data spaces. The status signal outputs Y/1ANC and C/2ANC are provided to indicate the position of ancillary data in the output data streams. These signals may be selected for output on the multi-function I/O port pins (*STAT[5:0]*).

The GS3470 indicates the presence of all types of ancillary data by detecting the 000<sub>h</sub>, 3FF<sub>h</sub>, 3FF<sub>h</sub> (00<sub>h</sub>, FF<sub>h</sub>, FF<sub>h</sub> for 8-bit video) ancillary data preamble.

By default (at power up or after system reset) the GS3470 indicates all types of ancillary data. Up to 5 types of ancillary data can be specifically programmed for recognition.

For HD video signals, ancillary data may be placed in both the Y and Cb/Cr video data streams separately. For SD video signals, the ancillary data is multiplexed and combined into the YCbCr data space.

For 3G signals, ancillary data may exist in either or both of the virtual interface data streams. Both data streams are examined for ancillary data.

For a 3G data stream formatted as per Level A mapping:

- The ancillary data is placed in Data Stream 1 first, with overflow into Data Stream 2
- SMPTE ST 352 packets are duplicated in both data streams

For a 3G data stream formatted as per Level B mapping:

- Each multiplexed data stream forming the 3G signal contains ancillary data embedded according to SMPTE ST 291
- Each multiplexed data stream forming the 3G signal contains SMPTE ST 352 packets embedded according to SMPTE ST 425

For Y/1ANC and C/2ANC assertion and de-assertion while operating in SD, HD and 3G Level A, please refer to [Figure 4-33: Y/1ANC and C/2ANC Signal Timing](#).

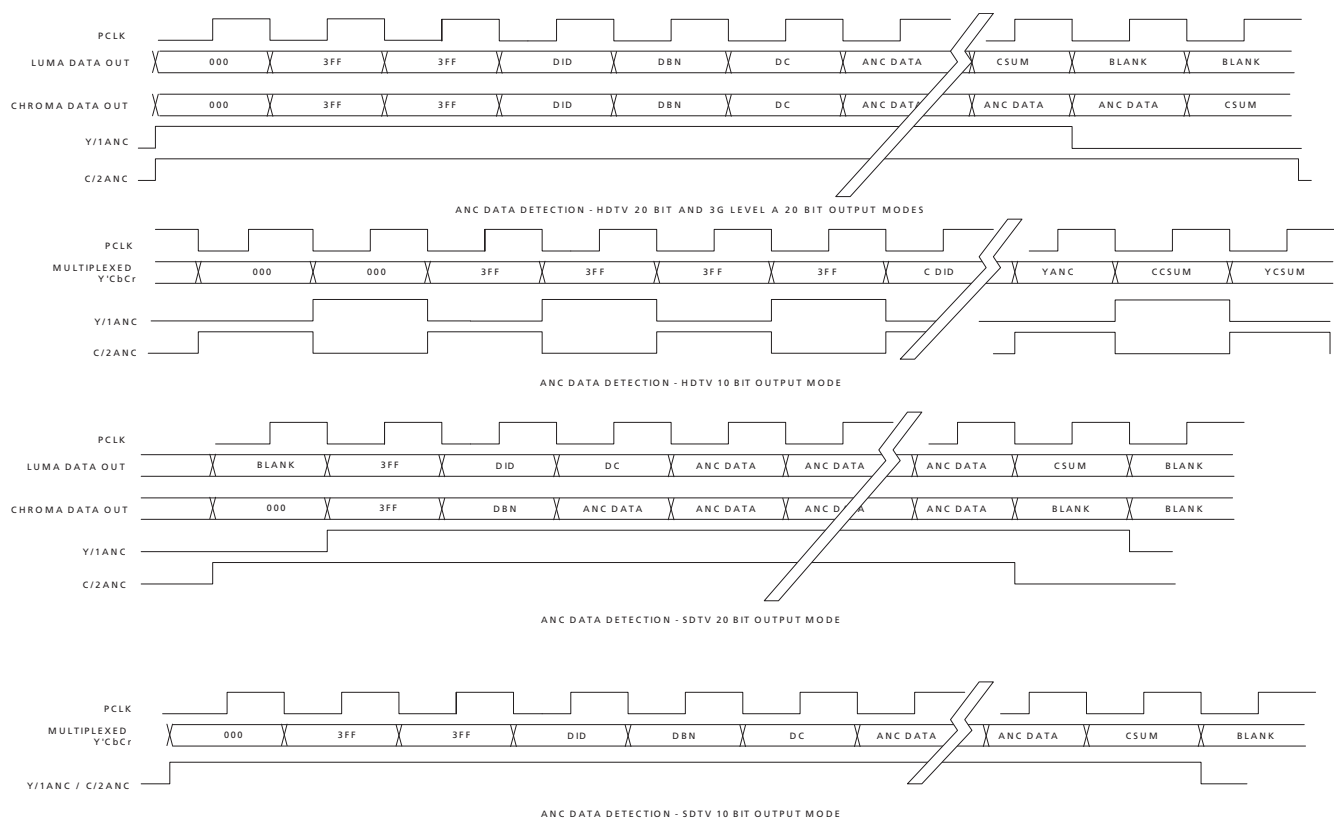
When detecting ancillary data in 3G Level B data, the Y/1ANC status output is HIGH when Data Stream 1 ancillary data is detected on either Y or C channels and the C/2ANC status output is HIGH whenever Data Stream 2 ancillary data is detected on either Y or C channels.

These status signal outputs are synchronous with PCLK and may be used as clock-enables for external logic, or as write-enables for an external FIFO or other memory devices.

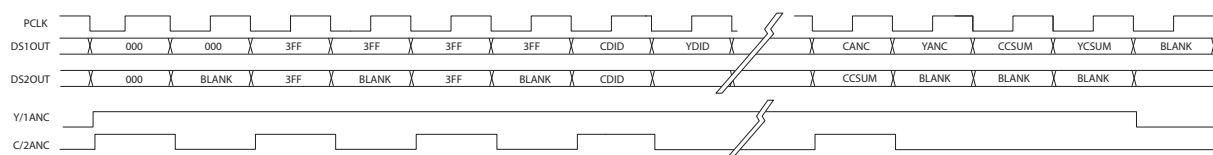
**Note 1:** When I/O processing is disabled, the Y/1ANC and C/2ANC flags may toggle, but they are invalid and should be ignored.

**Note 2:** For 3G Level B 20-bit data, the Y/1ANC flag identifies all ANC data on Data Stream 1 (Link A), whether it is embedded in the Y or C component – ANC data is not identified separately for each component. Similarly, the C/2ANC flag identifies all ANC data on Data Stream 2 (Link B), whether it is embedded in the Y or C component.

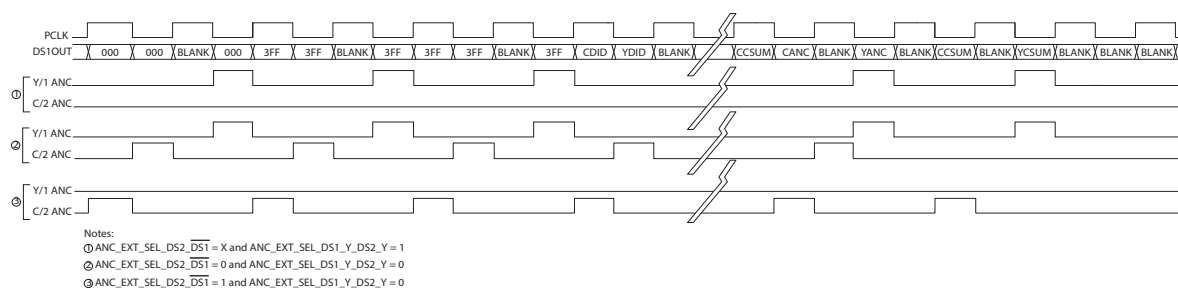
**Note 3:** For 3G level B 10-bit data, the Y/1 ANC flag and C/2 ANC flag outputs are dependent on the setting of **ANC\_EXT\_SEL\_DS2\_DS1** and **ANC\_EXT\_SEL\_DS1\_Y\_DS2\_Y** as shown in [Figure 4-35](#).



**Figure 4-33: Y/1ANC and C/2ANC Signal Timing**



**Figure 4-34: 3G Level B 20-bit Mode**



**Figure 4-35: 3G Level B 10-bit Mode**

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## 4.17.1 Programmable Ancillary Data Detection

As described above in [Section 4.17](#), the GS3470 detects and indicates all ancillary data types by default.

Up to 5 different ancillary data types may be programmed for detection in the **ANC\_TYPE\_[5:1]\_DS[2:1]** register for SD, HD, and 3G Level A. When these are programmed, the GS3470 only indicates the presence of the specified ancillary data types, ignoring all other types. For each data type to be detected, the user must program the DID and/or SDID of that ancillary data type. If no DID or SDID values are programmed, the GS3470 indicates the presence of all ancillary data.

For any DID or SDID value set to zero, no comparison or match is made. For example, if the DID is programmed and the SDID is not programmed, the GS3470 only detects a match to the DID value.

If both DID and SDID values are non-zero, then the received ancillary data type must match both the DID and SDID before Y/1ANC and/or C/2ANC is set HIGH.

**Note 1:** For 3G Level B data, the **ANC\_TYPE\_[5:1]\_DS1** registers are valid for Data Stream 1, and a second set of **ANC\_TYPE\_[5:1]\_DS2** is provided for detection of specific ancillary data in Data Stream 2.

**Note 2:** SMPTE ST 352 Payload Identifier packets and Error Detection and Handling (EDH) Packets are always detected by the GS3470, regardless of the settings of the **ANC\_TYPE\_[5:1]\_DS1** registers and cannot be overridden.

### 4.17.1.1 Programmable Ancillary Data Checksum Calculation

As described above, the GS3470 calculates and compares checksum values for all ancillary data types by default. It is possible to program which ancillary data types are checked as described in [Section 4.17.1](#).

When so programmed, the GS3470 only checks ancillary data checksums for the specified data types, ignoring all other ancillary data.

The **YCS\_ERR\_[2:1]** and/or **CCS\_ERR\_[2:1]** bits in the **ERROR\_STAT\_[2:1]** register are only set HIGH if an error condition is detected for the programmed ancillary data types.

## 4.17.2 SMPTE ST 352 Payload Identifier

The SMPTE ST 352 Payload Identifier is used to confirm the video format identified by the Automatic Video Standards Detection block.

Information contained in the packet is outlined in [Table 4-13](#).

**Table 4-13: SMPTE ST 352 Packet Data**

| Bit Name                                                                        | Bit  | Name                   | Description                                                                                                         | R/ $\overline{W}$ | Default |
|---------------------------------------------------------------------------------|------|------------------------|---------------------------------------------------------------------------------------------------------------------|-------------------|---------|
| <b>VIDEO_FORMAT_352_A [2:1]</b><br>Address: 828 <sub>h</sub> , 82C <sub>h</sub> | 15:8 | SMPTE ST 352<br>Byte 2 | Data is available in this register when<br>Video Payload Identification Packets are<br>detected in the data stream. | R                 | 0       |
|                                                                                 | 7:0  | SMPTE ST 352<br>Byte 1 |                                                                                                                     | R                 | 0       |
| <b>VIDEO_FORMAT_352_B [2:1]</b><br>Address: 829 <sub>h</sub> , 82D <sub>h</sub> | 15:8 | SMPTE ST 352<br>Byte 4 |                                                                                                                     | R                 | 0       |
|                                                                                 | 7:0  | SMPTE ST 352<br>Byte 3 |                                                                                                                     | R                 | 0       |
| <b>VIDEO_FORMAT_352_C [2:1]</b><br>Address: 82A <sub>h</sub> , 82E <sub>h</sub> | 15:8 | SMPTE ST 352<br>Byte 2 |                                                                                                                     | R                 | 0       |
|                                                                                 | 7:0  | SMPTE ST 352<br>Byte 1 |                                                                                                                     | R                 | 0       |
| <b>VIDEO_FORMAT_352_D [2:1]</b><br>Address: 82B <sub>h</sub> , 82F <sub>h</sub> | 15:8 | SMPTE ST 352<br>Byte 4 |                                                                                                                     | R                 | 0       |
|                                                                                 | 7:0  | SMPTE ST 352<br>Byte 3 |                                                                                                                     | R                 | 0       |

The GS3470 automatically extracts the SMPTE ST 352 payload identifier present in the input data stream. For SD, HD, and 3G Level A, the bytes are written to **VIDEO\_FORMAT\_352\_X\_1**. For 3G Level B, they are also written to **VIDEO\_FORMAT\_352\_X\_2**.

The device also indicates the version of the payload packet in **VERSION\_352M** (bit-7 of byte 1) of the **VIDEO\_FORMAT\_352\_X\_X** register as per SMPTE 352M. When the SMPTE ST 352 packet is formatted as a “version 1” packet, the **VERSION\_352M** bit is set LOW, when the packet is formatted as a “version 2” packet, this bit is set HIGH.

The **VIDEO\_FORMAT\_352\_X\_1** and **VIDEO\_FORMAT\_352\_X\_2** registers are only updated if checksum errors are not present.

By default (at power up or after system reset), the **VIDEO\_FORMAT\_352\_X\_1** and **VIDEO\_FORMAT\_352\_X\_2** bits are set to 0, indicating an undefined format.

#### 4.17.2.1 Extension for UHD Multi-Link 3G Identification

UHD formats that are transported in multi-link 3G formats will have a link identifier present in bits [7:4] of byte 4 of the 352M packet. This information is saved to 4 bits in the **VID\_STD\_DS[2:1]** register.

---

### 4.17.3 Ancillary Data Checksum Error

The GS3470 calculates checksums for all received ancillary data. These calculated checksums are compared with the received ancillary data checksum words.

If a mismatch in the calculated and received checksums is detected, then a checksum error is indicated.

When operating in HD mode, the device makes comparisons on both the Y and C channels separately. If an error condition in the Y channel is detected, the **YCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH. If an error condition in the C channel is detected, the **CCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH.

When operating in 3G Level A mode, the device makes comparisons on both the Y (Data Stream 1) and C (Data Stream 2) channels separately. If an error condition in the Y channel is detected, the **YCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH. If an error condition in the C channel is detected, the **CCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_[2:1]** register is set HIGH.

When operating in 3G Level B mode, the device makes comparisons on both the Y channel and the C channel of both Link A and Link B. For Link A, if an error condition in the Y channel is detected, the **YCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_1** register is set HIGH. If an error condition in the C channel is detected, the **CCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_1** register is set LOW. For Link B, if an error condition in the Y channel is detected, the **YCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_2** register is set HIGH. If an error condition in the C channel is detected, the **CCS\_ERR\_[2:1]** bit in the **ERROR\_STAT\_2** register is set LOW.

When operating in SD mode, only the **YCS\_ERR\_[2:1]** bit is set HIGH when checksum errors are detected.

## 4.18 Signal Processing

### 4.18.1 Audio De-Embedding Mode

The GS3470 includes an integrated audio de-embedder which is active when the deserializer is configured for SMPTE mode unless disabled using the **AUDIO\_EN/DIS** pin. In non-SMPTE modes, the audio de-embedder is powered down to reduce power consumption. All output pins are LOW when the de-embedder is powered down.

For detailed description of this feature, refer to [Section 4.19](#).

## 4.18.2 ANC Processing

The GS3470 can correct errors by inserting corrected code words, checksums, and CRC values into the data stream. The following processing can be performed by the GS3470:

1. TRS insertion
2. HD line based CRC insertion
3. EDH CRC insertion
4. HD line number insertion
5. Illegal code re-mapping
6. Ancillary data checksum insertion
7. Audio extraction
8. Ancillary data extraction
9. PID regeneration

All of the above features are only available in SMPTE mode ( $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$ ). To enable these features, the **IOPROC\_EN** bit must be set HIGH, and the individual feature must be enabled via bits in the **IOPROC\_1** and/or **IOPROC\_2** (depending on the data stream) register(s).

The **IOPROC\_1** and **IOPROC\_2** registers contain one bit for each processing feature allowing each one to be enabled/disabled individually.

By default (at power-up or after device reset), all of the **IOPROC\_1** and **IOPROC\_2** register bits described in Table 4-14 below are set to zero (0), which enables all of the processing features.

To disable an individual processing feature, set the corresponding bit to one (1) in the **IOPROC\_1** and/or **IOPROC\_2** register(s).

**Table 4-14: IOPROC\_1 and IOPROC\_2 Register Bits**

| Processing Feature                 | IOPROC_1 Register Bit           | IOPROC_2 Register Bit                           |
|------------------------------------|---------------------------------|-------------------------------------------------|
| TRS insertion                      | TRS_INS_DS1_MASK                | TRS_INS_DS2_MASK                                |
| Y and C line based CRC insertion   | CRC_INS_DS1_MASK                | CRC_INS_DS2_MASK                                |
| Y and C line number insertion      | LNUM_INS_DS1_MASK               | LNUM_INS_DS2_MASK                               |
| Ancillary data check sum insertion | ANC_CHECKSUM_INSERTION_DS1_MASK | ANC_CHECKSUM_INSERTION_DS2_MASK                 |
| EDH CRC insertion                  | EDH_CRC_INS_MASK                | N/A                                             |
| Illegal code re-mapping            | ILLEGAL_WORD_REMAP_DS1_MASK     | ILLEGAL_WORD_REMAP_DS2_MASK                     |
| H timing signal configuration      | H_CONFIG                        | N/A                                             |
| Update EDH Flags                   | EDH_FLAG_UPDATE_MASK            | N/A                                             |
| Audio Data Extraction              | AUD_EXT_MASK                    | AUDIO_SEL_DS2_DS1                               |
| Ancillary Data Extraction          | ANC_DATA_EXT_MASK               | ANC_EXT_SEL_DS2_DS1,<br>ANC_EXT_SEL_DS1_Y_DS2_Y |
| Regeneration of ST 352 packets     | N/A                             | REGEN_352M_MASK                                 |

---

### 4.18.3 TRS Insertion

When TRS Insertion is enabled, the GS3470 generates and overwrites TRS code words as required.

TRS Word Generation and Insertion is performed using the timing generated by the Timing Signal Generator, providing an element of noise immunity over using just the received TRS information.

This feature is enabled when the **IOPROC\_EN** bit is HIGH and the **TRS\_INS\_DS1\_MASK** or **TRS\_INS\_DS2\_MASK** bits in the **IOPROC\_1** or **IOPROC\_2** registers are set LOW. The **TRS\_INS\_DS1\_MASK** bit is in the **IOPROC\_1** register and is used to enable/disable TRS insertion for SD, HD, 3G-A data streams, and data stream 1 of 3G Level B. The **TRS\_INS\_DS2\_MASK** bit is in the **IOPROC\_2** register and is used to enable/disable TRS insertion for 3G-B data streams only.

For 3G Level A signals, TRS insertion occurs in both Data Stream 1 and Data Stream 2.

For 3G Level B signals, TRS insertion occurs in both Data Stream 1 and Data Stream 2 of both Link A and Link B.

**Note:** Inserted TRS code words are always 10-bit compliant, regardless of the bit depth of the incoming video stream.

### 4.18.4 Line Based CRC Insertion

When CRC Insertion is enabled, the GS3470 generates and inserts line based CRC words into both the Y and C channels of the data stream.

Line based CRC word generation and insertion only occurs in HD and 3G modes, and is enabled in when the **IOPROC\_EN** bit is HIGH and the **CRC\_INS\_DS[2:1]\_MASK** bit in the **ICPROC\_[2:1]** register is set LOW.

For 3G Level A signals, line based CRC word generation and insertion occurs in both Data Stream 1 and Data Stream 2.

For 3G Level B signals, line based CRC word generation and insertion occurs in both Data Stream 1 and Data Stream 2 of both Link A and Link B.

---

### 4.18.5 Line Number Insertion

When Line Number Insertion is enabled, the GS3470 calculates and inserts line numbers into the output data stream. Re-calculated line numbers are inserted into both the Y and C channels.

Line number generation is in accordance with the relevant HD or 3G video standard as determined by the Automatic Standards Detection block.

This feature is enabled when the device is operating in HD or 3G modes, the **IOPROC\_EN** bit is HIGH and the **LNUM\_ERR** bit in the **IOPROC\_[2:1]** register is set LOW.

For 3G Level A signals, line number insertion occurs in both Data Stream 1 and Data Stream 2.

For 3G Level B signals, line number insertion occurs in both Data Stream 1 and Data Stream 2 of both Link A and Link B.

### 4.18.6 ANC Data Checksum Insertion

When ANC data Checksum Insertion is enabled, the GS3470 generates and inserts ancillary data checksums for all ancillary data words by default.

Where user specified ancillary data has been programmed (see [Section 4.17.1](#)), only the checksums for the programmed ancillary data are corrected.

This feature is enabled when the **IOPROC\_EN** bit is HIGH and the **ANC\_CHECKSUM\_INSERTION\_DS[2:1]\_MASK** bit in the **IOPROC\_[2:1]** register is set LOW.

For 3G Level A signals, ANC data checksum insertion occurs in both Data Stream 1 and Data Stream 2.

For 3G Level B signals, ANC data checksum insertion occurs in both Y and C channels of both Data Stream 1 and Data Stream 2.

### 4.18.7 EDH CRC Insertion

When EDH CRC Insertion is enabled, the GS3470 generates and overwrites full field and active picture CRC check-words. Additionally, the device sets the active picture and full field CRC 'V' bits HIGH in the EDH packet. The **AP\_CRC\_V** and **FF\_CRC\_V** register bits only report the received EDH validity flags.

Although the GS3470 modifies and inserts EDH CRC's and EDH packet checksums, EDH error flags are only updated when the **EDH\_FLAG\_UPDATE\_MASK** bit is LOW.

This feature is enabled in SD mode, when the **IOPROC\_EN** bit is HIGH and the **EDH\_CRC\_INS\_MASK** bit in the **IOPROC\_1** register is set LOW.

### 4.18.8 Illegal Word Re-mapping

All words within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FC<sub>h</sub> and 3FF<sub>h</sub> are re-mapped to 3FB<sub>h</sub>. All words within the active picture area between the values of 000<sub>h</sub> and 003<sub>h</sub> are remapped to 004<sub>h</sub>.

---

This feature is enabled when the **IOPROC\_EN** bit is HIGH and the **ILLEGAL\_WORD\_REMAP\_DS[2:1]\_MASK** bit in the **IOPROC\_[2:1]** register is set LOW.

For 3G Level A signals, illegal code remapping occurs in both Data Stream 1 and Data Stream 2.

For 3G Level B signals, illegal code remapping occurs in both Data Stream 1 and Data Stream 2 of both Link A and Link B.

### 4.18.9 TRS and Ancillary Data Preamble Remapping

8-bit TRS and ancillary data preambles are re-mapped to 10-bit values. 8-bit to 10-bit mapping of TRS headers is only supported if the TRS values are 3FC 000 000<sub>h</sub>. Other values such as 3FD<sub>h</sub>, 3FE<sub>h</sub>, 001<sub>h</sub>, 002<sub>h</sub>, and 003<sub>h</sub> are not supported.

This feature is enabled by default, and can be disabled via the **IOPROC\_[2:1]** register.

### 4.18.10 Ancillary Data Extraction

The GS3470 includes a FIFO, which extracts ancillary data using read access via the host interface to ease system implementation. The FIFO stores up to 2048 x 16 bit words of ancillary data in two separate 1024 word memory banks.

As an alternative, ancillary data may be extracted externally from the GS3470 output stream using the Y/1ANC and C/2ANC signals, and external logic.

Data is accessed from both memory banks using the same host interface addresses, C00<sub>h</sub> to FFF<sub>h</sub>.

The device writes the contents of ANC packets into the FIFO, starting with the first Ancillary Data Flag (ADF), followed by up to 1024 words.

All Data Identification (DID), Secondary Data Identification (SDID), Data Count (DC), user data, and checksum words are written into the device memory.

The device detects ancillary data packet DID's placed anywhere in the video data stream, including the active picture area.

In HD and 3G mode, ancillary data from the Y channel or Data Stream 1 is placed in the Least Significant Word (LSW) of the FIFO, allocated to the lower 8 bits of each FIFO address.

Ancillary data from the C channel or Data Stream 2 is placed in the Most Significant Word (MSW) (upper 8 bits) of each FIFO address.

**Note:** Please refer to the ANC insertion and Extraction Application Note (Doc ID: GENDOC-053410), for discrete steps and example of Ancillary data extraction using the GS3470.

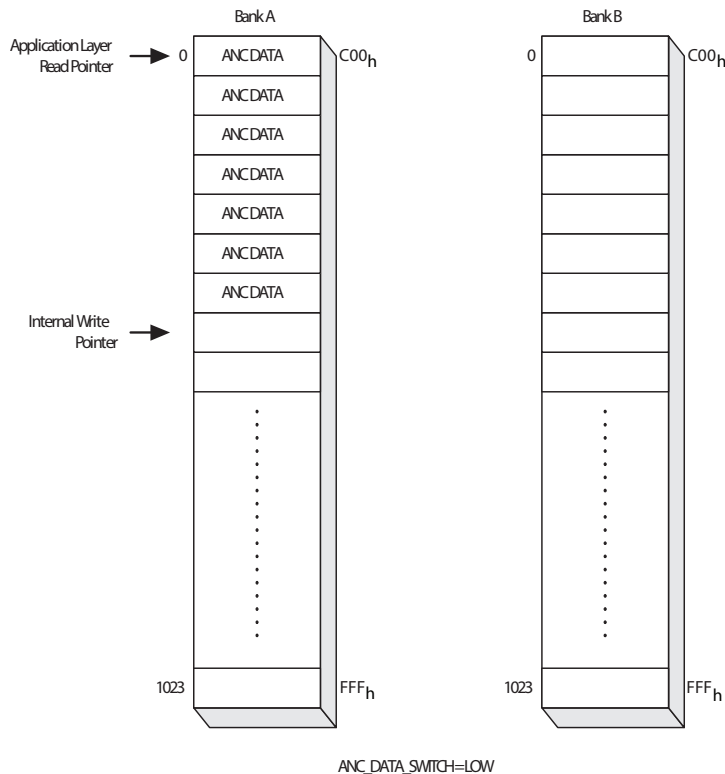
In SD mode, ancillary data is placed in the LSW of the FIFO. The MSW is set to zero.

If the **ANC\_TYPE[5:1]\_DS[2:1]** registers are all set to zero, the device extracts all types of ancillary data. If programmable ancillary data extraction is required, then up to five types of ancillary data to be extracted can be programmed in the

**ANC\_TYPE\_[5:1]\_DS[2:1]** registers (see [Section 4.17.1](#)).

Additionally, the lines from which the packets are to be extracted can be programmed into the **ANC\_LINEA** and **ANC\_LINEB** registers, allowing ancillary data from a maximum of two lines per frame to be extracted. If only one line number register is programmed (with the other set to zero), ancillary data packets are extracted from one line per frame only. When both registers are set to zero, the device extracts packets from all lines.

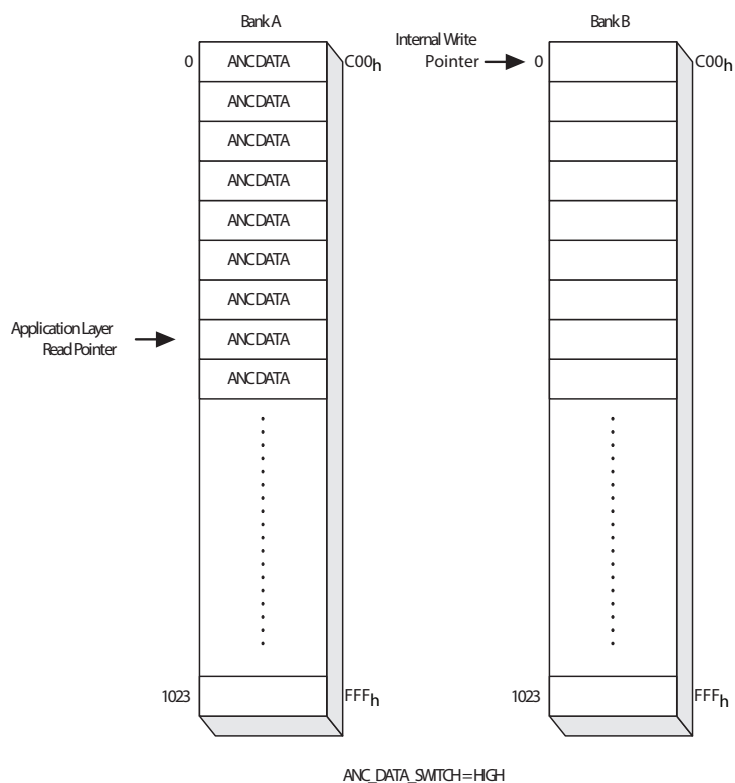
To start Ancillary Data Extraction, the **ANC\_DATA\_EXT\_MASK** bit of the host interface must be set LOW. Ancillary data packet extraction begins in the following frame (see [Figure 4-36: Ancillary Data Extraction - Step A](#)).



**Figure 4-36: Ancillary Data Extraction - Step A**

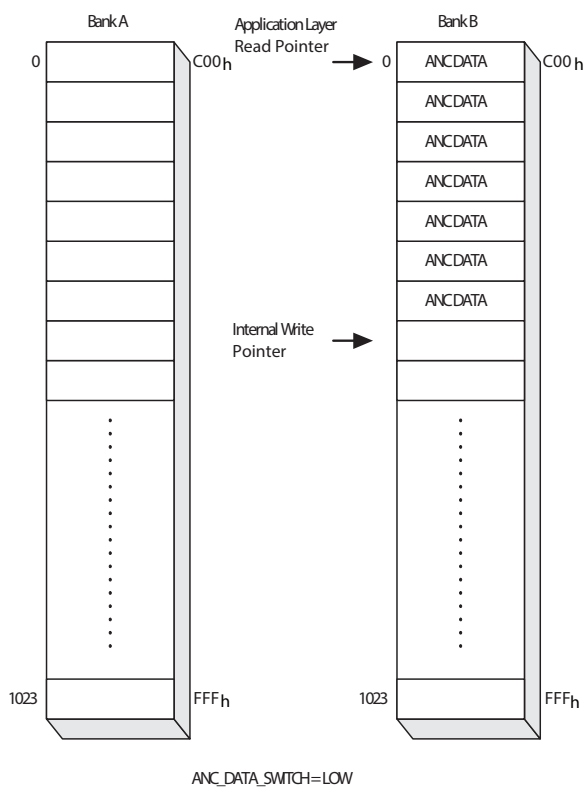
Ancillary data is written into Bank A until full. The Y/1ANC and C/2ANC output flags can be used to determine the length of the ancillary data extracted and when to begin reading the extracted data from memory.

While the **ANC\_DATA\_EXT\_MASK** bit is set LOW, the **ANC\_DATA\_SWITCH** bit can be set HIGH during or after reading the extracted data. New data is then written into Bank B (up to 1024 x 16-bit words), at the corresponding host interface addresses (see [Figure 4-37: Ancillary Data Extraction - Step B](#)).



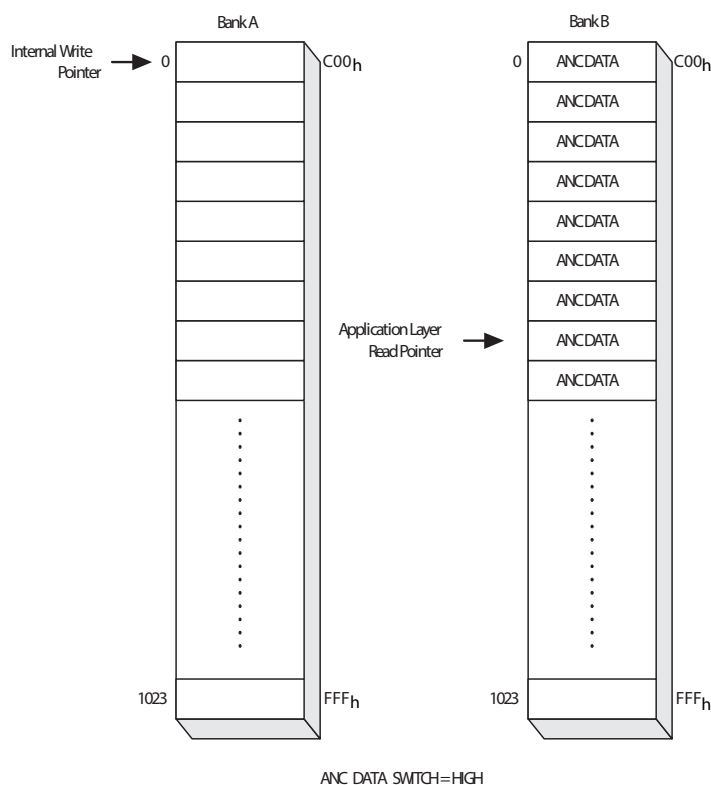
**Figure 4-37: Ancillary Data Extraction - Step B**

To read the new data, toggle the **ANC\_DATA\_SWITCH** bit LOW. The old data in Bank A is cleared to zero and extraction continues in Bank B (see [Figure 4-38: Ancillary Data Extraction - Step C](#)).



**Figure 4-38: Ancillary Data Extraction - Step C**

If the **ANC\_DATA\_SWITCH** bit is not toggled, extracted data is written into Bank B until full. To continue extraction in Bank A, the **ANC\_DATA\_SWITCH** bit must be toggled HIGH (see [Figure 4-39: Ancillary Data Extraction - Step D](#)).



**Figure 4-39: Ancillary Data Extraction - Step D**

Toggling the **ANC\_DATA\_SWITCH** bit LOW returns the process to step A (Figure 4-39).

**Note 1:** Toggling the **ANC\_DATA\_SWITCH** must occur at a time when no extraction is taking place, i.e. when the both the Y/1ANC and C/2ANC signals are LOW.

To turn extraction off, the **ANC\_DATA\_EXT\_MASK** bit must be set HIGH.

In HD mode, the device can detect ancillary data packets in the Luma video data only, Chroma video data only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from the Luma channel only.

In 3G mode Level A, the device can detect ancillary data packets in Luma video (Data Stream 1) only, Chroma video (Data Stream 2) only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from Data Stream 1 only.

In 3G mode Level B, the device can detect ancillary data packets in Luma video only, Chroma video only, or both from either Link A or Link B. Selection of Link A or Link B for ANC data extraction is done via the host interface.

In 3G Level B the device may be programmed via the user interface so that the YANC data from Link A is extracted as the YANC data and the YANC data from Link B is extracted as CANC data. By default, or at reset or power-up, this is the setup for 3G level B input signals.

---

To extract packets from the Chroma/Data Stream 2 channel only, the **HD\_ANC\_C2** bit of the host interface must be set HIGH. To extract packets from both Luma/Data Stream 1 and Chroma/Data Stream 2 video data, the **HD\_ANC\_Y1\_C2** bit must be set HIGH (the setting of the **HD\_ANC\_C2** bit is ignored).

The default setting of both the **HD\_ANC\_C2** and **HD\_ANC\_Y1\_C2** is LOW. The setting of these bits is ignored when the device is configured for SD video standards.

After extraction, the ancillary data may be deleted from the video stream by setting the **ANC\_DATA\_DEL** bit of the host interface HIGH. When set HIGH, all existing ancillary data is removed and replaced with blanking values. If any of the **ANC\_TYPE [5:1]\_DS[2:1]** registers are programmed with a DID and/or DID and SDID, only the ancillary data packets with the matching IDs are deleted from the video stream.

Ancillary data packet extraction and deletion is disabled when the **IOPROC\_EN** bit is set LOW.

**Note 2:** After the ancillary data determined by the **ANC\_TYPE [5:1]\_DS[2:1]** registers has been deleted, other existing ancillary data may not be contiguous. The device does not concatenate the remaining ancillary data.

**Note 3:** Reading extracted ancillary data from the host interface must be performed while there is a valid video signal present at the serial input and the device is locked (LOCKED signal is HIGH).

The value of the active write pointer is written to a host interface accessible register once per line, or at the end of the VANC period.

This allows a software only ANC data extraction application, which is only interfaced to the device via the host interface, and does not have access to the Y/1ANC and C/2ANC output flags, to determine when ANC data has been detected by the device.

## 4.19 Audio De-Embedder

Up to eight channels of audio may be extracted from the received serial digital video stream. The output signal formats supported by the device include AES/EBU, I2S (default), and industry standard serial digital formats.

16, 20, and 24-bit audio bit depths are supported for 48kHz synchronous audio for SD data rates. For HD and 3G data rates, 16, 20, and 24-bit audio bit depths are supported for 48kHz audio. The audio may be synchronous or asynchronous to the video.

In 3G mode:

- In Level A mode, all Audio Control Packets are extracted from Data Stream 1 and all Audio Data Packets are extracted from Data Stream 2, in accordance with SMPTE ST 425. This is similar to HD, in which Audio Control Packets are embedded in the Luma channel and Audio Data Packets in the Chroma channel
- In Level B mode, extraction of audio packets from Link A (default) or Link B is selectable via the **AUDIO\_SEL\_DS2\_DS1** bit in the host interface.

Additional audio processing features include audio mute on loss of lock, de-embed and delete, group selection, audio output re-mapping, ECC error detection and correction (HD/3G modes only), and audio channel status extraction.

## 4.19.1 Serial Audio Data I/O Signals

The Serial Audio Data I/O pins are listed in [Table 4-15: Serial Audio Pin Descriptions](#).

**Table 4-15: Serial Audio Pin Descriptions**

| Pin Name                          | Description                                           |
|-----------------------------------|-------------------------------------------------------|
| AUDIO_EN/ $\overline{\text{DIS}}$ | Enable Input for Audio Processing                     |
| AOUT_1_2                          | Serial Audio Output; Channels 1 and 2                 |
| AOUT_3_4                          | Serial Audio Output; Channels 3 and 4                 |
| AOUT_5_6                          | Serial Audio Output; Channels 5 and 6                 |
| AOUT_7_8                          | Serial Audio Output; Channels 7 and 8                 |
| ACLK                              | 64fs Audio Bit Clock                                  |
| WCLK                              | Word Clock                                            |
| AMCLK                             | Audio Master Clock, selectable 128fs, 256fs, or 512fs |

The timing of the serial audio out signals, the *WCLK* output signal and the *ACLK* output is shown in [Figure 4-45: ACLK to Data Signal Output Timing](#).

When *AUDIO\_EN/ $\overline{\text{DIS}}$*  pin is set HIGH, audio extraction is enabled and the audio output signals are extracted from the video data stream. When set LOW, the serial audio outputs, *ACLK*, and *WCLK* outputs are set LOW.

In addition, all functional logic associated with audio extraction is disabled to reduce power consumption.

## 4.19.2 Serial Audio Data Format Support

The GS3470 supports the following serial audio data formats:

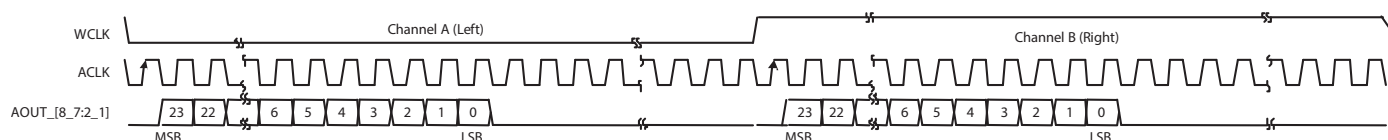
- I<sup>2</sup>S (default)
- AES/EBU
- Serial Audio Left Justified, MSB First
- Serial Audio Right Justified, MSB First (supported for HD and 3G only)

By default (at power up or after system reset) I<sup>2</sup>S is selected. The other data formats are selectable via the host interface using the **AMA/AMB[1:0]** bits of the **CFG\_AUD**(HD/3G) or **CFG\_OUTPUT**(SD) register.

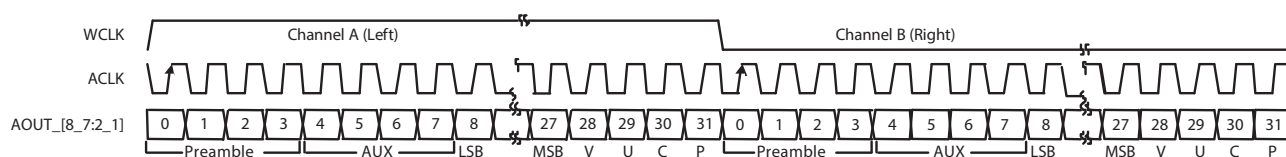
**Table 4-16: Audio Output Formats**

| AMA/AMB[1:0] | Audio Output Format                                                            |
|--------------|--------------------------------------------------------------------------------|
| 00           | AES/EBU audio output                                                           |
| 01           | Serial audio output: Left Justified; MSB first                                 |
| 10           | Serial audio output: Right Justified; MSB first (supported for HD and 3G only) |
| 11           | I <sup>2</sup> S (Default)                                                     |

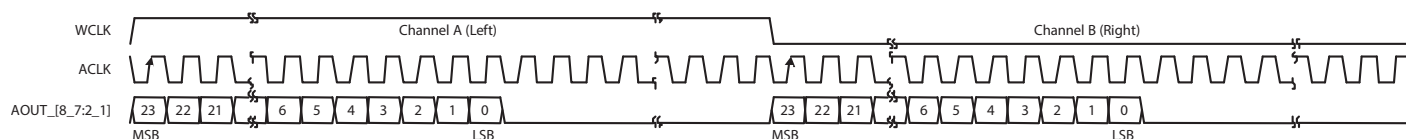
When I<sup>2</sup>S format is desired, both groups must be set to I<sup>2</sup>S (i.e. AMA = AMB = 11). This is because they share the same *WCLK*.



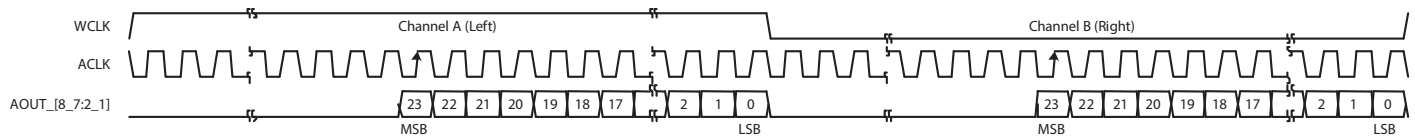
**Figure 4-40: I<sup>2</sup>S Audio Output Format**



**Figure 4-41: AES/EBU Audio Output Format**



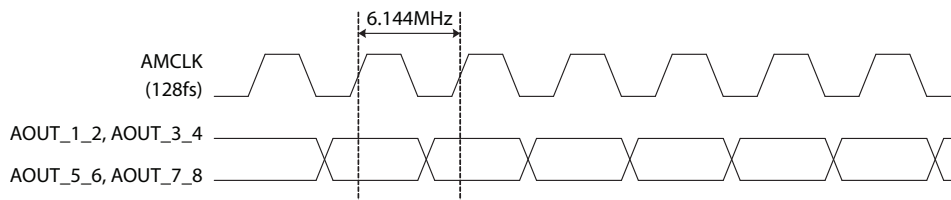
**Figure 4-42: Serial Audio, Left Justified, MSB First**



**Figure 4-43: Serial Audio, Right Justified, MSB First**

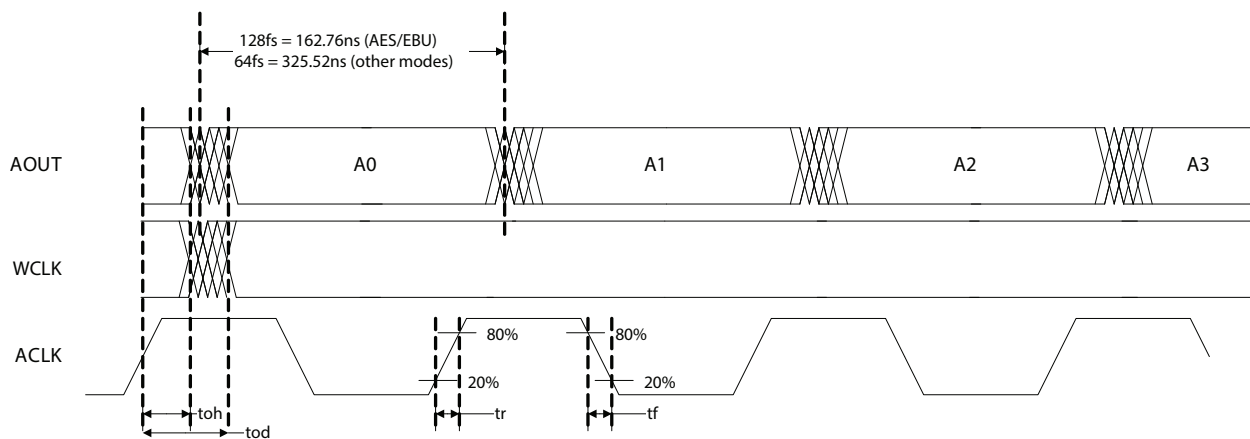
#### 4.19.2.1 AES/EBU Mode

In AES/EBU output mode, the audio de-embedder uses a 128fs (6.144MHz audio bit clock) clock as shown in [Figure 4-44](#).



**Figure 4-44: AES/EBU Audio Output to Bit Clock Timing**

The timing of the serial audio output signals and the ACLK output signal is shown in [Figure 4-45: ACLK to Data Signal Output Timing](#).



**Figure 4-45: ACLK to Data Signal Output Timing**

#### 4.19.2.2 Audio Data Packet Extraction Block

The audio de-embedder looks for audio data packets on every line of the incoming video.

The audio data must be embedded according to SMPTE ST 272 (SD) or SMPTE ST 299/299-1/299-2 (HD or 3G).

In 3G Level A signals, the audio data packets must be embedded only in Data Stream 2.

In 3G Level B signals, the audio data packets must be embedded in the Data Stream 2 of either Link A or Link B and have a data rate of 74.25MHz.

The Audio Group Detect registers are set HIGH when audio data packets with a corresponding group DID are detected in the input video stream. The host interface reports the individual audio groups detected.

**Table 4-17: Audio Data Packet Detect Register**

| Name      | Description                                                        | Default |
|-----------|--------------------------------------------------------------------|---------|
| ADPG8_DET | Audio Group Eight Data Packet Detection (1: Detected) (HD/3G only) | 0       |
| ADPG7_DET | Audio Group Seven Data Packet Detection (1: Detected) (HD/3G only) | 0       |
| ADPG6_DET | Audio Group Six Data Packet Detection (1: Detected) (HD/3G only)   | 0       |
| ADPG5_DET | Audio Group Five Data Packet Detection (1: Detected) (HD/3G only)  | 0       |
| ADPG4_DET | Audio Group Four Data Packet Detection (1: Detected)               | 0       |
| ADPG3_DET | Audio Group Three Data Packet Detection (1: Detected)              | 0       |
| ADPG2_DET | Audio Group Two Data Packet Detection (1: Detected)                | 0       |
| ADPG1_DET | Audio Group One Data Packet Detection (1: Detected)                | 0       |

For SD, when an audio data packet with a DID set in **IDA[1:0]** and **IDB[1:0]** is detected, the audio sample information is extracted and written into the audio FIFO. For HD and 3G, **EXTEND\_IDA** and **EXTEND\_IDB** are used in addition to **IDA[1:0]** and **IDB[1:0]** to select one of 8 audio groups.

The embedded audio group selected by **IDA[1:0]** is described henceforth in this document as Group A or Primary Group. The embedded audio group selected by **IDB[1:0]** is described henceforth in this document as Group B or Secondary Group.

#### 4.19.2.3 Audio Control Packets

The audio de-embedder automatically detects the presence of audio control packets in the video stream. When audio control packets for audio Group A are detected, the **CTRA\_DET** bit of the host interface is set HIGH. When audio control packets for audio Group B are detected, the **CTRB\_DET** bit of the host interface is set HIGH.

The audio control packet data is accessible via the host interface.

The audio control packets must be embedded according to SMPTE ST 272 (SD) or SMPTE ST 299 (HD and 3G). In 3G Level A signals, the audio control packets must be embedded only in Data Stream 1. In 3G Level B signals the audio control packets must be embedded in the Luma streams of each link that carries audio.

**Note 1:** In SD, HD, and 3G, the audio control packet reporting via the host interface updates automatically when a new control packet is detected.

**Note 2:** If there is an HD audio packet checksum error, no audio is extracted. The audio packet is not recognized, and the audio stays in the video stream. If nothing but the CLK phase parity bit is wrong, the audio will extract fine.

#### 4.19.2.4 Setting Packet DID

Table 4-19 below, shows the 2-bit host interface setting for the audio group DID's.

For 24-bit audio support in SD mode, extended audio packets for Group A must have the same group DID set in **IDA[1:0]** of the host interface. Extended audio packets for Group B must have the same group DID set in **IDB[1:0]** of the host interface.

The audio de-embedder automatically detects the presence of extended audio packets. When detected, the audio output format is set to 24-bit audio sample word length.

The audio de-embedder defaults to audio Groups One and Two, where Group A is extracted from packets with audio Group One DID, and Group B from packets with audio Group Two DID.

**Table 4-18: Audio Group DID Host Interface Settings**

| Audio Group | SD Data DID      | SD Extended DID  | SD Control DID   | HD Data DID      | HD Control DID   | Host interface Register (2-bit) | Extended_ID Register Bit |
|-------------|------------------|------------------|------------------|------------------|------------------|---------------------------------|--------------------------|
| 1           | 2FF <sub>h</sub> | 1FE <sub>h</sub> | 1EF <sub>h</sub> | 2E7 <sub>h</sub> | 2E3 <sub>h</sub> | 00 <sub>b</sub>                 | 0                        |
| 2           | 1FD <sub>h</sub> | 2FC <sub>h</sub> | 2EE <sub>h</sub> | 1E6 <sub>h</sub> | 2E2 <sub>h</sub> | 01 <sub>b</sub>                 | 0                        |
| 3           | 1FB <sub>h</sub> | 2FA <sub>h</sub> | 2ED <sub>h</sub> | 1E5 <sub>h</sub> | 2E1 <sub>h</sub> | 10 <sub>b</sub>                 | 0                        |
| 4           | 2F9 <sub>h</sub> | 1F8 <sub>h</sub> | 1EC <sub>h</sub> | 2E4 <sub>h</sub> | 1E0 <sub>h</sub> | 11 <sub>b</sub>                 | 0                        |
| 5           | —                | —                | —                | 1A7 <sub>h</sub> | 2A3 <sub>h</sub> | 00 <sub>b</sub>                 | 1                        |
| 6           | —                | —                | —                | 2A6 <sub>h</sub> | 1A2 <sub>h</sub> | 01 <sub>b</sub>                 | 1                        |
| 7           | —                | —                | —                | 2A5 <sub>h</sub> | 1A1 <sub>h</sub> | 10 <sub>b</sub>                 | 1                        |
| 8           | —                | —                | —                | 1A4 <sub>h</sub> | 2A0 <sub>h</sub> | 11 <sub>b</sub>                 | 1                        |

**Table 4-19: Audio Data and Control Packet DID Setting Register**

| Name       | Description                                                    | Default         |
|------------|----------------------------------------------------------------|-----------------|
| IDA[1:0]   | Group A Audio data and control packet DID setting              | 00 <sub>b</sub> |
| IDB[1:0]   | Group B Audio data and control packet DID setting              | 01 <sub>b</sub> |
| EXTEND_IDA | Group A Audio data and control packet DID setting (HD/3G only) | 0 <sub>b</sub>  |
| EXTEND_IDB | Group B Audio data and control packet DID setting (HD/3G only) | 0 <sub>b</sub>  |

### 4.19.2.5 Audio Packet Delete Block

To delete all ancillary data with a group DID shown in Table 4-18, the **ALL\_DEL** bit in the host interface must be set HIGH.

**Note:** Low latency mode option is not available when this feature is enabled.

### 4.19.2.6 ECC Error Detection & Correction Block (HD Mode Only)

The audio de-embedder performs BCH(31, 25) forward error detection and correction, as described in SMPTE ST 299. The error correction for all embedded audio data packets is activated when the host interface **ECC\_OFF** bit is set LOW (default LOW). The audio de-embedder corrects any errors in both the audio output and the embedded packet.

When a one-bit error is detected in a bit array of the ECC protected region of the audio data packet with audio group DID set in **IDA[1:0]**, the **ECCA\_ERROR** flag is set HIGH. When a one-bit error is detected in the ECC protected region of the audio data packet with audio group DID set in **IDB[1:0]**, the **ECCB\_ERROR** flag is set HIGH.

Figure 4-46 shows examples of error correction and detection. Up to 8 bits in error can be corrected, providing each bit error is in a different bit array (shown below). When there are two or more bits in error in the same 24-bit array, the errors are detected, but not corrected.

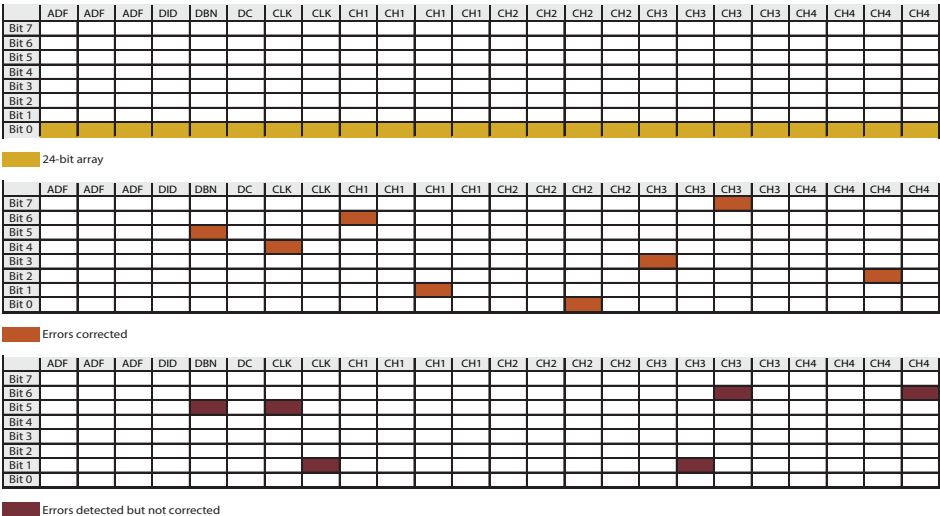


Figure 4-46: ECC 24-bit Array and Examples

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## 4.19.3 Audio Processing

### 4.19.3.1 Audio Clock Generation

For SD and HD/3G audio, a single set of audio frequencies is generated for all audio channels.

For Mapping structure one signals (1080p 50, 59.94, or 60 or 2048p 50, 59.94, or 60), the pixel clock is 148.5/(M)MHz, and the phase data are based on this rate. An Audio Master Clock (AMCLK) is also generated. The frequency is selectable via the host interface as:

- $fs \times 128$
- $fs \times 256$
- $fs \times 512$

In SD mode, audio clocks are derived from the *PCLK*.

In HD/3G modes, audio clocks are derived from the two embedded audio clock phase words in the audio data packet.

The audio de-embedder also includes a Flywheel block to overcome any inconsistencies in the embedded audio clock phase information.

If the audio phase data is not present or incorrect, the **INVALID\_EMBEDDED\_PHASE[B:A]** bit in the host interface will be asserted and audio will be de-embedded using a clock derived from *PCLK* and the M value.

Alternatively, when the **IGNORE\_PHASE** bit in the host interface is set HIGH, the M value can be programmed via the host interface. This can be done by setting the **FORCE\_M** bit HIGH, and programming the desired value into **FORCE\_MEQ1001**. The correct value can be obtained by reading the M bit from the Video Core Registers.

If the ADPLL is locked to phase data and audio data packets are lost or corrupted, the Clock Generator will flywheel for up to four audio data packets.

If the **IGNORE\_PHASE** bit in the host interface is HIGH, the clock will free-run based on the video format, the *PCLK* and the M value, independent of the **INVALID\_EMBEDDED\_PHASE[B:A]** bit.

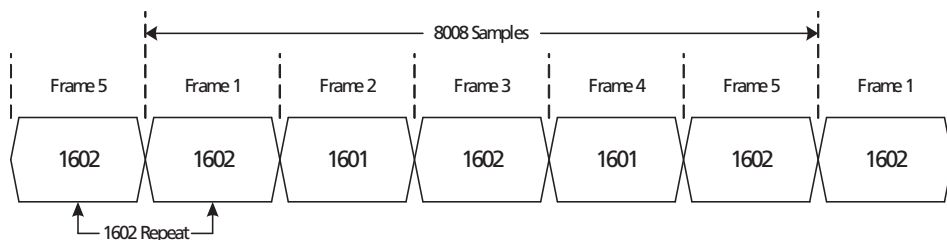
In the 720p/24 video format, the total line length is 4125 pixels, which requires a resolution of 13 bits for the audio clock phase words in the embedded audio data packets. SMPTE ST 299 only specifies a maximum of 12 bits resolution. The revised versions of SMPTE ST 299 require using bit 5 of UDW1 in the audio data packet as the MSB (ck13) for the audio clock phase data, providing 13 bits resolution.

Some audio encoders may hold the clock phase value at a maximum value when reached, until reset at the end of the line. This produces a small amount of audio phase jitter for the period of one sample.

To overcome this issue, the audio de-embedder checks for all cases. On detection of the maximum value, a comparison is made between previous clock phases and the correct position interpolated. If the clock phase data value starts to decrease, the de-embedder checks to see if bit 5 (ck13) of UDW1 in the audio data packet is asserted. If ck13 is asserted, the correct value is used. If ck13 is not set, the correct position is interpolated.

### 4.19.3.2 Detect 5-Frame Sequence Block

Five-frame sequence detection is required for 525-line based video formats only. If the Audio Frame Number words are set to  $200_{\text{h}}$ , the audio de-embedder detects the five-frame sequence by counting the number of samples per frame. Figure 4-47 shows the number of samples per frame over a five-frame sequence.



**Figure 4-47: Sample Distribution over 5 Video Frames (525-line Systems)**

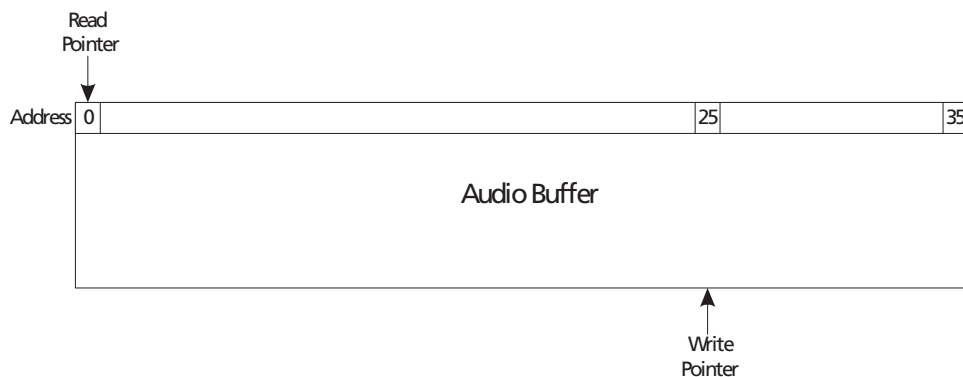
When the audio inputs are asynchronously switched or disrupted, the audio de-embedder continues to write audio samples into the audio buffer, based on the current five-frame sequence. The de-embedder then re-locks to the new 5-frame sequence, at which point a sample may be lost.

**Note:** In SD, all four channel pairs must follow the same five-frame sequence.

### 4.19.3.3 Audio FIFO Block

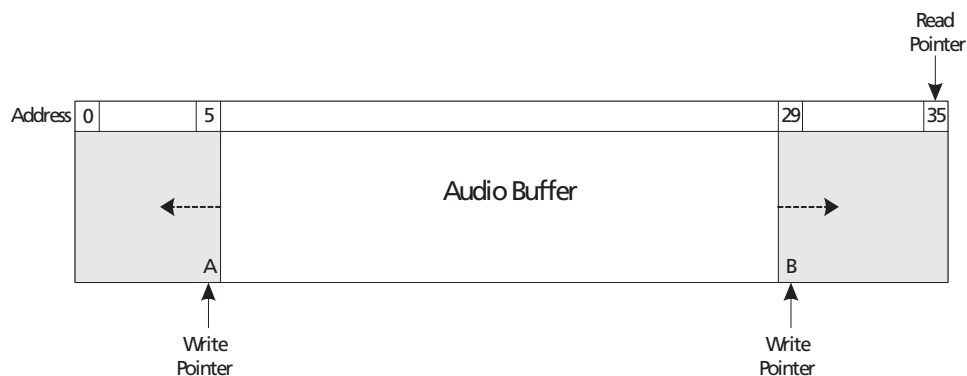
The function of the FIFO block is to change the audio data word rate from the ANC rate multiplexed with the video signal to the 48kHz audio output rate.

The audio FIFO block contains the audio sample buffers; one per audio channel. Each buffer is 36 audio samples deep. At power up or reset, the read pointer is held at the zero position until 26 samples have been written into the FIFO (allows for 6 lines per frame with no audio samples; a maximum of 4 samples per line in SD mode). See Figure 4-48.



**Figure 4-48: Audio Buffer After Initial 26 Sample Write**

The position of the write pointer with respect to the read pointer is monitored continuously. If the write pointer is less than 6 samples ahead of the read pointer (point A in Figure 4-49), a sample is repeated from the read-side of the FIFO. If the write pointer is less than 6 samples behind the read pointer (point B in Figure 4-49), a sample is dropped. This avoids buffer underflow/overflow conditions.



**Figure 4-49: Audio Buffer Pointer Boundary Checking**

The repeat or drop sample operation is performed a maximum of 28 consecutive times, after which the audio outputs are muted (all sample data set to zero). In SD mode, 26 samples are required to be written into the FIFO prior to starting the read operation again.

The audio buffer pointer offset may be reduced from 26 samples to 12 or 6 samples using the **OS\_SEL[1:0]** bits in the host interface. The default setting is 26 samples (see Table 4-20).

When the **OS\_SEL[1:0]** bits are set for 6-sample pointer offset, no boundary-checking is performed.

In HD mode the audio FIFO is a maximum of 10 samples deep. According to SMPTE ST 299, audio samples are multiplexed immediately in the next HANC region after the audio sample occurs.

**Table 4-20: Audio Buffer Pointer Offset Settings**

| OS_SEL[1:0]     | Buffer Pointer Offset | FIFO Size |
|-----------------|-----------------------|-----------|
| 00 <sub>b</sub> | 26 samples (default)  | 36        |
| 01 <sub>b</sub> | 12 samples            | 22        |
| 10 <sub>b</sub> | 6 samples             | 16        |

#### 4.19.3.4 Audio Crosspoint Block

The Audio Crosspoint is used for audio output channel re-mapping. This feature allows any of the selected audio channels in Group A or Group B to be output on any of the eight output channels. The default setting is for one to one mapping, where *AOUT\_1\_2* is extracted from Group A CH1 and CH2, *AOUT\_3\_4* is extracted from Group A CH3 and CH4, and so on.

**Note:** If audio samples from embedded audio packets with the group set in **IDA[1:0]** are to be paired with samples from the group set in **IDB[1:0]**, all of the channels must have been derived from the same Word Clock and must be synchronous.

The output channel is set in the **OP[8:1]\_SRC** parameter of the **OUTPUT\_SEL\_[2:1]** registers. [Table 4-21](#) lists the 3-bit address for audio channel mapping.

**Table 4-21: Audio Channel Mapping Codes**

| Audio Output Channel | 3-bit Host Interface Source Address |
|----------------------|-------------------------------------|
| 1                    | 000 <sub>b</sub>                    |
| 2                    | 001 <sub>b</sub>                    |
| 3                    | 010 <sub>b</sub>                    |
| 4                    | 011 <sub>b</sub>                    |
| 5                    | 100 <sub>b</sub>                    |
| 6                    | 101 <sub>b</sub>                    |
| 7                    | 110 <sub>b</sub>                    |
| 8                    | 111 <sub>b</sub>                    |

#### 4.19.3.5 Serial Audio Output Word Length

The audio output, in Serial mode, has a selectable 24, 20, or 16-bit sample word length. The **ASWL[D:A]** parameter is used to configure the audio output sample word length. [Table 4-22](#) shows the host interface 2-bit code for setting the audio sample word length. When the presence of extended audio packets is detected in SD mode, the audio de-embedder defaults to 24-bit audio sample word length.

**Table 4-22: Audio Sample Word Lengths**

| ASWL[D:A]       | Audio Sample Word Length (SD) | Audio Sample Word Length (HD) |
|-----------------|-------------------------------|-------------------------------|
| 00 <sub>b</sub> | 24-bit                        | 24-bit (default)              |
| 01 <sub>b</sub> | 20-bit                        | 20-bit                        |
| 10 <sub>b</sub> | 16-bit                        | 16-bit                        |
| 11 <sub>b</sub> | Auto 24/20-bit (default)      | Reserved                      |

#### 4.19.3.6 Audio Channel Status

The GS3470 detects the AES/EBU Audio Channel Status (ACS) block information for each of the selected channel pairs.

ACS data detection is indicated by corresponding **ACS\_DET** flag bits in the **DBN\_ERR** register. The flag is cleared by writing to the same location.

#### 4.19.3.7 Audio Channel Status Read

AES/EBU ACS data is available separately for each of the channels in a stereo pair. The GS3470 defaults to reading the first channel of each pair. There are 184 bits in each ACS packet, which are written to twelve 16-bit right-justified registers in the host interface.

The **ACS\_USE\_SECOND** bit (default LOW) selects the second channel in each audio pair when set HIGH.

Once all of the ACS data for a channel has been acquired, the corresponding **ACS\_DET** bit is asserted, and acquisition stops. The ACS data is overwritten with new data when the **ACS\_DET** bit is cleared in the system.

##### 4.19.3.7.1 Audio Channel Status Regeneration

When the **ACS\_REGEN** bit in the **REGEN** register is set HIGH, the audio de-embedder embeds the 24 bytes of the Audio Channel Status information programmed in the **ACSR[183:0]** registers into the 'C' bit of the AES/EBU outputs. The same Audio Channel Status information is used for all output channels.

In order to apply ACSR data:

1. Set the **ACS\_REGEN** bit to logic HIGH
2. Write the desired ACSR data to the **ACSR** registers
3. Set the **ACS\_APPLY** bit to HIGH

At the next status boundary, the device outputs the contents of the **ACSR** registers as ACS data. This event may occur at a different time for each of the output channels. While waiting for the status boundary, the device sets the appropriate **ACS\_APPLY\_WAIT[D:A]** flag.

Table 4-23 shows the host interface default settings for the Audio Channel Status block. The audio de-embedder automatically generates the CRC word.

**Table 4-23: Audio Channel Status Information Registers**

| Name                          | Description                                                                        | Default                                   |
|-------------------------------|------------------------------------------------------------------------------------|-------------------------------------------|
| ACSR[7:0]                     | Audio channel status block byte 0 set. Used when ACS_REGEN is set HIGH             | 85 <sub>h</sub>                           |
| ACSR[8:1]                     | Audio channel status block byte 1 set. Used when ACS_REGEN is set HIGH             | 08 <sub>h</sub>                           |
| ACSR[23:16]                   | Audio channel status block byte 2 set. Used when ACS_REGEN is set HIGH             | 28 <sub>h</sub> (SD) 2C <sub>h</sub> (HD) |
| ACSR[31:24],<br>ACSR[183:176] | Audio channel status block data for bytes 3 to 22. Used when ACS_REGEN is set HIGH | 00 <sub>h</sub>                           |
| ACS_REGEN                     | Audio channel status regenerate                                                    | 0                                         |
| ACS_APPLY                     | Apply new ACSR data                                                                | 0                                         |
| ACS_APPLY_W<br>AIT[D:A]       | Waiting to apply new ACSR data                                                     | 0                                         |
| ACS[7:0]:<br>ACS[183:176]     | Audio channel status block data for bytes 0 to 22                                  | 00 <sub>h</sub> : 00 <sub>h</sub>         |

**Table 4-24: Audio Channel Status Block for Regenerate Mode Default Settings**

| Name                       | Byte | Bit | Default           | Mode                                                                                  |
|----------------------------|------|-----|-------------------|---------------------------------------------------------------------------------------|
| PRO                        | 0    | 0   | 1 <sub>b</sub>    | Professional use of channel status block                                              |
| Emphasis                   | 0    | 4:2 | 100 <sub>b</sub>  | 100 <sub>b</sub> None. Rec. manual override disabled                                  |
| Sample Frequency           | 0    | 7:6 | 01 <sub>b</sub>   | 48kHz. Manual override or auto disabled                                               |
| Channel Mode               | 1    | 3:0 | 0001 <sub>b</sub> | Two channels. Manual override disabled                                                |
| AUX                        | 2    | 2:0 | 000 <sub>b</sub>  | SD Mode: Maximum audio word length is 20 bits                                         |
|                            |      |     | 001 <sub>b</sub>  | HD Mode: Maximum audio word length is 24 bits                                         |
| Source Word Length         | 2    | 5:3 | 101 <sub>b</sub>  | Maximum word length (based on AUX setting).<br>24-bit for HD Mode; 20-bit for SD Mode |
| All other bits set to zero |      |     |                   |                                                                                       |

#### 4.19.3.8 Audio Mute

When the **MUTE[B:A]** bits in the host interface are set HIGH, the audio outputs are muted (all audio sample bits are set to zero). To set all the audio output channels to mute, set the host interface **MUTE\_ALL** bit HIGH.

**Table 4-25: Audio Mute Control Bits**

| Name  | Description                                                                              | Default |
|-------|------------------------------------------------------------------------------------------|---------|
| MUTEB | Mute Secondary output channels 4 to 1; bits 3:0 = channel 4:1<br>0 = Normal<br>1 = Muted | 0       |
| MUTEA | Mute Primary output channels 4 to 1; bits 3:0 = channel 4:1<br>0 = Normal<br>1 = Muted   | 0       |

#### Mute On Loss Of Lock

When the GS3470 loses lock (LOCKED signal is LOW), the audio de-embedder sets all audio outputs LOW (no audio formatting is performed). The *ACLK*, *WCLK*, and *AMCLK* outputs are also forced LOW.

---

## 4.19.4 Error Reporting

### 4.19.4.1 Data Block Number Error

When the 1 to 255<sub>d</sub> count sequence in the Data Block Number (DBN) word of Group A audio data packets is discontinuous, the **DBNA\_ERR** bit in the host interface **ACS\_DET**(HD/3G) or **DBN\_ERR**(SD) register is set HIGH. When the 1 to 255 count sequence in the DBN word of Group B audio data packets is discontinuous, the **DBNB\_ERR** bit in the **ACS\_DET**(HD/3G) or **DBN\_ERR**(SD) register is set HIGH.

The **DBNA\_ERR** and **DBNB\_ERR** flags also have associated **INT\_ENABLE[2]** register flags for configuration of error reporting in the Receiver. The **DBNA\_ERR** and **DBNB\_ERR** flags remain set until cleared by writing to these locations.

### 4.19.4.2 ECC Error

The GS3470 monitors the ECC error status of the two selected audio groups, as described in [Section 4.19.2.6](#).

The **ECC[B:A]\_ERROR** flags also have associated **AUD\_DET2** register flags for configuration of error reporting in the Receiver. The **ECC[B:A]\_ERROR** flags remain set until written via the host interface.

**Note:** Low latency mode option is not available when ECC error is enabled.

## 4.20 GSPI - HOST Interface

The GS3470 is controlled via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (*SDIN* pin), serial data output signal (*SDOUT* pin), an active-low chip select ( $\overline{CS}$  pin) and a burst clock (*SCLK* pin).

The GS3470 is a slave device, so the *SCLK*, *SDIN* and  $\overline{CS}$  signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

Please refer to GS3470 Host Interface Register Map for a detailed description of the CSR registers available in the GS3470.

---

### 4.20.1 $\overline{CS}$ Pin

The Chip Select pin ( $\overline{CS}$ ) is an active-low signal provided by the host processor to the GS3470.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GS3470.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GS3470.

There is an option for each device to use a separate unique Chip Select signal from the host processor or for up to 32 devices to be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in the GSPI Command Word will respond to communication from the host processor (unless the B'CAST ALL bit in the GSPI Command Word is set to 1).

### 4.20.2 SDIN Pin

The SDIN pin is the GSPI serial data input pin of the GS3470.

The 16-bit Command and Data Words from the host processor or from the *SDOUT* pin of other devices are shifted into the device on the rising edge of *SCLK* when the  $\overline{CS}$  pin is low.

### 4.20.3 SDOUT Pin

The *SDOUT* pin is the GSPI serial data output of the GS3470.

All data transfers out of the GS3470 to the host processor or to the *SDIN* pin of other connected devices occur from this pin.

By default at power up or after system reset, the *SDOUT* pin provides a non-clocked path directly from the *SDIN* pin, regardless of the  $\overline{CS}$  pin state, except during the GSPI Data Word portion for read operations to the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the *SDOUT* pin is used to output data read from an internal Configuration and Status Register (CSR) when  $\overline{CS}$  is LOW. Data is shifted out of the device on the falling edge of *SCLK*, so that it can be read by the host processor or other downstream connected device on the subsequent *SCLK* rising edge.

### 4.20.3.1 GSPI Link Disable Operation

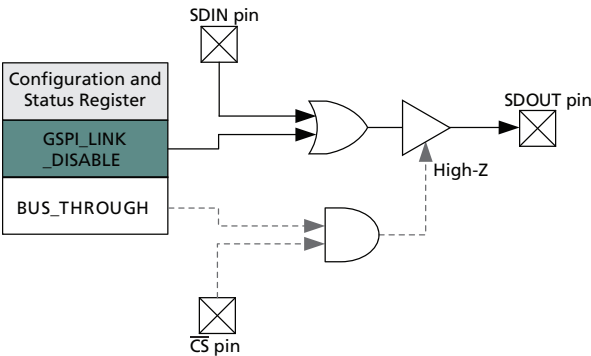
It is possible to disable the direct *SDIN* to *SDOUT* (Loop-Through) connection by writing a value of 1 to the **GSPI\_LINK\_DISABLE** bit in **REGISTER\_0**. When disabled, any data appearing at the *SDIN* pin will not appear at the *SDOUT* pin and the *SDOUT* pin is HIGH.

**Note:** Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter  $t_{cmd\_GSPI\_config}$  (4 SCLK cycles).

**Table 4-26: GSPI\_LINK\_DISABLE Bit Operation**

| Bit State | Description                                                             |
|-----------|-------------------------------------------------------------------------|
| 0         | SDIN pin is looped through to the SDOUT pin                             |
| 1         | Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH. |



**Figure 4-50: GSPI\_LINK\_DISABLE Operation**

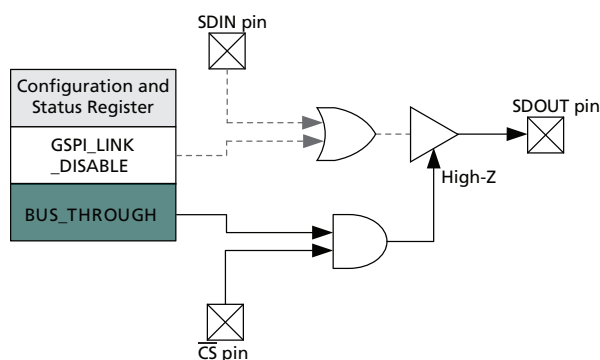
### 4.20.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS3470 can share a common PCB trace with other GSPI devices for *SDOUT* output.

When configured for Bus-Through operation, by setting **GSPI\_BUS\_THROUGH\_ENABLE** bit to 1, the *SDOUT* pin will be high-impedance when the  $\overline{CS}$  pin is HIGH.

When the  $\overline{CS}$  pin is LOW, the *SDOUT* pin will be driven and will follow regular read and write operation as described in [Section 4.20.3](#).

Multiple chains of GS3470 devices can share a single *SDOUT* bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ( $\overline{CS}$ ).



**Figure 4-51: GSPI\_BUS\_THROUGH\_ENABLE Operation**

## 4.20.4 SCLK Pin

The *SCLK* pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS3470 *SDIN* pin on the rising edge of *SCLK*. Serial data is clocked out of the device from the *SDOUT* pin on the falling edge of *SCLK* (read operation). *SCLK* is ignored when  $\overline{CS}$  is HIGH.

## 4.20.5 Command Word Description

All GSPI accesses are a minimum of 32 bits in length (a 16-bit Command Word followed by a 16-bit Data Word) and the start of each access is indicated by the high-to-low transition of the chip select ( $\overline{CS}$ ) pin of the GS3470.

The format of the Command Word and Data Words are shown in [Figure 4-52](#).

Data received immediately following this high-to-low transition will be interpreted as a new Command Word.

### 4.20.5.1 R/ $\overline{W}$ bit - B15 Command Word

This bit indicates a read or write operation.

When R/ $\overline{W}$  is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/ $\overline{W}$  is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

---

#### 4.20.5.2 B'CAST ALL - B14 Command Word

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B'CAST ALL is set to 1, the following Data Word (AUTOINC = 0) or Data Words (AUTOINC = 1) are written to the register specified by the ADDRESS field of the Command Word (and subsequent addresses when AUTOINC = 1), regardless of the setting of the UNIT ADDRESS(es).

When B'CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of the Command Word write the Data Word to the register specified by the ADDRESS field of the Command Word.

#### 4.20.5.3 EMEM - B13 Command Word

When the EMEM bit is 1 the Address Word is extended to 23 bits to allow access to registers located in the extended memory space.

When the EMEM bit is 0, the address word is limited to 7 bits.

#### 4.20.5.4 AUTOINC - B12 Command Word

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a low-to-high transition on the  $\overline{CS}$  pin is detected.

When AUTOINC is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in **HOST\_CONFIG**.

#### 4.20.5.5 UNIT ADDRESS - B11:B7 Command Word

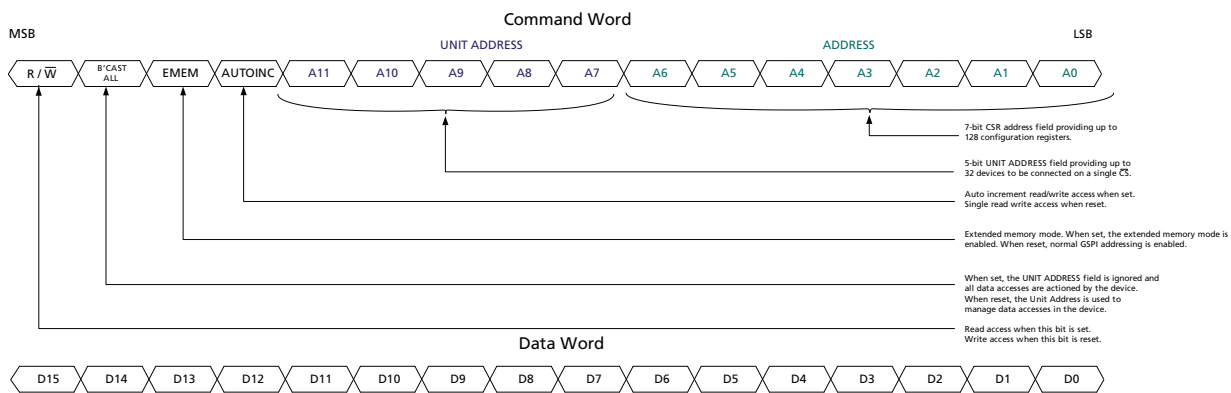
The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed **DEVICE\_UNIT\_ADDRESS** in **HOST\_CONFIG**.

By default at power-up or after a device reset, the **DEVICE\_UNIT\_ADDRESS** is set to 00<sub>h</sub>.

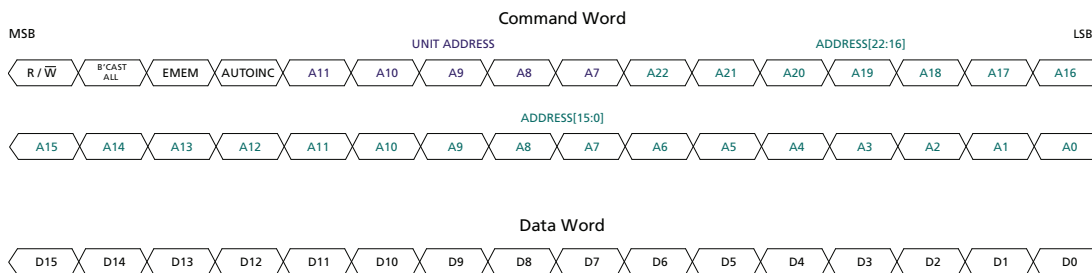
#### 4.20.5.6 ADDRESS - B6:B0 Command Word

If the extended memory is not being accessed (EMEM = 0), the 7 bits of the ADDRESS field are used to select one of 128 register addresses in the device in single read or write access mode, or to set the starting address for read or write accesses in Auto-Increment mode.



**Figure 4-52: Command and Data Word Format**

When EMEM is set to 1, the Address Word is extended to 23 bits. The Command and Data Word format will be extended by another 16 bits, and is shown in Figure 4-53 below.



**Figure 4-53: Command and Data Word Format with EMEM set to 1**

## 4.20.6 GSPI Transaction Timing

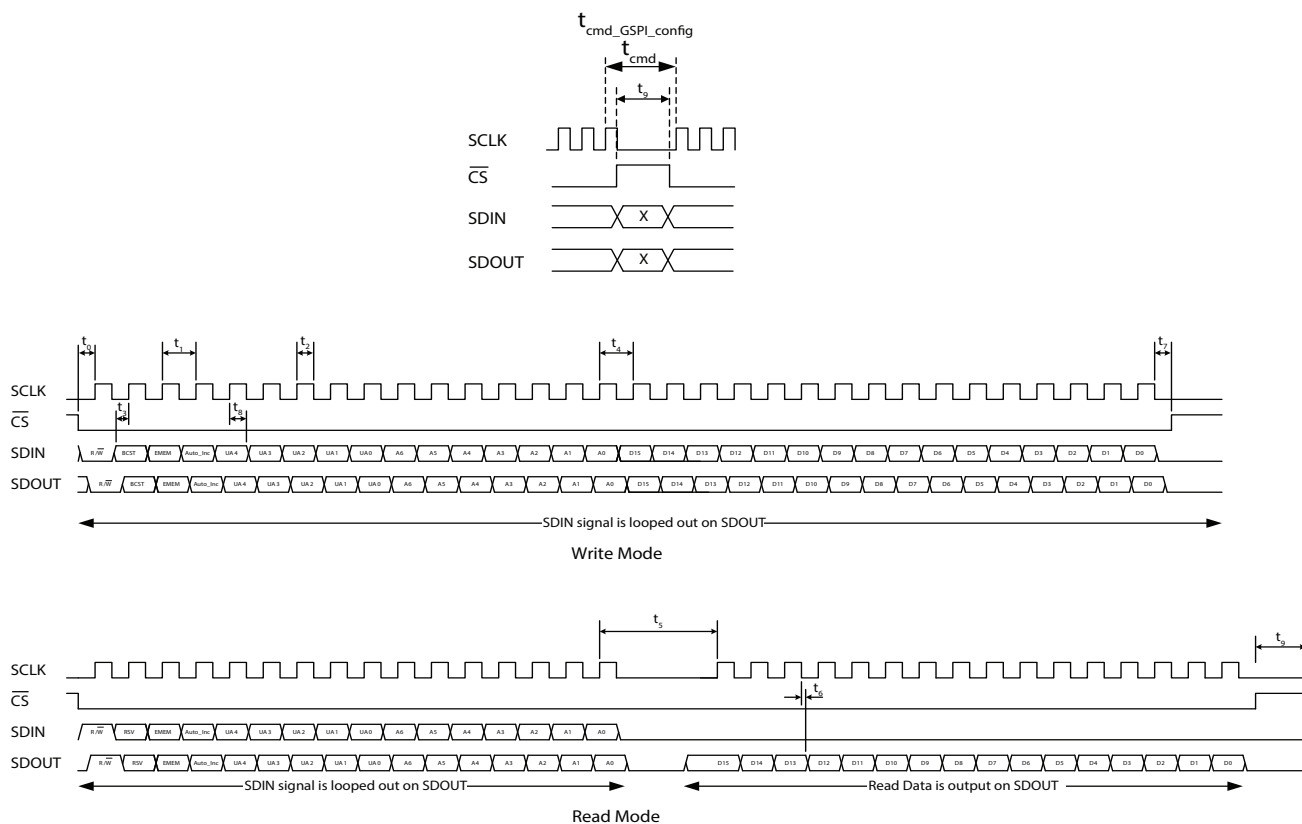


Figure 4-54: GSPI External Interface Timing

**Table 4-27: GSPI Timing Parameters**

| Parameter                                          | Symbol                                                 | Equivalent SCLK Cycles | Min | Typ | Max | Units         |
|----------------------------------------------------|--------------------------------------------------------|------------------------|-----|-----|-----|---------------|
| Time to GSPI ready after power up/reset            | $t_{\text{GSPI\_ready}}$                               |                        | —   | 500 | —   | $\mu\text{s}$ |
| $\overline{\text{CS}}$ low before SCLK rising edge | $t_0$                                                  |                        | 2.7 | —   | 22  | ns            |
| SCLK frequency                                     |                                                        |                        | —   | —   | 22  | MHz           |
| SCLK period                                        | $t_1$                                                  |                        | 45  | —   | —   | ns            |
| SCLK duty cycle                                    | $t_2$                                                  |                        | 40  | 50  | 60  | %             |
| Input data setup time                              | $t_3$                                                  |                        | 1.8 | —   | —   | ns            |
| SCLK idle time - write                             | $t_4$                                                  | 1                      | 45  | —   | —   | ns            |
| SCLK idle time - read                              | $t_5$                                                  | 4                      | 161 | —   | —   | ns            |
| Inter-command delay time                           | $t_{\text{cmd}}$                                       | 4                      | 161 | —   | —   | ns            |
| SDOUT after SCLK falling edge                      | $t_6$                                                  |                        | —   | —   | 9.1 | ns            |
| CS high after final SCLK falling edge              | $t_7$                                                  |                        | 0.0 | —   | —   | ns            |
| Input data hold time                               | $t_8$                                                  |                        | 1.1 | —   | —   | ns            |
| $\overline{\text{CS}}$ high time                   | $t_9$                                                  |                        | 45  | —   | —   | ns            |
| SDIN to SDOUT combinational delay                  |                                                        |                        | —   | —   | 7.4 | ns            |
| Max. chips daisy chained at max SCLK frequency     | When host clocks in SDOUT data on rising edge of SCLK  |                        | —   | —   | 1   | GS3470 chips  |
| Max. frequency for 32 daisy-chained devices        |                                                        |                        | —   | —   | 1.5 | MHz           |
| Max. chips daisy-chained at max. SCLK frequency    | When host clocks in SDOUT data on falling edge of SCLK |                        | —   | —   | 5   | GS3470 chips  |
| Max. frequency for 32 daisy-chained devices        |                                                        |                        | —   | —   | 3.5 | MHz           |

**Note:**

- $t_{\text{cmd\_GSPI\_conf}}$  inter-command delay must be used whenever modifying HOST\_CONFIG register at address 0x00

## 4.20.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-55 to Figure 4-59.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 32-bits long, consisting of a Command Word and a single Data Word. The read or write cycle begins with a high-to-low transition of the  $\overline{CS}$  pin. The read or write access is terminated by a low-to-high transition of the  $\overline{CS}$  pin.

The inter-command delay time indicated in the figures as  $t_{cmd}$ , is a minimum of 3 SCLK clock cycles. After modifying values in **HOST\_CONFIG**, the inter-command delay time,  $t_{cmd\_GSPI\_config}$ , is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of the Command Word to the start of the data output, as defined by  $t_s$ , corresponds to no less than 4 SCLK clock cycles.

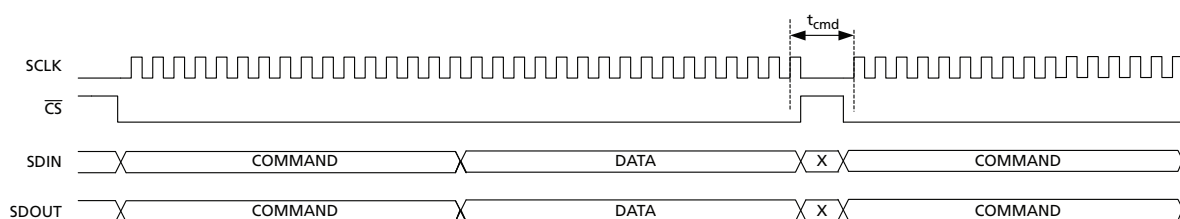


Figure 4-55: GSPI Write Timing – Single Write Access with Loop-Through Operation (default)

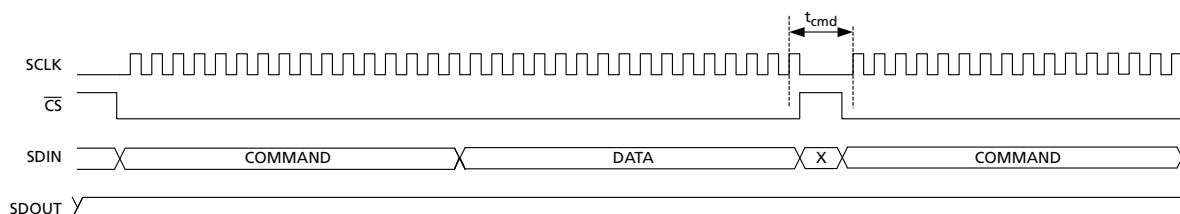


Figure 4-56: GSPI Write Timing – Single Write Access with GSPI Link-Disable Operation

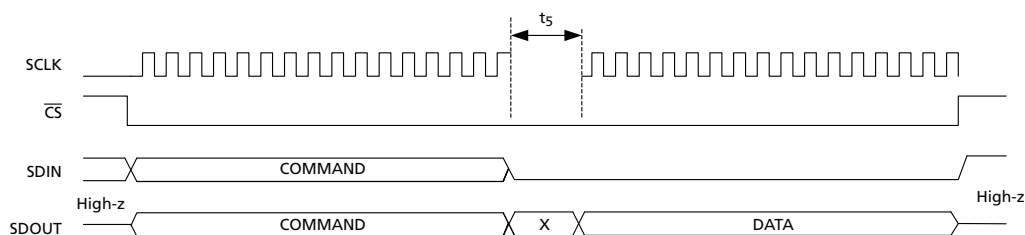
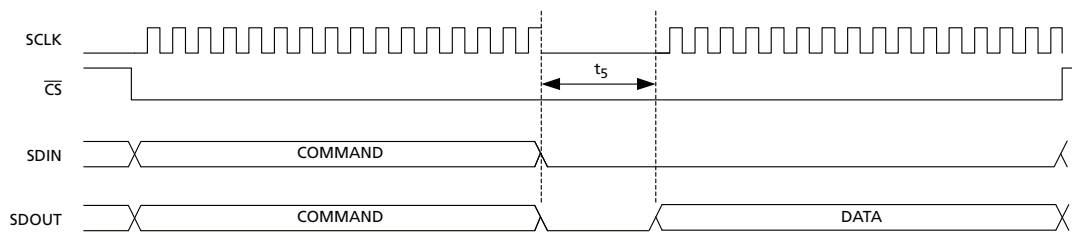
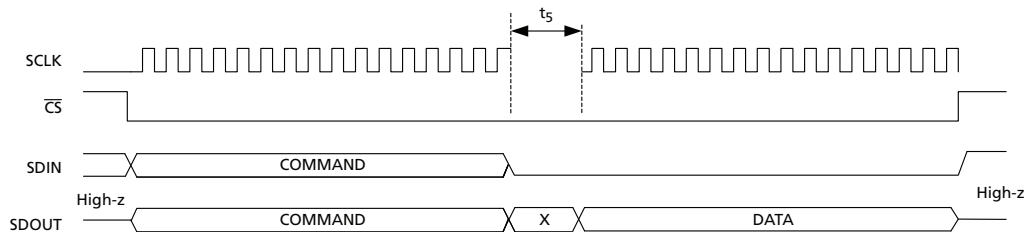


Figure 4-57: GSPI Write Timing – Single Write Access with Bus-Through Operation



**Figure 4-58: GSPI Read Timing – Single Read Access with Loop-Through Operation (default)**



**Figure 4-59: GSPI Read Timing – Single Read Access with Bus-Through Operation**

## 4.20.8 Auto-Increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in [Figure 4-60](#) to [Figure 4-64](#).

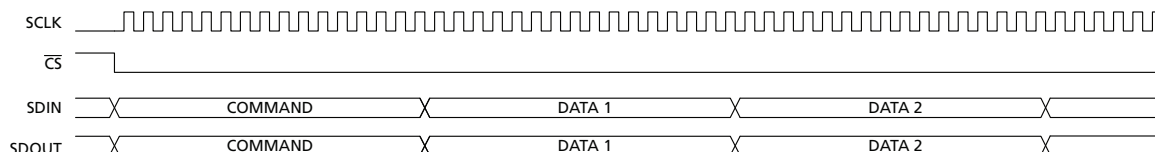
Auto-increment mode is enabled by the setting of the AUTOINC bit of the Command Word.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a high-to-low transition of the  $\overline{CS}$  pin, and consists of a Command Word and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a low-to-high transition of the  $\overline{CS}$  pin.

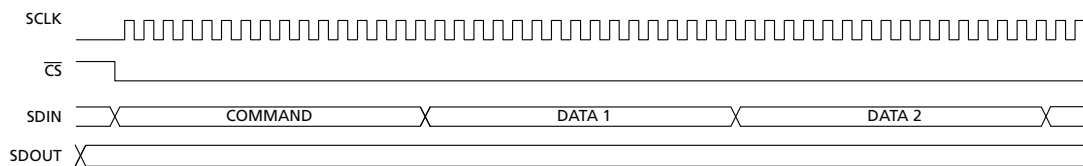
**Note:** Writing to **HOST\_CONFIG** using Auto-increment access is not allowed.

The inter-command delay time indicated in the diagram as  $t_{cmd}$ , is a minimum of 3 SCLK clock cycles.

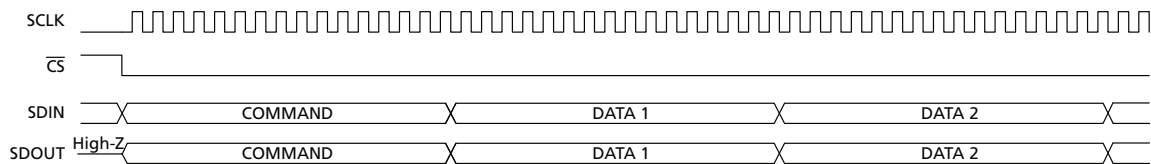
For read access, the time from the last bit of the first Command Word to the start of the data output of the first Data Word as defined by  $t_5$ , will be no less than 4 SCLK cycles. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.



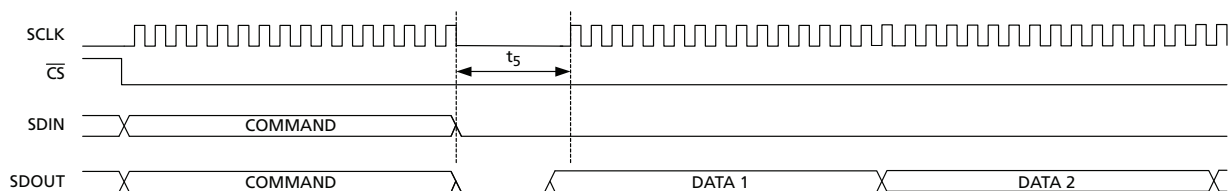
**Figure 4-60: GSPI Write Timing – Auto-Increment with Loop-Through Operation (default)**



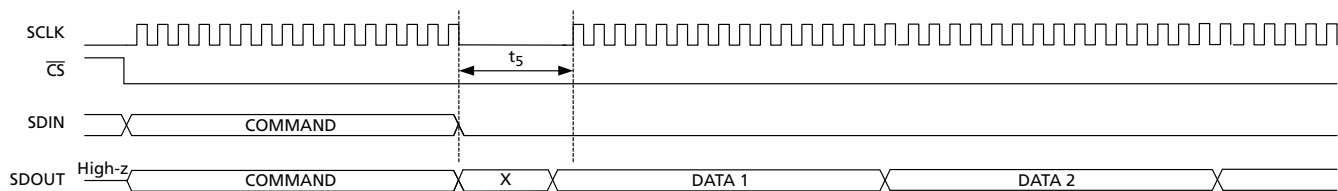
**Figure 4-61: GSPI Write Timing – Auto-Increment with GSPI Link Disable Operation**



**Figure 4-62: GSPI Write Timing – Auto-Increment with Bus-Through Operation**



**Figure 4-63: GSPI Read Timing – Auto-Increment Read with Loop-Through Operation (default)**



**Figure 4-64: GSPI Read Timing – Auto-Increment Read with Bus-through Operation**

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## 4.20.9 Setting a Device Unit Address

Multiple (up to 32) GS3470 devices can be connected to a common Chip Select ( $\overline{CS}$ ) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common  $\overline{CS}$  can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

**Note:** By default at power up or after a device reset, the **DEVICE\_UNIT\_ADDRESS** of each device is set to 0<sub>H</sub> and the *SDIN*->*SDOUT* non-clocked loop-through for each device is enabled.

These are the steps required to set the **DEVICE\_UNIT\_ADDRESS** of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting **HOST\_CONFIG** (ADDRESS = 0), with the **GSPI\_LINK\_DISABLE** bit set to 1 and the **DEVICE\_UNIT\_ADDRESS** field set to 0. This disables the direct *SDIN*->*SDOUT* non-clocked path for all devices on chip select.
2. Write to Unit Address 0 selecting **HOST\_CONFIG** (ADDRESS = 0), with the **GSPI\_LINK\_DISABLE** bit set to 0 and the **DEVICE\_UNIT\_ADDRESS** field set to a unique Unit Address. This configures **DEVICE\_UNIT\_ADDRESS** for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use **DEVICE\_UNIT\_ADDRESS** value 0.
3. Repeat step 2 using new, unique values for the **DEVICE\_UNIT\_ADDRESS** field in **HOST\_CONFIG** until all devices in the chain have been configured with their own unique Unit Address value.

**Note:**  $t_{cmd\_GSPI\_conf}$  delay must be observed after every write that modifies **HOST\_CONFIG**.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

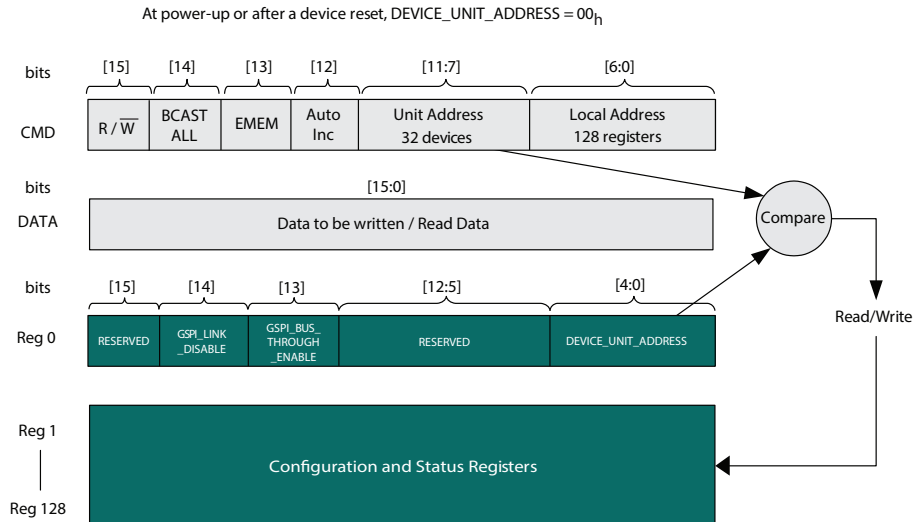
Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the **DEVICE\_UNIT\_ADDRESS** in **HOST\_CONFIG**

**Note:** Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's *SDOUT* connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final *SDOUT* outputs connected to a single application host processor input.

## 4.20.10 Default GSPI Operation

By default at power up or after a device reset, the GS3470 is set for Loop-Through Operation and the internal **DEVICE\_UNIT\_ADDRESS** field of the device is set to 0.

Figure 4-65 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS3470 for non-extended memory accesses (EMEM = 0).



**Figure 4-65: Internal Register Map Functional Block Diagram**

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word for write access ( $\text{R}/\overline{\text{W}} = 0$ ) to the local registers  $0_{\text{h}}$  to  $80_{\text{h}}$ ; set Auto Increment; set the Unit Address field in the Command Word to match the configured **DEVICE\_UNIT\_ADDRESS** which will be zero. Write the Command Word.
2. Write the Data Word to be written to the first register.
3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above with the exception of step 1, where the Command Word is set for read access ( $\text{R}/\overline{\text{W}} = 1$ ).

**Note:** The UNIT ADDRESS field of the Command Word must always match **DEVICE\_UNIT\_ADDRESS** for an access to be accepted by the device. Changing **DEVICE\_UNIT\_ADDRESS** to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration.)

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## 4.21 JTAG Test Operation

When the  $JTAG\_EN/\overline{DIS}$  pin of the GS3470 is set HIGH, test mode is enabled.

The JTAG can be used as a stand-alone in-circuit ATE (Automatic Test Equipment) during PCB assembly.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the  $JTAG\_EN/\overline{DIS}$  input signal. This is shown in [Figure](#) .

Scan coverage is limited to digital pins only. There is no scan coverage for analog pins  $DDO/\overline{DDO}$ ,  $RBIAS$ ,  $LF$ ,  $CT0$ , and  $CT1$ .

The  $JTAG\_EN/\overline{DIS}$  pin must be held LOW during scan and therefore has no scan coverage.

Please contact your Semtech representative to obtain the BSDL model for the GS3470.

## 5. Register Map

### 5.1 Control Registers

**Table 5-1: Host Configuration Register**

| Function                    | GSPI Address <sub>h</sub> | Register Name   |
|-----------------------------|---------------------------|-----------------|
| Host Configuration Register | 0                         | HOST_CONF_REG_0 |

**Table 5-2: Video Core Registers**

| Function                 | GSPI Address <sub>h</sub> | Register Name                    |
|--------------------------|---------------------------|----------------------------------|
| IO Processing            | 800                       | IOPROC_1                         |
|                          | 801                       | IOPROC_2                         |
| Flywheel Switch Line     | 802 to 803                | FWSL_LINE1_FE1 to FWSL_LINE2_FE1 |
|                          | 804 to 805                | FWSL_LINE1_FE2 to FWSL_LINE2_FE2 |
| Sticky Error Status      | 806                       | ERROR_STAT_1_STICKY              |
|                          | 808                       | ERROR_STAT_2_STICKY              |
| Error Status             | 807                       | ERROR_STAT_1                     |
|                          | 809                       | ERROR_STAT_2                     |
| Error Detected Flag      | 80A                       | EDH_FLAG_IN                      |
|                          | 80B                       | EDH_FLAG_OUT                     |
| Data Format              | 80C                       | DATA_FORMAT_DS1                  |
|                          | 80E                       | DATA_FORMAT_DS2                  |
| Video Standard Detection | 80D                       | VID_STD_DS1                      |
|                          | 80F                       | VID_STD_DS2                      |
| Power Down               | 811                       | POWER_DOWN                       |
| IO Configuration         | 812                       | IO_CONFIG                        |
|                          | 813                       | IO_CONFIG_2                      |

**Table 5-2: Video Core Registers (Continued)**

| Function                        | GSPI Address <sub>h</sub> | Register Name                                   |
|---------------------------------|---------------------------|-------------------------------------------------|
| ANC Control                     | 817                       | ANC_CONTROL                                     |
| ANC Extraction Line             | 818                       | ANC_LINEA                                       |
|                                 | 819                       | ANC_LINEB                                       |
| ANC Type                        | 81E to 822                | ANC_TYPE_1_DS1 to<br>ANC_TYPE_5_DS1             |
|                                 | 823 to 827                | ANC_TYPE_1_DS2 to<br>ANC_TYPE_5_DS2             |
| Video Format                    | 828 to 82B                | VIDEO_FORMAT_352_A_1 to<br>VIDEO_FORMAT_352_D_1 |
|                                 | 82C to 82F                | VIDEO_FORMAT_352_A_2 to<br>VIDEO_FORMAT_352_D_2 |
| Raster Information              | 830 to 833                | RASTER_STRUC_1_DS1 to<br>RASTER_STRUC_4_DS1     |
| Flywheel Status                 | 834                       | FLYWHEEL_STATUS                                 |
| Rate Selection                  | 835                       | RATE_SEL                                        |
| CEA-861-D Format                | 836                       | TIM_861_FORMAT                                  |
| CEA-861-D Configuration         | 837                       | TIM_861_CFG                                     |
| Error Mask                      | 848 to 84A                | ERROR_MASK_1 to<br>ERROR_MASK_3                 |
| Audio Clock Control             | 84B                       | ACG_CTRL                                        |
| Input Configuration             | 84D                       | INPUT_CONFIG                                    |
| PLL Control                     | 868                       | PLL_CTRL_0                                      |
|                                 | 869                       | PLD_CTRL_0                                      |
|                                 | 86A                       | PLD_CTRL_1                                      |
|                                 | 86B                       | PLL_STAT                                        |
| PLL Status Sticky               | 86C                       | PLL_STICKY_STAT                                 |
| Offset Correction Configuration | 86D                       | OFFSET_CORRECTION_CFG                           |
| LOS Control                     | 86F                       | LOS_CTRL                                        |
| Delay Line Control              | 870                       | DELAY_LINE_CTRL_1                               |
| Delay Line Control              | 871                       | DELAY_LINE_CTRL_2                               |

**Table 5-2: Video Core Registers (Continued)**

| Function                 | GSPI Address <sub>h</sub> | Register Name                               |
|--------------------------|---------------------------|---------------------------------------------|
| Clock Generation         | 874                       | CLK_GEN                                     |
| Phase Detection Control  | 875                       | PD_CTRL                                     |
| PIN/CSR Selector         | 877                       | PIN_CSR_SELECT                              |
| IO Drive Strength        | 878                       | IO_DRIVE_STRENGTH                           |
| Output Buffer Control    | 87B                       | OUTPUT_BUFFER_CTRL_1                        |
|                          | 87C                       | OUTPUT_BUFFER_CTRL_2                        |
| 16 Line Horizontal Count | 87D                       | H_16LINE_COUNT_DS1                          |
|                          | 87F                       | H_16LINE_COUNT_DS2                          |
| M Detection Tolerance    | 87E                       | M_DETECTION_TOLERANCE_DS1                   |
|                          | 880                       | M_DETECTION_TOLERANCE_DS2                   |
| Analog Path Control      | 882                       | XPOINT_PD                                   |
| Analog Mute Control      | 883                       | DDO_MUTE_CTRL                               |
| Analog Test Control      | 884                       | DDO_CTRL                                    |
| General Status           | 8CB                       | GENERAL_STATUS                              |
| Raster Information       | 8CF to 8D2                | RASTER_STRUC_1_DS2 to<br>RASTER_STRUC_4_DS2 |
| General Control          | 8D3                       | GENERAL_CONTROL                             |
| Power Down Path Select   | 989                       | PD_IB_HS_PATH_SEL                           |

**Table 5-3: HD and 3G Audio Core Registers**

| Function                       | GSPI Address <sub>h</sub> | Register Name |
|--------------------------------|---------------------------|---------------|
| Audio Configuration            | A01                       | CFG_AUD       |
|                                | A02                       | CFG_AUD1      |
| Audio Channel Status Detection | A03                       | ACS_DET       |
| Audio Detection                | A04                       | AUD_DET1      |
|                                | A05                       | AUD_DET2      |

**Table 5-3: HD and 3G Audio Core Registers (Continued)**

| Function                            | GSPI Address <sub>h</sub> | Register Name                          |
|-------------------------------------|---------------------------|----------------------------------------|
| Audio Channel Status Regeneration   | A06                       | REGEN                                  |
| Channel Mute                        | A07                       | CH_MUTE                                |
| Channel Validity                    | A08                       | CH_VALID                               |
| Interrupt Enable                    | A09                       | INT_ENABLE                             |
|                                     | A0A                       | INT_ENABLE2                            |
| Audio Configuration                 | A0B                       | CFG_AUD_2                              |
|                                     | A0C                       | CFG_AUD_3                              |
| Output Channel Selection            | A0D                       | OUTPUT_SEL_1                           |
|                                     | A0E                       | OUTPUT_SEL_2                           |
| Primary Audio Frame Number          | A20                       | AFNA                                   |
| Primary Audio Sampling Frequency    | A21                       | RATEA                                  |
| Primary Active Channels Indicator   | A22                       | ACTA                                   |
| Primary Audio Group Delay           | A23 to A28                | PRIM_AUD_DELAY_1 to PRIM_AUD_DELAY_6   |
| Secondary Audio Frame Number        | A30                       | AFNB                                   |
| Secondary Audio Sampling Frequency  | A31                       | RATEB                                  |
| Secondary Active Channels Indicator | A32                       | ACTB                                   |
| Secondary Audio Group Delay         | A33 to A38                | SEC_AUD_DELAY_1 to SEC_AUD_DELAY_6     |
| Audio Group A Channel Status        | A40 to A4A                | ACSR1_2A_BYTE0_1 to ACSR1_2A_BYTE20_21 |
|                                     | A4B                       | ACSR1_2A_BYTE22                        |
|                                     | A50 to A5A                | ACSR3_4A_BYTE0_1 to ACSR3_4A_BYTE20_21 |
|                                     | A5B                       | ACSR3_4A_BYTE22                        |

**Table 5-3: HD and 3G Audio Core Registers (Continued)**

| Function                                | GSPI Address <sub>h</sub> | Register Name                          |
|-----------------------------------------|---------------------------|----------------------------------------|
| Audio Group B Channel Status            | A60 to A6A                | ACSR1_2B_BYTE0_1 to ACSR1_2B_BYTE20_21 |
|                                         | A6B                       | ACSR1_2B_BYTE22                        |
|                                         | A70 to A7A                | ACSR3_4B_BYTE0_1 to ACSR3_4B_BYTE20_21 |
|                                         | A7B                       | ACSR3_4B_BYTE22                        |
| Audio Channel Status Regeneration Bytes | A80 to A96                | ACSR_BYTE_0 to ACSR_BYTE_22            |

**Table 5-4: SD Audio Core Registers**

| Function                          | GSPI Address <sub>h</sub> | Register Name |
|-----------------------------------|---------------------------|---------------|
| Audio Configuration               | B01                       | CFG_AUD       |
| Data Block Number Error           | B03                       | DBN_ERR       |
| Audio Channel Status Regeneration | B04                       | REGEN         |
| Audio Detection                   | B05                       | AUD_DET       |
| Checksum Error Detection          | B06                       | CSUM_ERR_DET  |
| Channel Mute                      | B07                       | CH_MUTE       |
| Channel Validity                  | B08                       | CH_VALID      |
| Interrupt Enable                  | B09                       | INT_ENABLE    |
| Output Configuration              | B0A                       | CFG_OUTPUT    |
| Output Channel Selection          | B0B                       | OUTPUT_SEL_1  |
|                                   | B0C                       | OUTPUT_SEL_2  |
| Primary Audio Frame Number        | B20                       | AFNA12        |
|                                   | B21                       | AFNA34        |
| Primary Audio Sampling Frequency  | B22                       | RATEA         |
| Primary Active Channels Indicator | B23                       | ACT_A         |

**Table 5-4: SD Audio Core Registers**

| Function                                | GSPI Address <sub>h</sub> | Register Name                          |
|-----------------------------------------|---------------------------|----------------------------------------|
| Primary Audio Group Delay               | B24 to B2F                | PRIM_AUD_DELAY_1 to PRIM_AUD_DELAY_12  |
| Secondary Audio Frame Number            | B30                       | AFNB12                                 |
|                                         | B31                       | AFNB34                                 |
| Secondary Audio Sampling Frequency      | B32                       | RATEB                                  |
| Secondary Active Channels Indicator     | B33                       | ACT_B                                  |
| Secondary Audio Group Delay             | B34 to B3F                | SEC_AUD_DELAY_1 to SEC_AUD_DELAY_12    |
| Audio Group A Channel Status            | B40 to B4A                | ACSR1_2A_BYTE0_1 to ACSR1_2A_BYTE20_21 |
|                                         | B4B                       | ACSR1_2A_BYTE22                        |
|                                         | B50 to B5A                | ACSR3_4A_BYTE0_1 to ACSR3_4A_BYTE20_21 |
|                                         | B5B                       | ACSR3_4A_BYTE22                        |
| Audio Group B Channel Status            | B60 to B6A                | ACSR1_2B_BYTE0_1 to ACSR1_2B_BYTE20_21 |
|                                         | B6B                       | ACSR1_2B_BYTE22                        |
|                                         | B70 to B7A                | ACSR3_4B_BYTE0_1 to ACSR3_4B_BYTE20_21 |
|                                         | B7B                       | ACSR3_4B_BYTE22                        |
| Audio Channel Status Regeneration Bytes | B80 to B96                | ACSR_BYTE_0 to ACSR_BYTE_22            |

**Table 5-5: ANC Extraction FIFO Access Registers**

| Function | GSPI Address <sub>h</sub> | Register Name               |
|----------|---------------------------|-----------------------------|
| ANC FIFO | C00 to FFF                | ANC_FIFO_0 to ANC_FIFO_1023 |

**Table 5-6: Glossary of Terms**

| Term              | Description               |
|-------------------|---------------------------|
| RW                | Read-write                |
| RO                | Read-only                 |
| WO                | Write-only                |
| ROCW <sup>1</sup> | Read-only, clear on write |
| ROCR              | Read-only, clear on read  |
| RSVD <sup>2</sup> | Read, modify, write       |

**Note:**

1) For each bit in the register that needs to be cleared, write 1.  
If all bits in the register need to be cleared, write FFFF<sub>h</sub>.

2) To modify a bit in a register that has other bits marked RSVD, read the existing value, modify only the non-reserved bits and then write the final value. For example, to change bit 9 in register 989<sub>h</sub>, a read would produce 0000<sub>h</sub>, modify to 0200<sub>h</sub> and write 0200<sub>h</sub>.

**Table 5-7: Host Configuration Register Descriptions**

| Address <sub>h</sub> | Register Name   | Parameter Name          | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                               |
|----------------------|-----------------|-------------------------|-----------|-----|--------------------------|-------------------------------------------|
| 0                    | HOST_CONF_REG_0 | RSVD                    | 15:15     | —   | —                        | Reserved.                                 |
|                      |                 | GSPI_LINK_DISABLE       | 14:14     | RW  | 0                        | GSPI loop-through disable.                |
|                      |                 | GSPI_BUS_THROUGH_ENABLE | 13:13     | RW  | 0                        | GSPI bus-through enable.                  |
|                      |                 | RSVD                    | 12:5      | —   | —                        | Reserved.                                 |
|                      |                 | DEVICE_UNIT_ADDRESS     | 4:0       | RW  | 0                        | Device address programmed by application. |

**Table 5-8: Video Core CSR Descriptions**

| Address <sub>h</sub> | Register Name | Parameter Name                  | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                                                                                           |
|----------------------|---------------|---------------------------------|-----------|-----|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 800                  | IOPROC_1      | RSVD                            | 15:15     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                             |
|                      |               | LOW_LATENCY_BYPASS              | 14:14     | RW  | 0                        | 0 = Takes the low latency bypass path through the audio and ancillary data extraction when possible (when not deleting or updating the packets).<br>1 = Takes the higher latency path through the audio and ANC extraction regardless of what specific features are enabled/disabled. |
|                      |               | FW_SWITCH_LINE_OVERRIDE_FE1     | 13:13     | RW  | 0                        | When HIGH, flywheel uses FW_SWITCH_LINE values instead of the indicated values in standards.                                                                                                                                                                                          |
|                      |               | TRS_WORD_REMAP_FE1_DISABLE_MASK | 12:12     | RW  | 0                        | When HIGH, disables TRS word remap.                                                                                                                                                                                                                                                   |
|                      |               | EDH_FLAG_UPDATE_MASK            | 11:11     | RW  | 0                        | When HIGH, disables update for EDH error flags.                                                                                                                                                                                                                                       |
|                      |               | EDH_CRC_INS_MASK                | 10:10     | RW  | 0                        | When HIGH, disables EDH CRC error correction and insertion.                                                                                                                                                                                                                           |
|                      |               | H_CONFIG                        | 9:9       | RW  | 0                        | Selects the H blanking indication:<br>0 = Active picture timing<br>1 = SMPTE H timing                                                                                                                                                                                                 |
|                      |               | ANC_DATA_EXT_MASK               | 8:8       | RW  | 0                        | When HIGH, disables ancillary data extraction FIFO.                                                                                                                                                                                                                                   |
|                      |               | AUD_EXT_MASK                    | 7:7       | RW  | 0                        | When HIGH, disables audio extraction.                                                                                                                                                                                                                                                 |
|                      |               | TIMING_861                      | 6:6       | RW  | 0                        | 0 = Selects digital FVH timing output<br>1 = Selects 861 timing output                                                                                                                                                                                                                |
|                      |               | RSVD                            | 5:5       | RW  | 0                        | Reserved.                                                                                                                                                                                                                                                                             |
|                      |               | ILLEGAL_WORD_REMAP_DS1_MASK     | 4:4       | RW  | 0                        | When HIGH, disables illegal word remapping.                                                                                                                                                                                                                                           |
|                      |               | ANC_CHECKSUM_INSERTION_DS1_MASK | 3:3       | RW  | 0                        | When HIGH, disables insertion of ancillary data checksums.                                                                                                                                                                                                                            |
|                      |               | CRC_INS_DS1_MASK                | 2:2       | RW  | 0                        | When HIGH, disables insertion of HD/3G CRC words.                                                                                                                                                                                                                                     |
|                      |               | LNUM_INS_DS1_MASK               | 1:1       | RW  | 0                        | When HIGH, disables insertion of HD/3G line numbers.                                                                                                                                                                                                                                  |
|                      |               | TRS_INS_DS1_MASK                | 0:0       | RW  | 0                        | When HIGH, disables insertion of TRS words.                                                                                                                                                                                                                                           |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name                  | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                    |
|----------------------|---------------|---------------------------------|-----------|-----|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 801                  | IOPROC_2      | RSVD                            | 15:15     | —   | —                        | Reserved.                                                                                                                                                                                      |
|                      |               | NONINV                          | 14:14     | RW  | 1                        | 0 = Forces inverted MPEG-2 decoding<br>1 = Forces non-inverted MPEG-2 decoding                                                                                                                 |
|                      |               | RSVD                            | 13:13     | RW  | 1                        | Reserved.                                                                                                                                                                                      |
|                      |               | FW_SWITCH_LINE_OVERRIDE_FE2     | 12:12     | RW  | 0                        | When HIGH, flywheel uses FW_SWITCH_LINE values instead of the indicated values in standards.                                                                                                   |
|                      |               | TRS_WORD_REMAP_FE2_DISABLE_MASK | 11:11     | RW  | 0                        | When HIGH, disables TRS word remapping.                                                                                                                                                        |
|                      |               | REGEN_352_MASK                  | 10:10     | RW  | 0                        | When HIGH, disables regeneration of the SMPTE 352 packet for 3G Level B data.<br><b>Note:</b> This bit needs to be enabled via the host interface to disable SMPTE ST 352 packet regeneration. |
|                      |               | DS_SWAP_3G                      | 9:9       | RW  | 0                        | Swaps DS1 and DS2 at the output in 3G mode.                                                                                                                                                    |
|                      |               | ANC_EXT_SEL_DS1_Y_DS2_Y         | 8:8       | RW  | 1                        | In 3G Level B mode,<br>0 = Selects Luma and Chroma inputs from DS1 or DS2 based on ANC_EXT_SEL_DS2_DS1B<br>1 = Selects Luma inputs from both DS1 and DS2                                       |
|                      |               | ANC_EXT_SEL_DS2_DS1             | 7:7       | RW  | 0                        | Selects data stream to extract ANC data from.                                                                                                                                                  |
|                      |               | AUDIO_SEL_DS2_DS1               | 6:6       | RW  | 0                        | Selects data stream to be sent to audio core.                                                                                                                                                  |
|                      |               | RSVD                            | 5:5       | RW  | 0                        | Reserved.                                                                                                                                                                                      |
|                      |               | ILLEGAL_WORD_REMAP_DS2_MASK     | 4:4       | RW  | 0                        | When HIGH, disables illegal word remapping.                                                                                                                                                    |
|                      |               | ANC_CHECKSUM_INSERTION_DS2_MASK | 3:3       | RW  | 0                        | When HIGH, disables insertion of ancillary data checksums.                                                                                                                                     |
|                      |               | CRC_INS_DS2_MASK                | 2:2       | RW  | 0                        | When HIGH, disables insertion of HD/3G CRC words.                                                                                                                                              |
|                      |               | LNUM_INS_DS2_MASK               | 1:1       | RW  | 0                        | When HIGH, disables insertion of HD/3G line numbers.                                                                                                                                           |
|                      |               | TRS_INS_DS2_MASK                | 0:0       | RW  | 0                        | When HIGH, disables insertion of TRS words.                                                                                                                                                    |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name       | Parameter Name        | Bit Slice | R/W  | Reset Value <sub>h</sub> | Description                                                                                            |
|----------------------|---------------------|-----------------------|-----------|------|--------------------------|--------------------------------------------------------------------------------------------------------|
| 802                  | FWSL_LINE1_FE1      | RSVD                  | 15:11     | —    | —                        | Reserved.                                                                                              |
|                      |                     | FWSL_LINE1_FE1        | 10:0      | RW   | 0                        | Value of flywheel line number to override for switch line 1 when FW_SWITCH_LINE_OVERRIDE_FE1 asserted. |
| 803                  | FWSL_LINE2_FE1      | RSVD                  | 15:11     | —    | —                        | Reserved.                                                                                              |
|                      |                     | FWSL_LINE2_FE1        | 10:0      | RW   | 0                        | Value of flywheel line number to override for switch line 2 when FW_SWITCH_LINE_OVERRIDE_FE1 asserted. |
| 804                  | FWSL_LINE1_FE2      | RSVD                  | 15:11     | —    | —                        | Reserved.                                                                                              |
|                      |                     | FWSL_SWITCH_LINE1_FE2 | 10:0      | RW   | 0                        | Value of flywheel line number to override for switch line 1 when FW_SWITCH_LINE_OVERRIDE_FE2 asserted. |
| 805                  | FWSL_LINE2_FE2      | RSVD                  | 15:11     | —    | —                        | Reserved.                                                                                              |
|                      |                     | FWSL_SWITCH_LINE2_FE2 | 10:0      | RW   | 0                        | Value of flywheel line number to override for switch line 2 when FW_SWITCH_LINE_OVERRIDE_FE2 asserted. |
| 806                  | ERROR_STAT_1_STICKY | RSVD                  | 15:10     | —    | —                        | Reserved.                                                                                              |
|                      |                     | FF_CRC_ERR_STICKY     | 9:9       | ROCR | 0                        | EDH full frame CRC error indication.                                                                   |
|                      |                     | AP_CRC_ERR_STICKY     | 8:8       | ROCR | 0                        | EDH active picture CRC error indication – sticky, clear on read.                                       |
|                      |                     | LOCK_ERR_STICKY       | 7:7       | ROCR | 0                        | Lock error indication – sticky, clear on read.                                                         |
|                      |                     | CCS_ERR_1_STICKY      | 6:6       | ROCR | 0                        | Chroma/DS2 ancillary data checksum error indication – sticky, clear on read.                           |
|                      |                     | YCS_ERR_1_STICKY      | 5:5       | ROCR | 0                        | Luma/DS1 ancillary data checksum error indication - sticky, clear on read.                             |
|                      |                     | CCRC_ERR_1_STICKY     | 4:4       | ROCR | 0                        | Chroma/DS2 CRC error indication (HD/3G only) – sticky, clear on read.                                  |
|                      |                     | YCRC_ERR_1_STICKY     | 3:3       | ROCR | 0                        | Luma/DS1 CRC error indication (HD/3G only) – sticky, clear on read.                                    |
|                      |                     | LNUM_ERR_1_STICKY     | 2:2       | ROCR | 0                        | Line number error indication (HD/3G only) – sticky, clear on read.                                     |
|                      |                     | SAV_ERR_1_STICKY      | 1:1       | ROCR | 0                        | SAV error indication – sticky, clear on read.                                                          |
|                      |                     | EAV_ERR_1_STICKY      | 0:0       | ROCR | 0                        | EAV error indication – sticky, clear on read.                                                          |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name       | Parameter Name    | Bit Slice | R/W  | Reset Value <sub>h</sub> | Description                                                                                                          |
|----------------------|---------------------|-------------------|-----------|------|--------------------------|----------------------------------------------------------------------------------------------------------------------|
| 807                  | ERROR_STAT_1        | RSVD              | 15:10     | —    | —                        | Reserved.                                                                                                            |
|                      |                     | FF_CRC_ERR        | 9:9       | ROCW | 0                        | EDH full frame CRC error indication.                                                                                 |
|                      |                     | AP_CRC_ERR        | 8:8       | ROCW | 0                        | EDH active picture CRC error indication.                                                                             |
|                      |                     | LOCK_ERR          | 7:7       | ROCW | 0                        | Lock error indication.                                                                                               |
|                      |                     | CCS_ERR_1         | 6:6       | ROCW | 0                        | Chroma/DS2 ancillary data checksum error indication.                                                                 |
|                      |                     | YCS_ERR_1         | 5:5       | ROCW | 0                        | Luma/DS1 ancillary data checksum error indication.                                                                   |
|                      |                     | CCRC_ERR_1        | 4:4       | ROCW | 0                        | Chroma/DS2 CRC error indication (HD/3G only).                                                                        |
|                      |                     | YCRC_ERR_1        | 3:3       | ROCW | 0                        | Luma/DS1 CRC error indication (HD/3G only).                                                                          |
|                      |                     | LNUM_ERR_1        | 2:2       | ROCW | 0                        | Line number error indication (HD/3G only).                                                                           |
|                      |                     | SAV_ERR_1         | 1:1       | ROCW | 0                        | SAV error indication.                                                                                                |
| 808                  | ERROR_STAT_2_STICKY | EAV_ERR_1         | 0:0       | ROCW | 0                        | EAV error indication.                                                                                                |
|                      |                     | RSVD              | 15:7      | —    | —                        | Reserved.                                                                                                            |
|                      |                     | CCS_ERR_2_STICKY  | 6:6       | ROCR | 0                        | Chroma ancillary data checksum error indication for the second stream of a 3G level B input – sticky, clear on read. |
|                      |                     | YCS_ERR_2_STICKY  | 5:5       | ROCR | 0                        | Luma ancillary data checksum error indication for the second stream of a 3G level B input– sticky, clear on read.    |
|                      |                     | CCRC_ERR_2_STICKY | 4:4       | ROCR | 0                        | Chroma CRC error indication for the second stream of a 3G level B input – sticky, clear on read.                     |
|                      |                     | YCRC_ERR_2_STICKY | 3:3       | ROCR | 0                        | Luma CRC error indication for the second stream of a 3G level B input – sticky, clear on read.                       |
|                      |                     | LNUM_ERR_2_STICKY | 2:2       | ROCR | 0                        | Line number error indication for the second stream of a 3G level B input – sticky, clear on read.                    |
|                      |                     | SAV_ERR_2_STICKY  | 1:1       | ROCR | 0                        | SAV error indication for the second stream of a 3G level B input– sticky, clear on read.                             |
|                      |                     | EAV_ERR_2_STICKY  | 0:0       | ROCR | 0                        | EAV error indication for the second stream of a 3G level B input – sticky, clear on read.                            |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit Slice | R/W  | Reset Value <sub>h</sub> | Description                                                                                  |
|----------------------|---------------|----------------|-----------|------|--------------------------|----------------------------------------------------------------------------------------------|
| 809                  | ERROR_STAT_2  | RSVD           | 15:7      | —    | —                        | Reserved.                                                                                    |
|                      |               | CCS_ERR_2      | 6:6       | ROCW | 0                        | Chroma ancillary data checksum error indication for the second stream of a 3G level B input. |
|                      |               | YCS_ERR_2      | 5:5       | ROCW | 0                        | Luma ancillary data checksum error indication for the second stream of a 3G level B input.   |
|                      |               | CCRC_ERR_2     | 4:4       | ROCW | 0                        | Chroma CRC error indication for the second stream of a 3G level B input.                     |
|                      |               | YCRC_ERR_2     | 3:3       | ROCW | 0                        | Luma CRC error indication for the second stream of a 3G level B input.                       |
|                      |               | LNUM_ERR_2     | 2:2       | ROCW | 0                        | Line number error indication for the second stream of a 3G level B input.                    |
|                      |               | SAV_ERR_2      | 1:1       | ROCW | 0                        | SAV error indication for the second stream of a 3G level B input                             |
|                      |               | EAV_ERR_2      | 0:0       | ROCW | 0                        | EAV error indication for the second stream of a 3G level B input                             |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                |
|----------------------|---------------|----------------|-----------|-----|--------------------------|------------------------------------------------------------|
| 80A                  | EDH_FLAG_IN   | EDH_DETECT     | 15:15     | RO  | 0                        | Embedded EDH packet detected.                              |
|                      |               | ANC_UES_IN     | 14:14     | RO  | 0                        | Ancillary data – unknown error status flag.                |
|                      |               | ANC_IDA_IN     | 13:13     | RO  | 0                        | Ancillary data – internal error detected already flag.     |
|                      |               | ANC_IDH_IN     | 12:12     | RO  | 0                        | Ancillary data – internal error detected here flag.        |
|                      |               | ANC_EDA_IN     | 11:11     | RO  | 0                        | Ancillary data – error detected already flag.              |
|                      |               | ANC_EDH_IN     | 10:10     | RO  | 0                        | Ancillary data – error detected here flag.                 |
|                      |               | FF_UES_IN      | 9:9       | RO  | 0                        | EDH Full Field – unknown error status flag.                |
|                      |               | FF_IDA_IN      | 8:8       | RO  | 0                        | EDH Full Field – internal error detected already flag.     |
|                      |               | FF_IDH_IN      | 7:7       | RO  | 0                        | EDH Full Field – internal error detected here flag.        |
|                      |               | FF_EDA_IN      | 6:6       | RO  | 0                        | EDH Full Field – error detected already flag.              |
|                      |               | FF_EDH_IN      | 5:5       | RO  | 0                        | EDH Full Field – error detected here flag.                 |
|                      |               | AP_UES_IN      | 4:4       | RO  | 0                        | EDH Active Picture – unknown error status flag.            |
|                      |               | AP_IDA_IN      | 3:3       | RO  | 0                        | EDH Active Picture – internal error detected already flag. |
|                      |               | AP_IDH_IN      | 2:2       | RO  | 0                        | EDH Active Picture – internal error detected here flag.    |
|                      |               | AP_EDA_IN      | 1:1       | RO  | 0                        | EDH Active Picture – error detected already flag.          |
|                      |               | AP_EDH_IN      | 0:0       | RO  | 0                        | EDH Active Picture – error detected here flag.             |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                |
|----------------------|---------------|----------------|-----------|-----|--------------------------|------------------------------------------------------------|
| 80B                  | EDH_FLAG_OUT  | RSVD           | 15:15     | —   | —                        | Reserved.                                                  |
|                      |               | ANC_UES        | 14:14     | RO  | 1                        | Ancillary data – unknown error status flag.                |
|                      |               | ANC_IDA        | 13:13     | RO  | 0                        | Ancillary data – internal error detected already flag.     |
|                      |               | ANC_IDH        | 12:12     | RO  | 0                        | Ancillary data – internal error detected here flag.        |
|                      |               | ANC_EDA        | 11:11     | RO  | 0                        | Ancillary data – error detected already flag.              |
|                      |               | ANC_EDH        | 10:10     | RO  | 0                        | Ancillary data – error detected here flag.                 |
|                      |               | FF_UES         | 9:9       | RO  | 1                        | EDH Full Field – unknown error status flag.                |
|                      |               | FF_IDA         | 8:8       | RO  | 0                        | EDH Full Field – internal error detected already flag.     |
|                      |               | FF_IDH         | 7:7       | RO  | 0                        | EDH Full Field – internal error detected here flag.        |
|                      |               | FF_EDA         | 6:6       | RO  | 0                        | EDH Full Field – error detected already flag.              |
|                      |               | FF_EDH         | 5:5       | RO  | 0                        | EDH Full Field – error detected here flag.                 |
|                      |               | AP_UES         | 4:4       | RO  | 1                        | EDH Active Picture – unknown error status flag.            |
|                      |               | AP_IDA         | 3:3       | RO  | 0                        | EDH Active Picture – internal error detected already flag. |
|                      |               | AP_IDH         | 2:2       | RO  | 0                        | EDH Active Picture – internal error detected here flag.    |
|                      |               | AP_EDA         | 1:1       | RO  | 0                        | EDH Active Picture – error detected already flag.          |
|                      |               | AP_EDH         | 0:0       | RO  | 0                        | EDH Active Picture – error detected here flag.             |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name   | Parameter Name   | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------|-----------------|------------------|-----------|-----|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 80C                  | DATA_FORMAT_DS1 | RSVD             | 15:10     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                      |                 | FF_CRC_V         | 9:9       | RO  | 0                        | EDH Full field CRC validity bit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                      |                 | AP_CRC_V         | 8:8       | RO  | 0                        | EDH Active Picture CRC validity bit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |                 | CDATA_FORMAT_AP1 | 7:4       | RO  | F                        | Data format as indicated in Chroma (DS2) channel:<br>0000 <sub>b</sub> = DVC Pro without ECC<br>0001 <sub>b</sub> = DVC Pro with ECC<br>0010 <sub>b</sub> = DV CAM<br>0011 <sub>b</sub> = SDTi CP<br>0100 <sub>b</sub> = Other fixed blocksize<br>0101 <sub>b</sub> = Other variable blocksize<br>0110 <sub>b</sub> = Other SDI<br>0111 <sub>b</sub> = Reserved<br>1000 <sub>b</sub> = TDM Video<br>1001 <sub>b</sub> = HD SDTi<br>1010 <sub>b</sub> to 1110 <sub>b</sub> = Reserved<br>1111 <sub>b</sub> = Unknown |
|                      |                 | YDATA_FORMAT_AP1 | 3:0       | RO  | F                        | Data format as indicated in Luma (DS1) channel:<br>0000 <sub>b</sub> = DVC Pro without ECC<br>0001 <sub>b</sub> = DVC Pro with ECC<br>0010 <sub>b</sub> = DV CAM<br>0011 <sub>b</sub> = SDTi CP<br>0100 <sub>b</sub> = Other fixed blocksize<br>0101 <sub>b</sub> = Other variable blocksize<br>0110 <sub>b</sub> = Other SDI<br>0111 <sub>b</sub> = Reserved<br>1000 <sub>b</sub> = TDM Video<br>1001 <sub>b</sub> = HD SDTi<br>1010 <sub>b</sub> to 1110 <sub>b</sub> = Reserved<br>1111 <sub>b</sub> = Unknown   |
|                      |                 | RSVD             | 15:11     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 80D                  | VID_STD_DS1     | LEVEL_B_DETECTED | 10:10     | RO  | 0                        | Level B detection as reported by the GS3470:<br>0 = SD, HD, or 3G Level A signal detected<br>1 = 3G Level B signal detected                                                                                                                                                                                                                                                                                                                                                                                         |
|                      |                 | LINK_DS1         | 9:6       | RO  | 0                        | Link indication: bits [7:4] of byte 4 of SMPTE 352 packet.                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                      |                 | VD_STD_DS1       | 5:0       | RO  | 1D                       | Detected video standard.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name   | Parameter Name   | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------------|-----------------|------------------|-----------|-----|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 80E                  | DATA_FORMAT_DS2 | RSVD             | 15:8      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |                 | CDATA_FORMAT_AP2 | 7:4       | RO  | F                        | Data format as indicated in Chroma channel of the second stream of a 3G level B input:<br>0000 <sub>b</sub> = DVC Pro without ECC<br>0001 <sub>b</sub> = DVC Pro with ECC<br>0010 <sub>b</sub> = DV CAM<br>0011 <sub>b</sub> = SDTi CP<br>0100 <sub>b</sub> = Other fixed blocksize<br>0101 <sub>b</sub> = Other variable blocksize<br>0110 <sub>b</sub> = Other SDI<br>0111 <sub>b</sub> = Reserved<br>1000 <sub>b</sub> = TDM Video<br>1001 <sub>b</sub> = HD SDTi<br>1010 <sub>b</sub> to 1110 <sub>b</sub> = Reserved<br>1111 <sub>b</sub> = Unknown |
|                      |                 | YDATA_FORMAT_AP2 | 3:0       | RO  | F                        | Data format as indicated in Luma channel of the second stream of a 3G level B input:<br>0000 <sub>b</sub> = DVC Pro without ECC<br>0001 <sub>b</sub> = DVC Pro with ECC<br>0010 <sub>b</sub> = DV CAM<br>0011 <sub>b</sub> = SDTi CP<br>0100 <sub>b</sub> = Other fixed blocksize<br>0101 <sub>b</sub> = Other variable blocksize<br>0110 <sub>b</sub> = Other SDI<br>0111 <sub>b</sub> = Reserved<br>1000 <sub>b</sub> = TDM Video<br>1001 <sub>b</sub> = HD SDTi<br>1010 <sub>b</sub> to 1110 <sub>b</sub> = Reserved<br>1111 <sub>b</sub> = Unknown   |
| 80F                  | VID_STD_DS2     | RSVD             | 15:10     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |                 | LINK_DS2         | 9:6       | RO  | 0                        | Link indication: bits [7:4] of Byte 4 of SMPTE 352 packet.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |                 | VD_STD_DS2       | 5:0       | RO  | 1D                       | Detected video standard.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 810                  | RSVD            | RSVD             | 15:0      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name     | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------|---------------|--------------------|-----------|-----|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 811                  | POWER_DOWN    | RSVD               | 15:4      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |               | PD_CSR_ACCESS      | 3:3       | RW  | 0                        | CSR access selection during power-down:<br>0 = Selects no CSR access during power-down when PWR_DWN is asserted<br>1 = Selects CSR access during power-down when PWR_DWN is asserted                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                      |               | RC_BYP             | 2:2       | RW  | 0                        | Retimer bypass selection:<br>0 = Selects retimed data (when DDO is enabled)<br>1 = Selects non-retimed data (when DDO is enabled)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                      |               | SERIAL_LOOPBACK_EN | 1:1       | RW  | 0                        | Serial loopback enable:<br>0 = The serial digital output signals DDO and $\overline{DDO}$ are disabled<br>1 = The serial digital output signals DDO and $\overline{DDO}$ are enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                      |               | PD_PCLK_ENABLE     | 0:0       | RW  | 0                        | PCLK enabled during power-down:<br>0 = Selects PCLK to be shut off when PWR_DWN is asserted<br>1 = Selects PCLK to be output when PWR_DWN is asserted                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 812                  | IO_CONFIG     | RSVD               | 15:15     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |               | STAT2_CONFIG       | 14:10     | RW  | 2                        | Configures STAT2 output pin:<br>00000 <sub>b</sub> = H/HSYNC<br>00001 <sub>b</sub> = V/VSNC<br>00010 <sub>b</sub> = F/DE<br>00011 <sub>b</sub> = LOCKED<br>00100 <sub>b</sub> = Y/1ANC<br>00101 <sub>b</sub> = C/2ANC<br>00110 <sub>b</sub> = $\overline{\text{DATA ERROR}}$<br>00111 <sub>b</sub> = $\overline{\text{VIDEO ERROR (GLOBAL\_ERR)}}$<br>01000 <sub>b</sub> = $\overline{\text{AUDIO ERROR}}$<br>01001 <sub>b</sub> = $\overline{\text{EDH\_DETECT}}$<br>01010 <sub>b</sub> = $\overline{\text{Carrier Detect}}$ (active LOW)<br>01011 <sub>b</sub> = $\overline{\text{SD\_HD}}$<br>01100 <sub>b</sub> = $\overline{\text{3G\_HD}}$<br>01101 <sub>b</sub> to 11111 <sub>b</sub> = Reserved |
|                      |               | STAT1_CONFIG       | 9:5       | RW  | 1                        | Configure STAT1 output pin. Refer to STAT2_CONFIG for decoding.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                      |               | STAT0_CONFIG       | 4:0       | RW  | 0                        | Configure STAT0 output pin. Refer to STAT2_CONFIG for decoding.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name  | Parameter Name  | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                            |
|----------------------|----------------|-----------------|-----------|-----|--------------------------|------------------------------------------------------------------------|
| 813                  | IO_CONFIG_2    | RSVD            | 15:15     | —   | —                        | Reserved.                                                              |
|                      |                | STAT5_CONFIG    | 14:10     | RW  | 6                        | Configure STAT5 output pin. Refer to STAT2_CONFIG for decoding.        |
|                      |                | STAT4_CONFIG    | 9:5       | RW  | 4                        | Configure STAT4 output pin. Refer to STAT2_CONFIG for decoding.        |
|                      |                | STAT3_CONFIG    | 4:0       | RW  | 3                        | Configure STAT3 output pin. Refer to STAT2_CONFIG for decoding.        |
| 814 to 816           | RSVD           | RSVD            | 15:0      | —   | —                        | Reserved.                                                              |
| 817                  | ANC_CONTROL    | RSVD            | 15:5      | —   | —                        | Reserved.                                                              |
|                      |                | WR_PTR_CLR      | 4:4       | RW  | 0                        | Clears the FIFO to idle.                                               |
|                      |                | ANC_DATA_SWITCH | 3:3       | RW  | 0                        | Switches between FIFO memories.                                        |
|                      |                | ANC_DATA_DEL    | 2:2       | RW  | 0                        | Removes ancillary data from output video stream.                       |
|                      |                | HD_ANC_Y1_C2    | 1:1       | RW  | 0                        | Extracts ancillary data from both Y (DS1) and C (DS2).                 |
|                      |                | HD_ANC_C2       | 0:0       | RW  | 0                        | Extracts ancillary data from C (DS2) only.                             |
| 818                  | ANC_LINEA      | RSVD            | 15:11     | —   | —                        | Reserved.                                                              |
|                      |                | ANC_LINE_A      | 10:0      | RW  | 0                        | Video line number to extract ancillary data from.                      |
| 819                  | ANC_LINEB      | RSVD            | 15:11     | —   | —                        | Reserved.                                                              |
|                      |                | ANC_LINE_B      | 10:0      | RW  | 0                        | Second video line number to extract ancillary data from.               |
| 81A to 81D           | RSVD           | RSVD            | 15:0      | —   | —                        | Reserved.                                                              |
| 81E                  | ANC_TYPE_1_DS1 | ANC_TYPE1_DS1   | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID |
| 81F                  | ANC_TYPE_2_DS1 | ANC_TYPE2_DS1   | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID |
| 820                  | ANC_TYPE_3_DS1 | ANC_TYPE3_DS1   | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID |
| 821                  | ANC_TYPE_4_DS1 | ANC_TYPE4_DS1   | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name        | Parameter Name            | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                  |
|----------------------|----------------------|---------------------------|-----------|-----|--------------------------|------------------------------------------------------------------------------------------------------------------------------|
| 822                  | ANC_TYPE_5_DS1       | ANC_TYPE5_DS1             | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID                                                       |
| 823                  | ANC_TYPE_1_DS2       | ANC_TYPE1_DS2             | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID                                                       |
| 824                  | ANC_TYPE_2_DS2       | ANC_TYPE2_DS2             | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID                                                       |
| 825                  | ANC_TYPE_3_DS2       | ANC_TYPE3_DS2             | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID                                                       |
| 826                  | ANC_TYPE_4_DS2       | ANC_TYPE4_DS2             | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID                                                       |
| 827                  | ANC_TYPE_5_DS2       | ANC_TYPE5_DS2             | 15:0      | RW  | 0                        | Programmable DID/SDID pair to extract:<br>[15:8] = DID<br>[7:0] = SDID                                                       |
| 828                  | VIDEO_FORMAT_352_A_1 | VIDEO_FORMAT_2_DS1_LUMA   | 15:8      | RO  | 0                        | SMPTE 352 embedded packet Luma – byte 2.                                                                                     |
|                      |                      | VIDEO_FORMAT_1_DS1_LUMA   | 7:0       | RO  | 0                        | SMPTE 352 embedded packet Luma – byte 1:<br>[7] = VERSION_352M<br>[6:0] = Video Payload Identifier                           |
| 829                  | VIDEO_FORMAT_352_B_1 | VIDEO_FORMAT_4_DS1_LUMA   | 15:8      | RO  | 0                        | SMPTE 352 embedded packet Luma – byte 4.                                                                                     |
|                      |                      | VIDEO_FORMAT_3_DS1_LUMA   | 7:0       | RO  | 0                        | SMPTE 352 embedded packet Luma – byte 3.                                                                                     |
| 82A                  | VIDEO_FORMAT_352_C_1 | VIDEO_FORMAT_2_DS1_CHROMA | 15:8      | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 2.                                                                                   |
|                      |                      | VIDEO_FORMAT_1_DS1_CHROMA | 7:0       | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 1.                                                                                   |
| 82B                  | VIDEO_FORMAT_352_D_1 | VIDEO_FORMAT_4_DS1_CHROMA | 15:8      | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 4.                                                                                   |
|                      |                      | VIDEO_FORMAT_3_DS1_CHROMA | 7:0       | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 3.                                                                                   |
| 82C                  | VIDEO_FORMAT_352_A_2 | VIDEO_FORMAT_2_DS2_LUMA   | 15:8      | RO  | 0                        | SMPTE 352 embedded packet – byte 2 (3G mode - second data stream).                                                           |
|                      |                      | VIDEO_FORMAT_1_DS2_LUMA   | 7:0       | RO  | 0                        | SMPTE 352 embedded packet – byte 1 (3G mode - second data stream):<br>[7] = VERSION_352M<br>[6:0] = Video Payload Identifier |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name        | Parameter Name            | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                               |
|----------------------|----------------------|---------------------------|-----------|-----|--------------------------|---------------------------------------------------------------------------|
| 82D                  | VIDEO_FORMAT_352_B_2 | VIDEO_FORMAT_4_DS2_LUMA   | 15:8      | RO  | 0                        | SMPTE 352 embedded packet – byte 4 (3G mode - second data stream).        |
|                      |                      | VIDEO_FORMAT_3_DS2_LUMA   | 7:0       | RO  | 0                        | SMPTE 352 embedded packet – byte 3 (3G mode - second data stream).        |
| 82E                  | VIDEO_FORMAT_352_C_2 | VIDEO_FORMAT_2_DS2_CHROMA | 15:8      | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 2 (3G mode - second data stream). |
|                      |                      | VIDEO_FORMAT_1_DS2_CHROMA | 7:0       | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 1 (3G mode - second data stream). |
| 82F                  | VIDEO_FORMAT_352_D_2 | VIDEO_FORMAT_4_DS2_CHROMA | 15:8      | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 4 (3G mode - second data stream). |
|                      |                      | VIDEO_FORMAT_3_DS2_CHROMA | 7:0       | RO  | 0                        | SMPTE 352 embedded packet Chroma – byte 3 (3G mode - second data stream). |
| 830                  | RASTER_STRUC_1_DS1   | RSVD                      | 15:14     | —   | —                        | Reserved.                                                                 |
|                      |                      | WORDS_PER_ACTLINE_DS1     | 13:0      | RO  | 0                        | Words per active line.                                                    |
| 831                  | RASTER_STRUC_2_DS1   | RSVD                      | 15:14     | —   | —                        | Reserved.                                                                 |
|                      |                      | WORDS_PER_LINE_DS1        | 13:0      | RO  | 0                        | Total words per line.                                                     |
| 832                  | RASTER_STRUC_3_DS1   | RSVD                      | 15:11     | —   | —                        | Reserved.                                                                 |
|                      |                      | LINES_PER_FRAME_DS1       | 10:0      | RO  | 0                        | Total lines per frame.                                                    |
| 833                  | RASTER_STRUC_4_DS1   | RATE_DET                  | 15:14     | RO  | 0                        | Detected rate:<br>00 = HD<br>01, 11 = SD<br>10 = 3G                       |
|                      |                      | M_DS1                     | 13:13     | RO  | 0                        | Specifies M value:<br>0 = 1.000<br>1 = 1.001                              |
|                      |                      | STD_LOCK_DS1              | 12:12     | RO  | 0                        | Video standard lock.                                                      |
|                      |                      | INT_PROG_DS1              | 11:11     | RO  | 0                        | Interlaced or progressive.                                                |
|                      |                      | ACTLINE_PER_FIELD_DS1     | 10:0      | RO  | 0                        | Active lines per frame.                                                   |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name   | Parameter Name                | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                   |
|----------------------|-----------------|-------------------------------|-----------|-----|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 834                  | FLYWHEEL_STATUS | RSVD                          | 15:5      | —   | —                        | Reserved.                                                                                                                                     |
|                      |                 | V_LOCK_FE2                    | 4:4       | RO  | 0                        | Indicates that flywheel is locked to V timing.                                                                                                |
|                      |                 | H_LOCK_FE2                    | 3:3       | RO  | 0                        | Indicates that flywheel is locked to H timing.                                                                                                |
|                      |                 | RSVD                          | 2:2       | —   | —                        | Reserved.                                                                                                                                     |
|                      |                 | V_LOCK_FE1                    | 1:1       | RO  | 0                        | Indicates that flywheel is locked to V timing.                                                                                                |
|                      |                 | H_LOCK_FE1                    | 0:0       | RO  | 0                        | Indicates that flywheel is locked to H timing.                                                                                                |
| 835                  | RATE_SEL        | RSVD                          | 15:5      | —   | —                        | Reserved.                                                                                                                                     |
|                      |                 | SMPTE_BYPASS                  | 4:4       | RW  | 1                        | When $\overline{\text{AUTO\_MAN}}$ is LOW, this is the SMPTE_BYPASS value.<br>0 = Input is in SMPTE_BYPASS mode<br>1 = Input is in SMPTE mode |
|                      |                 | DVB_ASI                       | 3:3       | RW  | 0                        | When $\overline{\text{AUTO\_MAN}}$ is LOW, this is the DVB_ASI value.<br>0 = Input is not DVB_ASI<br>1 = Input is DVB_ASI                     |
|                      |                 | $\overline{\text{AUTO\_MAN}}$ | 2:2       | RW  | 1                        | Data rate detect mode:<br>0 = Manual mode<br>1 = Automatic mode                                                                               |
|                      |                 | RATE_SEL_TOP                  | 1:0       | RW  | 0                        | Programmable rate select in manual mode:<br>00 <sub>b</sub> = HD<br>01 <sub>b</sub> , 11 <sub>b</sub> = SD<br>10 <sub>b</sub> = 3G            |
| 836                  | TIM_861_FORMAT  | RSVD                          | 15:7      | —   | —                        | Reserved.                                                                                                                                     |
|                      |                 | FORMAT_ERR                    | 6:6       | RO  | 1                        | Indicates standard is not recognized for CEA861-D conversion.                                                                                 |
|                      |                 | FORMAT_ID_861                 | 5:0       | RO  | 0                        | CEA-861-D format ID of input video stream.                                                                                                    |
| 837                  | TIM_861_CFG     | RSVD                          | 15:3      | —   | —                        | Reserved.                                                                                                                                     |
|                      |                 | VSYNC_INVERT                  | 2:2       | RW  | 0                        | Invert V-sync pulse.                                                                                                                          |
|                      |                 | HSYNC_INVERT                  | 1:1       | RW  | 0                        | Invert H-sync pulse.                                                                                                                          |
|                      |                 | RSVD                          | 0:0       | RW  | —                        | Reserved.                                                                                                                                     |
| 838 to 847           | RSVD            | RSVD                          | 15:0      | —   | —                        | Reserved.                                                                                                                                     |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name        | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------------|---------------|-----------------------|-----------|-----|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                      |               | RSVD                  | 15:10     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 848                  | ERROR_MASK_1  | ERROR_MASK_DS1_STICKY | 9:0       | RW  | 0                        | Error mask for global error vector - DS1 triggers (mask for sticky errors):<br>[9] = EDH full field CRC error mask<br>[8] = EDH active picture CRC error mask<br>[7] = Lock error mask<br>[6] = Chroma channel ancillary data checksum error mask<br>[5] = Luma channel ancillary data checksum error mask<br>[4] = Chroma channel CRC error mask<br>[3] = Luma channel CRC error mask<br>[2] = Line number error mask<br>[1] = SAV error mask<br>[0] = EAV error mask     |
|                      |               | RSVD                  | 15:10     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 849                  | ERROR_MASK_2  | ERROR_MASK_DS1        | 9:0       | RW  | 0                        | Error mask for global error vector - DS1 triggers (mask for non-sticky errors):<br>[9] = EDH full field CRC error mask<br>[8] = EDH active picture CRC error mask<br>[7] = Lock error mask<br>[6] = Chroma channel ancillary data checksum error mask<br>[5] = Luma channel ancillary data checksum error mask<br>[4] = Chroma channel CRC error mask<br>[3] = Luma channel CRC error mask<br>[2] = Line number error mask<br>[1] = SAV error mask<br>[0] = EAV error mask |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------------|---------------|----------------|-----------|-----|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 84A                  | ERROR_MASK_3  | RSVD           | 15:14     | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |               | ERROR_MASK_DS2 | 13:0      | RW  | 0                        | Error mask for global error vector - DS2 triggers (sticky and non-sticky):<br>[13] = Chroma channel ancillary data checksum error mask (non-sticky version)<br>[12] = Luma channel ancillary data checksum error mask (non-sticky version)<br>[11] = Chroma channel CRC error mask (non-sticky version)<br>[10] = Luma channel CRC error mask (non-sticky version)<br>[9] = Line number error mask (non-sticky version)<br>[8] = SAV error mask (non-sticky version)<br>[7] = EAV error mask (non-sticky version)<br>[6] = Chroma channel ancillary data checksum error mask (sticky version)<br>[5] = Luma channel ancillary data checksum error mask (sticky version)<br>[4] = Chroma channel CRC error mask (sticky version)<br>[3] = Luma channel CRC error mask (sticky version)<br>[2] = Line number error mask (sticky version)<br>[1] = SAV error mask (sticky version)<br>[0] = EAV error mask (sticky version) |
| 84B                  | ACG_CTRL      | RSVD           | 15:6      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |               | AUDIO_FREE_RUN | 5:5       | RW  | 0                        | 0 = Audio digital PLL runs in acquisition mode and tries to lock to REF_CLK<br>1 = Audio digital PLL runs in free run mode and ignores the REF_CLK                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                      |               | SCLK_INV       | 4:4       | RW  | 0                        | When HIGH, inverts polarity of output serial audio clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |               | AMCLK_INV      | 3:3       | RW  | 0                        | When HIGH, inverts polarity of output audio master clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |               | RSVD           | 2:2       | RW  | 0                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      |               | AMCLK_SEL      | 1:0       | RW  | 0                        | Audio Master Clock (AMCLK) select:<br>00 <sub>b</sub> = 128fs<br>01 <sub>b</sub> = 256fs<br>10 <sub>b</sub> = 512fs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 84C                  | RSVD          | RSVD           | 15:0      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                                                                                                                                              |
|----------------------|---------------|----------------|-----------|-----|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 84D                  | INPUT_CONFIG  | RSVD           | 15:8      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                |
|                      |               | SEL_TERM       | 7:6       | RW  | 0                        | Input termination control:<br>SEL_TERM[0] controls DDIO/DDIO<br>SEL_TERM[1] controls DDI1/DDI1<br>0 = Selects 50Ω termination<br>1 = Selects high impedance                                                                                                                                                                              |
|                      |               | RSVD           | 5:4       | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                |
|                      |               | SEL_INPUT      | 3:2       | RW  | 3                        | 00 <sub>b</sub> = Selects DDIO/DDIO parallel retimed output and DDO path<br>01 <sub>b</sub> = Selects DDI1/DDI1 parallel retimed output and DDIO/DDIO for DDO path<br>10 <sub>b</sub> = Selects DDIO/DDIO parallel retimed output and DDI1/DDI1 for DDO path<br>11 <sub>b</sub> = Selects DDI1/DDI1 parallel retimed output and DDO path |
|                      |               | RSVD           | 1:0       | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                |
| 84E to 867           | RSVD          | RSVD           | 15:0      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                |
| 868                  | PLL_CTRL_0    | RSVD           | 15:2      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                |
|                      |               | CD_SELECT      | 1:0       | RW  | 2                        | Controls the source of CARRIER_DETECT:<br>00 <sub>b</sub> = CD_DIGITAL_FILTER (edge detector)<br>01 <sub>b</sub> = CD_ANALOG_FILTER (LOS detector)<br>10 <sub>b</sub> = CD_DIGITAL_FILTER AND CD_ANALOG_FILTER<br>11 <sub>b</sub> = CD_DIGITAL_FILTER OR CD_ANALOG_FILTER                                                                |
| 869                  | PLD_CTRL_0    | RSVD           | 15:0      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                |
| 86A                  | PLD_CTRL_1    | RSVD           | 15:0      | —   | —                        | Reserved.                                                                                                                                                                                                                                                                                                                                |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name   | Parameter Name        | Bit Slice | R/W  | Reset Value <sub>h</sub> | Description                                                                                                                                         |
|----------------------|-----------------|-----------------------|-----------|------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 86B                  | PLL_STAT        | RSVD                  | 15:10     | —    | —                        | Reserved.                                                                                                                                           |
|                      |                 | PLLSM_CDRSEL          | 9:9       | RO   | 0                        | Unforced CDRSEL output:<br>0 = The device is using the clock as reference<br>1 = The device is using data as reference                              |
|                      |                 | PLLSM_LOCK            | 8:8       | RO   | 0                        | Unforced LOCK output.                                                                                                                               |
|                      |                 | LOS                   | 7:7       | RO   | 0                        | Loss of signal indicator. Inverse of CARRIER_DETECT.                                                                                                |
|                      |                 | PHASELOCK_ANALOG      | 6:6       | RO   | 0                        | Output of analog lock detector.                                                                                                                     |
|                      |                 | PLD_PHASELOCK_DIGITAL | 5:5       | RO   | 0                        | Output of digital phaselock detector.                                                                                                               |
|                      |                 | CD_CARRIER_DETECT     | 4:4       | RO   | 0                        | Unforced CARRIER_DETECT signal (after MUX).                                                                                                         |
|                      |                 | CD_DIGIAL_FILT        | 3:3       | RO   | 0                        | Filtered digital carrier detect status:<br>0 = The edge detection circuit is not detecting data<br>1 = The edge detection circuit is detecting data |
|                      |                 | CD_ANALOG_FILT        | 2:2       | RO   | 0                        | Filtered analog carrier detect status:<br>0 = When LOW, the LOS circuit is not detecting data<br>1 = When HIGH the LOS circuit is detecting data    |
|                      |                 | RSVD                  | 1:0       | —    | —                        | Reserved.                                                                                                                                           |
| 86C                  | PLL_STICKY_STAT | RSVD                  | 15:7      | —    | —                        | Reserved.                                                                                                                                           |
|                      |                 | LOCK_LOST_STICKY      | 6:6       | ROCW | 0                        | Sticky bit for loss of lock indicator. Inverse of LOCK output.                                                                                      |
|                      |                 | PHASELOCK_LOST_STICKY | 5:5       | ROCW | 0                        | Sticky bit for loss of phaselock indicator. Inverse of phaselock output from PHASE_DETECT.                                                          |
|                      |                 | LOS_STICKY            | 4:4       | ROCW | 0                        | Sticky bit for loss of signal indicator (after MUX). Inverse of CARRIER_DETECT.                                                                     |
|                      |                 | RSVD                  | 3:0       | ROCW | —                        | Reserved.                                                                                                                                           |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name         | Parameter Name       | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                              |
|----------------------|-----------------------|----------------------|-----------|-----|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 86D                  | OFFSET_CORRECTION_CFG | RSVD                 | 15:7      | —   | —                        | Reserved.                                                                                                                                |
|                      |                       | IB_PD_OFFSET_PATH_1  | 6:6       | RW  | 0                        | Powers down the offset DACs for input 1. Shuts off all offset correction from that input.                                                |
|                      |                       | IB_PD_OFFSET_PATH_0  | 5:5       | RW  | 0                        | Powers down the offset DACs for input 0. Shuts off all offset correction from that input.                                                |
|                      |                       | RSVD                 | 4:0       | RW  | 0                        | Reserved.                                                                                                                                |
| 86E                  | RSVD                  | RSVD                 | 15:0      | —   | —                        | Reserved.                                                                                                                                |
| 86F                  | LOS_CTRL              | RSVD                 | 15:9      | —   | —                        | Reserved.                                                                                                                                |
|                      |                       | LOS_AFE_SEL          | 8:8       | RW  | 1                        | AFE select:<br>0 = Selects DDI0 (directly from pin) for LOS sensing<br>1 = Selects DDI1 (directly from pin) for LOS sensing              |
|                      |                       | LOS_CD_TIME_CONSTANT | 7:6       | RW  | 1                        | Time constant.                                                                                                                           |
|                      |                       | LOS_CD_HYSTERESIS    | 5:4       | RW  | 1                        | LOS hysteresis.                                                                                                                          |
|                      |                       | RSVD                 | 3:0       | RW  | 5                        | Reserved.                                                                                                                                |
| 870                  | DELAY_LINE_CTRL_1     | RSVD                 | 15:15     | —   | —                        | Reserved.                                                                                                                                |
|                      |                       | PCLK_DELAY_SD        | 14:10     | RW  | 0                        | Controls the offset for the delay line in SD:<br>00000 <sub>b</sub> = No delay<br>11111 <sub>b</sub> = Max delay<br>Step Size = 0.006 UI |
|                      |                       | PCLK_DELAY_HD        | 9:5       | RW  | 0                        | Controls the offset for the delay line in HD:<br>00000 <sub>b</sub> = No delay<br>11111 <sub>b</sub> = Max delay<br>Step Size = 0.031 UI |
|                      |                       | PCLK_DELAY_3G        | 4:0       | RW  | 0                        | Controls the offset for the delay line in 3G:<br>00000 <sub>b</sub> = No delay<br>11111 <sub>b</sub> = Max delay<br>Step Size = 0.031 UI |
| 871                  | DELAY_LINE_CTRL_2     | RSVD                 | 15:3      | —   | —                        | Reserved.                                                                                                                                |
|                      |                       | PCLK_INVERT_SD       | 2:2       | RW  | 0                        | Controls the inversion of PCLK in SD.                                                                                                    |
|                      |                       | PCLK_INVERT_HD       | 1:1       | RW  | 0                        | Controls the inversion of PCLK in HD.                                                                                                    |
|                      |                       | PCLK_INVERT_3G       | 0:0       | RW  | 0                        | Controls the inversion of PCLK in 3G.                                                                                                    |
| 872 to 873           | RSVD                  | RSVD                 | 15:0      | —   | —                        | Reserved.                                                                                                                                |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name  | Parameter Name       | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                   |
|----------------------|----------------|----------------------|-----------|-----|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 874                  | CLK_GEN        | RSVD                 | 15:3      | —   | —                        | Reserved.                                                                                                                                                                     |
|                      |                | DDR_PHASE_DET_INVERT | 2:2       | RW  | 1                        | Swaps the phase in DDR mode.<br>User can choose whether to start data transmission from a rising edge or a falling edge of the DDR clock.                                     |
|                      |                | RSVD                 | 1:1       | RW  | 0                        | Reserved.                                                                                                                                                                     |
|                      |                | SD_HD_DDR_SEL        | 0:0       | RW  | 0                        | Enables DDR mode for SD, HD, and non-SMPTE data if DDR is supported for that specific rate.                                                                                   |
| 875                  | PD_CTRL        | RSVD                 | 15:12     | —   | —                        | Reserved.                                                                                                                                                                     |
|                      |                | POL_INV              | 11:11     | RW  | 0                        | Phase Detector Polarity Invert:<br>0 = PD uses normal data polarity<br>1 = PD uses inverted data polarity                                                                     |
|                      |                | RSVD                 | 10:0      | —   | —                        | Reserved.                                                                                                                                                                     |
| 876                  | RSVD           | RSVD                 | 15:0      | —   | —                        | Reserved.                                                                                                                                                                     |
| 877                  | PIN_CSR_SELECT | RSVD                 | 15:3      | —   | —                        | Reserved.                                                                                                                                                                     |
|                      |                | 20BIT_10BIT          | 2:2       | RW  | 0                        | CSR value for 20BIT_10BIT to be used when 20BIT_10BIT_PIN = 1<br>0 = Output parallel data bus is 10 bits<br>1 = Output parallel data bus is 20 bits                           |
|                      |                | 20BIT_10BIT_PIN      | 1:1       | RW  | 0                        | Override for 20BIT_10BIT pin:<br>0 = Selects pin value<br>1 = Selects CSR value                                                                                               |
|                      |                | IOPROC_EN            | 0:0       | RW  | 1                        | CSR value for IOPROC_EN:<br>0 = Disables all video and audio processing<br>1 = Enables all video and audio processing that are not masked in the IOPROC_1, IOPROC_2 registers |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name        | Parameter Name       | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                                                              |
|----------------------|----------------------|----------------------|-----------|-----|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 878                  | IO_DRIVE_STRENGTH    | RSVD                 | 15:9      | —   | —                        | Reserved.                                                                                                                                                                                                                |
|                      |                      | CSR_PCLK_HIZ         | 9:9       | RW  | 0                        | In auto rate detection mode (AUTO_MAN = 1), when PCLK_UNLOCKED_HIZ_SEL is HIGH,<br>0 = PCLK is active, regardless of locked condition of device<br>1 = PCLK is HIZ when device is unlocked, active when device is locked |
|                      |                      | MUTE_ON_NO_LOCK      | 8:8       | RW  | 1                        | 0 = Video data output bus is not muted when not locked<br>1 = Parallel video data output bus is muted (set to zero) when not locked                                                                                      |
|                      |                      | IO_DS_CTRL           | 7:6       | RW  | 1                        | Drive strength control for PCLK:<br>00 <sub>b</sub> = 4mA<br>01 <sub>b</sub> , 10 <sub>b</sub> = 8mA<br>11 <sub>b</sub> = 12mA                                                                                           |
|                      |                      | IO_DS_CTRL_STAT      | 5:4       | RW  | 1                        | Drive strength control for STAT[5:0]:<br>00 <sub>b</sub> = 4mA<br>01 <sub>b</sub> , 10 <sub>b</sub> = 8mA<br>11 <sub>b</sub> = 12mA                                                                                      |
|                      |                      | IO_DS_CTRL_DOUT_LSBS | 3:2       | RW  | 1                        | Drive strength control for DOUT[9:0]:<br>00 <sub>b</sub> = 4mA<br>01 <sub>b</sub> , 10 <sub>b</sub> = 8mA<br>11 <sub>b</sub> = 12mA                                                                                      |
|                      |                      | IO_DS_CTRL_DOUT_MSBS | 1:0       | RW  | 1                        | Drive strength control for DOUT[19:10]:<br>00 <sub>b</sub> = 4mA<br>01 <sub>b</sub> , 10 <sub>b</sub> = 8mA<br>11 <sub>b</sub> = 12mA                                                                                    |
| 879 to 87A           | RSVD                 | RSVD                 | 15:0      | —   | —                        | Reserved.                                                                                                                                                                                                                |
| 87B                  | OUTPUT_BUFFER_CTRL_1 | RSVD                 | 15:12     | —   | —                        | Reserved.                                                                                                                                                                                                                |
|                      |                      | SWING_3G             | 11:8      | RW  | 3                        | 3G swing control.<br>Range = 482mV.<br>Step Size = 40mV.                                                                                                                                                                 |
|                      |                      | SWING_HD             | 7:4       | RW  | 3                        | HD swing control.<br>Range = 486mV.<br>Step Size = 40mV.                                                                                                                                                                 |
|                      |                      | SWING_SD             | 3:0       | RW  | 3                        | SD swing control.<br>Range = 498mV.<br>Step Size = 40mV.                                                                                                                                                                 |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name             | Parameter Name            | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                            |
|----------------------|---------------------------|---------------------------|-----------|-----|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 87C                  | OUTPUT_BUFFER_CTRL_2      | RSVD                      | 15:10     | —   | —                        | Reserved.                                                                                                                                              |
|                      |                           | DRIVER_POL_INV_D2A        | 9:9       | RW  | 0                        | Input signal polarity invert within the driver block.                                                                                                  |
|                      |                           | DE_LEVEL_3G               | 8:6       | RW  | 0                        | De-emphasis level control for 3G rate.<br>0 = 0 dB<br>1 = 0.6 dB<br>2 = 1.9 dB<br>3 = 3.5 dB<br>4 = 5.5 dB<br>5 = 8.0 dB<br>6 = 11.5 dB<br>7 = 17.2 dB |
|                      |                           | DE_LEVEL_HD               | 5:3       | RW  | 0                        | De-emphasis level control for HD rate.<br>0 = 0 dB<br>1 = 0.9 dB<br>2 = 2.1 dB<br>3 = 3.7 dB<br>4 = 5.6 dB<br>5 = 8.1 dB<br>6 = 11.6 dB<br>7 = 17.4 dB |
|                      |                           | DE_LEVEL_SD               | 2:0       | RW  | 0                        | De-emphasis level control for SD rate.<br>0 = 0 dB<br>1 = 0.8 dB<br>2 = 2.2 dB<br>3 = 3.8 dB<br>4 = 5.8 dB<br>5 = 8.2 dB<br>6 = 11.6 dB<br>7 = 17.3 dB |
| 87D                  | H_16LINE_COUNT_DS1        | RSVD                      | 15:15     | —   | —                        | Reserved.                                                                                                                                              |
|                      |                           | H_16LINE_COUNT_DS1        | 14:0      | RO  | 0                        | Current value of 16 line horizontal count 0 to 27648 <sub>d</sub> ±10 <sub>d</sub> .                                                                   |
| 87E                  | M_DETECTION_TOLERANCE_DS1 | RSVD                      | 15:4      | —   | —                        | Reserved.                                                                                                                                              |
|                      |                           | M_DETECTION_TOLERANCE_DS1 | 3:0       | RW  | 2                        | 16 line count tolerance window horizontal count from reference count.                                                                                  |
| 87F                  | H_16LINE_COUNT_DS2        | RSVD                      | 15:15     | —   | —                        | Reserved.                                                                                                                                              |
|                      |                           | H_16LINE_COUNT_DS2        | 14:0      | RO  | 0                        | Current value of 16 line horizontal count 0 to 27648 <sub>d</sub> ±10 <sub>d</sub> .                                                                   |
| 880                  | M_DETECTION_TOLERANCE_DS2 | RSVD                      | 15:4      | —   | —                        | Reserved.                                                                                                                                              |
|                      |                           | M_DETECTION_TOLERANCE_DS2 | 3:0       | RW  | 2                        | 16 line count tolerance window horizontal count from reference count.                                                                                  |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name  | Parameter Name       | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                  |
|----------------------|----------------|----------------------|-----------|-----|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 881                  | RSVD           | RSVD                 | 15:0      | —   | —                        | Reserved.                                                                                                                                                    |
| 882                  | XPOINT_PD      | RSVD                 | 15:2      | —   | —                        | Reserved.                                                                                                                                                    |
|                      |                | XPOINT_PD            | 1:0       | RW  | 0                        | When PB_IB_HS_PATH_SEL = 1:<br>0 = Individual IB_HS_PATHS are not powered down<br>1 = Powers-down the individual IB_HS_PATHS                                 |
| 883                  | DDO_MUTE_CTRL  | RSVD                 | 15:3      | —   | —                        | Reserved.                                                                                                                                                    |
|                      |                | FORCE_DDO_MUTE_VAL   | 2:2       | RW  | 0                        | When FORCE_DDO_MUTE is HIGH:<br>0 = Sets DDO_MUTE_D2A (does not mute DDO)<br>1 = Sets DDO_MUTE_D2A (mutes DDO)                                               |
|                      |                | FORCE_DDO_MUTE       | 1:1       | RW  | 0                        | Forces the DDO output mute to the value in FORCE_DDO_MUTE_VAL.                                                                                               |
|                      |                | RSVD                 | 0:0       | —   | —                        | Reserved.                                                                                                                                                    |
| 884                  | DDO_CTRL       | RSVD                 | 15:10     | —   | —                        | Reserved.                                                                                                                                                    |
|                      |                | DDO_DATA_CLKB_D2A    | 9:9       | RW  | 1                        | 0 = Selects high-speed serial clock to be output on DDO<br>1 = Selects data to be output on DDO                                                              |
|                      |                | RSVD                 | 8:0       | —   | —                        | Reserved.                                                                                                                                                    |
| 885 to 8CA           | RSVD           | RSVD                 | 15:0      | —   | —                        | Reserved.                                                                                                                                                    |
| 8CB                  | GENERAL_STATUS | VERSION_ID           | 15:8      | RO  | 0                        | Version ID.                                                                                                                                                  |
|                      |                | SMPTE_BYPASSB_STATUS | 7:7       | RO  | 0                        | Same as value that can be brought on STAT outputs, indicates if the device is in SMPTE_BYPASS mode:<br>0 = SMPTE_BYPASS mode<br>1 = Not in SMPTE_BYPASS mode |
|                      |                | DVB_ASI_STATUS       | 6:6       | RO  | 0                        | Same as value that can be brought on STAT outputs, indicates if the device is locked to DVB_ASI:<br>0 = Not locked to DVB_ASI<br>1 = Locked to DVB_ASI       |
|                      |                | RSVD                 | 5:3       | RO  | —                        | Reserved.                                                                                                                                                    |
|                      |                | RSVD                 | 2:0       | RO  | —                        | Reserved.                                                                                                                                                    |
| 8CC to 8CE           | RSVD           | RSVD                 | 15:0      | —   | —                        | Reserved.                                                                                                                                                    |

**Table 5-8: Video Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name      | Parameter Name        | Bit Slice | R/W | Reset Value <sub>h</sub> | Description                                                                                                                                                                        |
|----------------------|--------------------|-----------------------|-----------|-----|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8CF                  | RASTER_STRUC_1_DS2 | RSVD                  | 15:14     | —   | —                        | Reserved.                                                                                                                                                                          |
|                      |                    | WORDS_PER_ACTLINE_DS2 | 13:0      | RO  | 0                        | Words per active line.                                                                                                                                                             |
| 8D0                  | RASTER_STRUC_2_DS2 | RSVD                  | 15:14     | —   | —                        | Reserved.                                                                                                                                                                          |
|                      |                    | WORDS_PER_LINE_DS2    | 13:0      | RO  | 0                        | Total words per line.                                                                                                                                                              |
| 8D1                  | RASTER_STRUC_3_DS2 | RSVD                  | 15:11     | —   | —                        | Reserved.                                                                                                                                                                          |
|                      |                    | LINES_PER_FRAME_DS2   | 10:0      | RO  | 0                        | Total lines per frame.                                                                                                                                                             |
| 8D2                  | RASTER_STRUC_4_DS2 | RSVD                  | 15:14     | —   | —                        | Reserved.                                                                                                                                                                          |
|                      |                    | M_DS2                 | 13:13     | RO  | 0                        | Specifies M value:<br>0 = 1.000<br>1 = 1.001                                                                                                                                       |
|                      |                    | STD_LOCK_DS2          | 12:12     | RO  | 0                        | Video standard lock.                                                                                                                                                               |
|                      |                    | INT_PROG_DS2          | 11:11     | RO  | 0                        | Interlaced or progressive.                                                                                                                                                         |
|                      |                    | ACTLINE_PER_FIELD_DS2 | 10:0      | RO  | 0                        | Active lines per frame.                                                                                                                                                            |
| 8D3                  | GENERAL_CONTROL    | RSVD                  | 15:5      | —   | —                        | Reserved.                                                                                                                                                                          |
|                      |                    | DVB_NOISE_IMMUNITY    | 4:4       | RW  | 0                        | Enables extra noise immunity when in DVB_ASI mode:<br>0 = Exit DVB_ASI and enter SMPTE mode when 3 TRSs in 2 lines<br>1 = Exit DVB_ASI and enter SMPTE mode when 7 TRSs in 4 lines |
|                      |                    | LOCK_NOISE_IMM_INCR   | 3:3       | RW  | 0                        | Enables extra noise immunity on SMPTE detected lock when HIGH by forcing detection of 3 TRS words with the last 2 TRS words having the same alignment before locking to SMPTE.     |
|                      |                    | RSVD                  | 2:0       | RW  | 0                        | Reserved.                                                                                                                                                                          |
| 8D4 to 988           | RSVD               | RSVD                  | 15:0      | —   | —                        | Reserved.                                                                                                                                                                          |
| 989                  | PD_IB_HS_PATH_SEL  | RSVD                  | 15:10     | —   | —                        | Reserved.                                                                                                                                                                          |
|                      |                    | PD_IB_HS_PATH_SEL     | 9:9       | RW  | 0                        | When set, XPOINT_PD can be used to control the power down for the input buffer high speed path.                                                                                    |
|                      |                    | RSVD                  | 8:0       | —   | —                        | Reserved.                                                                                                                                                                          |

**Table 5-9: HD and 3G Audio Core CSR Descriptions**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit   | R/W | Reset Value | Description                                                                                                                                                                                                                                       |
|----------------------|---------------|----------------|-------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A00                  | RSVD          | RSVD           | 15:0  | —   | —           | Reserved.                                                                                                                                                                                                                                         |
|                      |               | RSVD           | 15:14 | —   | —           | Reserved.                                                                                                                                                                                                                                         |
|                      |               | ASWLB          | 13:12 | RW  | 0           | Secondary group output word length.<br>00 <sub>b</sub> = 24 bits<br>01 <sub>b</sub> = 20 bits<br>10 <sub>b</sub> = 16 bits<br>11 <sub>b</sub> = Invalid                                                                                           |
|                      |               | ASWLA          | 11:10 | RW  | 0           | Primary group output word length.<br>00 <sub>b</sub> = 24 bits<br>01 <sub>b</sub> = 20 bits<br>10 <sub>b</sub> = 16 bits<br>11 <sub>b</sub> = Invalid                                                                                             |
| A01                  | CFG_AUD       | AMB            | 9:8   | RW  | 3           | Secondary group output format selector.<br>00 <sub>b</sub> = AES/EBU audio output<br>01 <sub>b</sub> = Serial audio output: left justified<br>10 <sub>b</sub> = Serial audio output: right justified<br>11 <sub>b</sub> = I2S serial audio output |
|                      |               | AMA            | 7:6   | RW  | 3           | Primary group output format selector.<br>00 <sub>b</sub> = AES/EBU audio output<br>01 <sub>b</sub> = Serial audio output: left justified<br>10 <sub>b</sub> = Serial audio output: right justified<br>11 <sub>b</sub> = I2S serial audio output   |
|                      |               | EXTEND_IDB     | 5:5   | RW  | 0           | 0 = Secondary audio group will extracted audio groups 1, 2, 3, or 4<br>1 = Secondary audio group will extracted audio groups 5, 6, 7, or 8                                                                                                        |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name          | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------------------|------------------------|----------------|------|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A01<br>(Continued)   | CFG_AUD<br>(Continued) | IDB            | 4:3  | RW  | 1           | <p>Along with EXTEND_IDB, specifies the Secondary audio group to extract.</p> <p>00<sub>b</sub> = Audio group #1 or #5<br/>           01<sub>b</sub> = Audio group #2 or #6<br/>           10<sub>b</sub> = Audio group #3 or #7<br/>           11<sub>b</sub> = Audio group #4 or #8</p> <p><b>Note:</b> Should IDA &amp; EXTEND_IDA and IDB &amp; EXTEND_IDB be set to the same audio group, IDA and IDB automatically revert to their default values.</p> |
|                      |                        | EXTEND_IDA     | 2:2  | RW  | 0           | <p>0 = Primary audio group will extracted audio groups 1, 2, 3 or 4.<br/>           1 = Primary audio group will extracted audio groups 5, 6, 7 or 8.</p>                                                                                                                                                                                                                                                                                                    |
|                      |                        | IDA            | 1:0  | RW  | 0           | <p>Along with EXTEND_IDA, specifies the Primary audio group to extract.</p> <p>00<sub>b</sub> = Audio group #1 or #5<br/>           01<sub>b</sub> = Audio group #2 or #6<br/>           10<sub>b</sub> = Audio group #3 or #7<br/>           11<sub>b</sub> = Audio group #4 or #8</p> <p><b>Note:</b> Should IDA &amp; EXTEND_IDA and IDB &amp; EXTEND_IDB be set to the same audio group, IDA and IDB automatically revert to their default values.</p>   |
| A02                  | CFG_AUD1               | RSVD           | 15:4 | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                      |                        | ECC_OFF        | 3:3  | RW  | 0           | When HIGH, disables ECC error correction.                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                      |                        | ALL_DEL        | 2:2  | RW  | 0           | <p>Selects deletion of all audio data and all audio control packets:</p> <p>0 = Do not delete existing audio data and control packets<br/>           1 = Delete existing audio data and control packets</p>                                                                                                                                                                                                                                                  |
|                      |                        | MUTE_ALL       | 1:1  | RW  | 0           | <p>Mute all output channels:</p> <p>0 = Normal<br/>           1 = Muted</p>                                                                                                                                                                                                                                                                                                                                                                                  |
|                      |                        | ACS_USE_SECOND | 0:0  | RW  | 0           | Extract Audio Channel Status from second channel pair.                                                                                                                                                                                                                                                                                                                                                                                                       |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W  | Reset Value | Description                                                                 |
|----------------------|---------------|----------------|------|------|-------------|-----------------------------------------------------------------------------|
| A03                  | ACS_DET       | RSVD           | 15:8 | —    | —           | Reserved.                                                                   |
|                      |               | DBNB_ERR       | 7:7  | ROCW | 0           | Set when Secondary group audio Data Block Number sequence is discontinuous. |
|                      |               | DBNA_ERR       | 6:6  | ROCW | 0           | Set when Primary group audio Data Block Number sequence is discontinuous.   |
|                      |               | CTRB_DET       | 5:5  | ROCW | 0           | Set when Secondary group audio control packet is detected.                  |
|                      |               | CTRA_DET       | 4:4  | ROCW | 0           | Set when Primary group audio control packet is detected.                    |
|                      |               | ACS_DET3_4B    | 3:3  | ROCW | 0           | Secondary group audio status detected for channels 3 and 4.                 |
|                      |               | ACS_DET1_2B    | 2:2  | ROCW | 0           | Secondary group audio status detected for channels 1 and 2.                 |
|                      |               | ACS_DET3_4A    | 1:1  | ROCW | 0           | Primary group audio status detected for channels 3 and 4.                   |
|                      |               | ACS_DET1_2A    | 0:0  | ROCW | 0           | Primary group audio status detected for channels 1 and 2.                   |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit   | R/W  | Reset Value | Description                                                                                                                   |
|----------------------|---------------|----------------|-------|------|-------------|-------------------------------------------------------------------------------------------------------------------------------|
| A04                  | AUD_DET1      | RSVD           | 15:13 | —    | —           | Reserved.                                                                                                                     |
|                      |               | IDB_READBACK   | 12:11 | RO   | 1           | Actual value of IDB in the hardware.                                                                                          |
|                      |               | IDA_READBACK   | 10:9  | RO   | 0           | Actual value of IDA in the hardware.                                                                                          |
|                      |               | ADPG8_DET      | 8:8   | RO   | 0           | Set to 1 and remains set while Group 8 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ADPG7_DET      | 7:7   | RO   | 0           | Set to 1 and remains set while Group 7 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ADPG6_DET      | 6:6   | RO   | 0           | Set to 1 and remains set while Group 6 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ADPG5_DET      | 5:5   | RO   | 0           | Set to 1 and remains set while Group 5 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ADPG4_DET      | 4:4   | RO   | 0           | Set to 1 and remains set while Group 4 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ADPG3_DET      | 3:3   | RO   | 0           | Set to 1 and remains set while Group 3 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ADPG2_DET      | 2:2   | RO   | 0           | Set to 1 and remains set while Group 2 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ADPG1_DET      | 1:1   | RO   | 0           | Set to 1 and remains set while Group 1 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame. |
|                      |               | ACS_APPLY_WAIT | 0:0   | RO   | 0           | Set while output channels 1 and 2 are waiting for a status boundary to apply the ACSR[183:0] data.                            |
| A05                  | AUD_DET2      | RSVD           | 15:2  | —    | —           | Reserved.                                                                                                                     |
|                      |               | ECCA_ERROR     | 1:1   | ROCW | 0           | Primary group audio data packet error detected.                                                                               |
|                      |               | ECCB_ERROR     | 0:0   | ROCW | 0           | Secondary group audio data packet error detected.                                                                             |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                                                                                                                                       |
|----------------------|---------------|----------------|------|-----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A06                  | REGEN         | RSVD           | 15:2 | —   | —           | Reserved.                                                                                                                                                                                                         |
|                      |               | ACS_APPLY      | 1:1  | RW  | 0           | When set to 1, this causes channel status data in ACSR[183:0] (ACSR_BYTE_* registers) to be transferred to the channel status replacement mechanism. The transfer shall not occur until the next status boundary. |
|                      |               | ACS_REGEN      | 0:0  | RW  | 0           | Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field (ACSR_BYTE_* registers).<br>0 = Do not replace Channel Status<br>1 = Replace Channel Status of all channels         |
| A07                  | CH_MUTE       | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                                                                                                         |
|                      |               | MUTEB          | 7:4  | RW  | 0           | Mute Secondary output channels 4 to 1; bits 3:0 = channel 4:1<br>0 = Normal<br>1 = Muted                                                                                                                          |
|                      |               | MUTEA          | 3:0  | RW  | 0           | Mute Primary output channels 4 to 1; bits 3:0 = channel 4:1<br>0 = Normal<br>1 = Muted                                                                                                                            |
| A08                  | CH_VALID      | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                                                                                                         |
|                      |               | CH4_VALIDDB    | 7:7  | RO  | 0           | Secondary group channel 4 sample validity flag.                                                                                                                                                                   |
|                      |               | CH3_VALIDDB    | 6:6  | RO  | 0           | Secondary group channel 3 sample validity flag.                                                                                                                                                                   |
|                      |               | CH2_VALIDDB    | 5:5  | RO  | 0           | Secondary group channel 2 sample validity flag.                                                                                                                                                                   |
|                      |               | CH1_VALIDDB    | 4:4  | RO  | 0           | Secondary group channel 1 sample validity flag.                                                                                                                                                                   |
|                      |               | CH4_VALIDA     | 3:3  | RO  | 0           | Primary group channel 4 sample validity flag.                                                                                                                                                                     |
|                      |               | CH3_VALIDA     | 2:2  | RO  | 0           | Primary group channel 3 sample validity flag.                                                                                                                                                                     |
|                      |               | CH2_VALIDA     | 1:1  | RO  | 0           | Primary group channel 2 sample validity flag.                                                                                                                                                                     |
|                      |               | CH1_VALIDA     | 0:0  | RO  | 0           | Primary group channel 1 sample validity flag.                                                                                                                                                                     |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                              |
|----------------------|---------------|----------------|------|-----|-------------|----------------------------------------------------------------------------------------------------------|
| A09                  | INT_ENABLE    | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                |
|                      |               | EN_ADPG8_DET   | 7:7  | RW  | 0           | Interrupt mask enable for ADPG8_DET pulse.<br>When enabled, interrupt will assert when ADPG8_DET is set. |
|                      |               | EN_ADPG7_DET   | 6:6  | RW  | 0           | Interrupt mask enable for ADPG7_DET pulse.<br>When enabled, interrupt will assert when ADPG7_DET is set. |
|                      |               | EN_ADPG6_DET   | 5:5  | RW  | 0           | Interrupt mask enable for ADPG6_DET pulse.<br>When enabled, interrupt will assert when ADPG6_DET is set. |
|                      |               | EN_ADPG5_DET   | 4:4  | RW  | 0           | Interrupt mask enable for ADPG5_DET pulse.<br>When enabled, interrupt will assert when ADPG5_DET is set. |
|                      |               | EN_ADPG4_DET   | 3:3  | RW  | 0           | Interrupt mask enable for ADPG4_DET pulse.<br>When enabled, interrupt will assert when ADPG4_DET is set. |
|                      |               | EN_ADPG3_DET   | 2:2  | RW  | 0           | Interrupt mask enable for ADPG3_DET pulse.<br>When enabled, interrupt will assert when ADPG3_DET is set. |
|                      |               | EN_ADPG2_DET   | 1:1  | RW  | 0           | Interrupt mask enable for ADPG2_DET pulse.<br>When enabled, interrupt will assert when ADPG2_DET is set. |
|                      |               | EN_ADPG1_DET   | 0:0  | RW  | 0           | Interrupt mask enable for ADPG1_DET pulse.<br>When enabled, interrupt will assert when ADPG1_DET is set. |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name   | Bit   | R/W | Reset Value | Description                                                                                                      |
|----------------------|---------------|------------------|-------|-----|-------------|------------------------------------------------------------------------------------------------------------------|
| A0A                  | INT_ENABLE2   | RSVD             | 15:11 | —   | —           | Reserved.                                                                                                        |
|                      |               | EN_MISSING_PHASE | 10:10 | RW  | 0           | Interrupt mask enable. When enabled, interrupt will assert when chosen group's phase data is missing or invalid. |
|                      |               | EN_ACS_DET3_4B   | 9:9   | RW  | 0           | Interrupt mask enable for ACS_DET3_4B. When enabled, interrupt will assert when ACS_DET3_4B is set.              |
|                      |               | EN_ACS_DET1_2B   | 8:8   | RW  | 0           | Interrupt mask enable for ACS_DET1_2B. When enabled, interrupt will assert when ACS_DET1_2B is set.              |
|                      |               | EN_ACS_DET3_4A   | 7:7   | RW  | 0           | Interrupt mask enable for ACS_DET3_4A. When enabled, interrupt will assert when ACS_DET3_4A is set.              |
|                      |               | EN_ACS_DET1_2A   | 6:6   | RW  | 0           | Interrupt mask enable for ACS_DET1_2A. When enabled, interrupt will assert when ACS_DET1_2A is set.              |
|                      |               | EN_CTRB_DET      | 5:5   | RW  | 0           | Interrupt mask enable for CTRB_DET. When enabled, interrupt will assert when CTRB_DET is set.                    |
|                      |               | EN_CTRA_DET      | 4:4   | RW  | 0           | Interrupt mask enable for CTRA_DET. When enabled, interrupt will assert when CTRA_DET is set.                    |
|                      |               | EN_DBNB_ERR      | 3:3   | RW  | 0           | Interrupt mask enable for DBNB_ERR. When enabled, interrupt will assert when DBNB_ERR is set.                    |
|                      |               | EN_DBNA_ERR      | 2:2   | RW  | 0           | Interrupt mask enable for DBNA_ERR. When enabled, interrupt will assert when DBNA_ERR is set.                    |
|                      |               | EN_ECCB_ERR      | 1:1   | RW  | 0           | Interrupt mask enable for ECCB_ERROR. When enabled, interrupt will assert when ECCB_ERROR is set.                |
|                      |               | EN_ECCA_ERR      | 0:0   | RW  | 0           | Interrupt mask enable for ECCA_ERROR. When enabled, interrupt will assert when ECCA_ERROR is set.                |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name              | Bit   | R/W | Reset Value | Description                                                                                                                                                                            |
|----------------------|---------------|-----------------------------|-------|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0B                  | CFG_AUD_2     | RSVD                        | 15:12 | —   | —           | Reserved.                                                                                                                                                                              |
|                      |               | SEL_PHASE_SRC               | 11:11 | RW  | 0           | Selects between the Primary and Secondary embedded phase info when FORCE_PHASE_SRC set to 1.<br>0 = Use primary group phase information<br>1 = Use secondary group phase information   |
|                      |               | FORCE_PHASE_SRC             | 10:10 | RW  | 0           | Phase source override:<br>0 = Auto phase source selection<br>1 = Manually set the phase source using SEL_PHASE_SRC                                                                     |
|                      |               | RSVD                        | 9:8   | —   | —           | Reserved.                                                                                                                                                                              |
|                      |               | FORCE_M                     | 7:7   | RW  | 0           | Disables auto-detection of M value and forces it to the state specified by the FORCE_MEQ1001 signal.                                                                                   |
|                      |               | FORCE_MEQ1001               | 6:6   | RW  | 0           | Specifies M value when FORCE_M is set:<br>0 = M is 1.000<br>1 = M is 1.001                                                                                                             |
|                      |               | IGNORE_PHASE                | 5:5   | RW  | 0           | When HIGH, causes the HD_DEMUX to ignore the embedded clock info in both the Primary and Secondary group audio data packets. Clock is generated based on the video format and M value. |
|                      |               | FORCE_ACLK128               | 4:4   | RW  | 0           | When HIGH, causes the HD_DEMUX to ignore embedded clock info and derive phase information from ACLK128.                                                                                |
|                      |               | EN_NOT_LOCKED               | 3:3   | RW  | 0           | Interrupt mask enable. When enabled, interrupt will assert when locked is not asserted.                                                                                                |
|                      |               | EN_NO_VIDEO                 | 2:2   | RW  | 0           | Interrupt mask enable. When enabled, interrupt will assert when the video format is unknown.                                                                                           |
|                      |               | EN_INVALID_EMBEDDED_PHASE_B | 1:1   | RW  | 0           | Interrupt mask enable for INVALID_EMBEDDED_PHASE_B. When enabled, interrupt will assert when INVALID_EMBEDDED_PHASE_B is set.                                                          |
|                      |               | EN_INVALID_EMBEDDED_PHASE_A | 0:0   | RW  | 0           | Interrupt mask enable for INVALID_EMBEDDED_PHASE_A. When enabled, interrupt will assert when INVALID_EMBEDDED_PHASE_A is set.                                                          |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name           | Bit   | R/W | Reset Value | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------------|---------------|--------------------------|-------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0C                  | CFG_AUD_3     | RSVD                     | 15:6  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |               | SELECTED_PHASE_SRC       | 5:5   | RO  | 0           | Indicates the source audio group for the embedded phase information:<br>0 = Using primary group phase information<br>1 = Using secondary group phase information                                                                                                                                                                                                                                                                                                          |
|                      |               | MISSING_PHASE            | 4:4   | RO  | 0           | When HIGH, either INVALID_EMBEDDED_PHASE_A or INVALID_EMBEDDED_PHASE_B is asserted based on SELECTED_PHASE_SRC.                                                                                                                                                                                                                                                                                                                                                           |
|                      |               | INVALID_EMBEDDED_PHASE_B | 3:3   | RO  | 0           | When HIGH, secondary group audio data packets have invalid embedded phase data.                                                                                                                                                                                                                                                                                                                                                                                           |
|                      |               | INVALID_EMBEDDED_PHASE_A | 2:2   | RO  | 0           | When HIGH, primary group audio data packets have invalid embedded phase data.                                                                                                                                                                                                                                                                                                                                                                                             |
|                      |               | EMBEDDED_PHASE_IGNORED_B | 1:1   | RO  | 0           | When HIGH, secondary group audio data packets have invalid embedded phase data or when IGNORE_PHASE or FORCE_ACLK128 are asserted.                                                                                                                                                                                                                                                                                                                                        |
|                      |               | EMBEDDED_PHASE_IGNORED_A | 0:0   | RO  | 0           | When HIGH, primary group audio data packets have invalid embedded phase data or when IGNORE_PHASE or FORCE_ACLK128 are asserted.                                                                                                                                                                                                                                                                                                                                          |
| A0D                  | OUTPUT_SEL_1  | RSVD                     | 15:12 | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |               | OP4_SRC                  | 11:9  | RW  | 3           | Output channel 4 source selector:<br>000 <sub>b</sub> = Primary audio group channel 1<br>001 <sub>b</sub> = Primary audio group channel 2<br>010 <sub>b</sub> = Primary audio group channel 3<br>011 <sub>b</sub> = Primary audio group channel 4<br>100 <sub>b</sub> = Secondary audio group channel 1<br>101 <sub>b</sub> = Secondary audio group channel 2<br>110 <sub>b</sub> = Secondary audio group channel 3<br>111 <sub>b</sub> = Secondary audio group channel 4 |
|                      |               | OP3_SRC                  | 8:6   | RW  | 2           | Output channel 3 source selector. See OP4_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |               | OP2_SRC                  | 5:3   | RW  | 1           | Output channel 2 source selector. See OP4_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |               | OP1_SRC                  | 2:0   | RW  | 0           | Output channel 1 source selected. See OP4_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name    | Parameter Name | Bit   | R/W | Reset Value | Description                                                     |
|----------------------|------------------|----------------|-------|-----|-------------|-----------------------------------------------------------------|
| A0E                  | OUTPUT_SEL_2     | RSVD           | 15:12 | —   | —           | Reserved.                                                       |
|                      |                  | OP8_SRC        | 11:9  | RW  | 7           | Output channel 8 source selector. See OP4_SRC for decoding.     |
|                      |                  | OP7_SRC        | 8:6   | RW  | 6           | Output channel 7 source selector. See OP4_SRC for decoding.     |
|                      |                  | OP6_SRC        | 5:3   | RW  | 5           | Output channel 6 source selector. See OP4_SRC for decoding.     |
|                      |                  | OP5_SRC        | 2:0   | RW  | 4           | Output channel 5 source selector. See OP4_SRC for decoding.     |
| A0F to A1F           | RSVD             | RSVD           | 15:0  | —   | —           | Reserved.                                                       |
| A20                  | AFNA             | RSVD           | 15:9  | —   | —           | Reserved.                                                       |
|                      |                  | AFNA           | 8:0   | RO  | 0           | Primary group audio frame number.                               |
| A21                  | RATEA            | RSVD           | 15:4  | —   | —           | Reserved.                                                       |
|                      |                  | RATEA          | 3:1   | RO  | 0           | Primary group sampling frequency for channels 1 and 2.          |
|                      |                  | ASXA           | 0:0   | RO  | 0           | Primary group asynchronous mode for channels 1 and 2.           |
| A22                  | ACTA             | RSVD           | 15:4  | —   | —           | Reserved.                                                       |
|                      |                  | ACTA           | 3:0   | RO  | 0           | Primary group active channels.                                  |
| A23                  | PRIM_AUD_DELAY_1 | RSVD           | 15:9  | —   | —           | Reserved.                                                       |
|                      |                  | DEL1_2A_1      | 8:1   | RO  | 0           | Primary Audio group delay data for channels 1 and 2 [7:0].      |
|                      |                  | EBIT1_2A       | 0:0   | RO  | 0           | Primary Audio group delay data valid flag for channels 1 and 2. |
| A24                  | PRIM_AUD_DELAY_2 | RSVD           | 15:9  | —   | —           | Reserved.                                                       |
|                      |                  | DEL1_2A_2      | 8:0   | RO  | 0           | Primary Audio group delay data for channels 1 and 2 [16:8].     |
| A25                  | PRIM_AUD_DELAY_3 | RSVD           | 15:9  | —   | —           | Reserved.                                                       |
|                      |                  | DEL1_2A_3      | 8:0   | RO  | 0           | Primary Audio group delay data for channels 1 and 2 [25:17].    |
| A26                  | PRIM_AUD_DELAY_4 | RSVD           | 15:9  | —   | —           | Reserved.                                                       |
|                      |                  | DEL3_4A_4      | 8:1   | RO  | 0           | Primary Audio group delay data for channels 3 and 4 [7:0].      |
|                      |                  | EBIT3_4A       | 0:0   | RO  | 0           | Primary Audio group delay data valid flag for channels 3 and 4. |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name    | Parameter Name | Bit  | R/W | Reset Value | Description                                                       |
|----------------------|------------------|----------------|------|-----|-------------|-------------------------------------------------------------------|
| A27                  | PRIM_AUD_DELAY_5 | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | DEL3_4A_5      | 8:0  | RO  | 0           | Primary Audio group delay data for channels 3 and 4 [16:8].       |
| A28                  | PRIM_AUD_DELAY_6 | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | DEL3_4A_6      | 8:0  | RO  | 0           | Primary Audio group delay data for channels 3 and 4 [25:17].      |
| A29 to A2F           | RSVD             | RSVD           | 15:0 | —   | —           | Reserved.                                                         |
| A30                  | AFNB             | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | AFNB           | 8:0  | RO  | 0           | Secondary group audio frame number.                               |
| A31                  | RATEB            | RSVD           | 15:4 | —   | —           | Reserved.                                                         |
|                      |                  | RATEB          | 3:1  | RO  | 0           | Secondary group sampling frequency for channels 1 and 2.          |
|                      |                  | ASXB           | 0:0  | RO  | 0           | Secondary group asynchronous mode for channels 1 and 2.           |
| A32                  | ACTB             | RSVD           | 15:4 | —   | —           | Reserved.                                                         |
|                      |                  | ACTB           | 3:0  | RO  | 0           | Secondary group active channels.                                  |
| A33                  | SEC_AUD_DELAY_1  | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | DEL1_2B_1      | 8:1  | RO  | 0           | Secondary Audio group delay data for channels 1 and 2 [7:0].      |
|                      |                  | EBIT1_2B       | 0:0  | RO  | 0           | Secondary Audio group delay data valid flag for channels 1 and 2. |
| A34                  | SEC_AUD_DELAY_2  | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | DEL1_2B_2      | 8:0  | RO  | 0           | Secondary Audio group delay data for channels 1 and 2 [16:8].     |
| A35                  | SEC_AUD_DELAY_3  | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | DEL1_2B_3      | 8:0  | RO  | 0           | Secondary Audio group delay data for channels 1 and 2 [25:17].    |
| A36                  | SEC_AUD_DELAY_4  | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | DEL3_4B_4      | 8:1  | RO  | 0           | Secondary Audio group delay data for channels 3 and 4 [7:0].      |
|                      |                  | EBIT3_4B       | 0:0  | RO  | 0           | Secondary Audio group delay data valid flag for channels 3 and 4. |
| A37                  | SEC_AUD_DELAY_5  | RSVD           | 15:9 | —   | —           | Reserved.                                                         |
|                      |                  | DEL3_4B_5      | 8:0  | RO  | 0           | Secondary Audio group delay data for channels 3 and 4 [16:8].     |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name      | Parameter Name | Bit  | R/W | Reset Value | Description                                                           |
|----------------------|--------------------|----------------|------|-----|-------------|-----------------------------------------------------------------------|
| A38                  | SEC_AUD_DELAY_6    | RSVD           | 15:9 | —   | —           | Reserved.                                                             |
|                      |                    | DEL3_4B_6      | 8:0  | RO  | 0           | Secondary Audio group delay data for channels 3 and 4 [25:17].        |
| A39 to A3F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                             |
| A40                  | ACSR1_2A_BYTE0_1   | ACSR1_2A_0     | 15:0 | RO  | 0           | Bytes 0 and 1 of audio group A channel status for channels 1 and 2.   |
| A41                  | ACSR1_2A_BYTE2_3   | ACSR1_2A_2     | 15:0 | RO  | 0           | Bytes 2 and 3 of audio group A channel status for channels 1 and 2.   |
| A42                  | ACSR1_2A_BYTE4_5   | ACSR1_2A_4     | 15:0 | RO  | 0           | Bytes 4 and 5 of audio group A channel status for channels 1 and 2.   |
| A43                  | ACSR1_2A_BYTE6_7   | ACSR1_2A_6     | 15:0 | RO  | 0           | Bytes 6 and 7 of audio group A channel status for channels 1 and 2.   |
| A44                  | ACSR1_2A_BYTE8_9   | ACSR1_2A_8     | 15:0 | RO  | 0           | Bytes 8 and 9 of audio group A channel status for channels 1 and 2.   |
| A45                  | ACSR1_2A_BYTE10_11 | ACSR1_2A_10    | 15:0 | RO  | 0           | Bytes 10 and 11 of audio group A channel status for channels 1 and 2. |
| A46                  | ACSR1_2A_BYTE12_13 | ACSR1_2A_12    | 15:0 | RO  | 0           | Bytes 12 and 13 of audio group A channel status for channels 1 and 2. |
| A47                  | ACSR1_2A_BYTE14_15 | ACSR1_2A_14    | 15:0 | RO  | 0           | Bytes 14 and 15 of audio group A channel status for channels 1 and 2. |
| A48                  | ACSR1_2A_BYTE16_17 | ACSR1_2A_16    | 15:0 | RO  | 0           | Bytes 16 and 17 of audio group A channel status for channels 1 and 2. |
| A49                  | ACSR1_2A_BYTE18_19 | ACSR1_2A_18    | 15:0 | RO  | 0           | Bytes 18 and 19 of audio group A channel status for channels 1 and 2. |
| A4A                  | ACSR1_2A_BYTE20_21 | ACSR1_2A_20    | 15:0 | RO  | 0           | Bytes 20 and 21 of audio group A channel status for channels 1 and 2. |
| A4B                  | ACSR1_2A_BYTE22    | RSVD           | 15:8 | —   | —           | Reserved.                                                             |
|                      |                    | ACSR1_2A_22    | 7:0  | RO  | 0           | Bytes 22 of audio group A channel status for channels 1 and 2.        |
| A4C to A4F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                             |
| A50                  | ACSR3_4A_BYTE0_1   | ACSR3_4A_0     | 15:0 | RO  | 0           | Bytes 0 and 1 of audio group A channel status for channels 3 and 4.   |
| A51                  | ACSR3_4A_BYTE2_3   | ACSR3_4A_2     | 15:0 | RO  | 0           | Bytes 2 and 3 of audio group A channel status for channels 3 and 4.   |
| A52                  | ACSR3_4A_BYTE4_5   | ACSR3_4A_4     | 15:0 | RO  | 0           | Bytes 4 and 5 of audio group A channel status for channels 3 and 4.   |
| A53                  | ACSR3_4A_BYTE6_7   | ACSR3_4A_6     | 15:0 | RO  | 0           | Bytes 6 and 7 of audio group A channel status for channels 3 and 4.   |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name      | Parameter Name | Bit  | R/W | Reset Value | Description                                                           |
|----------------------|--------------------|----------------|------|-----|-------------|-----------------------------------------------------------------------|
| A54                  | ACSR3_4A_BYTE8_9   | ACSR3_4A_8     | 15:0 | RO  | 0           | Bytes 8 and 9 of audio group A channel status for channels 3 and 4.   |
| A55                  | ACSR3_4A_BYTE10_11 | ACSR3_4A_10    | 15:0 | RO  | 0           | Bytes 10 and 11 of audio group A channel status for channels 3 and 4. |
| A56                  | ACSR3_4A_BYTE12_13 | ACSR3_4A_12    | 15:0 | RO  | 0           | Bytes 12 and 13 of audio group A channel status for channels 3 and 4. |
| A57                  | ACSR3_4A_BYTE14_15 | ACSR3_4A_14    | 15:0 | RO  | 0           | Bytes 14 and 15 of audio group A channel status for channels 3 and 4. |
| A58                  | ACSR3_4A_BYTE16_17 | ACSR3_4A_16    | 15:0 | RO  | 0           | Bytes 16 and 17 of audio group A channel status for channels 3 and 4. |
| A59                  | ACSR3_4A_BYTE18_19 | ACSR3_4A_18    | 15:0 | RO  | 0           | Bytes 18 and 19 of audio group A channel status for channels 3 and 4. |
| A5A                  | ACSR3_4A_BYTE20_21 | ACSR3_4A_20    | 15:0 | RO  | 0           | Bytes 20 and 21 of audio group A channel status for channels 3 and 4. |
| A5B                  | ACSR3_4A_BYTE22    | RSVD           | 15:8 | —   | —           | Reserved.                                                             |
|                      |                    | ACSR3_4A_22    | 7:0  | RO  | 0           | Bytes 22 of audio group A channel status for channels 3 and 4.        |
| A5C to A5F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                             |
| A60                  | ACSR1_2B_BYTE0_1   | ACSR1_2B_0     | 15:0 | RO  | 0           | Bytes 0 and 1 of audio group B channel status for channels 1 and 2.   |
| A61                  | ACSR1_2B_BYTE2_3   | ACSR1_2B_2     | 15:0 | RO  | 0           | Bytes 2 and 3 of audio group B channel status for channels 1 and 2.   |
| A62                  | ACSR1_2B_BYTE4_5   | ACSR1_2B_4     | 15:0 | RO  | 0           | Bytes 4 and 5 of audio group B channel status for channels 1 and 2.   |
| A63                  | ACSR1_2B_BYTE6_7   | ACSR1_2B_6     | 15:0 | RO  | 0           | Bytes 6 and 7 of audio group B channel status for channels 1 and 2.   |
| A64                  | ACSR1_2B_BYTE8_9   | ACSR1_2B_8     | 15:0 | RO  | 0           | Bytes 8 and 9 of audio group B channel status for channels 1 and 2.   |
| A65                  | ACSR1_2B_BYTE10_11 | ACSR1_2B_10    | 15:0 | RO  | 0           | Bytes 10 and 11 of audio group B channel status for channels 1 and 2. |
| A66                  | ACSR1_2B_BYTE12_13 | ACSR1_2B_12    | 15:0 | RO  | 0           | Bytes 12 and 13 of audio group B channel status for channels 1 and 2. |
| A67                  | ACSR1_2B_BYTE14_15 | ACSR1_2B_14    | 15:0 | RO  | 0           | Bytes 14 and 15 of audio group B channel status for channels 1 and 2. |
| A68                  | ACSR1_2B_BYTE16_17 | ACSR1_2B_16    | 15:0 | RO  | 0           | Bytes 16 and 17 of audio group B channel status for channels 1 and 2. |
| A69                  | ACSR1_2B_BYTE18_19 | ACSR1_2B_18    | 15:0 | RO  | 0           | Bytes 18 and 19 of audio group B channel status for channels 1 and 2. |
| A6A                  | ACSR1_2B_BYTE20_21 | ACSR1_2B_20    | 15:0 | RO  | 0           | Bytes 20 and 21 of audio group B channel status for channels 1 and 2. |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name      | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                                                    |
|----------------------|--------------------|----------------|------|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------|
| A6B                  | ACSR1_2B_BYTE22    | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |                    | ACSR1_2B_22    | 7:0  | RO  | 0           | Bytes 22 of audio group B channel status for channels 1 and 2.                                                                 |
| A6C to A6F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                                                                                      |
| A70                  | ACSR3_4B_BYTE0_1   | ACSR3_4B_0     | 15:0 | RO  | 0           | Bytes 0 and 1 of audio group B channel status for channels 3 and 4.                                                            |
| A71                  | ACSR3_4B_BYTE2_3   | ACSR3_4B_2     | 15:0 | RO  | 0           | Bytes 2 and 3 of audio group B channel status for channels 3 and 4.                                                            |
| A72                  | ACSR3_4B_BYTE4_5   | ACSR3_4B_4     | 15:0 | RO  | 0           | Bytes 4 and 5 of audio group B channel status for channels 3 and 4.                                                            |
| A73                  | ACSR3_4B_BYTE6_7   | ACSR3_4B_6     | 15:0 | RO  | 0           | Bytes 6 and 7 of audio group B channel status for channels 3 and 4.                                                            |
| A74                  | ACSR3_4B_BYTE8_9   | ACSR3_4B_8     | 15:0 | RO  | 0           | Bytes 8 and 9 of audio group B channel status for channels 3 and 4.                                                            |
| A75                  | ACSR3_4B_BYTE10_11 | ACSR3_4B_10    | 15:0 | RO  | 0           | Bytes 10 and 11 of audio group B channel status for channels 3 and 4.                                                          |
| A76                  | ACSR3_4B_BYTE12_13 | ACSR3_4B_12    | 15:0 | RO  | 0           | Bytes 12 and 13 of audio group B channel status for channels 3 and 4.                                                          |
| A77                  | ACSR3_4B_BYTE14_15 | ACSR3_4B_14    | 15:0 | RO  | 0           | Bytes 14 and 15 of audio group B channel status for channels 3 and 4.                                                          |
| A78                  | ACSR3_4B_BYTE16_17 | ACSR3_4B_16    | 15:0 | RO  | 0           | Bytes 16 and 17 of audio group B channel status for channels 3 and 4.                                                          |
| A79                  | ACSR3_4B_BYTE18_19 | ACSR3_4B_18    | 15:0 | RO  | 0           | Bytes 18 and 19 of audio group B channel status for channels 3 and 4.                                                          |
| A7A                  | ACSR3_4B_BYTE20_21 | ACSR3_4B_20    | 15:0 | RO  | 0           | Bytes 20 and 21 of audio group B channel status for channels 3 and 4.                                                          |
| A7B                  | ACSR3_4B_BYTE22    | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |                    | ACSR3_4B_22    | 7:0  | RO  | 0           | Bytes 22 of audio group B channel status for channels 3 and 4.                                                                 |
| A7C to A7F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                                                                                      |
| A80                  | ACSR_BYTE_0        | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |                    | ACSR0          | 7:0  | WO  | 0           | Byte 0 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A81                  | ACSR_BYTE_1        | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |                    | ACSR1          | 7:0  | WO  | 0           | Byte 1 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                                                    |
|----------------------|---------------|----------------|------|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------|
| A82                  | ACSR_BYTE_2   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR2          | 7:0  | WO  | 0           | Byte 2 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A83                  | ACSR_BYTE_3   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR3          | 7:0  | WO  | 0           | Byte 3 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A84                  | ACSR_BYTE_4   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR4          | 7:0  | WO  | 0           | Byte 4 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A85                  | ACSR_BYTE_5   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR5          | 7:0  | WO  | 0           | Byte 5 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A86                  | ACSR_BYTE_6   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR6          | 7:0  | WO  | 0           | Byte 6 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A87                  | ACSR_BYTE_7   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR7          | 7:0  | WO  | 0           | Byte 7 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A88                  | ACSR_BYTE_8   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR8          | 7:0  | WO  | 0           | Byte 8 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A89                  | ACSR_BYTE_9   | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                      |
|                      |               | ACSR9          | 7:0  | WO  | 0           | Byte 9 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                                                     |
|----------------------|---------------|----------------|------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------|
| A8A                  | ACSR_BYTE_10  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR10         | 7:0  | WO  | 0           | Byte 10 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A8B                  | ACSR_BYTE_11  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR11         | 7:0  | WO  | 0           | Byte 11 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A8C                  | ACSR_BYTE_12  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR12         | 7:0  | WO  | 0           | Byte 12 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A8D                  | ACSR_BYTE_13  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR13         | 7:0  | WO  | 0           | Byte 13 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A8E                  | ACSR_BYTE_14  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR14         | 7:0  | WO  | 0           | Byte 14 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A8F                  | ACSR_BYTE_15  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR15         | 7:0  | WO  | 0           | Byte 15 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A90                  | ACSR_BYTE_16  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR16         | 7:0  | WO  | 0           | Byte 16 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A91                  | ACSR_BYTE_17  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR17         | 7:0  | WO  | 0           | Byte 17 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |

**Table 5-9: HD and 3G Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                                                     |
|----------------------|---------------|----------------|------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------|
| A92                  | ACSR_BYTE_18  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR18         | 7:0  | WO  | 0           | Byte 18 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A93                  | ACSR_BYTE_19  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR19         | 7:0  | WO  | 0           | Byte 19 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A94                  | ACSR_BYTE_20  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR20         | 7:0  | WO  | 0           | Byte 20 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A95                  | ACSR_BYTE_21  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR21         | 7:0  | WO  | 0           | Byte 21 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A96                  | ACSR_BYTE_22  | RSVD           | 15:8 | —   | —           | Reserved.                                                                                                                       |
|                      |               | ACSR22         | 7:0  | WO  | 0           | Byte 22 of 22 audio channel status bytes to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. |
| A97 to A99           | RSVD          | RSVD           | 15:0 | —   | —           | Reserved.                                                                                                                       |

**Table 5-10: SD Audio Core CSR Descriptions**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit   | R/W | Reset Value | Description                                                                                                                                                                                                                                                                                                        |
|----------------------|---------------|----------------|-------|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B00                  | RSVD          | RSVD           | 15:0  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                          |
|                      |               | RSVD           | 15:14 | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                          |
|                      |               | ALL_DEL        | 13:13 | RW  | 0           | Selects deletion of all audio data and all audio control packets:<br>0 = Do not delete existing audio control packets<br>1 = Delete existing audio control packets                                                                                                                                                 |
|                      |               | MUTE_ALL       | 12:12 | RW  | 0           | Mute all output channels:<br>0 = Normal<br>1 = Muted                                                                                                                                                                                                                                                               |
|                      |               | ACS_USE_SECOND | 11:11 | RW  | 0           | Extract Audio Channel Status from second channel pair.                                                                                                                                                                                                                                                             |
|                      |               | CLEAR_AUDIO    | 10:10 | RW  | 0           | Clears all audio FIFO buffers and puts them in start-up state.                                                                                                                                                                                                                                                     |
|                      |               | OS_SEL         | 9:8   | RW  | 0           | Specifies the audio FIFO buffer size:<br>00 <sub>b</sub> = 36 samples deep, 26 sample start-up count<br>01 <sub>b</sub> = 22 samples deep, 12 sample start-up count<br>10 <sub>b</sub> = 16 samples deep, 6 sample start-up count<br>11 <sub>b</sub> = Reserved                                                    |
|                      |               | RSVD           | 7:4   | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                          |
|                      |               | IDB            | 3:2   | RW  | 1           | Specifies the Secondary audio group to extract:<br>00 <sub>b</sub> = Audio group #1<br>01 <sub>b</sub> = Audio group #2<br>10 <sub>b</sub> = Audio group #3<br>11 <sub>b</sub> = Audio group #4<br><br><b>Note:</b> Should IDA and IDB be set to the same value, they automatically revert to their default values |
|                      |               | IDA            | 1:0   | RW  | 0           | Specifies the Primary audio group to extract:<br>00 <sub>b</sub> = Audio group #1<br>01 <sub>b</sub> = Audio group #2<br>10 <sub>b</sub> = Audio group #3<br>11 <sub>b</sub> = Audio group #4<br><br><b>Note:</b> Should IDA and IDB be set to the same value, they automatically revert to their default values   |
| B01                  | CFG_AUD       |                |       |     |             |                                                                                                                                                                                                                                                                                                                    |
| B02                  | RSVD          | RSVD           | 15:0  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                          |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit   | R/W  | Reset Value | Description                                                                                                  |
|----------------------|---------------|----------------|-------|------|-------------|--------------------------------------------------------------------------------------------------------------|
| B03                  | DBN_ERR       | EXT_DET3_4B    | 15:15 | ROCW | 0           | Set when Secondary group channels 3 and 4 have extended data. Write 1 to clear.                              |
|                      |               | EXT_DET1_2B    | 14:14 | ROCW | 0           | Set when Secondary group channels 1 and 2 have extended data. Write 1 to clear.                              |
|                      |               | EXT_DET3_4A    | 13:13 | ROCW | 0           | Set when Primary group channels 3 and 4 have extended data. Write 1 to clear                                 |
|                      |               | EXT_DET1_2A    | 12:12 | ROCW | 0           | Set when Primary group channels 1 and 2 have extended data. Write 1 to clear                                 |
|                      |               | CTL_DBNB_ERR   | 11:11 | ROCW | 0           | Set when Secondary group control packet Data Block Number sequence is discontinuous. Write 1 to clear        |
|                      |               | CTL_DBNA_ERR   | 10:10 | ROCW | 0           | Set when Primary group control packet Data Block Number sequence is discontinuous. Write 1 to clear.         |
|                      |               | EXT_DBNB_ERR   | 9:9   | ROCW | 0           | Set when Secondary group extended data packet Data Block Number sequence is discontinuous. Write 1 to clear. |
|                      |               | EXT_DBNA_ERR   | 8:8   | ROCW | 0           | Set when Primary group extended data packet Data Block Number sequence is discontinuous. Write 1 to clear.   |
|                      |               | SAMP_DBNB_ERR  | 7:7   | ROCW | 0           | Set when Secondary group data packet Data Block Number sequence is discontinuous. Write 1 to clear.          |
|                      |               | SAMP_DBNA_ERR  | 6:6   | ROCW | 0           | Set when Primary group data packet Data Block Number sequence is discontinuous. Write 1 to clear.            |
|                      |               | CTRB_DET       | 5:5   | ROCW | 0           | Set when Secondary group audio control packet is detected. Write 1 to clear.                                 |
|                      |               | CTRA_DET       | 4:4   | ROCW | 0           | Set when Primary group audio control packet is detected. Write 1 to clear.                                   |
|                      |               | ACS_DET3_4B    | 3:3   | ROCW | 0           | Secondary group audio status detected for channels 3 and 4. Write 1 to clear.                                |
|                      |               | ACS_DET1_2B    | 2:2   | ROCW | 0           | Secondary group audio status detected for channels 1 and 2. Write 1 to clear.                                |
|                      |               | ACS_DET3_4A    | 1:1   | ROCW | 0           | Primary group audio status detected for channels 3 and 4. Write 1 to clear.                                  |
|                      |               | ACS_DET1_2A    | 0:0   | ROCW | 0           | Primary group audio status detected for channels 1 and 2. Write 1 to clear.                                  |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W | Reset Value | Description                                                                                                                                                                       |
|----------------------|---------------|----------------|------|-----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B04                  | REGEN         | RSVD           | 15:2 | —   | —           | Reserved.                                                                                                                                                                         |
|                      |               | ACS_APPLY      | 1:1  | RW  | 0           | Causes channel status data in ACSR[183:0] to be transferred to the channel status replacement mechanism. The transfer does not occur until the next status boundary.              |
|                      |               | ACS_REGEN      | 0:0  | RW  | 0           | Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field:<br>0 = Do not replace Channel Status<br>1 = Replace Channel Status of all channels |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name  | Bit   | R/W  | Reset Value | Description                                                                                        |
|----------------------|---------------|-----------------|-------|------|-------------|----------------------------------------------------------------------------------------------------|
| B05                  | AUD_DET       | IDB_READBACK    | 15:14 | RO   | 1           | Actual value of IDB in the hardware.                                                               |
|                      |               | IDA_READBACK    | 13:12 | RO   | 0           | Actual value of IDA in the hardware.                                                               |
|                      |               | XDPG4_DET       | 11:11 | RO   | 0           | Set while embedded Group 4 audio extended packets are detected.                                    |
|                      |               | XDPG3_DET       | 10:10 | RO   | 0           | Set while embedded Group 3 audio extended packets are detected.                                    |
|                      |               | XDPG2_DET       | 9:9   | RO   | 0           | Set while embedded Group 2 audio extended packets are detected.                                    |
|                      |               | XDPG1_DET       | 8:8   | RO   | 0           | Set while embedded Group 1 audio extended packets are detected.                                    |
|                      |               | ADPG4_DET       | 7:7   | RO   | 0           | Set while Group 4 audio data packets are detected.                                                 |
|                      |               | ADPG3_DET       | 6:6   | RO   | 0           | Set while Group 3 audio data packets are detected.                                                 |
|                      |               | ADPG2_DET       | 5:5   | RO   | 0           | Set while Group 2 audio data packets are detected.                                                 |
|                      |               | ADPG1_DET       | 4:4   | RO   | 0           | Set while Group 1 audio data packets are detected.                                                 |
|                      |               | ACS_APPLY_WAITD | 3:3   | RO   | 0           | Set while output channels 7 and 8 are waiting for a status boundary to apply the ACSR[183:0] data. |
|                      |               | ACS_APPLY_WAITC | 2:2   | RO   | 0           | Set while output channels 5 and 6 are waiting for a status boundary to apply the ACSR[183:0] data  |
|                      |               | ACS_APPLY_WAITB | 1:1   | RO   | 0           | Set while output channels 3 and 4 are waiting for a status boundary to apply the ACSR[183:0] data  |
|                      |               | ACS_APPLY_WAITA | 0:0   | RO   | 0           | Set while output channels 1 and 2 are waiting for a status boundary to apply the ACSR[183:0] data  |
| B06                  | CSUM_ERR_DET  | RSVD            | 15:1  | —    | —           | Reserved.                                                                                          |
|                      |               | CSUM_ERROR      | 0:0   | ROCW | 0           | Embedded packet checksum error detected. Write 1 to clear.                                         |
| B07                  | CH_MUTE       | RSVD            | 15:8  | —    | —           | Reserved.                                                                                          |
|                      |               | MUTE            | 7:0   | RW   | 0           | Mutes output channels 8 to 1 Bits [7:0] = Channels 8:1.<br>0 = Normal<br>1 = Mute                  |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit  | R/W | Reset Value | Description                                     |
|----------------------|---------------|----------------|------|-----|-------------|-------------------------------------------------|
| B08                  | CH_VALID      | RSVD           | 15:8 | —   | —           | Reserved.                                       |
|                      |               | CH4_VALIDB     | 7:7  | RO  | 0           | Secondary group channel 4 sample validity flag. |
|                      |               | CH3_VALIDB     | 6:6  | RO  | 0           | Secondary group channel 3 sample validity flag. |
|                      |               | CH2_VALIDB     | 5:5  | RO  | 0           | Secondary group channel 2 sample validity flag. |
|                      |               | CH1_VALIDB     | 4:4  | RO  | 0           | Secondary group channel 1 sample validity flag. |
|                      |               | CH4_VALIDA     | 3:3  | RO  | 0           | Primary group channel 4 sample validity flag.   |
|                      |               | CH3_VALIDA     | 2:2  | RO  | 0           | Primary group channel 3 sample validity flag.   |
|                      |               | CH2_VALIDA     | 1:1  | RO  | 0           | Primary group channel 2 sample validity flag.   |
|                      |               | CH1_VALIDA     | 0:0  | RO  | 0           | Primary group channel 1 sample validity flag.   |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit   | R/W | Reset Value | Description                                           |
|----------------------|---------------|----------------|-------|-----|-------------|-------------------------------------------------------|
| B09                  | INT_ENABLE    | RSVD           | 15:15 | —   | —           | Reserved.                                             |
|                      |               | EN_NOT_LOCKED  | 14:14 | RW  | 0           | Asserts interrupt when LOCKED signal is not asserted. |
|                      |               | EN_NO_VIDEO    | 13:13 | RW  | 0           | Asserts interrupt when video format is unknown.       |
|                      |               | EN_CSUM_ERROR  | 12:12 | RW  | 0           | Asserts interrupt when checksum error is detected.    |
|                      |               | EN_ACS_DET3_4B | 11:11 | RW  | 0           | Asserts interrupt when ACS_DET3_4B flag is set.       |
|                      |               | EN_ACS_DET1_2B | 10:10 | RW  | 0           | Asserts interrupt when ACS_DET1_2B flag is set.       |
|                      |               | EN_ACS_DET3_4A | 9:9   | RW  | 0           | Asserts interrupt when ACS_DET3_4A flag is set.       |
|                      |               | EN_ACS_DET1_2A | 8:8   | RW  | 0           | Asserts interrupt when ACS_DET1_2A flag is set.       |
|                      |               | EN_CTRB_DET    | 7:7   | RW  | 0           | Asserts interrupt when CTRB_DET flag is set.          |
|                      |               | EN_CTRA_DET    | 6:6   | RW  | 0           | Asserts interrupt when CTRA_DET flag is set.          |
|                      |               | EN_DBNB_ERR    | 5:5   | RW  | 0           | Asserts interrupt when DBNB_ERR flag is set.          |
|                      |               | EN_DBNA_ERR    | 4:4   | RW  | 0           | Asserts interrupt when DBNA_ERR flag is set.          |
|                      |               | EN_ADPG4_DET   | 3:3   | RW  | 0           | Asserts interrupt when ADPG4_DET flag is set.         |
|                      |               | EN_ADPG3_DET   | 2:2   | RW  | 0           | Asserts interrupt when ADPG3_DET flag is set.         |
|                      |               | EN_ADPG2_DET   | 1:1   | RW  | 0           | Asserts interrupt when ADPG2_DET flag is set.         |
|                      |               | EN_ADPG1_DET   | 0:0   | RW  | 0           | Asserts interrupt when ADPG1_DET flag is set.         |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name | Parameter Name | Bit   | R/W | Reset Value | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------------|---------------|----------------|-------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BOA                  | CFG_OUTPUT    | ASWLD          | 15:14 | RW  | 3           | Output channels 7 and 8 word length:<br>00 <sub>b</sub> = 24 bits<br>01 <sub>b</sub> = 20 bits<br>10 <sub>b</sub> = 16 bits<br>11 <sub>b</sub> = Automatic 20-bit or 24-bit                                                                                                                                                                                                                                                                                               |
|                      |               | ASWLC          | 13:12 | RW  | 3           | Output channels 5 and 6 word length. See ASWLD for decoding.                                                                                                                                                                                                                                                                                                                                                                                                              |
|                      |               | ASWLB          | 11:10 | RW  | 3           | Output channels 3 and 4 word length. See ASWLD for decoding.                                                                                                                                                                                                                                                                                                                                                                                                              |
|                      |               | ASWLA          | 9:8   | RW  | 3           | Output channels 1 and 2 word length. See ASWLD for decoding.                                                                                                                                                                                                                                                                                                                                                                                                              |
|                      |               | AMD            | 7:6   | RW  | 3           | Output channels 7 and 8 format selector:<br>00 <sub>b</sub> = AES/EBU audio output<br>01 <sub>b</sub> = Serial audio output. Left justified; MSB first<br>10 <sub>b</sub> = Serial audio output. Right justified; MSB first<br>11 <sub>b</sub> = I <sup>2</sup> S serial audio output                                                                                                                                                                                     |
|                      |               | AMC            | 5:4   | RW  | 3           | Output channels 5 and 6 format selector. See AMD for decoding.                                                                                                                                                                                                                                                                                                                                                                                                            |
|                      |               | AMB            | 3:2   | RW  | 3           | Output channels 3 and 4 format selector. See AMD for decoding.                                                                                                                                                                                                                                                                                                                                                                                                            |
|                      |               | AMA            | 1:0   | RW  | 3           | Output channels 1 and 2 format selector. See AMD for decoding.                                                                                                                                                                                                                                                                                                                                                                                                            |
|                      |               | RSVD           | 15:12 | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| BOB                  | OUTPUT_SEL_1  | OP4_SRC        | 11:9  | RW  | 3           | Output channel 4 source selector:<br>000 <sub>b</sub> = Primary audio group channel 1<br>001 <sub>b</sub> = Primary audio group channel 2<br>010 <sub>b</sub> = Primary audio group channel 3<br>011 <sub>b</sub> = Primary audio group channel 4<br>100 <sub>b</sub> = Secondary audio group channel 1<br>101 <sub>b</sub> = Secondary audio group channel 2<br>110 <sub>b</sub> = Secondary audio group channel 3<br>111 <sub>b</sub> = Secondary audio group channel 4 |
|                      |               | OP3_SRC        | 8:6   | RW  | 2           | Output channel 3 source selector. See OP4_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |               | OP2_SRC        | 5:3   | RW  | 1           | Output channel 2 source selector. See OP4_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |               | OP1_SRC        | 2:0   | RW  | 0           | Output channel 1 source selector. See OP4_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name    | Parameter Name | Bit   | R/W | Reset Value | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------------|------------------|----------------|-------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B0C                  | OUTPUT_SEL_2     | RSVD           | 15:12 | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |                  | OP8_SRC        | 11:9  | RW  | 7           | Output channel 8 source selector:<br>000 <sub>b</sub> = Primary audio group channel 1<br>001 <sub>b</sub> = Primary audio group channel 2<br>010 <sub>b</sub> = Primary audio group channel 3<br>011 <sub>b</sub> = Primary audio group channel 4<br>100 <sub>b</sub> = Secondary audio group channel 1<br>101 <sub>b</sub> = Secondary audio group channel 2<br>110 <sub>b</sub> = Secondary audio group channel 3<br>111 <sub>b</sub> = Secondary audio group channel 4 |
|                      |                  | OP7_SRC        | 8:6   | RW  | 6           | Output channel 7 source selector. See OP8_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |                  | OP6_SRC        | 5:3   | RW  | 5           | Output channel 6 source selector. See OP8_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |
|                      |                  | OP5_SRC        | 2:0   | RW  | 4           | Output channel 5 source selector. See OP8_SRC for decoding.                                                                                                                                                                                                                                                                                                                                                                                                               |
| B0D to B1F           | RSVD             | RSVD           | 15:0  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| B20                  | AFNA12           | RSVD           | 15:9  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |                  | AFN1_2A        | 8:0   | RO  | 0           | Primary group audio frame number for channels 1 and 2.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| B21                  | AFNA34           | RSVD           | 15:9  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |                  | AFN3_4A        | 8:0   | RO  | 0           | Primary group audio frame number for channels 3 and 4.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| B22                  | RATEA            | RSVD           | 15:8  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |                  | RATE3_4A       | 7:5   | RO  | 0           | Primary group sampling frequency for channels 3 and 4.                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                      |                  | ASX3_4A        | 4:4   | RO  | 0           | Primary group asynchronous mode for channels 3 and 4.                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                      |                  | RATE1_2A       | 3:1   | RO  | 0           | Primary group sampling frequency for channels 1 and 2.                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                      |                  | ASX1_2A        | 0:0   | RO  | 0           | Primary group asynchronous mode for channels 1 and 2.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| B23                  | ACT_A            | RSVD           | 15:4  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |                  | ACTA           | 3:0   | RO  | 0           | Primary group active channels.                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| B24                  | PRIM_AUD_DELAY_1 | RSVD           | 15:9  | —   | —           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                      |                  | DEL1A_1        | 8:1   | RO  | 0           | Primary Audio group delay data for channel 1.                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                      |                  | EBIT1A         | 0:0   | RO  | 0           | Primary Audio group delay data valid flag for channel 1.                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name     | Parameter Name | Bit  | R/W | Reset Value | Description                                              |
|----------------------|-------------------|----------------|------|-----|-------------|----------------------------------------------------------|
| B25                  | PRIM_AUD_DELAY_2  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL1A_2        | 8:0  | RO  | 0           | Primary Audio group delay data for channel 1.            |
| B26                  | PRIM_AUD_DELAY_3  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL1A_3        | 8:0  | RO  | 0           | Primary Audio group delay data for channel 1.            |
| B27                  | PRIM_AUD_DELAY_4  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL2A_4        | 8:1  | RO  | 0           | Primary Audio group delay data for channel 2.            |
|                      |                   | EBIT2A         | 0    | RO  | 0           | Primary Audio group delay data valid flag for channel 2. |
| B28                  | PRIM_AUD_DELAY_5  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL2A_5        | 8:0  | RO  | 0           | Primary Audio group delay data for channel 2.            |
| B29                  | PRIM_AUD_DELAY_6  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL2A_6        | 8:0  | RO  | 0           | Primary Audio group delay data for channel 2.            |
| B2A                  | PRIM_AUD_DELAY_7  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL3A_7        | 8:1  | RO  | 0           | Primary Audio group delay data for channel 3.            |
|                      |                   | EBIT3A         | 0    | RO  | 0           | Primary Audio group delay data valid flag for channel 3. |
| B2B                  | PRIM_AUD_DELAY_8  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL3A_8        | 8:0  | RO  | 0           | Primary Audio group delay data for channel 3.            |
| B2C                  | PRIM_AUD_DELAY_9  | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL3A_9        | 8:0  | RO  | 0           | Primary Audio group delay data for channel 3.            |
| B2D                  | PRIM_AUD_DELAY_10 | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL4A_10       | 8:1  | RO  | 0           | Primary Audio group delay data for channel 4.            |
|                      |                   | EBIT4A         | 0:0  | RO  | 0           | Primary Audio group delay data valid flag for channel 4. |
| B2E                  | PRIM_AUD_DELAY_11 | RSVD           | 15:9 | —   | —           | Reserved.                                                |
|                      |                   | DEL4A_11       | 8:0  | RO  | 0           | Primary Audio group delay data for channel 4.            |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name     | Parameter Name | Bit  | R/W | Reset Value | Description                                                |
|----------------------|-------------------|----------------|------|-----|-------------|------------------------------------------------------------|
| B2F                  | PRIM_AUD_DELAY_12 | RSVD           | 15:9 | —   | —           | Reserved.                                                  |
|                      |                   | DEL4A_12       | 8:0  | RO  | 0           | Primary Audio group delay data for channel 4.              |
| B30                  | AFNB12            | RSVD           | 15:9 | —   | —           | Reserved.                                                  |
|                      |                   | AFN1_2B        | 8:0  | RO  | 0           | Secondary group audio frame number for channels 1 and 2.   |
| B31                  | AFNB34            | RSVD           | 15:9 | —   | —           | Reserved.                                                  |
|                      |                   | AFN3_4B        | 8:0  | RO  | 0           | Secondary group audio frame number for channels 3 and 4.   |
| B32                  | RATEB             | RSVD           | 15:8 | —   | —           | Reserved.                                                  |
|                      |                   | RATE3_4B       | 7:5  | RO  | 0           | Secondary group sampling frequency for channels 3 and 4.   |
|                      |                   | ASX3_4B        | 4:4  | RO  | 0           | Secondary group asynchronous mode for channels 3 and 4.    |
|                      |                   | RATE1_2B       | 3:1  | RO  | 0           | Secondary group sampling frequency for channels 1 and 2.   |
|                      |                   | ASXB           | 0:0  | RO  | 0           | Secondary group asynchronous mode for channels 1 and 2.    |
| B33                  | ACT_B             | RSVD           | 15:4 | —   | —           | Reserved.                                                  |
|                      |                   | ACTB           | 3:0  | RO  | 0           | Secondary group active channels.                           |
| B34                  | SEC_AUD_DELAY_1   | RSVD           | 15:9 | —   | —           | Reserved.                                                  |
|                      |                   | DEL1B_1        | 8:1  | RO  | 0           | Secondary Audio group delay data for channel 1.            |
|                      |                   | EBIT1B         | 0:0  | RO  | 0           | Secondary Audio group delay data valid flag for channel 1. |
| B35                  | SEC_AUD_DELAY_2   | RSVD           | 15:9 | —   | —           | Reserved.                                                  |
|                      |                   | DEL1B_2        | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 1.            |
| B36                  | SEC_AUD_DELAY_3   | RSVD           | 15:9 | —   | —           | Reserved.                                                  |
|                      |                   | DEL1B_3        | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 1.            |
| B37                  | SEC_AUD_DELAY_4   | RSVD           | 15:9 | —   | —           | Reserved.                                                  |
|                      |                   | DEL2B_4        | 8:1  | RO  | 0           | Secondary Audio group delay data for channel 2.            |
|                      |                   | EBIT2B         | 0:0  | RO  | 0           | Secondary Audio group delay data valid flag for channel 2. |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name    | Parameter Name | Bit  | R/W | Reset Value | Description                                                                      |
|----------------------|------------------|----------------|------|-----|-------------|----------------------------------------------------------------------------------|
| B38                  | SEC_AUD_DELAY_5  | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL2B_5        | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 2.                                  |
| B39                  | SEC_AUD_DELAY_6  | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL2B_6        | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 2.                                  |
| B3A                  | SEC_AUD_DELAY_7  | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL3B_7        | 8:1  | RO  | 0           | Secondary Audio group delay data for channel 3.                                  |
|                      |                  | EBIT3B         | 0    | RO  | 0           | Secondary Audio group delay data valid flag for channel 3.                       |
| B3B                  | SEC_AUD_DELAY_8  | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL3B_8        | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 3.                                  |
| B3C                  | SEC_AUD_DELAY_9  | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL3B_9        | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 3.                                  |
| B3D                  | SEC_AUD_DELAY_10 | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL4B_10       | 8:1  | RO  | 0           | Secondary Audio group delay data for channel 4.                                  |
|                      |                  | EBIT4B         | 0    | RO  | 0           | Secondary Audio group delay data valid flag for channel 4.                       |
| B3E                  | SEC_AUD_DELAY_11 | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL4B_11       | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 4.                                  |
| B3F                  | SEC_AUD_DELAY_12 | RSVD           | 15:9 | —   | —           | Reserved.                                                                        |
|                      |                  | DEL4B_12       | 8:0  | RO  | 0           | Secondary Audio group delay data for channel 4.                                  |
| B40                  | ACSR1_2A_BYTE0_1 | ACSR1_2A_0     | 15:0 | RO  | 0           | Bytes 0 [7:0] and 1 [15:8] of audio group A channel status for channels 1 and 2. |
| B41                  | ACSR1_2A_BYTE2_3 | ACSR1_2A_2     | 15:0 | RO  | 0           | Bytes 2 [7:0] and 3 [15:8] of audio group A channel status for channels 1 and 2. |
| B42                  | ACSR1_2A_BYTE4_5 | ACSR1_2A_4     | 15:0 | RO  | 0           | Bytes 4 [7:0] and 5 [15:8] of audio group A channel status for channels 1 and 2. |
| B43                  | ACSR1_2A_BYTE6_7 | ACSR1_2A_6     | 15:0 | RO  | 0           | Bytes 6 [7:0] and 7 [15:8] of audio group A channel status for channels 1 and 2. |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name      | Parameter Name | Bit  | R/W | Reset Value | Description                                                                        |
|----------------------|--------------------|----------------|------|-----|-------------|------------------------------------------------------------------------------------|
| B44                  | ACSR1_2A_BYTE8_9   | ACSR1_2A_8     | 15:0 | RO  | 0           | Bytes 8 [7:0] and 9 [15:8] of audio group A channel status for channels 1 and 2.   |
| B45                  | ACSR1_2A_BYTE10_11 | ACSR1_2A_10    | 15:0 | RO  | 0           | Bytes 10 [7:0] and 11 [15:8] of audio group A channel status for channels 1 and 2. |
| B46                  | ACSR1_2A_BYTE12_13 | ACSR1_2A_12    | 15:0 | RO  | 0           | Bytes 12 [7:0] and 13 [15:8] of audio group A channel status for channels 1 and 2. |
| B47                  | ACSR1_2A_BYTE14_15 | ACSR1_2A_14    | 15:0 | RO  | 0           | Bytes 14 [7:0] and 15 [15:8] of audio group A channel status for channels 1 and 2. |
| B48                  | ACSR1_2A_BYTE16_17 | ACSR1_2A_16    | 15:0 | RO  | 0           | Bytes 16 [7:0] and 17 [15:8] of audio group A channel status for channels 1 and 2. |
| B49                  | ACSR1_2A_BYTE18_19 | ACSR1_2A_18    | 15:0 | RO  | 0           | Bytes 18 [7:0] and 19 [15:8] of audio group A channel status for channels 1 and 2. |
| B4A                  | ACSR1_2A_BYTE20_21 | ACSR1_2A_20    | 15:0 | RO  | 0           | Bytes 20 [7:0] and 21 [15:8] of audio group A channel status for channels 1 and 2. |
| B4B                  | ACSR1_2A_BYTE22    | RSVD           | 15:8 | —   | —           | Reserved.                                                                          |
|                      |                    | ACSR1_2A_22    | 7:0  | RO  | 0           | Bytes 22 of audio group A channel status for channels 1 and 2.                     |
| B4C to B4F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                                          |
| B50                  | ACSR3_4A_BYTE0_1   | ACSR3_4A_0     | 15:0 | RO  | 0           | Bytes 0 [7:0] and 1 [15:8] of audio group A channel status for channels 3 and 4.   |
| B51                  | ACSR3_4A_BYTE2_3   | ACSR3_4A_2     | 15:0 | RO  | 0           | Bytes 2 [7:0] and 3 [15:8] of audio group A channel status for channels 3 and 4.   |
| B52                  | ACSR3_4A_BYTE4_5   | ACSR3_4A_4     | 15:0 | RO  | 0           | Bytes 4 [7:0] and 5 [15:8] of audio group A channel status for channels 3 and 4.   |
| B53                  | ACSR3_4A_BYTE6_7   | ACSR3_4A_6     | 15:0 | RO  | 0           | Bytes 6 [7:0] and 7 [15:8] of audio group A channel status for channels 3 and 4.   |
| B54                  | ACSR3_4A_BYTE8_9   | ACSR3_4A_8     | 15:0 | RO  | 0           | Bytes 8 [7:0] and 9 [15:8] of audio group A channel status for channels 3 and 4.   |
| B55                  | ACSR3_4A_BYTE10_11 | ACSR3_4A_10    | 15:0 | RO  | 0           | Bytes 10 [7:0] and 11 [15:8] of audio group A channel status for channels 3 and 4. |
| B56                  | ACSR3_4A_BYTE12_13 | ACSR3_4A_12    | 15:0 | RO  | 0           | Bytes 12 [7:0] and 13 [15:8] of audio group A channel status for channels 3 and 4. |
| B57                  | ACSR3_4A_BYTE14_15 | ACSR3_4A_14    | 15:0 | RO  | 0           | Bytes 14 [7:0] and 15 [15:8] of audio group A channel status for channels 3 and 4. |
| B58                  | ACSR3_4A_BYTE16_17 | ACSR3_4A_16    | 15:0 | RO  | 0           | Bytes 16 [7:0] and 17 [15:8] of audio group A channel status for channels 3 and 4. |

**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name      | Parameter Name | Bit  | R/W | Reset Value | Description                                                                        |
|----------------------|--------------------|----------------|------|-----|-------------|------------------------------------------------------------------------------------|
| B59                  | ACSR3_4A_BYTE18_19 | ACSR3_4A_18    | 15:0 | RO  | 0           | Bytes 18 [7:0] and 19 [15:8] of audio group A channel status for channels 3 and 4. |
| B5A                  | ACSR3_4A_BYTE20_21 | ACSR3_4A_20    | 15:0 | RO  | 0           | Bytes 20 [7:0] and 21 [15:8] of audio group A channel status for channels 3 and 4. |
| B5B                  | ACSR3_4A_BYTE22    | RSVD           | 15:8 | —   | —           | Reserved.                                                                          |
|                      |                    | ACSR3_4A_22    | 7:0  | RO  | 0           | Bytes 22 of audio group A channel status for channels 3 and 4.                     |
| B5C to B5F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                                          |
| B60                  | ACSR1_2B_BYTE0_1   | ACSR1_2B_0     | 15:0 | RO  | 0           | Bytes 0 [7:0] and 1 [15:8] of audio group B channel status for channels 1 and 2.   |
| B61                  | ACSR1_2B_BYTE2_3   | ACSR1_2B_2     | 15:0 | RO  | 0           | Bytes 2 [7:0] and 3 [15:8] of audio group B channel status for channels 1 and 2.   |
| B62                  | ACSR1_2B_BYTE4_5   | ACSR1_2B_4     | 15:0 | RO  | 0           | Bytes 4 [7:0] and 5 [15:8] of audio group B channel status for channels 1 and 2.   |
| B63                  | ACSR1_2B_BYTE6_7   | ACSR1_2B_6     | 15:0 | RO  | 0           | Bytes 6 [7:0] and 7 [15:8] of audio group B channel status for channels 1 and 2.   |
| B64                  | ACSR1_2B_BYTE8_9   | ACSR1_2B_8     | 15:0 | RO  | 0           | Bytes 8 [7:0] and 9 [15:8] of audio group B channel status for channels 1 and 2.   |
| B65                  | ACSR1_2B_BYTE10_11 | ACSR1_2B_10    | 15:0 | RO  | 0           | Bytes 10 [7:0] and 11 [15:8] of audio group B channel status for channels 1 and 2. |
| B66                  | ACSR1_2B_BYTE12_13 | ACSR1_2B_12    | 15:0 | RO  | 0           | Bytes 12 [7:0] and 13 [15:8] of audio group B channel status for channels 1 and 2. |
| B67                  | ACSR1_2B_BYTE14_15 | ACSR1_2B_14    | 15:0 | RO  | 0           | Bytes 14 [7:0] and 15 [15:8] of audio group B channel status for channels 1 and 2. |
| B68                  | ACSR1_2B_BYTE16_17 | ACSR1_2B_16    | 15:0 | RO  | 0           | Bytes 16 [7:0] and 17 [15:8] of audio group B channel status for channels 1 and 2. |
| B69                  | ACSR1_2B_BYTE18_19 | ACSR1_2B_18    | 15:0 | RO  | 0           | Bytes 18 [7:0] and 19 [15:8] of audio group B channel status for channels 1 and 2. |
| B6A                  | ACSR1_2B_BYTE20_21 | ACSR1_2B_20    | 15:0 | RO  | 0           | Bytes 20 [7:0] and 21 [15:8] of audio group B channel status for channels 1 and 2. |
| B6B                  | ACSR1_2B_BYTE22    | RSVD           | 15:8 | —   | —           | Reserved.                                                                          |
|                      |                    | ACSR1_2B_22    | 7:0  | RO  | 0           | Byte 22 of audio group B channel status for channels 1 and 2.                      |
| B6C to B6F           | RSVD               | RSVD           | 15:0 | —   | —           | Reserved.                                                                          |
| B70                  | ACSR3_4B_BYTE0_1   | ACSR3_4B_0     | 15:0 | RO  | 0           | Bytes 0 [7:0] and 1 [15:8] of audio group B channel status for channels 3 and 4.   |

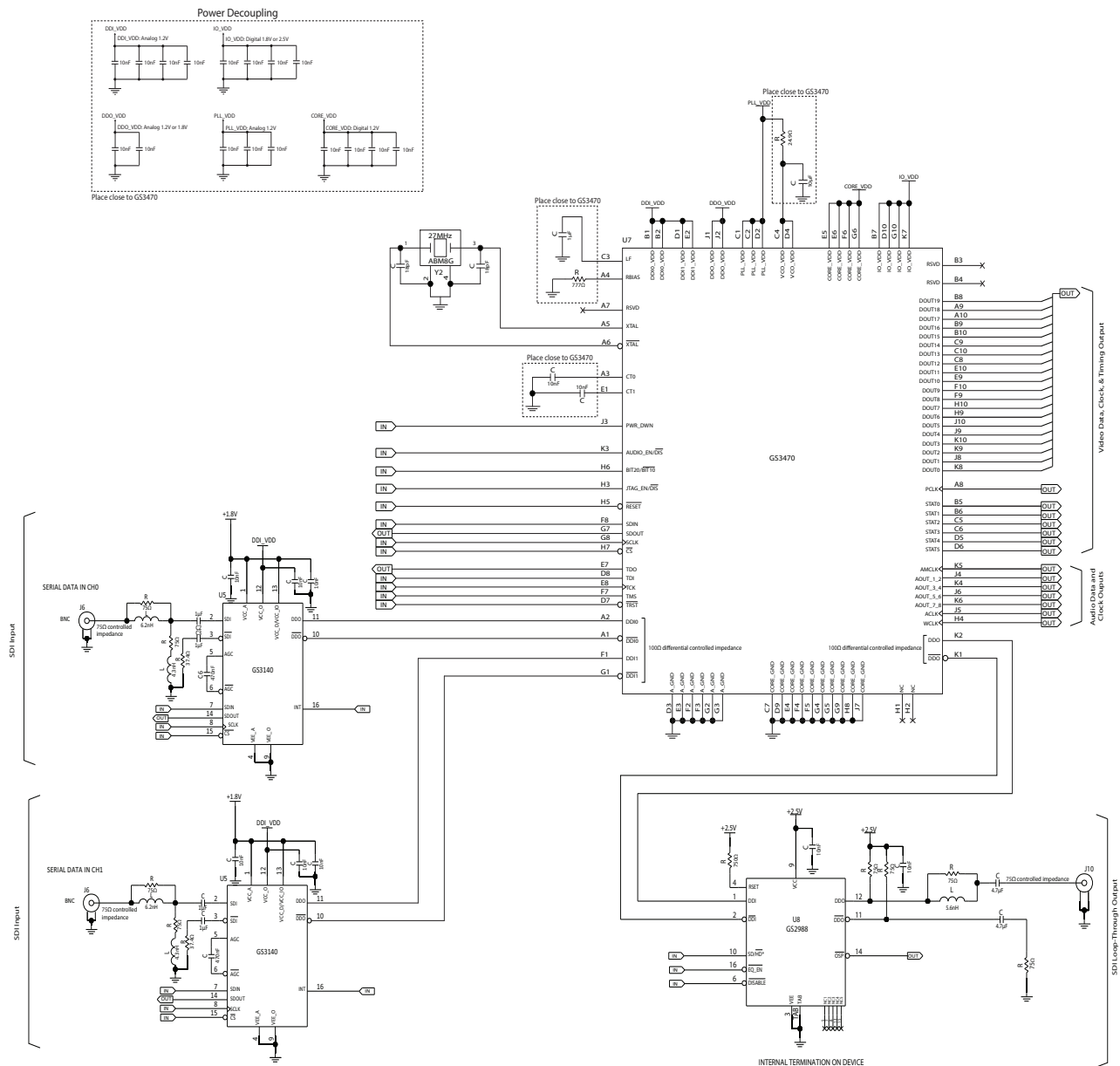
**Table 5-10: SD Audio Core CSR Descriptions (Continued)**

| Address <sub>h</sub> | Register Name               | Parameter Name            | Bit  | R/W | Reset Value | Description                                                                                                                                       |
|----------------------|-----------------------------|---------------------------|------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| B71                  | ACSR3_4B_BYTE2_3            | ACSR3_4B_2                | 15:0 | RO  | 0           | Bytes 2 [7:0] and 3 [15:8] of audio group B channel status for channels 3 and 4.                                                                  |
| B72                  | ACSR3_4B_BYTE4_5            | ACSR3_4B_4                | 15:0 | RO  | 0           | Bytes 4 [7:0] and 5 [15:8] of audio group B channel status for channels 3 and 4.                                                                  |
| B73                  | ACSR3_4B_BYTE6_7            | ACSR3_4B_6                | 15:0 | RO  | 0           | Bytes 6 [7:0] and 7 [15:8] of audio group B channel status for channels 3 and 4.                                                                  |
| B74                  | ACSR3_4B_BYTE8_9            | ACSR3_4B_8                | 15:0 | RO  | 0           | Bytes 8 [7:0] and 9 [15:8] of audio group B channel status for channels 3 and 4.                                                                  |
| B75                  | ACSR3_4B_BYTE10_11          | ACSR3_4B_10               | 15:0 | RO  | 0           | Bytes 10 [7:0] and 11 [15:8] of audio group B channel status for channels 3 and 4.                                                                |
| B76                  | ACSR3_4B_BYTE12_13          | ACSR3_4B_12               | 15:0 | RO  | 0           | Bytes 12 [7:0] and 13 [15:8] of audio group B channel status for channels 3 and 4.                                                                |
| B77                  | ACSR3_4B_BYTE14_15          | ACSR3_4B_14               | 15:0 | RO  | 0           | Bytes 14 [7:0] and 15 [15:8] of audio group B channel status for channels 3 and 4.                                                                |
| B78                  | ACSR3_4B_BYTE16_17          | ACSR3_4B_16               | 15:0 | RO  | 0           | Bytes 16 [7:0] and 17 [15:8] of audio group B channel status for channels 3 and 4.                                                                |
| B79                  | ACSR3_4B_BYTE18_19          | ACSR3_4B_18               | 15:0 | RO  | 0           | Bytes 18 [7:0] and 19 [15:8] of audio group B channel status for channels 3 and 4.                                                                |
| B7A                  | ACSR3_4B_BYTE20_21          | ACSR3_4B_20               | 15:0 | RO  | 0           | Bytes 20 [7:0] and 21 [15:8] of audio group B channel status for channels 3 and 4.                                                                |
| B7B                  | ACSR3_4B_BYTE22             | ACSR3_4B_22               | 7:0  | RO  | 0           | Byte 22 of audio group B channel status for channels 3 and 4.                                                                                     |
| B7C to B7F           | RSVD                        | RSVD                      | 15:0 | —   | —           | Reserved.                                                                                                                                         |
|                      | RSVD                        | RSVD                      | 15:8 | —   | —           | Reserved.                                                                                                                                         |
| B80 to B96           | ACSR_BYTE_0 to ACSR_BYTE_22 | ACSR_BYTE0 to ACSR_BYTE22 | 7:0  | WO  | 0           | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register for 23 registers. |
| B97                  | RSVD                        | RSVD                      | 15:0 | —   | —           | Reserved.                                                                                                                                         |

**Table 5-11: ANC Extraction FIFO Access CSR Descriptions**

| Address <sub>h</sub> | Register Name                  | Parameter Name                 | Bit  | R/W | Reset Value | Description                                                                                                                                                                                                                                                                                     |
|----------------------|--------------------------------|--------------------------------|------|-----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C00 to FFF           | ANC_FIFO_0 to<br>ANC_FIFO_1023 | ANC_FIFO_0 to<br>ANC_FIFO_1023 | 15:0 | RO  | 0           | <p>Top of the ANC FIFO. Register addresses shared with the bottom of the ANC FIFO registers.</p> <p>ANC_DATA_SWITCH (817<sub>h</sub>) is used to switch between the top and bottom registers of the ANC FIFO.</p> <p>Please refer to the <a href="#">4.18.10 Ancillary Data Extraction</a>.</p> |

## 6.1 Typical Application Circuit



### Figure 6-1: Typical Application Circuit

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## 6.2 Layout Considerations

General best practices for high-speed board layout should be followed when designing with the GS3470. These general best practices can be found in a number of Semtech design guides including:

- GS3471 Receiver Design Guide (TBD)
- GS2972 Transmitter Design Guide (GENDOC-048581)
- Multi-Gigabit Serial Routing Products (PDS-060967)
- GS2989 Cable Driver Design Guide (GENDOC-052070) or most recent CD design guide available

The following layout considerations are specific to the GS3470:

- GS3470's analog supplies, particularly its 1.2V VCC supply, are sensitive to noise. For optimal performance, it is recommended that the power supplies are isolated to avoid external noise coupling. **DDI\_VDD** and **DDO\_VDD** may be combined if they are powered at the same supply level. However, **PLL\_VDD**, **CORE\_VDD** and **IO\_VDD** should be routed separately.
- Linearly regulated power supplies are recommended wherever possible as they provide the cleanest power.
- Critical components such as power supply decoupling capacitors, LF capacitor, RBIAS resistor, CT0 and CT1 capacitors and VCO filter should be placed as close as possible to the GS3470.
- $\overline{DDI0}/DDI0$ ,  $\overline{DDI1}/DDI1$ , and  $\overline{DDO}/DDO$  differential inputs and outputs should be routed using 100Ω differential controlled impedance transmission lines.
- When paired with a compatible cable equalizer or cable driver, it is possible to DC-couple the differential high-speed inputs and outputs. In cases requiring AC-coupling, anti-pads should be used underneath AC-coupling capacitors to minimize the parasitic capacitance associated with these components. Details on the use of anti-pads can be found in the Semtech video design guides referenced above.
- The parallel data outputs and timing signals should be electrically phase matched to within 1/20th of a wavelength. For 300MHz, this is approximately equivalent to 1" of FR4 micro-strip.
- Serial termination on the parallel data outputs and timing signals may be required for very long traces or traces going through connectors.

## 7. References & Relevant Standards

|              |                                                                                                     |
|--------------|-----------------------------------------------------------------------------------------------------|
| SMPTE ST 125 | Component video signal 4:2:2 – bit parallel interface                                               |
| SMPTE ST 259 | 10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface                |
| SMPTE ST 260 | 1125 / 60 high definition production system – digital representation and bit parallel interface     |
| SMPTE ST 267 | Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio                   |
| SMPTE ST 272 | Formatting AES/EBU Audio and Auxiliary Data into Digital Video Ancillary Data Space                 |
| SMPTE ST 274 | 1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates              |
| SMPTE ST 291 | Ancillary Data Packet and Space Formatting                                                          |
| SMPTE 292    | Bit-Serial Digital Interface for High-Definition Television Systems                                 |
| SMPTE ST 293 | 720 x 483 active line at 59.94Hz progressive scan production – digital representation               |
| SMPTE ST 296 | 1280 x 720 scanning, analog and digital representation and analog interface                         |
| SMPTE ST 299 | 24-Bit Digital Audio Format for HDTV Bit-Serial Interface                                           |
| SMPTE ST 352 | Video Payload Identification for Digital Television Interfaces                                      |
| SMPTE ST 424 | Television - 3Gb/s Signal/Data Serial Interface                                                     |
| SMPTE ST 425 | Television - 3Gb/s Signal/Data Serial Interface - Source Image Format Mapping                       |
| SMPTE RP165  | Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television |
| SMPTE RP168  | Definition of Vertical Interval Switching Point for Synchronous Video Switching                     |

# 8. Package & Ordering Information

## 8.1 Package Dimensions

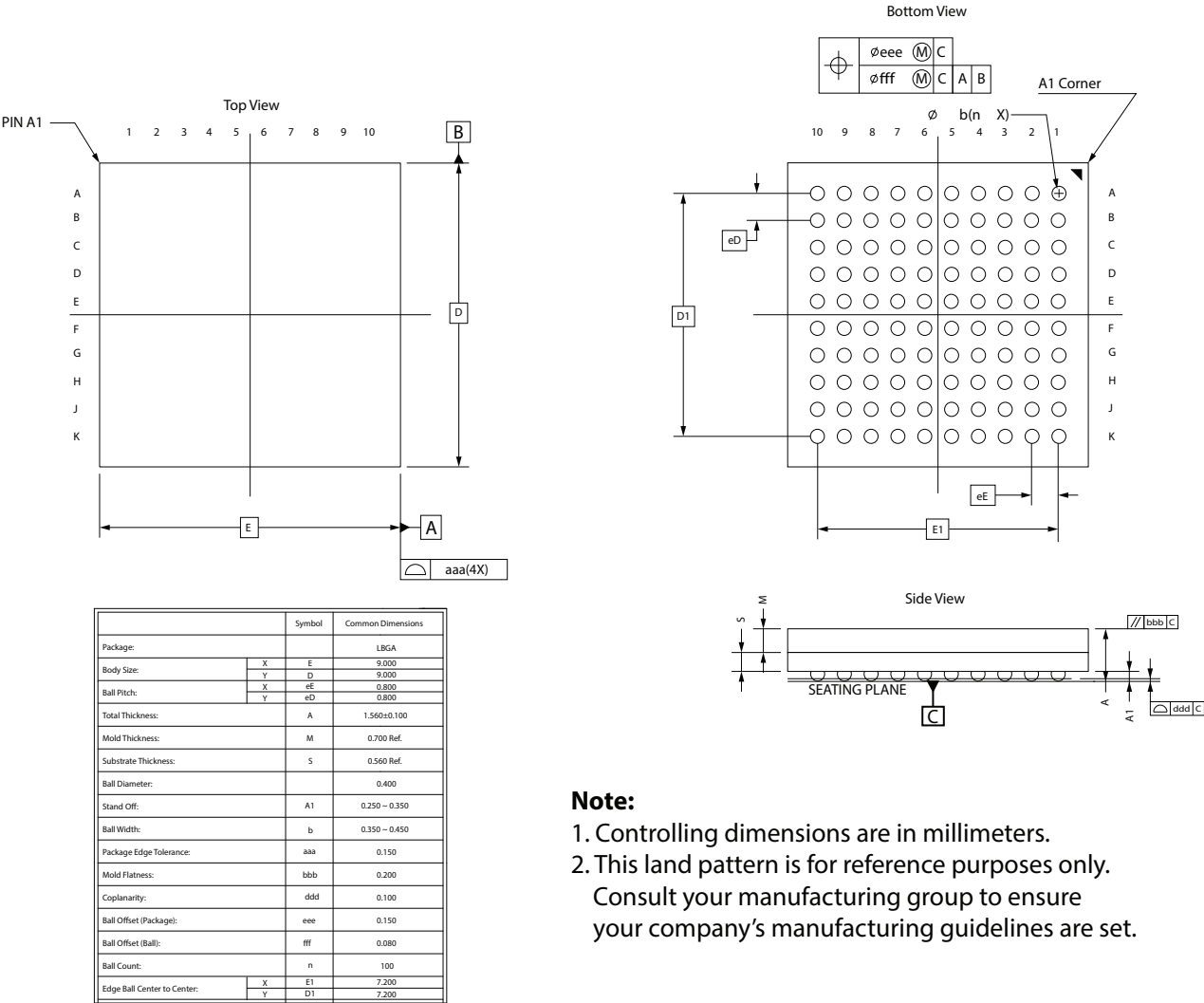


Figure 8-1: Package Dimensions

## 8.2 Recommended PCB Footprint

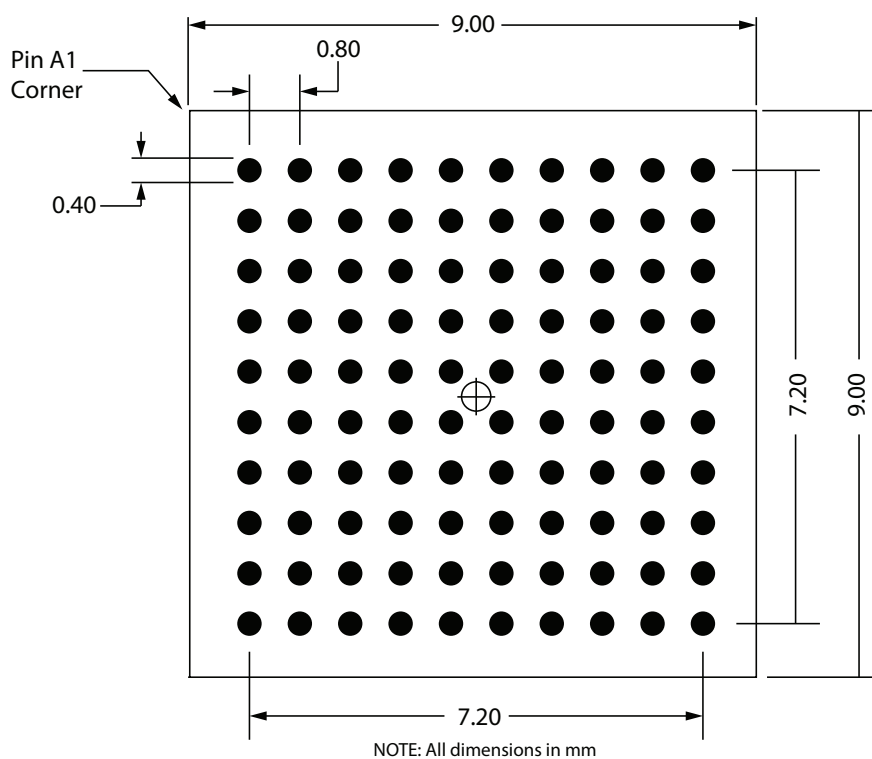


Figure 8-2: Recommended PCB Footprint

## 8.3 Packaging Data

Table 8-1: Packaging Data

| Parameter                                                            | Value                                                                       |
|----------------------------------------------------------------------|-----------------------------------------------------------------------------|
| Package Type                                                         | 9mm x 9mm 100-ball LBGA package (0.80mm Ball Pitch)                         |
| Package Drawing Reference                                            | JEDEC M0192 (with exceptions noted in <a href="#">Package Dimensions</a> ). |
| Moisture Sensitivity Level                                           | 3                                                                           |
| Junction to Case Thermal Resistance, $\theta_{j-c}$                  | 28°C/W                                                                      |
| Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow) | 48°C/W                                                                      |
| Junction to Board Thermal Resistance, $\theta_{j-b}$                 | 41°C/W                                                                      |
| Pb-free and RoHS Compliant                                           | Yes                                                                         |

## 8.4 Marking Diagram



Figure 8-3: Marking Diagram

## 8.5 Ordering Information

Table 8-2: Ordering Information

| Part Number  | Minimum Order Quantity | Format        |
|--------------|------------------------|---------------|
| GS3470-IBE3  | 260                    | Tray          |
| GS3470-IBE3Z | 2500                   | Tape and Reel |



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- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,  
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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