ISL8202M

3A Single Channel High Efficiency DC/DC Step-Down Power Module

FN8761
Rev.4.00
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The ISL8202M power module is a single channel synchronous step-down complete power supply, capable of delivering up to 3A of continuous current. Operating from a single 2.6V to 5.5V input power rail and integrating controller, power inductor and MOSFETs, the ISL8202M only requires a few external components to operate and is optimized for space constrained and portable battery operated applications.

Based on current mode PWM control scheme, the ISL8202M provides a fast transient response and excellent loop stability as well as a very low duty cycle with an adjustable output voltage as low as 0.6V and better than 1.6% accuracy over line and load conditions. Operation frequency is selectable through an external resistor, with a 1.8MHz default setting, or may be synchronized with an external clock signal up to 3.5MHz. The ISL8202M also implements a selectable PFM mode to improve light-load efficiency and a 100% duty cycle LDO mode to extend battery life. A programmable soft-start reduces the inrush current required from the input supply while an automatic output discharge ensures a soft stop. Dedicated enable pin and power-good flag allow for easy system power rails sequencing.

An array of protection features, including input Undervoltage Lockout (UVLO), over-temperature, overcurrent/short-circuit with hiccup mode, overvoltage and negative overcurrent, guarantees safe operations under abnormal operating conditions.

The ISL8202M is available in a compact RoHS compliant 22 Ld 4.5x7.5x1.85mm QFN package.

Related Literature

- TB389, "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"
- UG071, "ISL8202MEVAL1Z Evaluation Board User Guide"

Features

- 3A single channel complete power supply
  - Integrates controller, MOSFETs and inductor
  - Pin compatible with the 5A ISL8205M
- 2.6V to 5.5V input voltage range
- Adjustable output voltage range
  - As low as 0.6V with ±1.6% accuracy over line/load/temperature
  - Up to 95% efficiency
- Default 1.8MHz current mode control operations
  - 680kHz to 3.5MHz resistor adjustable
  - External synchronization up to 3.5MHz
  - Selectable light-load efficiency mode
  - 100% duty cycle LDO mode
- Programmable soft-start
- Soft-stop output discharge
- Dedicated enable pin and power-good flag
- UVLO, over-temperature, overcurrent, overvoltage and negative overcurrent protections
  - Overcurrent/short-circuit hiccup mode
- 4.5mmx7.5mmx1.85mm 22 Ld QFN package

Applications

- DC to DC POL power module
- µC/µP, FPGA and DSP power
- Portable equipment
- Battery operated equipment

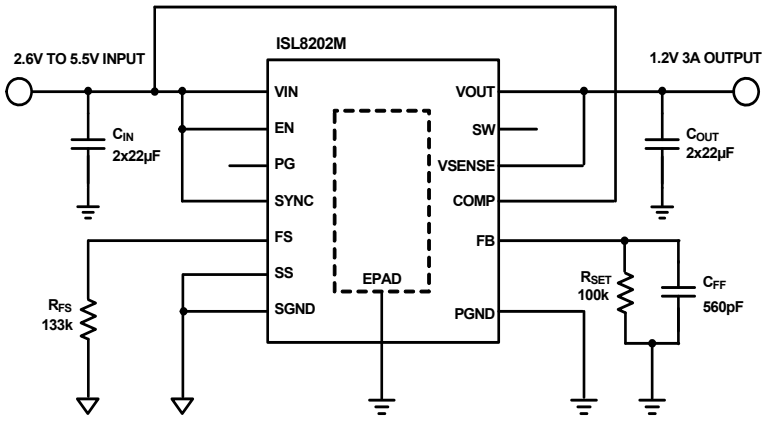

FIGURE 1. TYPICAL APPLICATION DIAGRAM AT $5V_{IN}$, $1.2V_{OUT}$, 1.5MHz f_{SW}, 3A

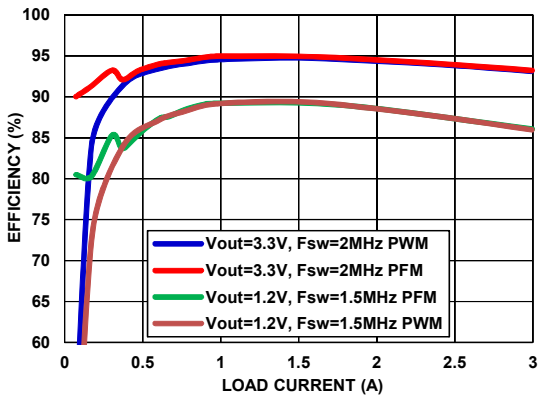

FIGURE 2. EFFICIENCY vs LOAD $5V_{IN}$

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Functional Block Diagram

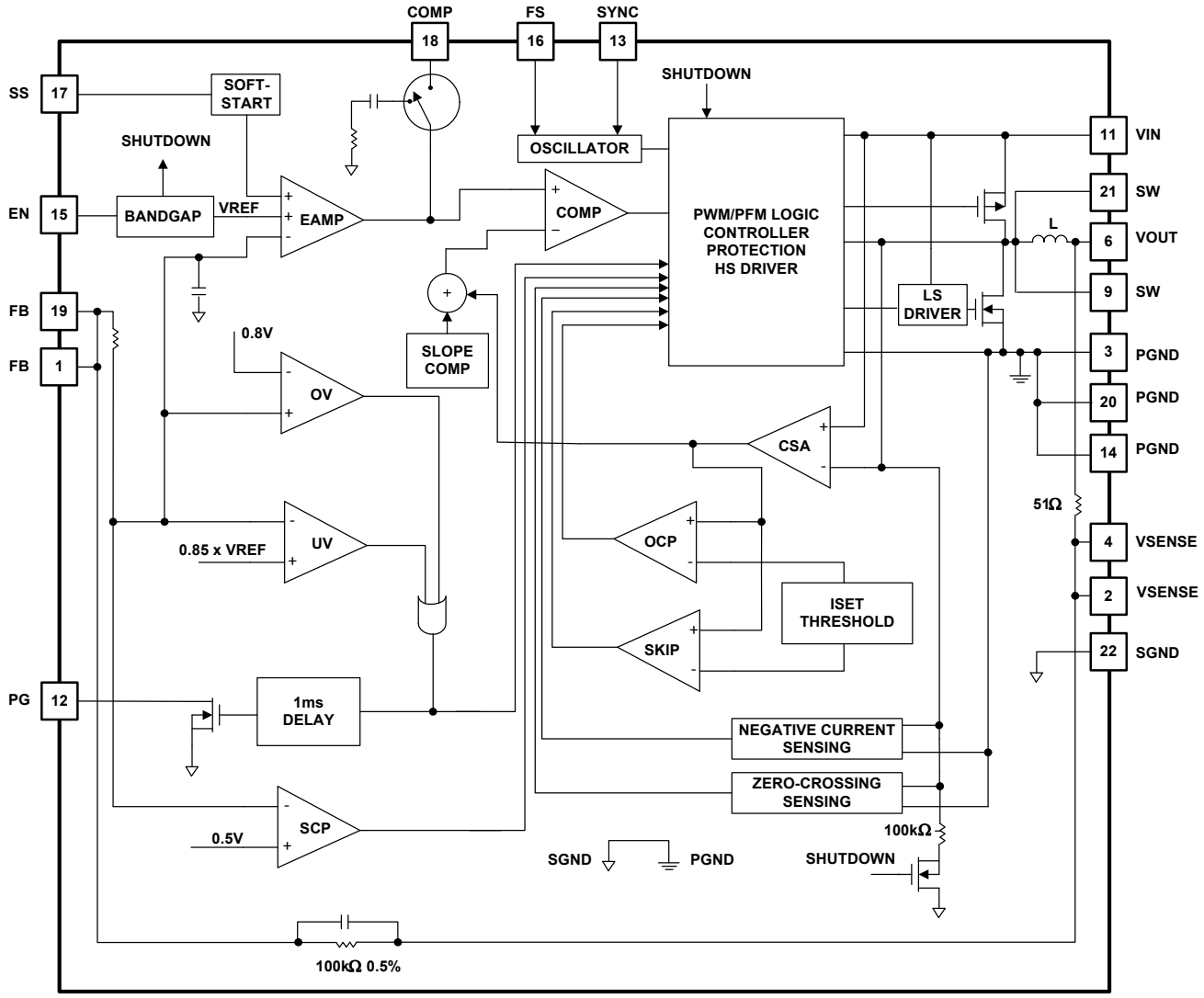
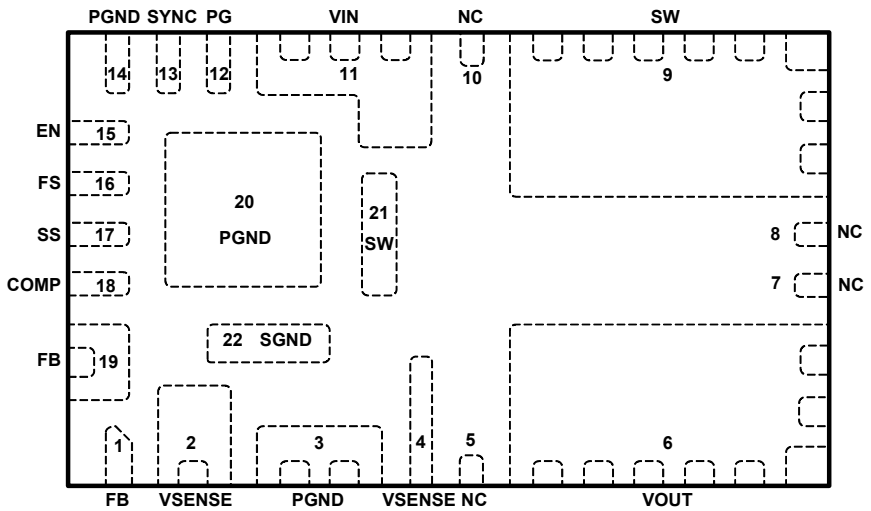
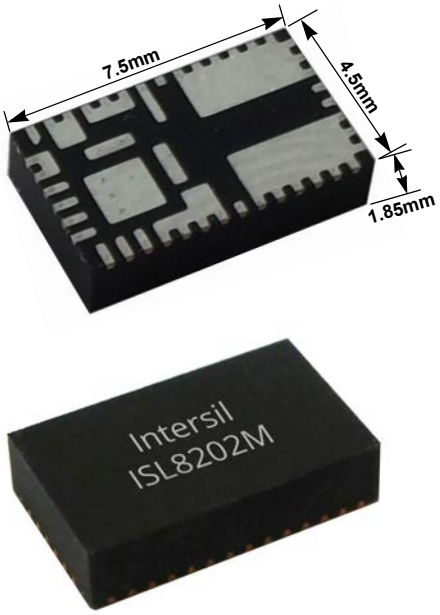


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Pin Configuration

ISL8202M
(22 LD QFN)
TOP VIEW





Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 19	FB	**Voltage setting pin.** Module output voltage is set by connecting a resistor R_{SET} from this pin to SGND. A ceramic capacitor is also recommended to be placed in parallel with R_{SET} from FB to SGND to ensure system stability in extreme operation conditions. Refer to Table 2 on page 14 for the resistor and capacitor values for various typical output voltage.
2, 4	VSENSE	**Voltage sense pin.** Pins 2 and 4 are shorted together internally. An internal 51Ω resistor is connected from VOUT (Pad 6) to VSENSE for local output voltage feedback in case remote sensing is not present. To achieve best regulation performance at point of load, remote sensing trace needs to be directly routed to VSENSE.
3, 14	PGND	**Power ground.** Power ground pins. Place output capacitor across VOUT and PGND close to Pin 3 since it is the return path for output current.
5, 7, 8, 10	NC	**No connection pins.** These pins have no connections inside. Leave these pins floating.
6	VOUT	**Power output.** Power output of the module. Output capacitors should be placed across this pad and Pin 3 PGND and close to the module. Apply load between this pin and PGND Pin 3. Output voltage range: 0.6V to 5.0V.
9, 21	SW	**Switching node.** These pins can be used to monitor switch node waveform to examine switching frequency. These pins can also be used for snubber connection. To improve system efficiency, it is recommended to connect Pin 9 and Pin 21 with wide copper shape. However, avoid connecting SW to large copper shape to minimize radiated EMI noise.
11	VIN	**Power input.** Input voltage range: 2.6V to 5.5V. Tie directly to the input rail. It is required to have minimum total input capacitance of 44µF at module input. Add additional capacitance if possible. Use X5R or X7R ceramic capacitors. It is critical to place input ceramic capacitors as close as possible to module input. Refer to "PCB Layout Recommendations" on page 19 for more information.
12	PG	**Power-good pin.** Power-good is an open-drain output. Use a 10kΩ to 100kΩ pull-up resistor connected between VIN and PG. During power-up or EN pin start-up, PG rising edge is delayed by 1ms upon output reached within regulation.
13	SYNC	**Synchronization pin.** Mode Selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external clock for synchronization with the positive edge trigger. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case SYNC pin is floating. Therefore, PFM mode is enabled when SYNC is left floating.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
15	EN	**Power enable pin.** Enable the output, when driven to high. Shutdown the output and discharge output capacitor when driven to low. Typically tie to VIN pin directly. Do not leave this pin floating.
16	FS	**Frequency selection pin.** This pin sets module switching frequency. The default frequency is 1.8MHz if FS is connected to VIN. In spite of default setting, a resistor, R_{FS}, can be connected from the FS pin to SGND to adjust switching frequency ranging from 680kHz to 3.5MHz.
17	SS	**Soft-start pin.** SS is used to adjust the soft-start time. Connect to SGND for internal 1ms rise time. Connect a capacitor from SS to SGND to adjust the soft-start time. The capacitor value should be less than 33nF to ensure proper operation.
18	COMP	**Compensation pin.** COMP is the output of voltage feedback error amplifier. For most applications, internal compensation network can be used to stabilize the system and achieve optimal transient response. This can be done by directly connecting COMP to VIN. For other applications where external compensation is desired, COMP needs to be disconnected from VIN and tied to external compensation network.
Exposed Pad 20	PGND	The exposed pad is connected internally to PGND. Solid connection should be made between Pad 20 and PGND plane on PCB. Place as many vias as possible under the pad connecting to PGND plane(s) for optimal electrical and thermal performance. Refer to "PCB Layout Recommendations" on page 19 for more information.
22	SGND	**Signal ground pin.** Connect PCB SGND plane to this pin. Internally, this pin is single-point connected to module PGND.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL8202MIRZ-T	ISL8202M	-40 to +85	3k	22 Ld QFN	L22.4.5x7.5
ISL8202MIRZ-T7A	ISL8202M	-40 to +85	250	22 Ld QFN	L22.4.5x7.5
ISL8202MEVAL1Z	Evaluation Board				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I. They employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL8202M. For more information on MSL, please see Technical Brief TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	MAX OUTPUT CURRENT I_{OUT} (DC)
ISL8205M	5A
ISL8203M	3A dual, 6A single
ISL8202M	3A

Absolute Maximum Ratings (Reference to GND)

VIN ..... -0.3V to 5.8V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB .....-0.3V (DC) to VIN +0.3V
SW ..... -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
COMP, SS ..... -0.3V to 2.7V
ESD Ratings
Human Body Model (Tested per JS-001-2010) 2kV
Charged Device Model (Tested per JS-002-2014) 750V
Machine Model (Tested per JESD22-A115C) 200V
Latch-Up (Tested per JESD-78D; Class 2, Level A) ..... 100mA at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
22 Ld QFN (Notes 4, 5)	27.4	4.8

Junction Temperature Range .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range ..... 2.6V to 5.5V
V_{OUT} Voltage Range ..... 0.6V to 5.0V
Load Current Range ..... 0A to 3A
Ambient Temperature Range .....-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on the ISL8202MEVAL1Z evaluation board with "direct attach" features. Refer to ISL8202MEVAL1Z User Guide for evaluation board details. Also see Tech Brief TB379 for general thermal metric information.
5. For θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, typical specifications are measured at V_{IN} = 3.6V, V_{OUT} = 1.2V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold (Note 7)	V_{UVLO}	Rising, no load		2.3	**2.5**	V
		Falling, no load	**2.10**	2.25		V
Quiescent Supply Current	I_{VIN}	SYNC = GND, EN = high, I_{OUT} = 0A		50		µA
		SYNC = V_{IN}, f_{SW} = 1.5MHz, EN = high, I_{OUT} = 0A		13	**20**	mA
Shutdown Supply Current	I_{SD}	SYNC = GND, V_{IN} = 5.5V, EN = low		5	**20**	µA
OUTPUT REGULATION						
Output Continuous Current Range	$I_{OUT(DC)}$				**3**	A
Line Regulation	$\Delta V_{OUT}/V_{OUT}$	V_{IN} = 2.6V to 5.5V, V_{OUT} = 1.2V, f_{SW} = 1.5MHz, I_{OUT} = 0A, PWM mode		0.58		%
		V_{IN} = 2.6V to 5.5V, V_{OUT} = 1.2V, f_{SW} = 1.5MHz, I_{OUT} = 3A, PWM mode		0.66		%
Load Regulation		V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 1.5MHz, I_{OUT} = 0A to 3A, PWM mode		0.34		%
		V_{IN} = 5V, V_{OUT} = 3.3V, f_{SW} = 2MHz, I_{OUT} = 0A to 3A, PWM mode		0.21		%
Output Voltage Accuracy (Note 8)		Over line/load/temperature range, PWM mode, V_{OUT} = 1.2V to 3.3V	**-1.6**		**1.6**	%
Output Ripple Voltage	ΔV_{OUT}	V_{IN} = 5V, 2x22µF ceramic output capacitor, PWM mode				
		I_{OUT} = 0A, V_{OUT} = 1.2V, f_{SW} = 1.5MHz		7		mV_{P-P}
		I_{OUT} = 3A, V_{OUT} = 1.2V, f_{SW} = 1.5MHz		8		mV_{P-P}
		I_{OUT} = 0A, V_{OUT} = 3.3V, f_{SW} = 2MHz		7		mV_{P-P}
		I_{OUT} = 3A, V_{OUT} = 3.3V, f_{SW} = 2MHz		8		mV_{P-P}
Reference Voltage (Note 7)	V_{REF}		**0.594**	0.600	**0.606**	V

Electrical Specifications Unless otherwise noted, typical specifications are measured at V_{IN} = 3.6V, V_{OUT} = 1.2V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{FB} Bias Current (Note 7)	I_{FB}	V_{FB} = 0.75V		0.1		µA
Soft-Start Ramp Time Cycle (Note 7)		SS = GND		1		ms
Soft-Start Charging Current (Note 7)	I_{SS}	V_{SS} = 0.1V	**1.45**	1.85	**2.25**	µA
DYNAMIC CHARACTERISTICS						
Voltage Change for Positive Load Step	ΔV_{OUT-DP}	Current slew rate = 1A/µs, V_{IN} = 5V, 2x22µF ceramic output capacitor				
		V_{OUT} = 1.2V, I_{OUT} = 0A to 3A, f_{SW} = 1.5MHz		59		mV_{P-P}
		V_{OUT} = 3.3V, I_{OUT} = 0A to 3A, f_{SW} = 2MHz		47		mV_{P-P}
Voltage Change for Negative Load Step	ΔV_{OUT-DP}	Current slew rate = 1A/µs, V_{IN} = 5V, 2x22µF ceramic output capacitor				
		V_{OUT} = 1.2V, I_{OUT} = 3A to 0A, f_{SW} = 1.5MHz		73		mV_{P-P}
		V_{OUT} = 3.3V, I_{OUT} = 3A to 0A, f_{SW} = 2MHz		51		mV_{P-P}
OVERCURRENT PROTECTION (Note 7)						
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Overcurrent Limit	I_{PLIMIT}		**7.5**	9	**11**	A
Positive Skip Limit	I_{SKIP}		**1**	1.3	**1.8**	A
Zero Cross Threshold			**-300**		**300**	mA
Negative Current Limit	I_{NLIMIT}		**-4.5**	-3	**-1.5**	A
COMPENSATION (Note 7)						
Current Sensing Gain	R_t		**0.119**	0.140	**0.166**	Ω
Error Amplifier Transconductance		Internal compensation		60		µA/V
		External compensation		120		µA/V
SWITCH NODE (Note 7)						
P-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		36	**63**	mΩ
		V_{IN} = 2.7V, I_O = 200mA		52	**89**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		13	**30**	mΩ
		V_{IN} = 2.7V, I_O = 200mA		17	**36**	mΩ
SW Maximum Duty Cycle				100		%
SW Minimum On-Time		SYNC = High			**115**	ns
OSCILLATOR						
Nominal Switching Frequency	f_{SW}	SYNC = V_{IN}	**1600**	1835	**2070**	kHz
		f_{SW} with R_{FS} = 261kΩ		800		kHz
		f_{SW} with R_{FS} = 133kΩ		1500		kHz
SYNC Logic LOW to HIGH Transition Range			**0.70**	0.75	**0.80**	V
SYNC Hysteresis				0.15		V
SYNC Logic Input Leakage Current		V_{IN} = 3.6V		3.6	**5**	µA

Electrical Specifications Unless otherwise noted, typical specifications are measured at V_{IN} = 3.6V, V_{OUT} = 1.2V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
PG (Note 7)						
Output Low Voltage					**0.3**	V
PG Pin Leakage Current		PG = V_{IN}		0.01	**0.10**	µA
OVP PG Rising Threshold				0.80		V
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				30		mV
Delay Time (Rising Edge)		Time from VOUT_ reached regulation	**0.5**	1.0	**2.0**	ms
PGOOD Delay Time (Falling Edge)				7.5		µs
EN (Note 7)						
Logic Input Low					**0.4**	V
Logic Input High			**0.9**			V
Enable Logic Input Leakage Current		Pulled up to 3.6V		0.1	**1.0**	µA
Thermal Shutdown		Temperature Rising		150		°C
Thermal Shutdown Hysteresis		Temperature Falling		25		°C

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Parameters with MIN and/or MAX limits are 100% tested for internal IC prior to module assembly, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. A 0.1% tolerance resistor is used for R_{SET}.

Typical Performance Characteristics

Efficiency T_A = +25°C.

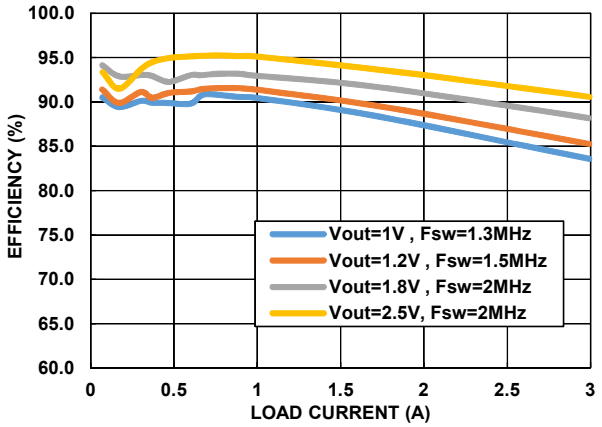


FIGURE 4. EFFICIENCY T_A = +25°C, V_{IN} = 3.3V PFM MODE

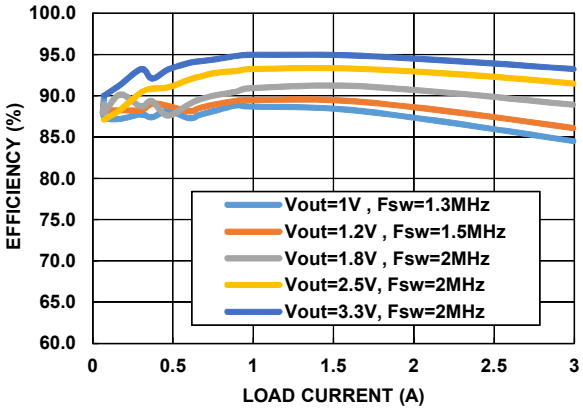


FIGURE 5. EFFICIENCY T_A = +25°C, V_{IN} = 5V PFM MODE

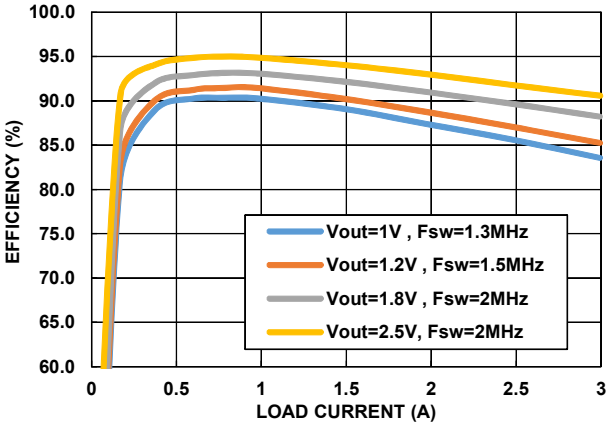


FIGURE 6. EFFICIENCY T_A = +25°C, V_{IN} = 3.3V PWM MODE

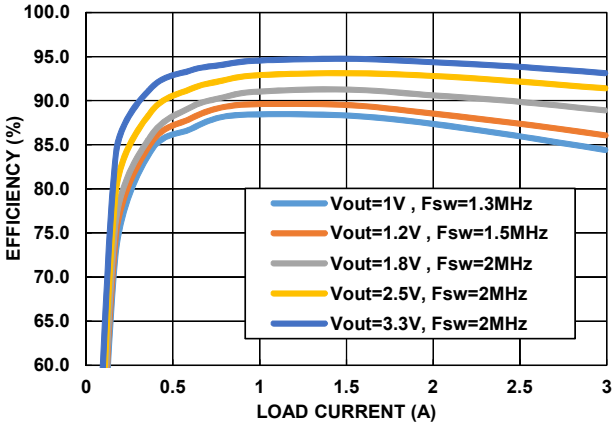


FIGURE 7. EFFICIENCY T_A = +25°C, V_{IN} = 5V PWM MODE

Output Voltage Ripple T_A = +25°C.

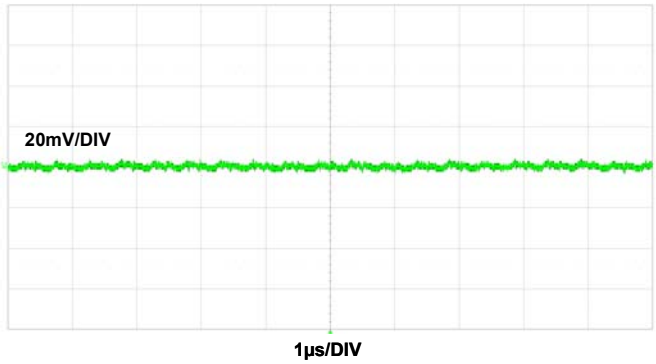


FIGURE 8. V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0A, f_{SW} = 2MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

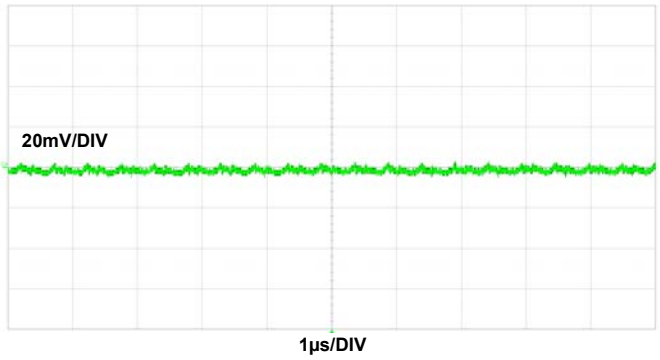


FIGURE 9. V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 2MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

Typical Performance Characteristics (Continued)

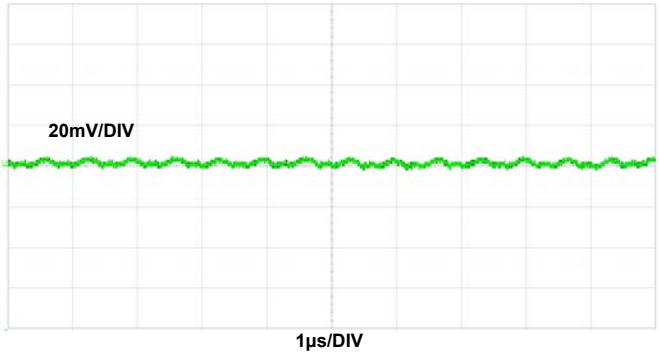


FIGURE 10. V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A, f_{SW} = 1.5MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

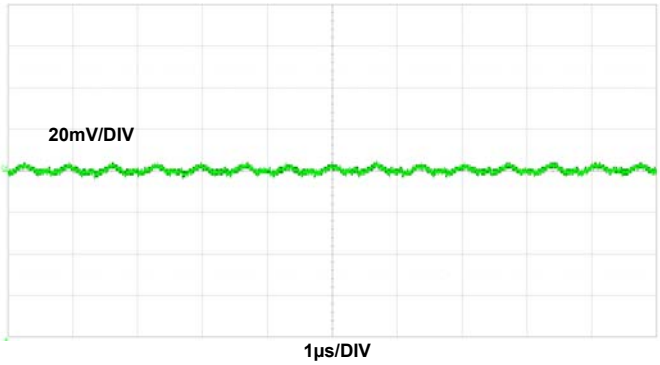


FIGURE 11. V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A, f_{SW} = 1.5MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

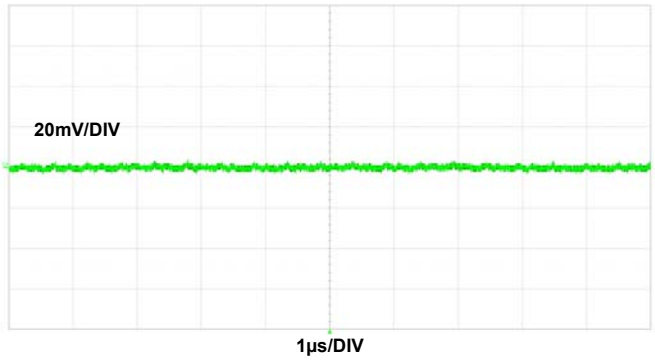


FIGURE 12. V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{OUT} = 0A, f_{SW} = 2MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

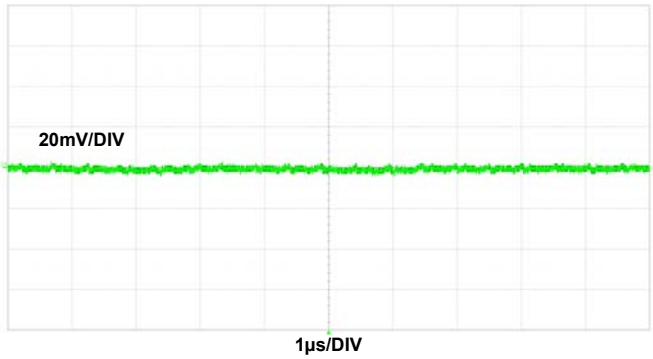


FIGURE 13. V_{IN} = 3.3V, V_{OUT} =2.5V, I_{OUT} = 3A, f_{SW} = 2MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

Load Transient Response

T_A = +25°C, load current step slew rate: 1A/µs.

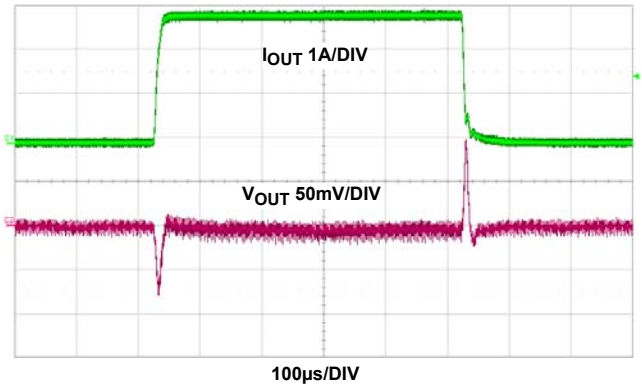


FIGURE 14. V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 0 TO 3A, f_{SW} = 1.3MHz, C_{OUT} = 3x22µF CERAMIC CAPACITORS

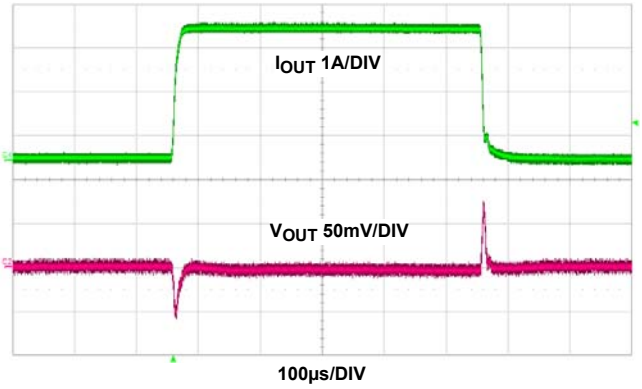


FIGURE 15. V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0 TO 3A, f_{SW} = 1.5MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

Typical Performance Characteristics (Continued)

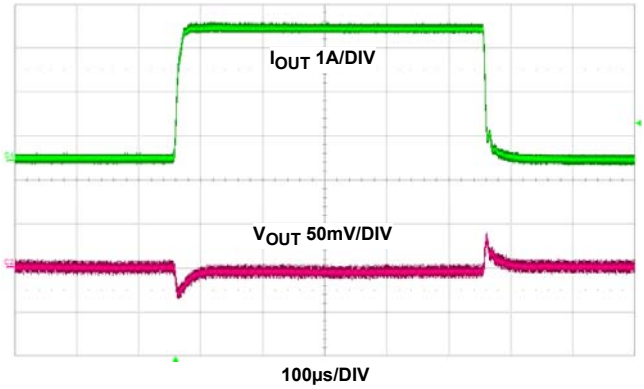


FIGURE 16. V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 0 TO 3A, f_{SW} = 2MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

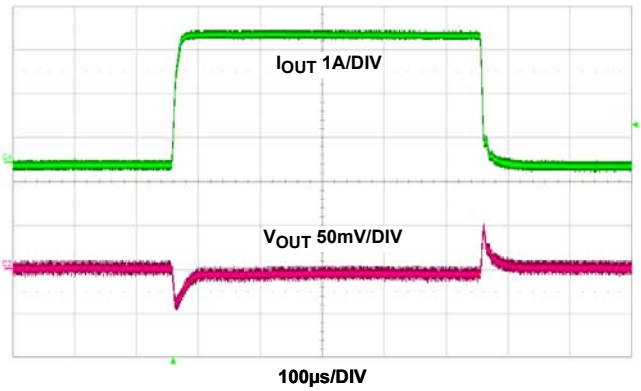


FIGURE 17. V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0 TO 3A, f_{SW} = 2MHz, C_{OUT} = 2x22µF CERAMIC CAPACITORS

Start-Up

T_A = +25°C, Resistor load is used in the test.

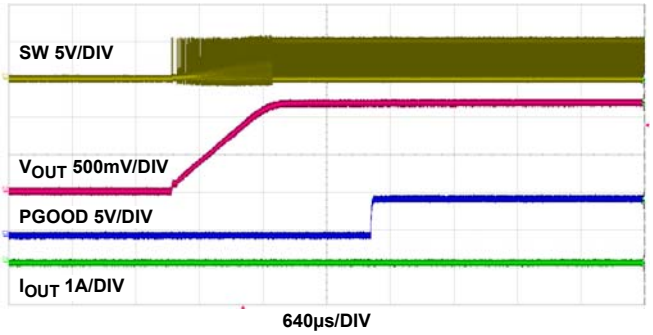


FIGURE 18. SOFT-START WITH 0A LOAD PWM MODE, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A, C_{OUT} = 2x22µF CERAMIC CAPACITORS, C_{IN} = 100µF POSCAP + 2x22µF CERAMIC CAPACITORS

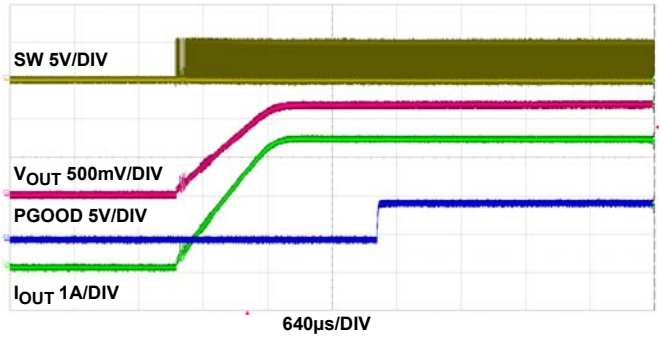


FIGURE 19. SOFT-START WITH 3A LOAD PWM MODE, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A, C_{OUT} = 2x22µF CERAMIC CAPACITORS, C_{IN} = 100µF POSCAP + 2x22µF CERAMIC CAPACITORS

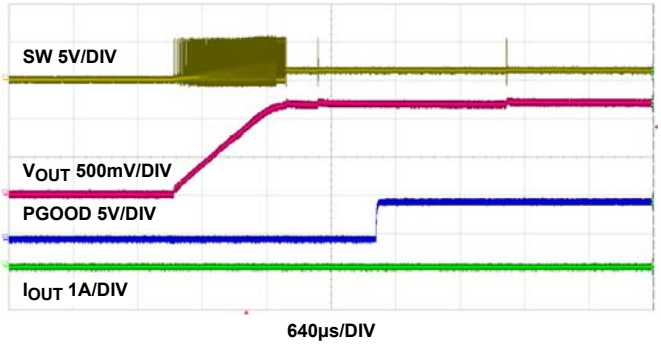


FIGURE 20. SOFT-START WITH 0A LOAD PFM MODE, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A, C_{OUT} = 2x22µF CERAMIC CAPACITORS, C_{IN} = 100µF POSCAP + 2x22µF CERAMIC CAPACITORS

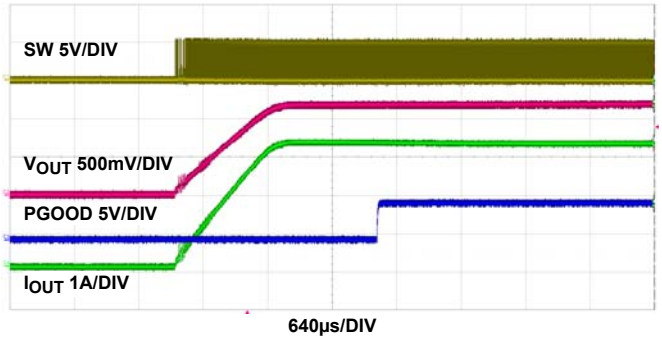


FIGURE 21. SOFT-START WITH 3A LOAD PFM MODE, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A, C_{OUT} = 2x22µF CERAMIC CAPACITORS, C_{IN} = 100µF POSCAP + 2x22µF CERAMIC CAPACITORS

Typical Performance Characteristics (Continued)

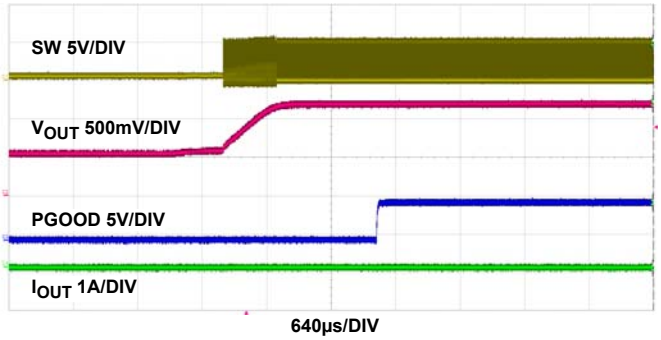


FIGURE 22. PREBIAS SOFT-START WITH 0A LOAD PWM MODE, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A, C_{OUT} = 2x22µF CERAMIC CAPACITORS, C_{IN} = 100µF POSCAP + 2 x 22µF CERAMIC CAPACITORS

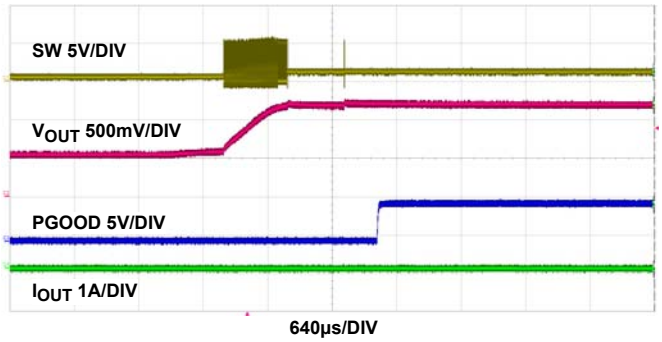


FIGURE 23. PREBIAS SOFT-START WITH 0A LOAD PFM MODE, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A, C_{OUT} = 2x22µF CERAMIC CAPACITORS, C_{IN} = 100µF POSCAP + 2 x 22µF CERAMIC CAPACITORS

Short-Circuit Protection

T_A = +25°C, V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 100µF POScap + 22µF ceramic capacitors, C_{OUT} = 2x22µF ceramic capacitors, output short-circuit during normal operation.

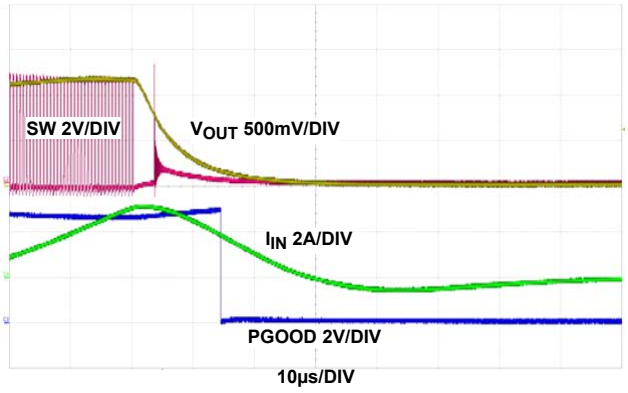


FIGURE 24. OUTPUT SHORT-CIRCUIT PROTECTION

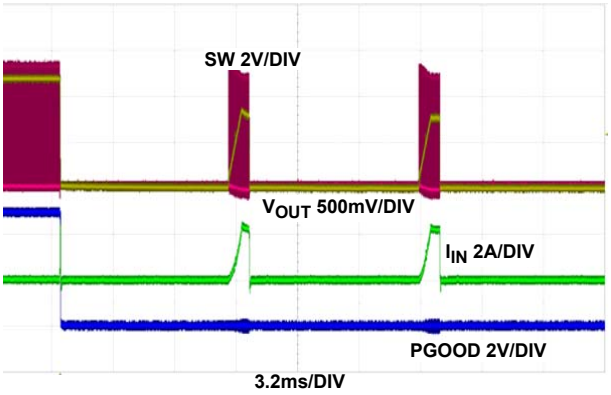


FIGURE 25. OUTPUT SHORT-CIRCUIT PROTECTION, HICCUP MODE

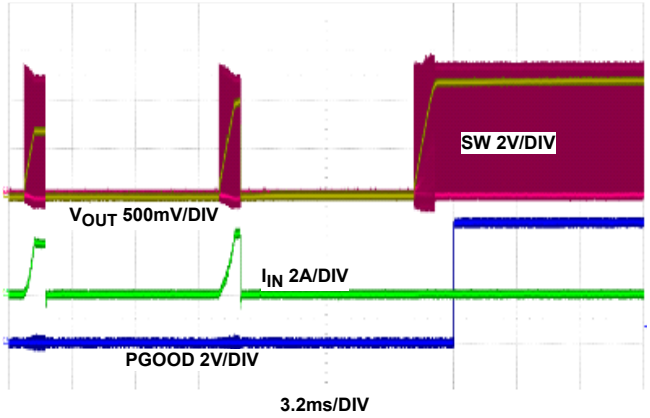


FIGURE 26. OUTPUT SHORT-CIRCUIT RECOVER FROM HICCUP

Typical Performance Characteristics (Continued)

Overvoltage Protection

T_A = +25°C, V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 100µF POScap + 22µF ceramic capacitors, C_{OUT} = 2x22µF ceramic capacitors.

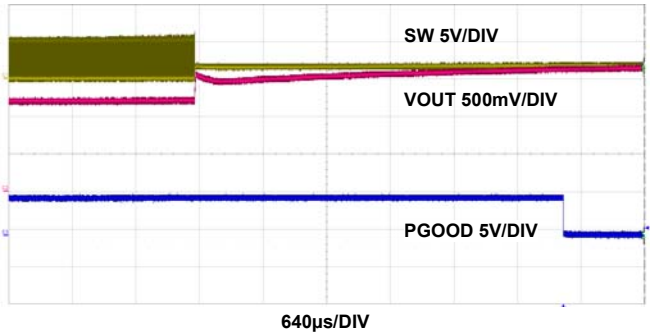


FIGURE 27. OUTPUT OVERVOLTAGE PROTECTION

Power Loss

T_A = +25°C, C_{IN} = 100µF POScap + 22µF ceramic capacitors, C_{OUT} = 2x22µF ceramic capacitors.

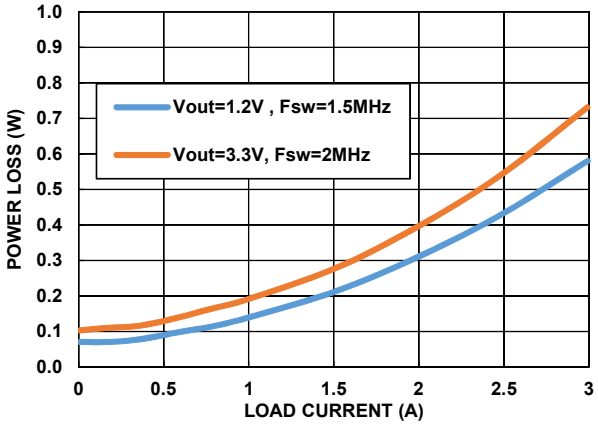


FIGURE 28. POWER LOSS AT V_{IN} = 5V, T_A = +25°C

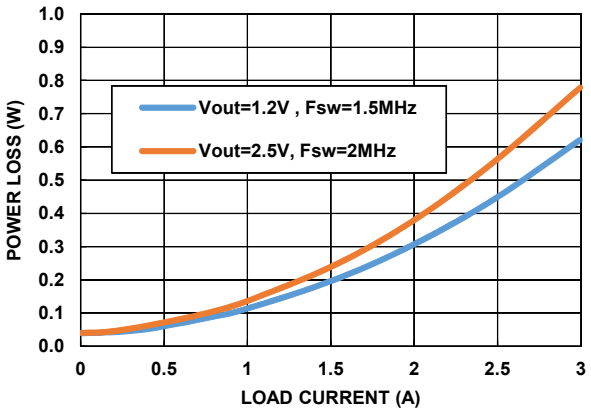


FIGURE 29. POWER LOSS AT V_{IN} = 3.3V, T_A = +25°C

Derating

All of the following curves were plotted at T_J = +120°C.

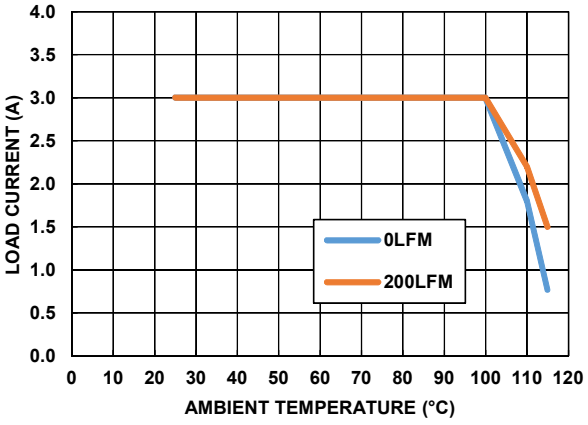


FIGURE 30. DERATING CURVES AT V_{IN} = 5V, V_{OUT} = 1.2V

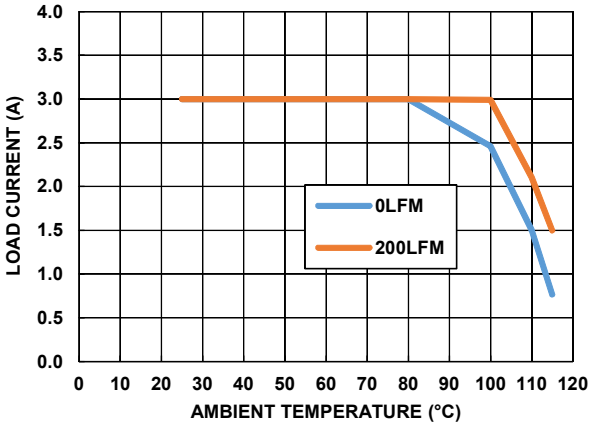


FIGURE 31. DERATING CURVES AT V_{IN} = 5V, V_{OUT} = 3.3V

Typical Performance Characteristics (Continued)

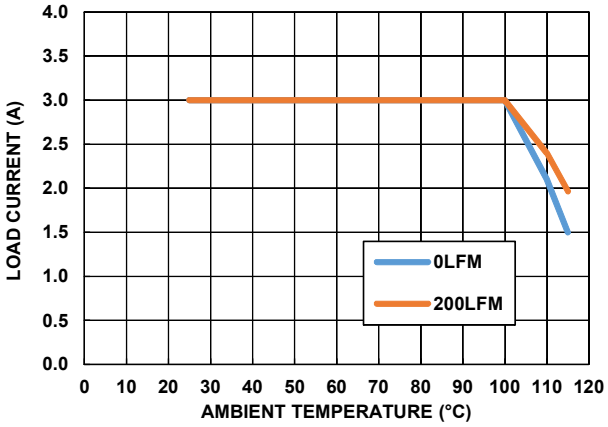


FIGURE 32. DERATING CURVES AT V_{IN} = 3.3V, V_{OUT} = 1.2V

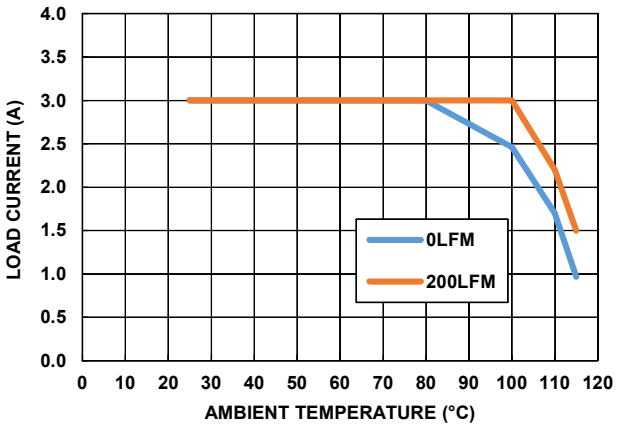


FIGURE 33. DERATING CURVES AT V_{IN} = 3.3V, V_{OUT} = 2.5V

TABLE 2. ISL8202M DESIGN GUIDE MATRIX (REFER TO Figure 1)

V_{IN} (V)	V_{OUT} (V)	f_{SW} (MHz)	C_{IN} (µF)	C_{OUT} (µF)	R_{FS} (kΩ)	R_{SET} (kΩ)	C_{FF} (pF)
5	0.6	0.8	2x22	3x22	261	OPEN	680
5	0.9	1.2	2x22	3x22	169	200	680
5	1	1.3	2x22	2x22	154	150	680
5	1.2	1.5	2x22	2x22	133	100	560
5	1.5	1.9	2x22	2x22	102	66.5	390
5	1.8	2	2x22	2x22	95.3	49.9	390
5	2.5	2	2x22	2x22	95.3	31.6	220
5	3.3	2	2x22	2x22	95.3	22.1	330
3.3	0.6	0.8	2x22	3x22	261	OPEN	680
3.3	0.9	1.2	2x22	3x22	169	200	680
3.3	1	1.3	2x22	2x22	154	150	680
3.3	1.2	1.5	2x22	2x22	133	100	560
3.3	1.5	1.9	2x22	2x22	102	66.5	390
3.3	1.8	2	2x22	2x22	95.3	49.9	390
3.3	2.5	2	2x22	2x22	95.3	31.6	220

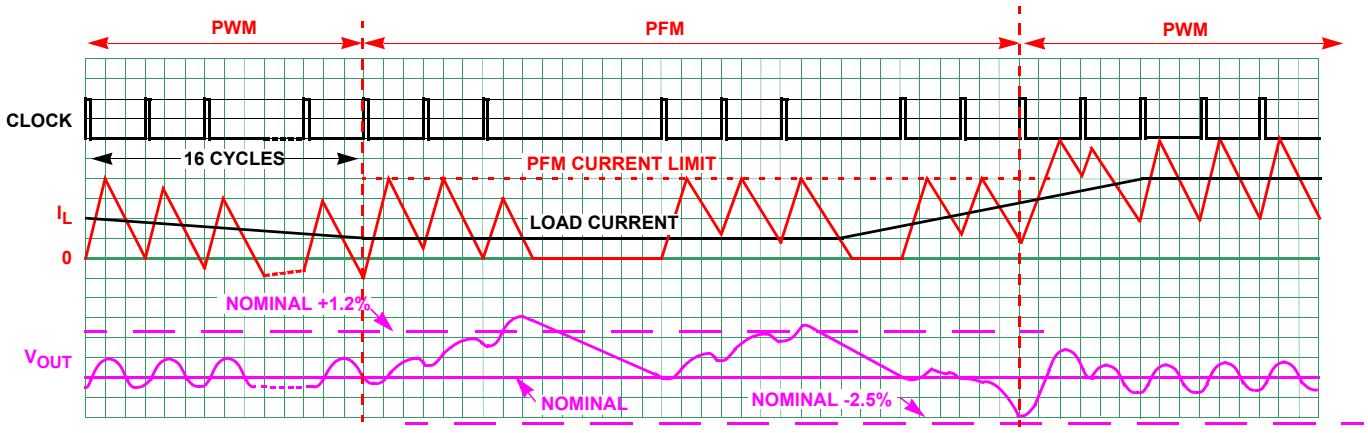


FIGURE 34. PFM MODE OPERATION WAVEFORMS

Functional Description

The ISL8202M is a single channel 3A step-down high efficiency power module optimized for FPGA, DSP and Li-ion battery power devices. The module switches at 1.8MHz by default when the FS pin is shorted to VIN. The switching frequency is also adjustable from 680kHz to 3.5MHz through a resistor, R_{FS}, from FS to SGND. To boost light-load efficiency, ISL8202M can also be configured to operate in PFM mode by pulling the SYNC pin to SGND. Peak current mode control scheme is implemented for fast transient response. By shorting the COMP pin to VIN, the module utilizes internal compensation to stabilize system and optimize transient response. Other excellent features include external synchronization, 100% duty cycle operation and very low quiescent current.

PWM Control Scheme

Pulling the SYNC pin high (>0.8V) forces the module into PWM mode, regardless of output current. The ISL8202M employs the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. As shown in Figure 3 on page 3, the current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 140mV/A. The control reference for the current loops comes from the Error Amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier, CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the PFET and turn on the N-channel MOSFET. The NFET stays on until the end of the PWM cycle. Figure 35 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the Current-Sense Amplifier's (CSA) output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during start-up and will be discussed separately, please refer to "Soft Start-Up" on page 16. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. When the COMP is tied to VIN, the voltage loop is internally compensated with the 55pF and 100kΩ RC network.

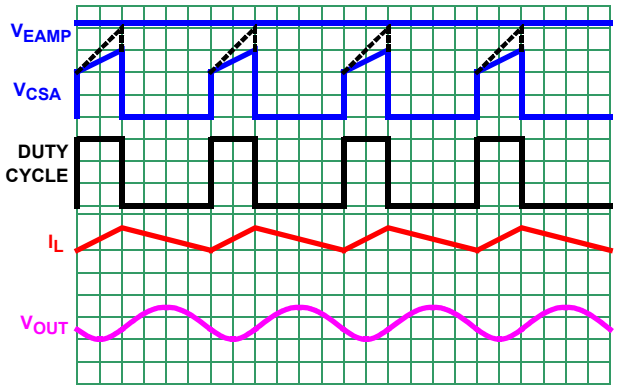


FIGURE 35. PWM OPERATION WAVEFORMS

PFM (Skip) Mode

Pulling the SYNC pin LOW (<0.4V) forces the module into PFM mode. The ISL8202M enters a pulse-skipping mode at light load to minimize the switching losses by reducing the switching frequency. Figure 34 illustrates the Skip mode operation. A zero-cross sensing circuit shown in Figure 3 on page 3 monitors the NFET current for zero crossing. When 16 consecutive cycles are detected, the module enters the Skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the Skip mode is entered, the pulse modulation starts being controlled by the skip comparator shown in Figure 3 on page 3. Each pulse cycle is still synchronized by the PWM clock. The PFET is turned on at the clock's rising edge and turned off when the output is higher than 1.2% of the nominal regulation or when its current reaches the peak skip current limit value. Then, the inductor current is discharged to 0A and stays at zero (the internal clock is disabled) and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the PFET will be turned on again at the rising edge of the internal clock as it repeats the previous operations. The module resumes normal PWM mode operation when the output voltage drops 2.5% below the nominal voltage.

Frequency Adjust

The switching frequency of ISL8202M is adjustable ranging from 680kHz to 3.5MHz via a simple resistor, R_{FS}, across FS to SGND. The switching frequency setting is based on Equation 1:

$$R_{FS}[k\Omega] = \frac{220 \cdot 10^3}{f_{OSC}[kHz]} - 14 \quad \text{(EQ. 1)}$$

When the FS pin is directly tied to VIN, the frequency of operation is fixed at 1.8MHz. For selections of switching frequency of typical operation conditions, refer to Table 2 on page 14. More detailed information on recommended switching frequency recommendation is provided in "Recommended Switching Frequency" on page 17.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 3 on page 3. The current sensing circuit has a gain of 140mV/A, from the PFET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripled and turns off the PFET immediately. The overcurrent function protects the module from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the module will be shut down under an overcurrent fault condition. An overcurrent fault condition will result in the module attempting to restart in a hiccup mode within the delay of eight soft-start periods. At the end of the 8^{th} soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of 8 soft-start periods, the output will resume back into regulation after hiccup mode expires.

Negative Current Protection

Similar to overcurrent, the negative current protection is realized by monitoring the current across the low-side NFET, as shown in Figure 3 on page 3. When the valley point of the inductor current reaches -3A for 4 consecutive cycles, both PFET and NFET are turned off. The 100Ω in parallel to the NFET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The module will be in PFM for 20µs before switching to PWM, if necessary.

Power-Good

PG is an open-drain output of a window comparator that continuously monitors the module output voltage. PG is actively held low when EN is low and during the module soft-start period. After 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within the nominal regulation voltage set by V_{FB}. Under output overvoltage fault condition (output voltage is 33% higher than nominal value) or output undervoltage fault condition (output voltage is 15% lower than nominal value), the PG will be pulled low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor, between PG and VIN. A 100kΩ resistor works well in most applications.

UVLO

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the module is disabled.

Soft Start-Up

The soft start-up reduces the inrush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed, so that the output voltage rises in a controlled fashion. When V_{FB} is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz, so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the Skip mode to support prebiased output condition.

Tie SS to SGND for internal soft-start, which is approximately 1ms. Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 1.85µA current source sets the soft-start interval of the module, t_{SS}, as shown by Equation 2:

$$C_{SS}[\mu F] = 3.1 \cdot t_{SS}[s] \quad \text{(EQ. 2)}$$

C_{SS} must be less than 33nF to insure proper soft-start reset after fault condition.

External Synchronization Control

The frequency of operation can be synchronized up to 3.5MHz by an external signal applied to the SYNC pin. The rising edge of SYNC signal triggers the rising edge of PWM ON pulse. To ensure proper operation, it is recommended that the external SYNC frequency is within ±25% of the switching frequency set by FS pin.

Enable

The enable (EN) input allows the user to control the turning on or off of the module for purposes such as power-up sequencing. When the module is enabled, there is typically a 600µs delay for waking up the bandgap reference and then the soft start-up begins.

Discharge Mode (Soft-Stop)

When a transition to Shutdown mode occurs or the VIN UVLO is set, the output discharges to PGND through an internal 100Ω switch.

100% Duty Cycle

The ISL8202M features a 100% duty cycle operation to minimize switching loss. When the input voltage drops to a level that the ISL8202M can no longer maintain the regulation at the output, the module completely turns on the PFET.

Thermal Shutdown

The ISL8202M has built-in thermal protection. When the internal temperature reaches +150°C, the module is completely shut down. As the temperature drops to +125°C, the ISL8202M resumes operation by stepping through the soft-start.

Applications Information

Programming the Output Voltage

The output voltage of the module is programmed by an external resistor, as R_{SET} in Figure 1 on page 1 applied from FB pin to SGND. R_{SET} in combination with the internal 100kΩ 0.5% resistor connected from FB to VSENSE forms resistor divider that sets the output voltage. The output voltage is governed by Equation 3:

$$V_{OUT} = V_{REF} \cdot \frac{R_{SET} + 100k\Omega}{R_{SET}} \quad \text{(EQ. 3)}$$

TABLE 3. TYPICAL VOLTAGE SETTING RESISTOR VALUES

V_{OUT} (V)	R_{SET} (kΩ)
0.6	OPEN
0.8	300
1.0	150
1.2	100
1.8	49.9
2.5	31.6
3.3	22.1

Please note that the output voltage accuracy is also dependent on the resistor accuracy of R_{SET}. The user needs to select high accuracy resistors in order to achieve the overall output accuracy.

Recommended Switching Frequency

With varieties of input and output voltage combinations, one must choose wisely on which frequency to operate at. Selection of switching frequency for each V_{IN} and V_{OUT} combination needs to take in to account a few trade-offs. Generally, lower switching frequency will lead to higher efficiency. However, switching frequency should not be decreased too low due to negative current protection limit. Moreover, when output voltage is relatively high, low switching frequency will result in more sub-harmonic oscillation. Therefore, operating frequency needs to be kept relatively high under high V_{OUT} conditions. However, again, switching frequency cannot be increased too much. Otherwise, the minimum on-time limit could be violated. Based on these considerations, Figure 36 provides the recommended switching frequency under various typical V_{IN} and across V_{OUT} range.

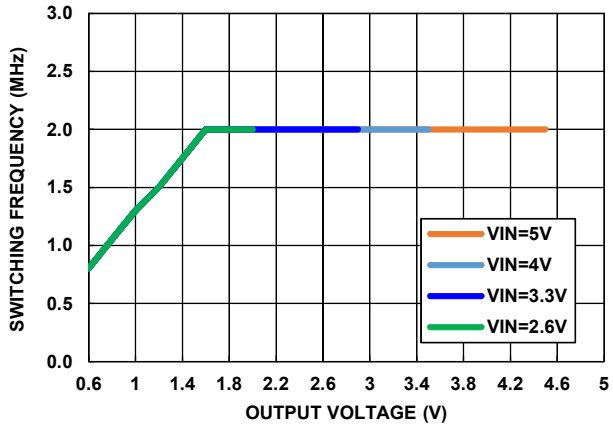


FIGURE 36. SWITCHING FREQUENCY RECOMMENDATION

Input Capacitor Selection

Selection of the input filter capacitor is based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, however, consideration should be given to the higher surge current during power-up. The ISL8202M provides a soft-start function that controls and limits the current surge. The total capacitance the input capacitor can be calculated based on Equation 4:

$$C_{IN(MIN)} = \frac{I_O \bullet D(1-D)}{V_{P-P} \bullet f_{SW}} \quad \text{(EQ. 4)}$$

Where:

- $C_{IN(MIN)}$ is the minimum required input capacitance (µF)
- I_O is the output current (A)
- D is the duty cycle
- V_{P-P} is the allowable peak-to-peak voltage (V)
- f_{SW} is the switching frequency (Hz)

Low Equivalent Series Resistance (ESR) ceramic capacitance is recommended to be placed as close as possible to the module input to reduce input voltage ripple and decouple between the VIN and PGND. This capacitance not only reduces voltage ringing created by the switching current across parasitic circuit elements but also reduce the input noise seen by the module. Moreover, the estimated RMS ripple current should be considered in choosing ceramic capacitors. The RMS ripple current can be calculated by Equation 5:

$$I_{IN(RMS)} = \frac{Io\sqrt{D(1-D)}}{\eta} \quad \text{(EQ. 5)}$$

Each 22µF X5R or X7R ceramic capacitor is typically good for 2A to 3A of RMS ripple current. Refer to the capacitor vendor to check the RMS current ratings.

Based on the above considerations, minimum total input capacitance of 44µF is required for ISL8202M. Add additional capacitance if possible. Use X5R or X7R ceramic capacitors. The placement of the input ceramic capacitors should be as close as possible to the module input. Refer to "PCB Layout Pattern Design" on page 20 for more information. A bulk input capacitance may also be needed if the input source does not have enough output capacitance. A typical value of bulk input capacitor is 100µF. In such conditions, this bulk input capacitance can supply the current during output load transient conditions.

Output Capacitor Selection

Ceramic capacitors are typically used as the output capacitors for the ISL8202M. Refer to Table 2 on page 14 for recommended output capacitor values. Bulk output capacitors that have adequately low Equivalent Series Resistance (ESR), such as low ESR polymer capacitors or a low ESR tantalum capacitor, may also be used in combination with the ceramic capacitors, depending on the output voltage ripple and transient requirements.

Feed-Forward Capacitor Selection

In typical applications where the output capacitors are all ceramic, a feed-forward capacitor, as shown as C_{FF} in Figure 1 on page 1, is needed to insure loop stability in extreme operating conditions. With internal compensation mode enabled, the C_{FF} values for typical operating conditions are optimized and listed in Table 2 on page 14. Please note that, for system parameters that are different from Table 2 or external instead of internal compensation is used, the optimized value of C_{FF} needs to be adjusted.

Typical Application Circuit

Figure 1 on page 1 only illustrates the application circuit with minimum external components required for operation in PWM mode. A more comprehensive typical application circuit diagram is shown in Figure 37. In this example, a pull-up resistor is added to the PG pin to allow power-good signal monitoring. Soft start-up time adjustment is achieved by adding a capacitor, C_{SS}, to the SS pin. Typical application circuit of PFM mode operation can also be found in Figure 38.

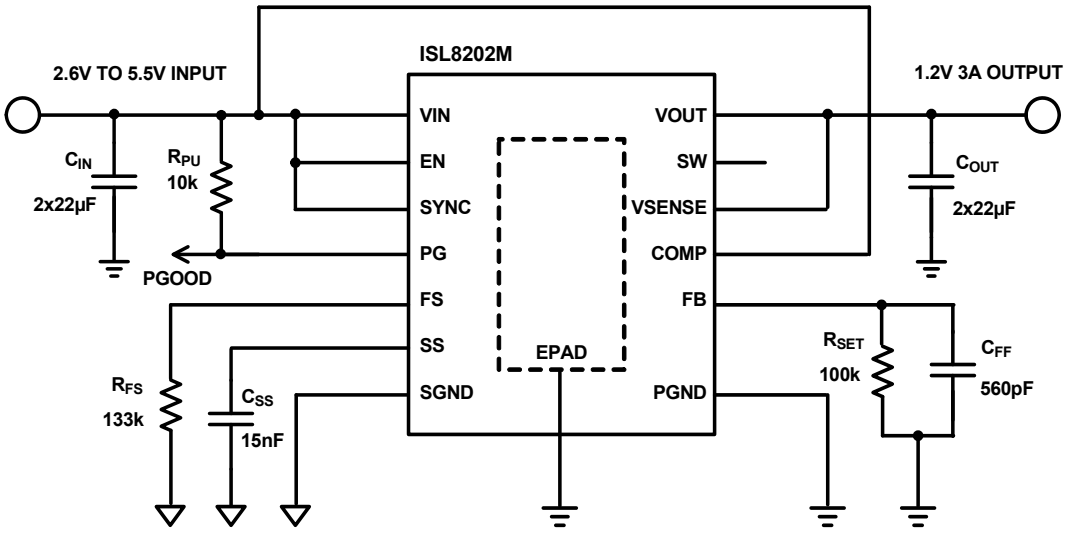


FIGURE 37. COMPLETE APPLICATION CIRCUIT DIAGRAM

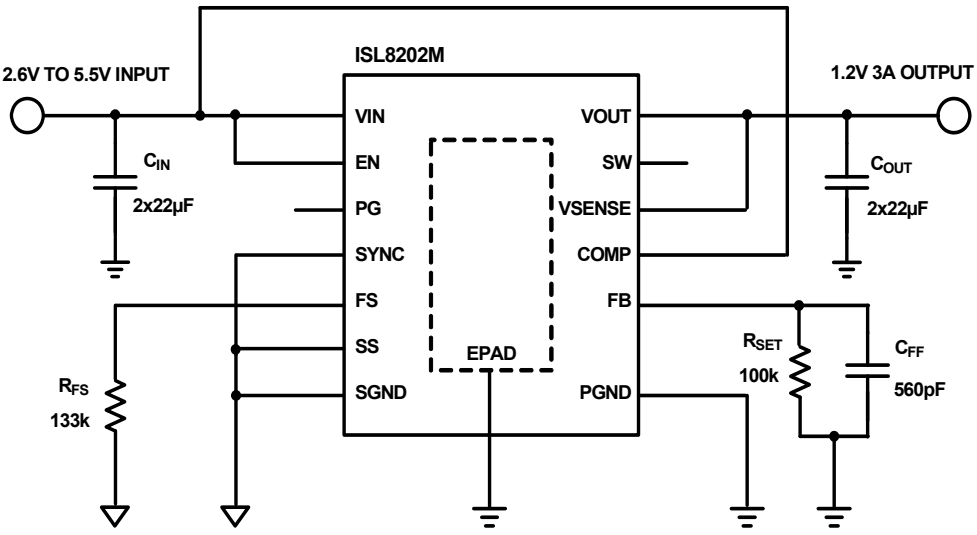


FIGURE 38. TYPICAL APPLICATION CIRCUIT DIAGRAM IN PFM MODE

Thermal Consideration and Current Derating

The ISL8202M's thermally enhanced package offers typical junction to ambient thermal resistance θ_{JA} of approximately 27.4°C/W at natural convection with a typical 4-layer PCB board. In applications with elevated ambient temperature, the continuous current handling capability of the module may need to be derated. The derating curves (Figure 30 through 33) are fully tested. They are on the basis of determining the maximum continuous load current while limiting the maximum junction temperature to +120°C, which provides 5°C margin of safety from the rated junction temperature of +125°C. The test was done across various typical operation conditions, providing a starting point for system thermal design. Note that all the derating curves are obtained based on tests in free air with the module mounted on the ISL8202MEVAL1Z evaluation board with "direct attach" features. Refer to ISL8202MEVAL1Z User Guide for evaluation board details. Also see Tech Brief TB379 for general thermal metric information.

In real applications where the system parameters and layout are different than the evaluation board, the customer can adjust the margin of safety. Other heat sources and design margins also need to be taken into consideration.

PCB Layout Recommendations

A few layout considerations need to be taken into account in order to achieve proper operation of ISL8202M. An optimized layout design also allows the module to have lower power loss and good thermal performance. An illustrative layout example is shown in Figures 39 and 40. Key points are listed in the following:

- Place the input ceramic capacitors as close as possible to the module input. These ceramic capacitors are used to minimize the high frequency noise by reducing parasitic inductance of the switching loop. Optimized placement of these capacitors will not only lead to less switch node ringing but also minimize the noise seen by the module to insure proper operation. It is recommended to use X5R or X7R ceramic capacitors with minimum total capacitance of 44µF at module input. It is a **MUST** that one of the input capacitors (C_{IN1}) with no less than 3.3µF capacitance should be placed on the same layer (assuming top layer) as module and within less than 70 mil clearance to module input (refer to Figure 39). For capacitors on the bottom layer, it is recommended to have one (C_{IN2}) placed from VIN to PGND copper close to exposed pad (Pad 20) vias (as shown in the layout example in Figure 40).
- Use large copper areas for power path (VIN, PGND) to minimize conduction loss and thermal stress. Also, it is recommended to use multiple vias to connect the power planes in different layers. Use at least 5 vias on the exposed Pad 20 connected to PGND plane(s) for the best thermal relief.
- Use a separate SGND ground copper area for components that are connected to signal ground. Connect SGND copper to module Pad 22 through multiple vias (refer to Figure 40). Because Pad 22 is connected to module internal PGND at a single location, the SGND copper area and PGND plane on the PCB can be left separated.
- It is recommended to keep the SW pads only on the top and inner layers of the PCB. Do not expose the SW pads to the outside on the bottom layer of the PCB. In order to minimize switch node resistance, connect Pads 21 and 9 using wide trace or shape.
- If remote sense is needed, route remote sensing trace from point-of-load to module VSENSE pin through quiet inner layer that is shielded by PGND planes.
- Avoid routing noise-sensitive signal traces such as FB, COMP near the noisy SW pins.
- The feedback and compensation network should be placed as close as possible to the FB pins and far away from the SW pins.

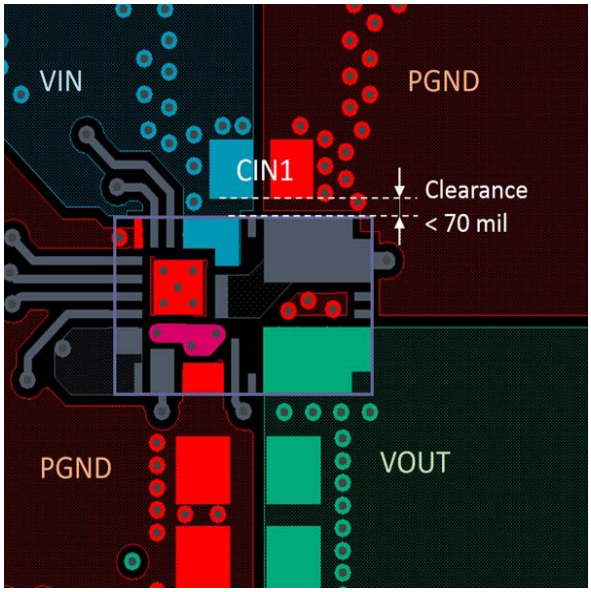


FIGURE 39. LAYOUT EXAMPLE - TOP LAYER

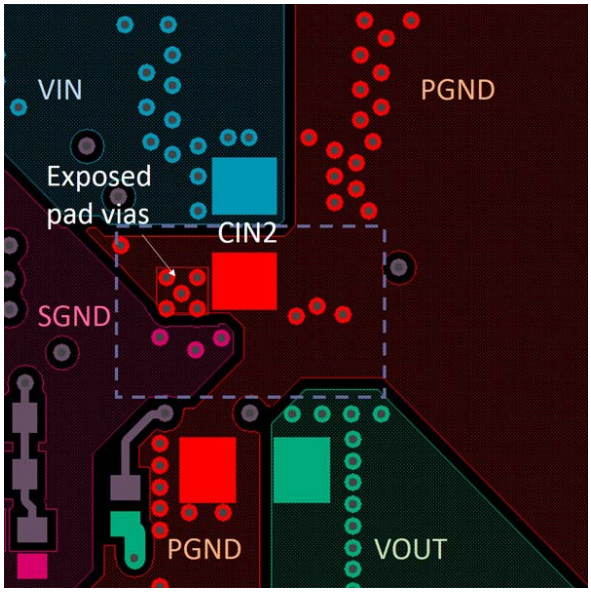


FIGURE 40. LAYOUT EXAMPLE - BOTTOM LAYER

Package Description

The ISL8202M is integrated into a Quad Flatpack No-lead (QFN) package. This package has such advantages as good thermal and electrical conductivity, low weight and small size. The QFN package is applicable for surface mounting technology and is becoming more common in the industry. The ISL8202M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly are overmolded with polymer mold compound to protect these devices.

The package outline, typical PCB layout pattern and typical stencil pattern design are shown in the L22.4.5x7.5 "Package Outline Drawing" on page 22. TB493 shows typical reflow profile parameters. These guidelines are general design rules. Users can modify parameters according to specific applications.

PCB Layout Pattern Design

The bottom of ISL8202M is a leadframe footprint, which is attached to the PCB by surface mounting. The PCB layout pattern is shown in the L22.4.5x7.5 "Package Outline Drawing" on page 22. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and the I/O termination dimensions, except that the PCB lands are slightly longer than the QFN terminations by about 0.2mm (0.4mm maximum). This extension allows for solder filleting around the package periphery and ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitched thermal vias, which drops down and connects to buried copper planes, should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 2.0 ounce copper. Although adding more vias (by decreasing pitch) improves thermal performance, it also diminishes results as more vias are added. Use only as many vias are needed for the thermal land size and as your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. The stencil aperture size to land size ratio should typically be 1:1. Aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands.

To reduce solder paste volume on the larger thermal lands, an array of smaller apertures instead of one large aperture is recommended. The stencil printing area should cover 50% to 80% of the PCB layout pattern. Consider the symmetry of the whole stencil pattern when designing the pads.

A laser-cut, stainless-steel stencil with electropolished trapezoidal walls is recommended. Electropolishing smooths the aperture walls, resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick-like paste deposit, which assists in firm component placement.

Reflow Parameters

Due to the low mount height of the QFN, "No Clean" Type 3 solder paste, per ANSI/J-STD-005, is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board. Thus it is not practical to define a specific soldering profile just for the QFN. The profile given in TB493 is provided as a guideline to customize for varying manufacturing practices and applications.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Mar 17, 2017	FN8761.4	Updated Ordering Information table tape and reel units for ISL8202MIRZ-T from 4k to 3k.
Aug 16, 2016	FN8761.3	Ordering Information table, Note 2 updated.
May 19, 2016	FN8761.2	Related Literature on page 1: Added UG071 link.
May 10, 2016	FN8761.1	Updated default setting from 1.9MHz to 1.8MHz throughout datasheet. Updated title of datasheet. Replaced Figure 1 on page 1. Updated Figure 3 on page 3. Updated typical specification for “Nominal Switching Frequency” on page 7 from 1900 to 1835. Added Note 8 on page 8. Added “Typical Application Circuit” section on page 18. On page 25, replaced Recommended Stencil Perimeter Pads view to match POD.
Mar 21, 2016	FN8761.0	Initial release.

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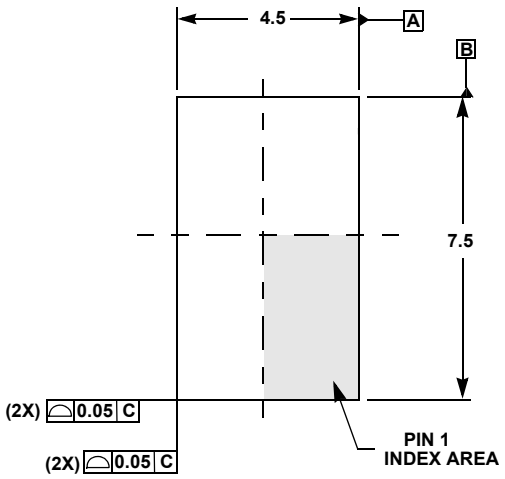
Package Outline Drawing

L22.4.5x7.5

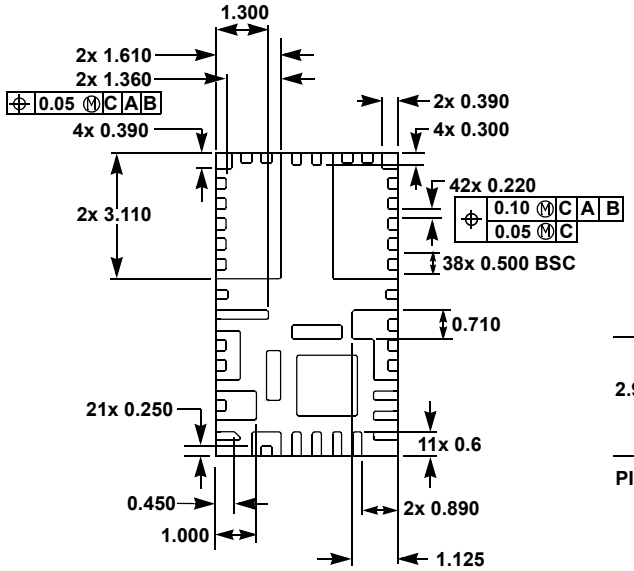
22 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

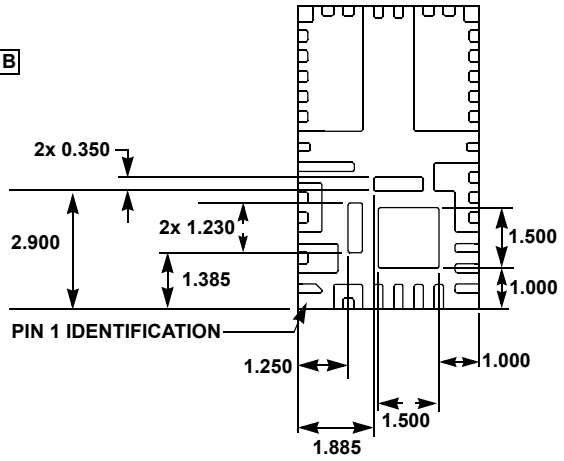
Rev 0, 9/15

For the most recent package outline drawing, see L22.4.5x7.5.

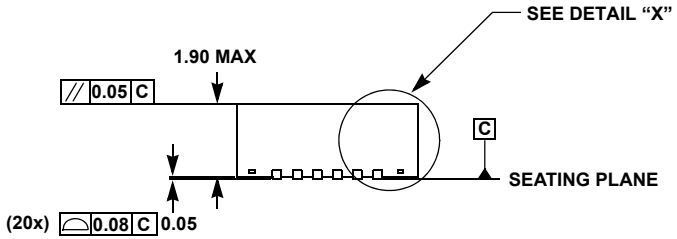


TOP VIEW

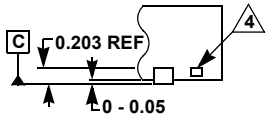




BOTTOM VIEW



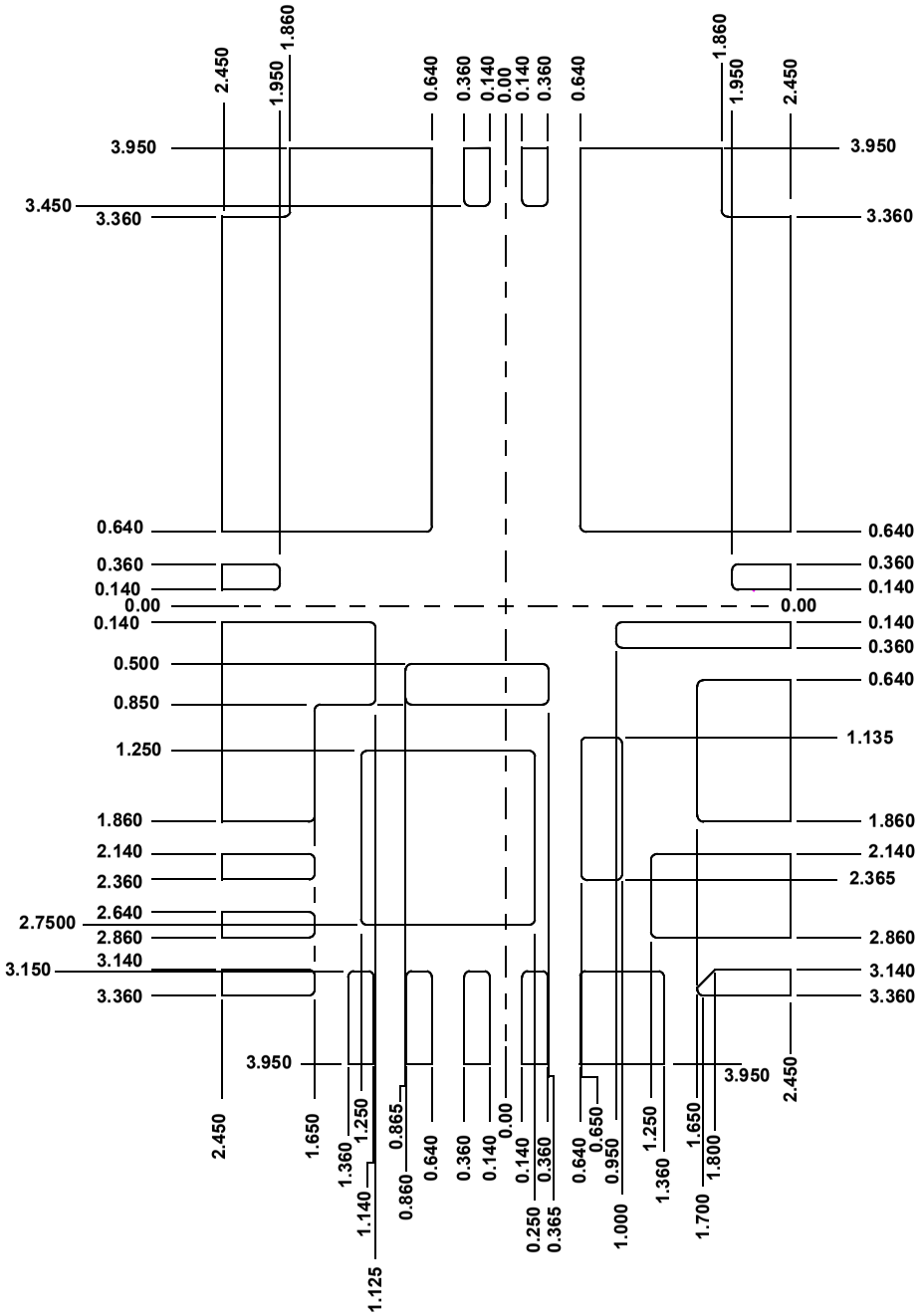
SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to ASMEY 14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05.
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.


PCB LAND PATTERN
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1.950
1.860
0.640
0.360
0.140
0.00
0.140
0.360
0.640
1.860
1.950
2.450
3.950
3.450
3.360
3.950
3.360
0.640
0.360
0.140
0.00
0.00
0.140
0.500
0.850
1.250
1.860
2.140
2.360
2.640
2.7500
2.860
3.140
3.150
3.360
0.140
0.360
0.640
1.135
1.860
2.140
2.365
2.860
3.140
3.360
3.950
3.950
2.450
2.450
1.650
1.360
1.250
1.140
1.125
0.865
0.860
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0.360
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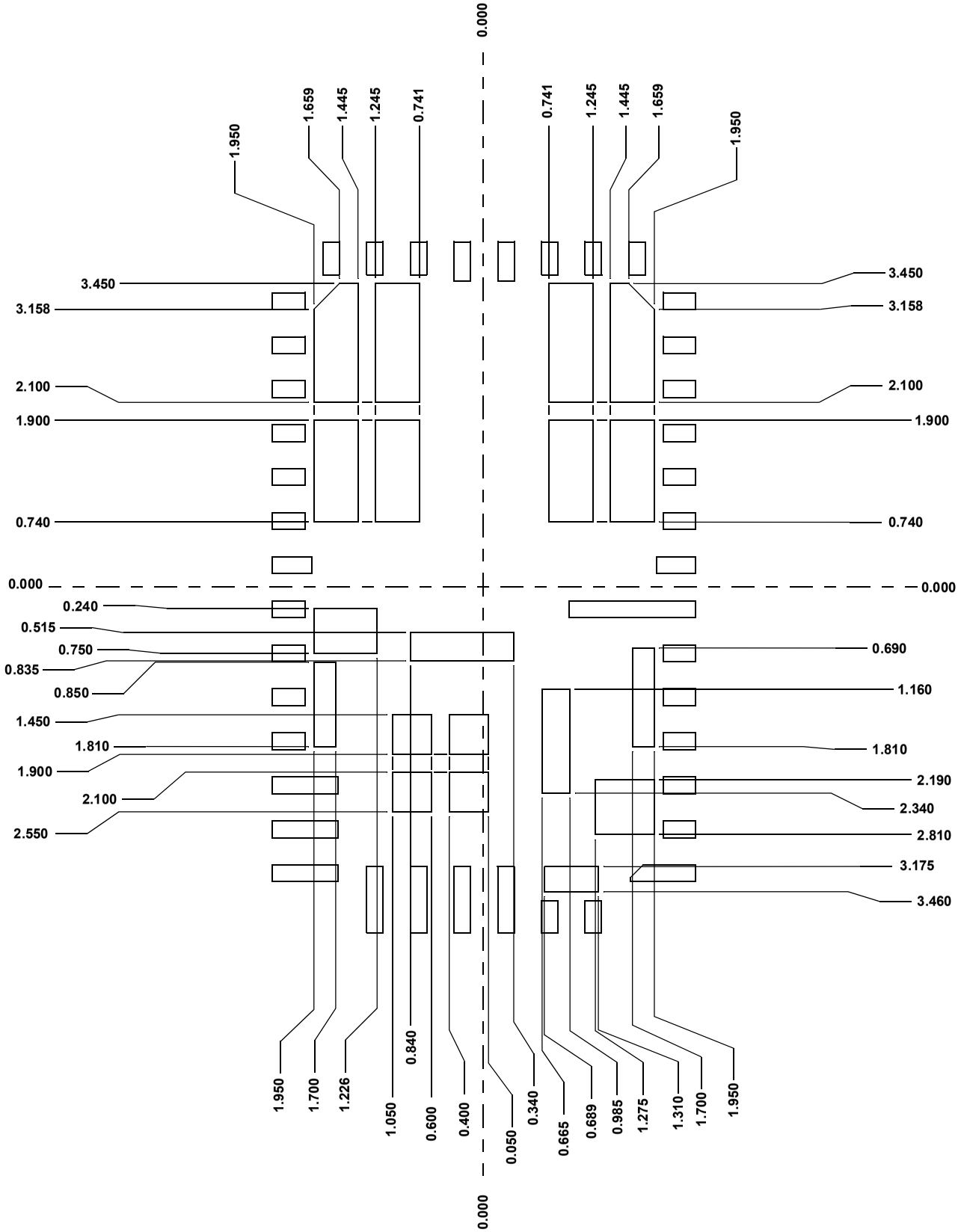
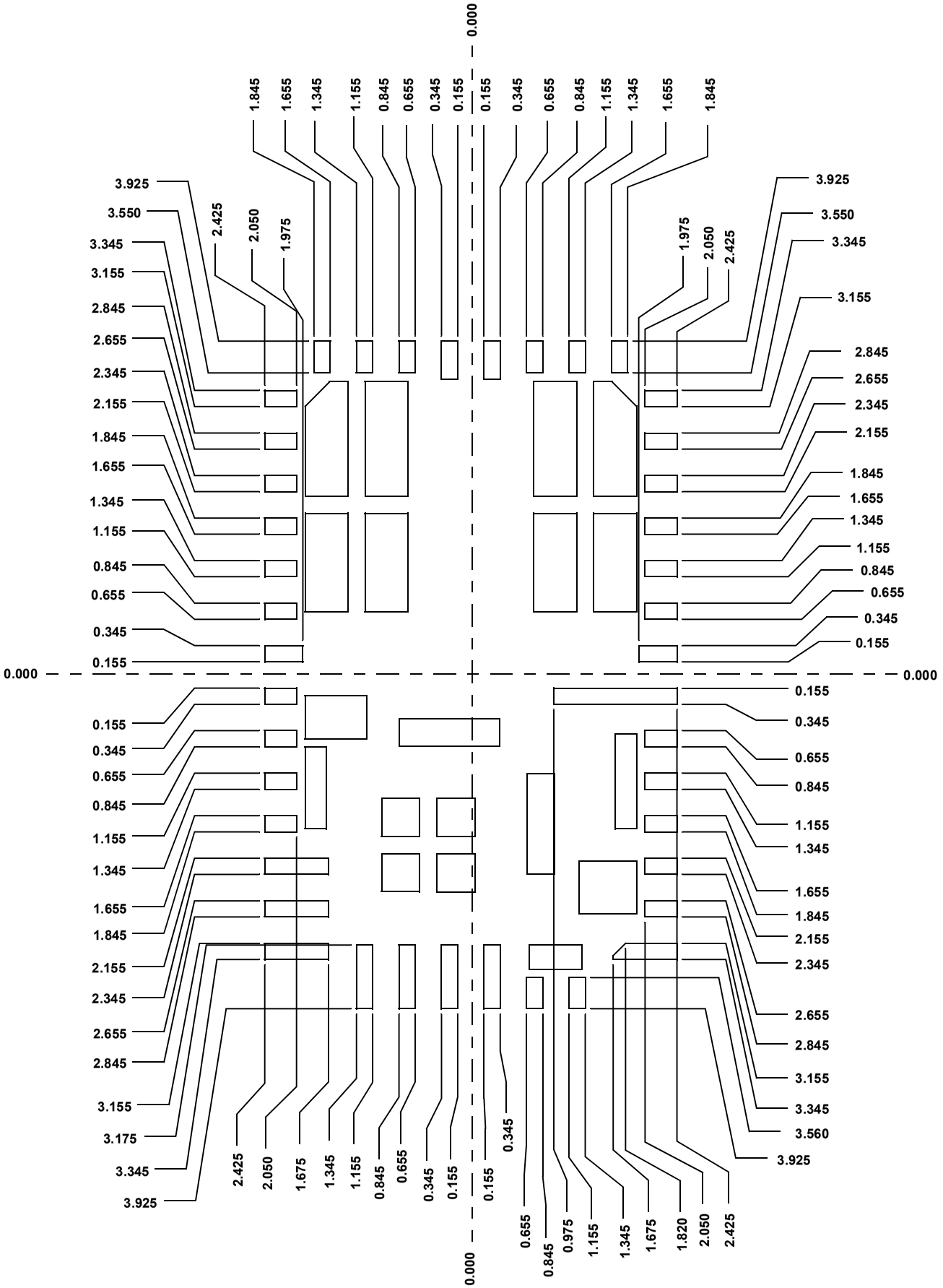
1.700



RECOMMENDED STENCIL INTERIOR PADS



RECOMMENDED STENCIL PERIMETER PADS

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