



## DC to DC Regulator

### FEATURES

- Optimized for VR12.0
- 48V (38 to 60 V<sub>IN</sub>), non-isolated ZVS buck-boost regulator
- 5 to 55 V adjustable output range
- Building block for high efficiency DC-DC systems
- 145W Output Power in 0.57 in<sup>2</sup> footprint
- 97% typical efficiency, at full load
- 1,342 W/in<sup>3</sup> (82 W/cm<sup>3</sup>) Power Density
- Enables a 48 V to 1.2 V, 130 A isolated, regulated solution with total footprint of 1.7in<sup>2</sup> (11cm<sup>2</sup>)
- Flexible “Remote Sense” architecture optimizes regulation / feedback loop design to fit application requirements
- Current Feedback signal allows dynamic adjustment of current limit setpoint
- 9.32 MHrs MTBF (MIL-HDBK-217Plus Parts Count)

### TYPICAL APPLICATIONS

- High Efficiency Server Processor and Memory Power
- High Density ATE system DC-DC power
- Telecom NPU and ASIC core power
- LED drivers
- High Density Power Supply DC-DC rail outputs
- Non-isolated power converters

### DESCRIPTION

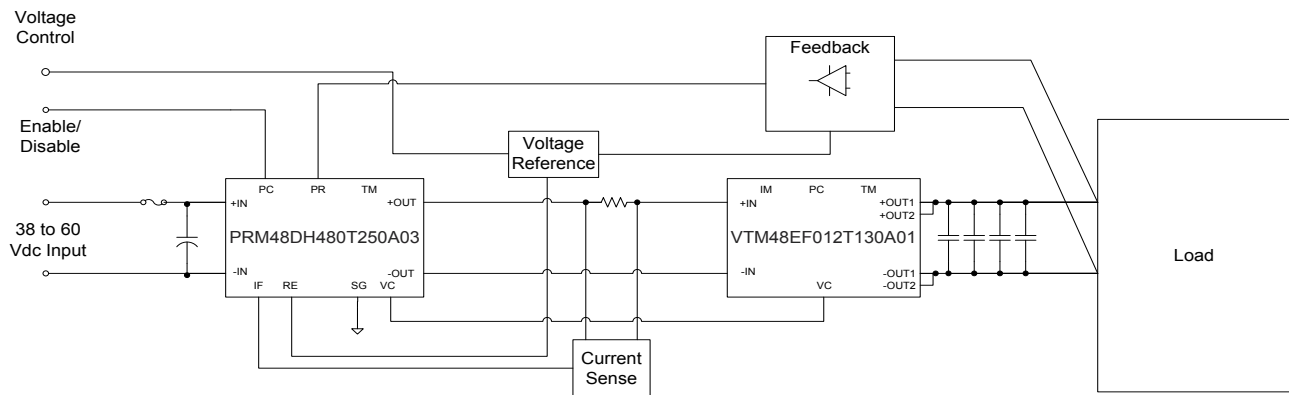
The VI Chip PRM<sup>®</sup> Regulator is a high efficiency converter, operating from a 38 to 60 Vdc input to generate a regulated 5 to 55 Vdc output. The ZVS Buck – Boost topology enables high switching frequency (~1.5 MHz) operation with high conversion efficiency. High switching frequency reduces the size of reactive components enabling power density up to 1,342 W/in<sup>3</sup>.

The half VI Chip package is compatible with standard pick-and-place and surface mount assembly processes with a planar thermal interface area and superior thermal conductivity.

In a Factorized Power Architecture<sup>™</sup> system, the PRM48DH480T250A03 and downstream VTM<sup>®</sup> transformer minimize distribution and conversion losses in a high power solution.

An external control loop and current sensor maintain regulation and enable flexibility both in the design of voltage and current compensation loops to control of output voltages and currents.

### 48 V to 1.2 V, 130A Voltage Regulator



## 1.0 ABSOLUTE MAXIMUM RATINGS

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. All voltages are specified relative to SG unless otherwise noted. Positive pin current represents current flowing out of the pin.

	Min	Max	Unit
PR	-0.3	10.5	V
PC	-0.3	5.7	V
TM	-0.3	5.7	V
+IN to -IN	-1	70	V
VS	-0.5	10.5	V
SG		±100	mA
IF	-0.5	5.7	V
RE	-0.3	5	V
VC to -OUT	-0.5	18	V
+OUT to -OUT	-1	62	V
Output Current		±5.5	A
Operating Analog IC Junction Temperature	-40	125	°C
Storage Temperature	-40	125	°C

## 2.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions,  $T_J = 25\text{ °C}$  and output voltage from 20V to 55V, unless otherwise noted.

**Boldface specifications apply over the temperature range of  $0\text{ °C} < T_J < 125\text{ °C}$ .**

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
<b>POWER INPUT SPECIFICATION</b>						
Input Voltage range	$V_{IN}$		38	48	60	V
$V_{IN}$ Slew Rate	$dV_{IN}/dt$	$0 < V_{IN} < 18\text{ V}$	0.001		1000	V/ms
No Load Power Dissipation	$P_{NL}$	PC High, $V_{IN} = 48\text{ V}$ , $V_{OUT} = 48\text{ V}$		2.2	4	W
Input Quiescent current	$I_{QC}$	PC Low, $V_{IN} = 48\text{ V}$ . $I_{QC}$ is roughly 33% of value listed if PC has never been permitted to go HIGH since power applied.		5.0	10.0	mA
Input Current	$I_{IN\ DC}$	$I_{OUT} = 4.17\text{ A}$ , $V_{IN} = 38\text{ V}$ , $V_{OUT} = 48\text{ V}$		5.5	5.7	A
Input Capacitance (Internal)	$C_{IN\ INT}$	Effective value, $V_{IN} = 48\text{ V}$ (see Fig. 20)		2		μF
Input Capacitance (Internal) ESR	$R_{Cin}$			3		mΩ
<b>POWER OUTPUT SPECIFICATION</b>						
Output Voltage range	$V_{OUT}$	See Fig.16, SOA	20	48	55	V
Output Current	$I_{OUT}$	See Fig.16, SOA			3.2	A
Output Current (Peak)	$I_{OUT\ PEAK}$	$T_{PEAK} \leq 5\text{ s}$ , $I_{OUT\ AVG} \leq 3.2\text{ A}$ , $V_{OUT\ MAX} < 52\text{ V}$			4.17	A
Output Power	$P_{OUT}$	See Fig.16, SOA			145	W
Output Turn-ON Delay	$T_{ON}$	From PC pin release to $V_{OUT}$ , $V_{IN}$ pre-applied and $T_{OFF}$ already expired		20		μs
	$T_{OFF} + T_{ON}$	From $V_{IN}$ applied to $V_{OUT}$ , PC floating		18.02		ms
Current Sharing accuracy	$I_{OUT\ FS}$	Equal input, output and PR voltage at full load; $V_{IN} = 48\text{ V}$ , $V_{OUT} = 48\text{ V}$ , exclusive of current limit			±10	%
		Equal input, output and PR voltage at full load; Over line, trim, and temperature; exclusive of current limit			See sec 10.6	%
Efficiency	$\eta$	Nominal line, full load, $V_{OUT} = 48\text{ V}$	95.3	96.7		%
		50% load and $V_{OUT} = 48\text{ V}$ ; over temperature	93			%
		50% load; over temperature	88			%
Output Discharge current	$I_{OD}$	N/A		N/A		mA
Output Voltage Ripple	$V_{OUT\ PP}$	$C_{OUT\ EXT} = 0\text{ F}$ , $I_{OUT} = 4.17\text{ A}$ , $V_{IN} = 48\text{ V}$ , $V_{OUT} = 48\text{ V}$ , 20 MHz BW		700	1050	mV
Output Inductance (Parasitic)	$L_{OUT\ PAR}$	Frequency @ 1 MHz, Simulated J-Lead model		2.5		nH
Output Capacitance (Internal)	$C_{OUT\ INT}$	Effective value, $V_{OUT} = 48\text{ V}$ (see Fig. 20)		2		μF
Output Capacitance (Internal) ESR	$R_{Cout}$			3		mΩ
<b>POWERTRAIN PROTECTIONS</b>						
Input Undervoltage Turn-ON	$V_{IN\ UVLO+}$	Instantaneous powertrain shutdown, latched after $T_{BLNK}$		36.36	37.7	V
Input Undervoltage Turn-OFF	$V_{IN\ UVLO-}$		32.1	33.56		V
Input Overvoltage Turn-ON	$V_{IN\ OVLO+}$	Instantaneous powertrain shutdown, latched after $T_{BLNK}$	60.6	63.05		V
Input Overvoltage Turn-OFF	$V_{IN\ OVLO-}$			64.12	66	V
Overcurrent (IF) and Input Over/Undervoltage Blanking Time	$T_{BLNK}$		50	120	150	μs
Output Overvoltage Threshold	$V_{OUT\ OVLO+}$	N/A	N/A	N/A	N/A	V
Thermal Shutdown Setpoint	$T_{J\ OTP}$	Instantaneous, latched shutdown; guaranteed by design, not production tested; $V_{TM} = 4.03\text{ V}$	130			°C
Overtemperature, Output Overvoltage and PC Shutdown Response Time	$T_{PROT}$			2		μs
Short Circuit Vout Threshold	$V_{SC\ VOUT}$			3.42		V
Short Circuit Vout Recovery Threshold	$V_{SC\ VOUTR}$			4.53		V
Short Circuit Vpr Threshold	$V_{SC\ VPR}$			7.1		V
Short Circuit Vpr Recovery Threshold	$V_{SC\ VPRR}$			6.9		V
Short Circuit Timeout	$T_{SC}$	Short Circuit fault latched after $V_{SC\ VOUT}$ and $V_{SC\ VPR}$ thresholds persist for this time		20		ms
Short Circuit Fault Recovery Time	$T_{SCR}$			0.1		ms
Output Power Limit	$P_{PROT}$		200			W

### 3.0 SIGNAL CHARACTERISTICS

Specifications apply over all line and load conditions,  $T_J = 25\text{ }^\circ\text{C}$  and Output Voltage from 20V to 55V, unless otherwise noted.

**Boldface specifications apply over the temperature range of  $0\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$ .**

Primary Control		PC							
<ul style="list-style-type: none"> <li>The PC pin enables and disables the PRM; When held below ~2.4 V the PRM will be disabled.</li> <li>In PRM array configurations, PC pins should be connected in order to synchronize startup.</li> <li>PC pin is 5 V during normal operation.</li> <li>It is a weak pull-down during any fault mode excluding short circuit. PC is a strong pull-down to SG if a Short Circuit fault is latched.</li> </ul>									
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit	
Analog Output	Regular Operation	PC Voltage	$V_{PC}$		<b>4.7</b>		<b>5.3</b>	V	
		PC Available Current	$I_{PC\_OP}$		<b>1.8</b>			mA	
	Startup	PC Source Current	$I_{PC\_EN}$	After $T_{OFF}$		90		$\mu\text{A}$	
		Minimum Time to Start	$T_{OFF}$	Section 5.0	<b>6.8</b>	12.3	<b>17.8</b>	ms	
Digital Input / Output	Startup	PC Enable Threshold	$V_{PC\_EN}$			2.50	<b>3.20</b>	V	
		PC Disable Threshold	$V_{PC\_DIS}$		<b>1.75</b>	2.40		V	
	Standby	PC Resistance to disable	$R_{PC\_EXT}$	Max Resistance to SG required to disable the PRM			<b>300</b>	$\Omega$	
Digital Output [Short Circuit Fault]	Fault	PC Sink Current to SG	$I_{PC\_SC}$	Short circuit, PC Voltage 1 V or above		25		mA	
Digital Output [All other Faults]	Fault	PC Sink Current to ~1V	$I_{PC\_FAULT}$	Temperature, Over- and Under-Voltage, Overcurrent		10		$\mu\text{A}$	

Voltage Source		VS							
<ul style="list-style-type: none"> <li>Intended to power feedback components and/or auxiliary circuits.</li> <li>9 V, 5mA regulated voltage source</li> <li>With &gt; 5% output load, VS ripple typically 100mV</li> </ul>									
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit	
Analog Output	Regular Operation	VS Voltage	$V_{VS}$		<b>8.55</b>	9.00	<b>9.45</b>	V	
		VS Available Current	$I_{VS}$		<b>5</b>			mA	
		VS Voltage Ripple	$V_{VS\_PP}$	I <sub>out</sub> = 0A, C <sub>vs_ext</sub> =0. Maximum specification includes powertrain operation in burst mode.		330	<b>500</b>	mV	
	Transition	VS Capacitance (External)	$C_{VS\_EXT}$				<b>0.04</b>	$\mu\text{F}$	
		VS Fault Response Time	$T_{FR\_VS}$	From fault recognition to VS = 1.5 V		30		$\mu\text{s}$	

Reference Enable		RE							
<ul style="list-style-type: none"> <li>RE signals successful startup and powertrain ready to operate</li> <li>Intended to power and enable the feedback circuit reference</li> <li>3.3V, 8mA regulated voltage source</li> </ul>									
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit	
Analog Output	Regular Operation	RE Voltage	$V_{RE}$		<b>3.0</b>	3.3	<b>3.6</b>	V	
		RE Available Current	$I_{RE}$		<b>8.0</b>			mA	
		RE Regulation	$\%_{RE}$	across load and temperature		$\pm 2.5$		%	
		RE Voltage Ripple	$V_{RE\_PP}$	includes powertrain in burst mode		105		mV	
	Transition	PC to RE Delay	$T_{PC\_RE}$	Fault detected		100		$\mu\text{s}$	
		RE Capacitance (External)	$C_{RE\_EXT}$				<b>0.1</b>	$\mu\text{F}$	
		VS to RE Delay	$T_{VS\_RE}$	VS = 8.1 V to RE high, $V_{IN} > V_{IN\_UVLO}$		1		ms	

Control Node		PR							
<ul style="list-style-type: none"> <li>Modulator control node input</li> <li>0.5mA constant current sink when externally driven</li> <li>0.79V, up to 2mA voltage source when externally pulled low</li> </ul>									
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit	
Analog Input	Regular Operation	PR Voltage Active Range	$V_{PR}$		<b>0.79</b>		<b>7.40</b>	V	
		PR Source Current	$I_{PR}$	$V_{PR} \leq 0.79\text{V}$			<b>2</b>	mA	
		PR Sink Current	$I_{PR\_LOW}$	$V_{PR} > 0.79\text{V}$	<b>250</b>	500	<b>750</b>	$\mu\text{A}$	
		PR Resistance to SG (Internal)	$R_{PR}$			93.3		k $\Omega$	

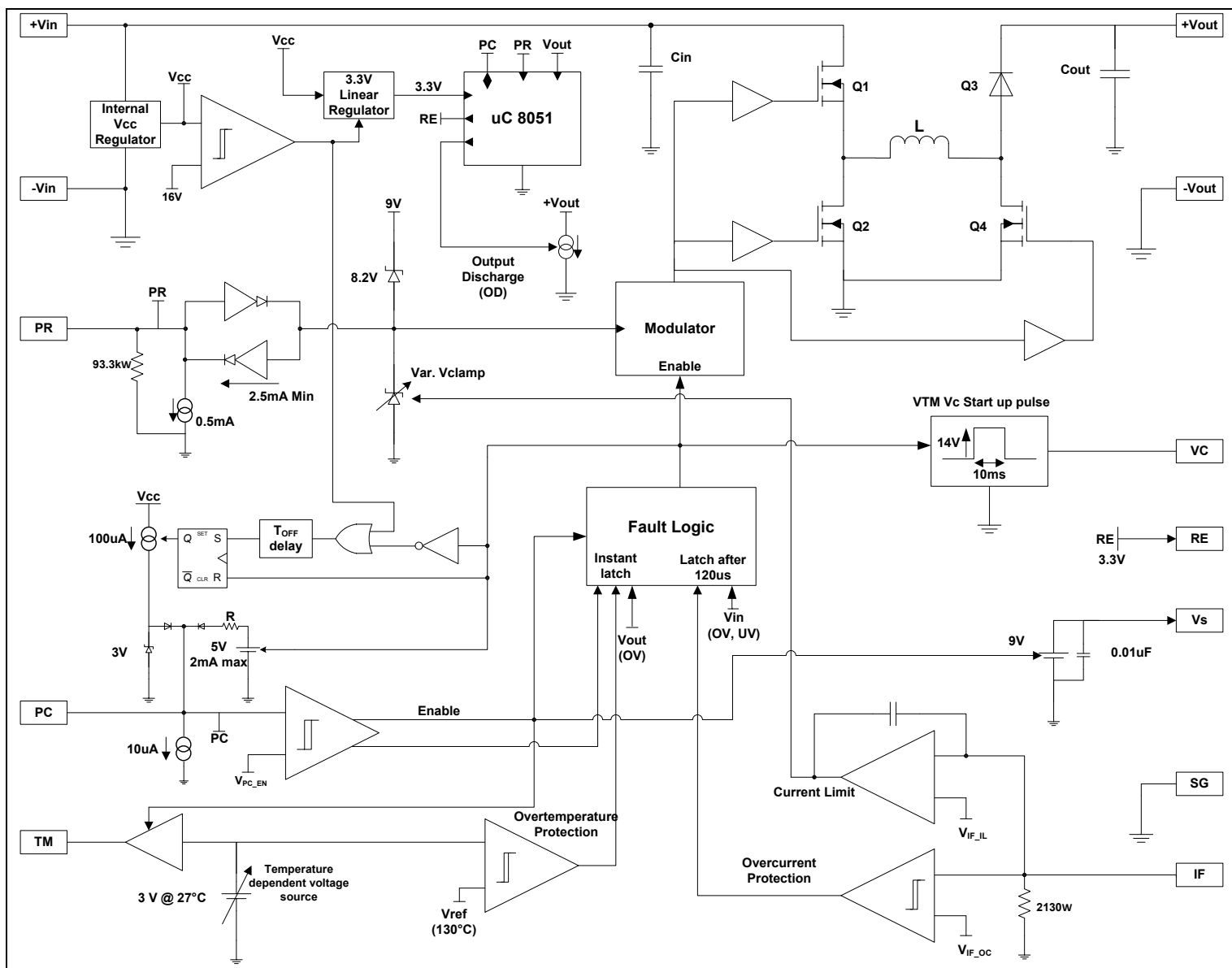
Current Feedback		IF							
<ul style="list-style-type: none"> <li>A voltage proportional to the PRM output current must be supplied externally to the IF pin in order for the device to properly protect overcurrent events and to enable output current limit (clamp)</li> <li>Overcurrent protection trip will cause instantaneous powertrain disable, latched after <math>T_{BLNK}</math></li> </ul>									
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit	
Analog Input	Regular Operation	Current Limit (clamp) Threshold	$V_{IF\_IL}$	$V_{IN} = 48\text{V}; T_J = 25\text{ }^\circ\text{C}$	1.90	2.00	2.10	V	
		Overcurrent Protection Threshold	$V_{IF\_OC}$	Not Production Tested; Guaranteed by Design; $T_J = 25\text{ }^\circ\text{C}$	2.58	2.69	2.80	V	
		IF Input Impedance	$R_{IF}$		<b>2.11</b>	2.13	<b>2.15</b>	k $\Omega$	
		Current Limit Bandwidth	$BW_{IL}$			2		kHz	

Temperature Monitor		TM						
<ul style="list-style-type: none"> <li>The TM pin monitors the internal temperature of the PRM analog control IC to within <math>\pm 5</math> °C.</li> <li>Room temperature setpoint is <math>\sim 3</math> V, approximate gain is 10 mV/°C.</li> <li>"Power Good" flag to verify that the PRM is operating</li> </ul>								
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Regular Operation	TM Voltage	$V_{TM}$	Full temperature range	2.12		4.04	V
		TM Voltage reference	$V_{TM\_AMB}$	$T_J = 27$ °C	2.94	3.00	3.06	V
		TM Voltage Ripple	$V_{VS\_PP}$	powertrain in burst mode		210		mV
		TM Available Current	$I_{TM}$		100			$\mu$ A
		TM Gain	$A_{TM}$			10		mV/°C
Digital Output [Fault Flag]	Fault or Standby	TM Disabled Current	$I_{TM\_DIS}$	DC state with TM Voltage +/- 0.5V. This is a high impedance state.		0.0		mA

Signal Ground		SG						
<ul style="list-style-type: none"> <li>All control signals must be referenced to this pin, with the exception of VC</li> <li>SG is internally connected to -IN and -OUT</li> </ul>								
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input / Output	Any	Maximum Allowable Current	$I_{SG}$		-100		100	mA

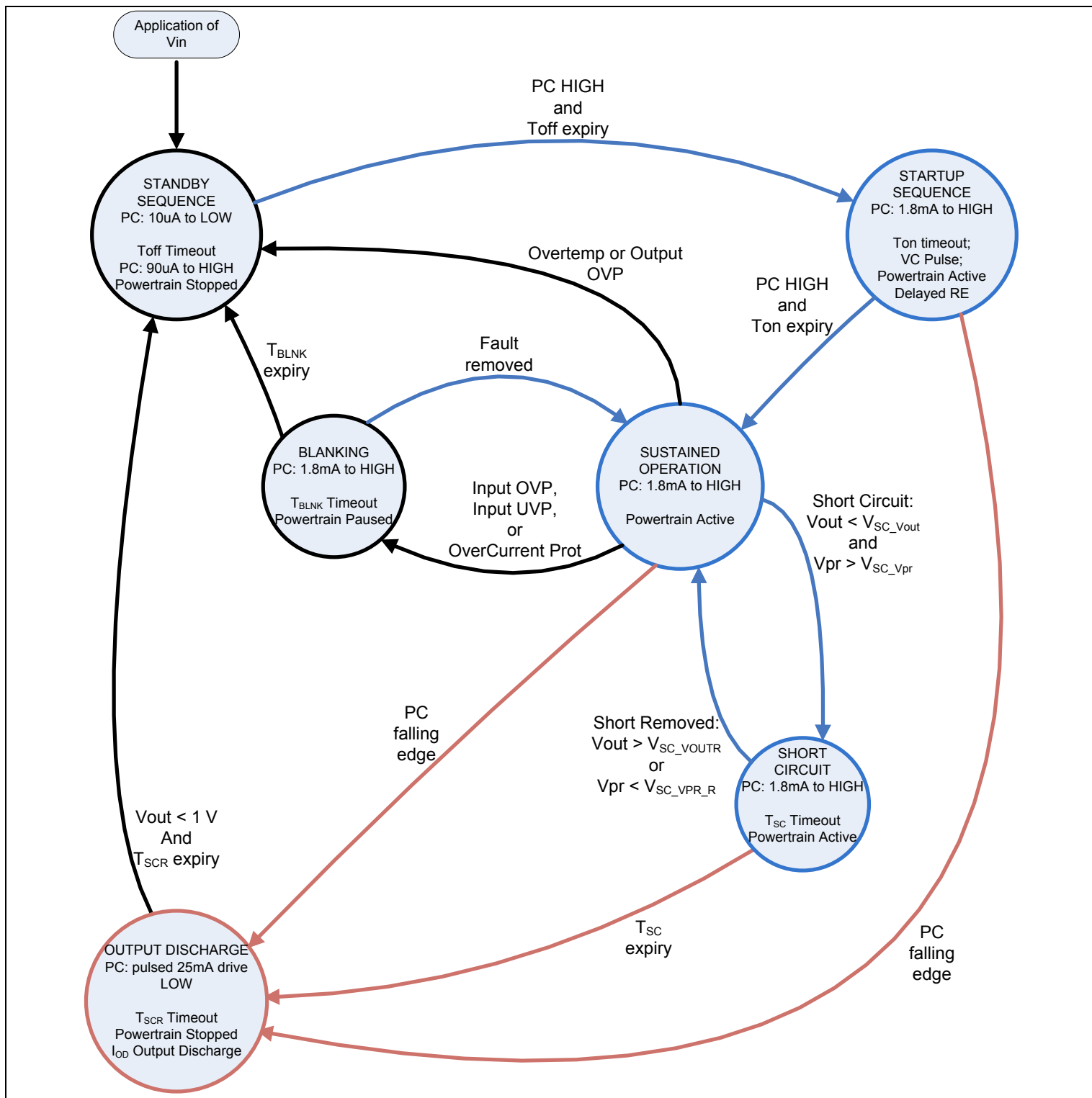
VTM Control		VC						
<ul style="list-style-type: none"> <li>Used to synchronize start up of downstream VTM converter.</li> <li>14V nominal, 10ms voltage pulse</li> <li>If not used, must be resistively terminated to -OUT</li> </ul>								
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Startup	VC Voltage	$V_{VC}$	$R_{VC} = 68\Omega$	13			V
		VC Current Limit	$I_{VC}$	$V_C = 14$ V, $V_{IN} > 20$ V	200	500		mA
		VC duration	$T_{VC}$		7	10		ms
		VC Slew Rate	$dV_C/dt$	$R_{VC} = 1k\Omega$		20		V/ $\mu$ s

4.0 FUNCTIONAL BLOCK DIAGRAM



**HIGH LEVEL FUNCTIONAL STATE DIAGRAM**

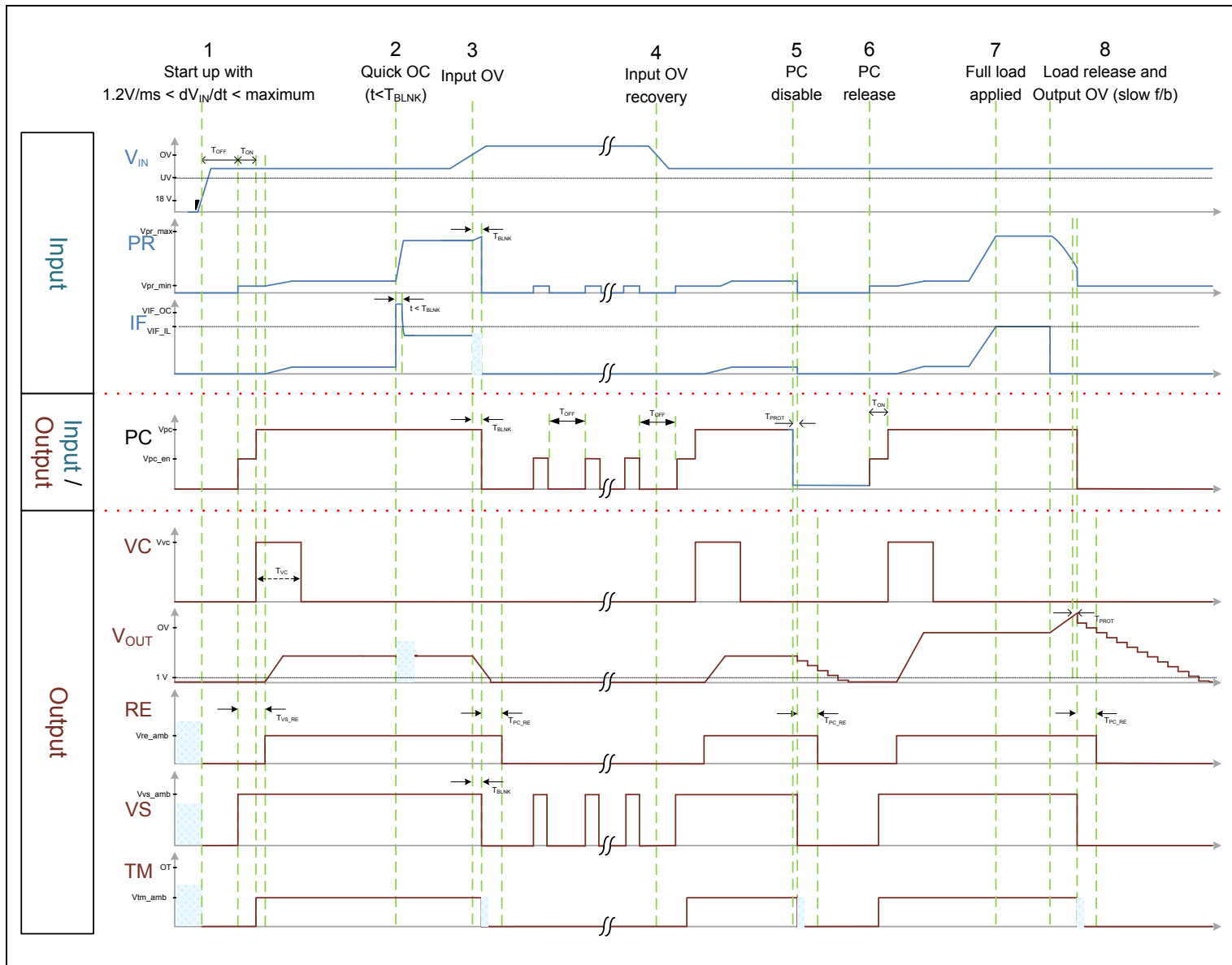
Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.

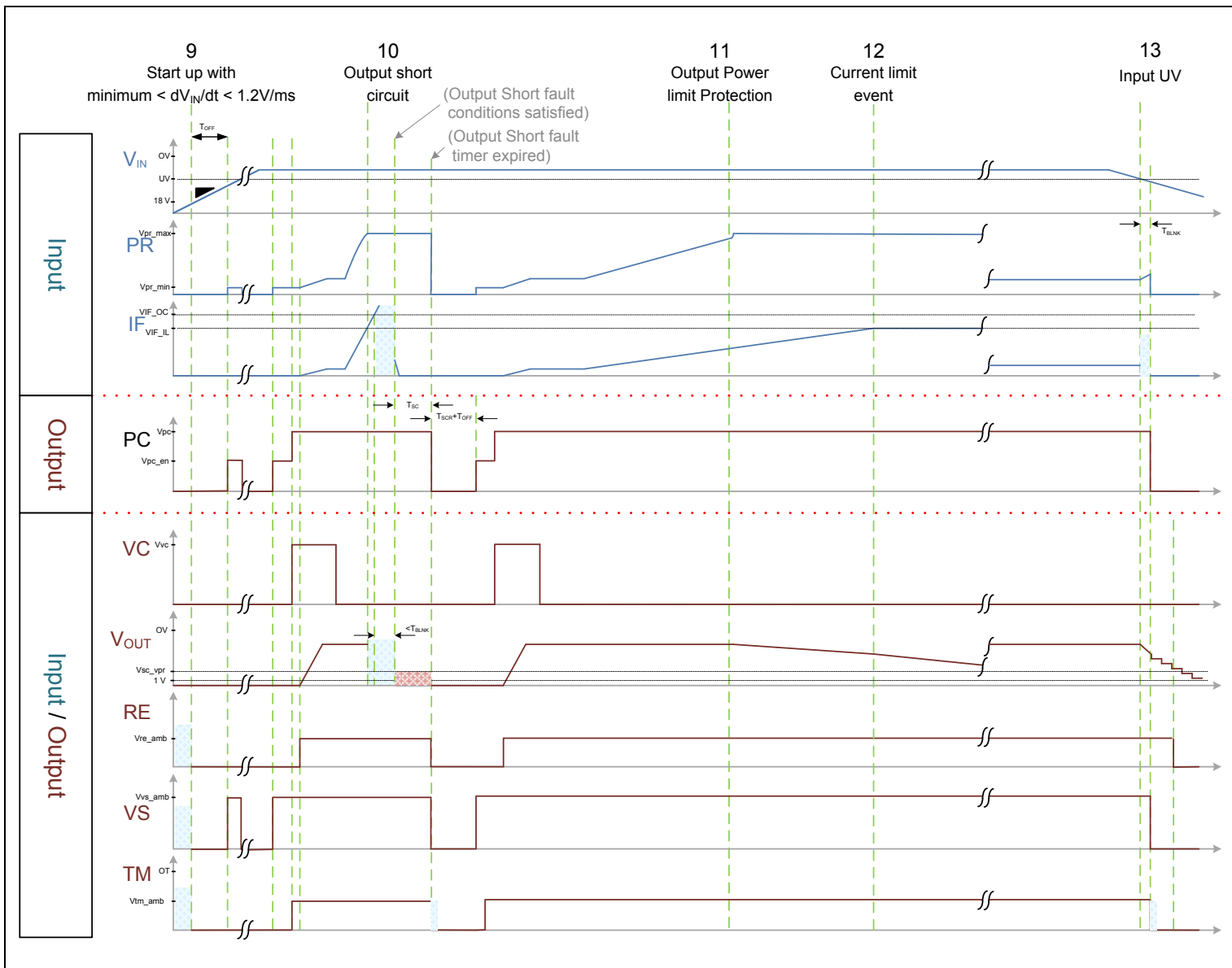


5.0 TIMING DIAGRAMS

Module Inputs are shown in blue; Module Outputs are shown in brown; Timing diagrams assumes the following:

- Single PRM (no array)
- VS powers error amplifier
- RE powers voltage reference and output current transducer
- I<sub>OUT</sub> is sensed, scaled, and fed back to IF pin such that IF = 2.00 V at full load







6.0 APPLICATIONS CHARACTERISTICS

The following figures present typical performance at  $T_C = 25^\circ\text{C}$ , unless otherwise noted. See associated figures for general trend data.

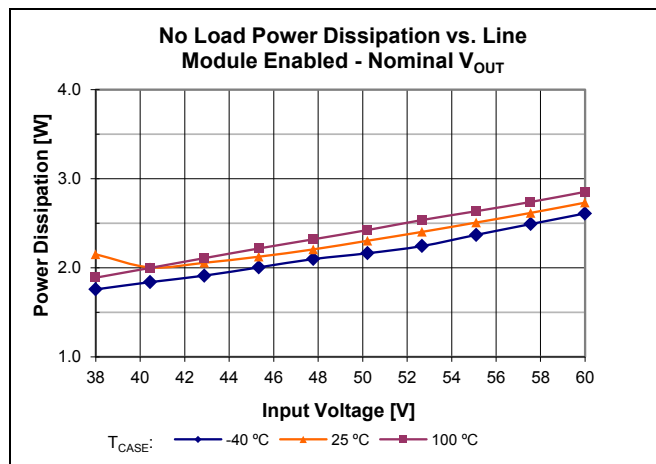


Figure 1 - No load power dissipation vs.  $V_{IN}$ , module enabled

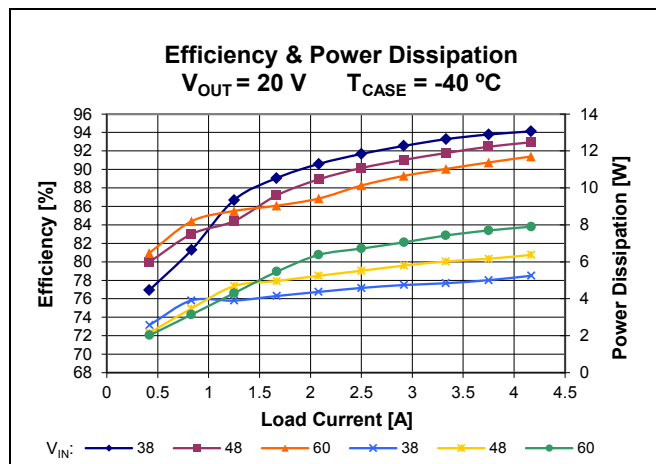


Figure 3 - Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 20\text{V}$ ,  $T_{CASE} = -40^\circ\text{C}$

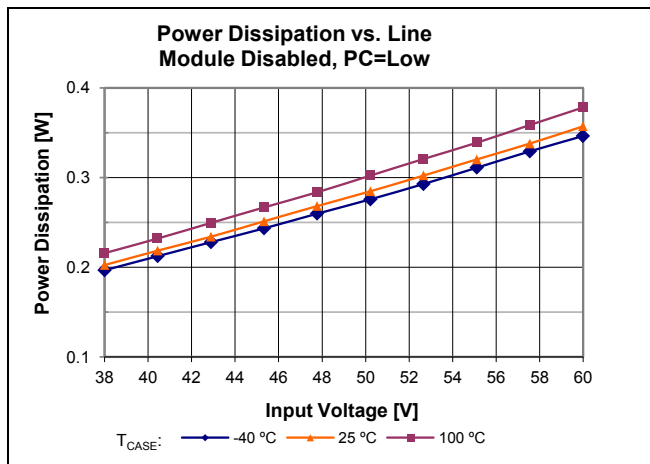


Figure 2 - Power dissipation vs.  $V_{IN}$ , module disabled

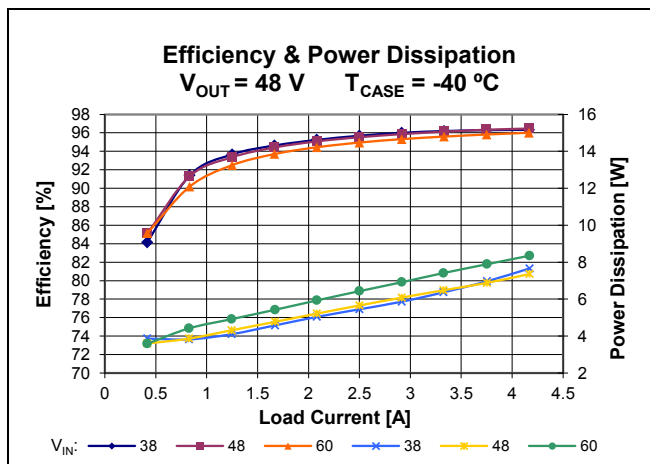


Figure 4 - Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 48\text{V}$ ,  $T_{CASE} = -40^\circ\text{C}$

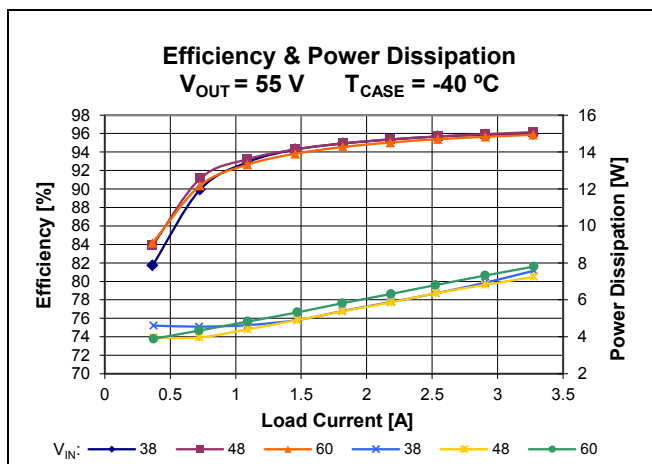


Figure 5 – Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 55V$ ,  $T_{CASE} = -40^{\circ}C$

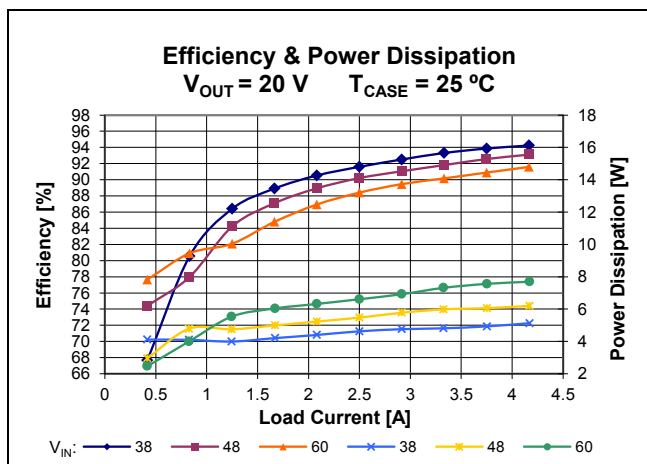


Figure 6 – Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 20V$ ,  $T_{CASE} = 25^{\circ}C$

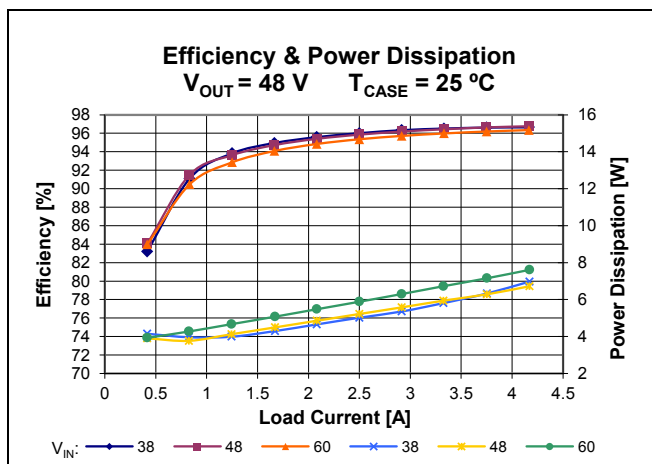


Figure 7 – Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 48V$ ,  $T_{CASE} = 25^{\circ}C$

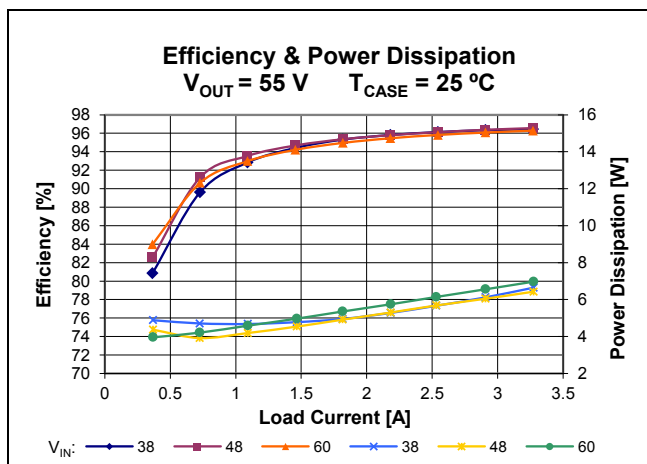


Figure 8 – Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 55V$ ,  $T_{CASE} = 25^{\circ}C$

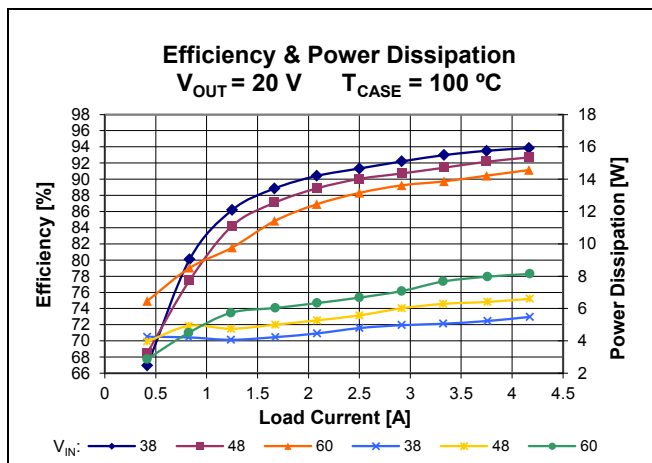


Figure 9 – Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 20V$ ,  $T_{CASE} = 100^{\circ}C$

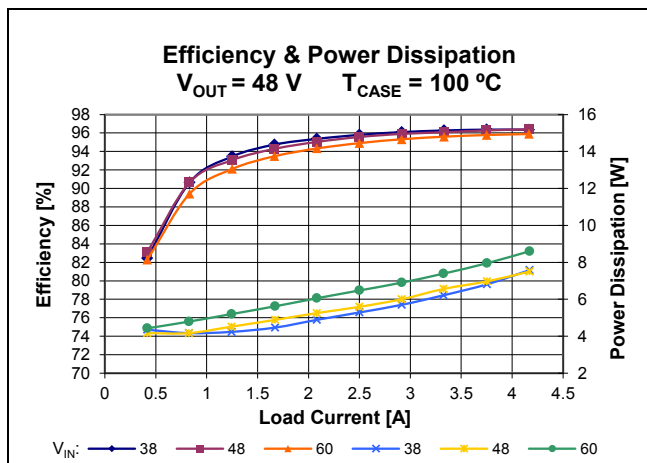


Figure 10 – Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 48V$ ,  $T_{CASE} = 100^{\circ}C$

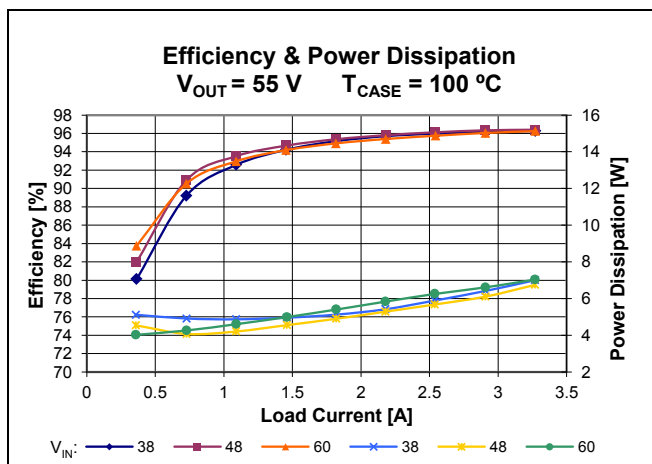


Figure 11 – Total efficiency and power dissipation vs.  $V_{IN}$  and  $I_{OUT}$ ,  $V_{OUT} = 55V$ ,  $T_{CASE} = 100^{\circ}C$

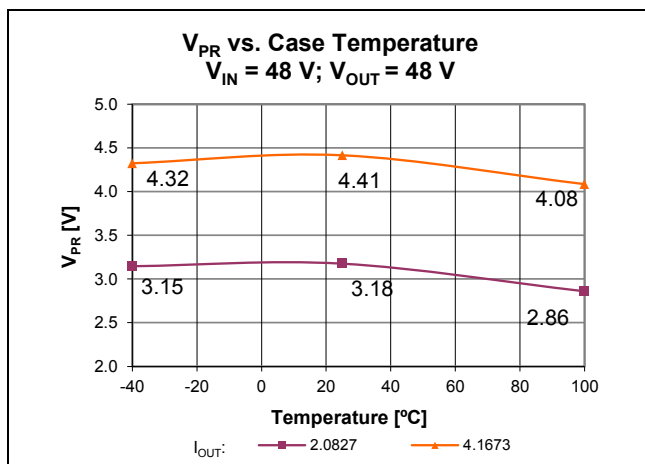


Figure 12 – Typical control node voltage vs.  $T_{CASE}$ , and  $I_{OUT}$ ;  $V_{IN} = 48V$ ,  $V_{OUT} = 48V$

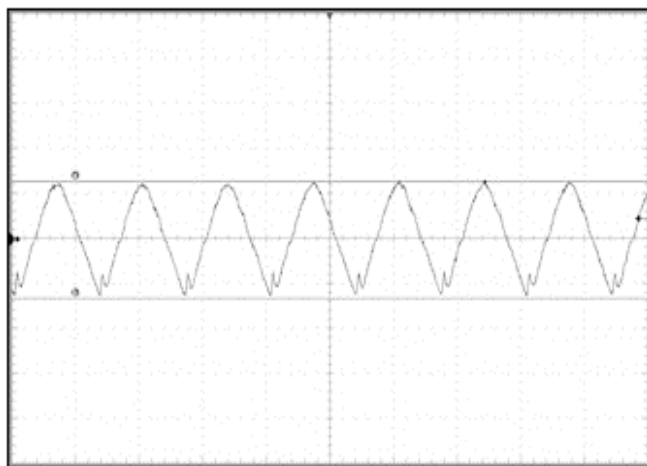


Figure 13 – Typical output voltage ripple waveform, 200 mV/div, 500 ns/div  $T_{CASE} = 30^{\circ}C$ ,  $V_{IN} = 48V$ ,  $V_{OUT} = 48V$ ,  $I_{OUT} = 3.2 A$ , no external output capacitance.

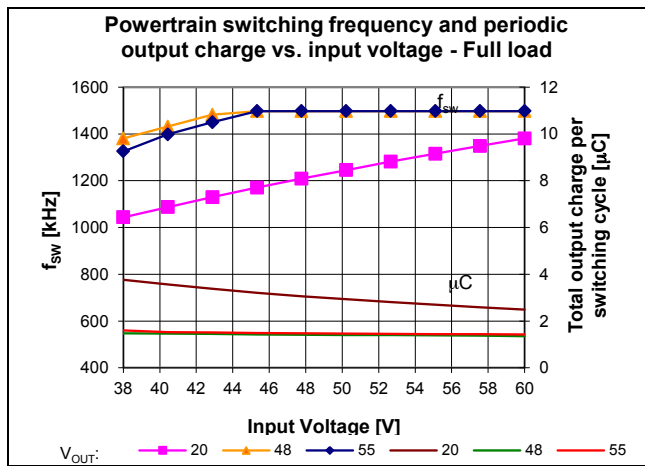


Figure 14 – Powertrain switching frequency and periodic output charge vs.  $V_{IN}$ ,  $V_{OUT}$ ;  $I_{OUT} = 3.2 A$

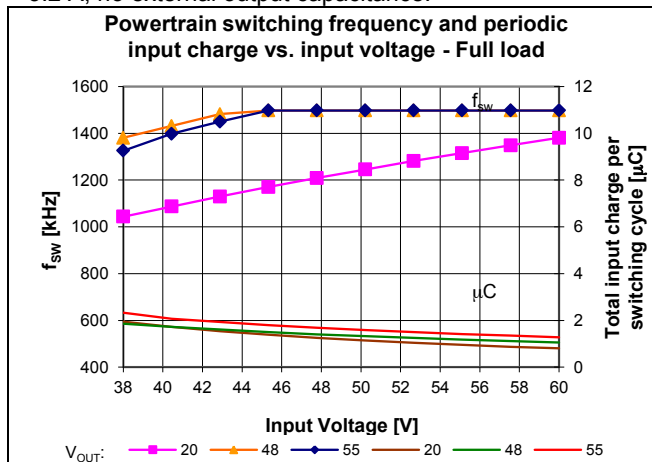


Figure 15 – Powertrain switching frequency and periodic input charge vs.  $V_{IN}$ ,  $V_{OUT}$ ;  $I_{OUT} = 3.2 A$

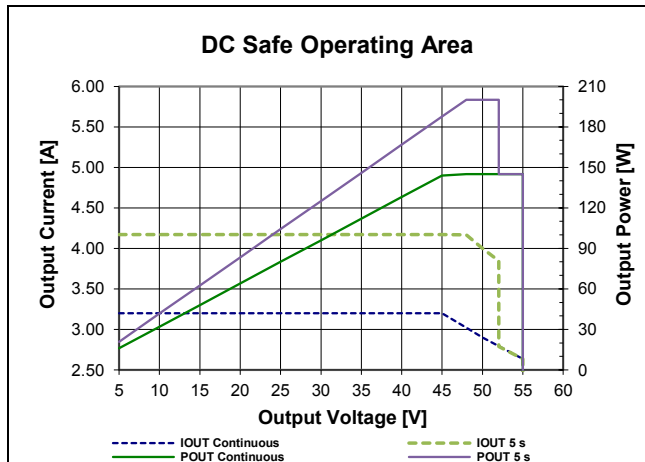


Figure 16 – DC Output Safe Operating Area

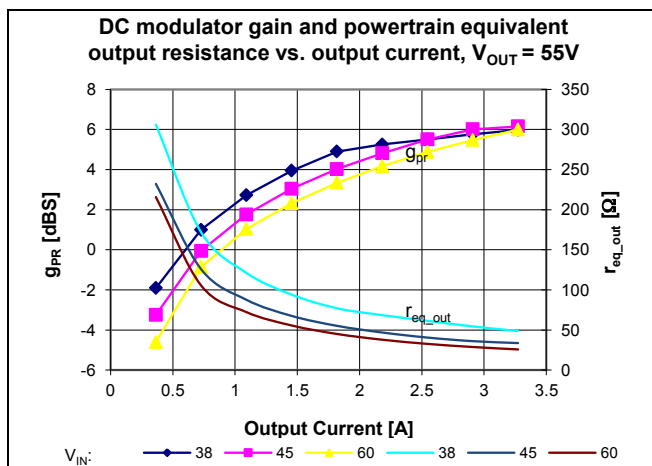


Figure 17 – Powertrain characteristics vs.  $I_{OUT}$ ; Resistive load,  $V_{OUT} = 55V$ , various  $V_{IN}$

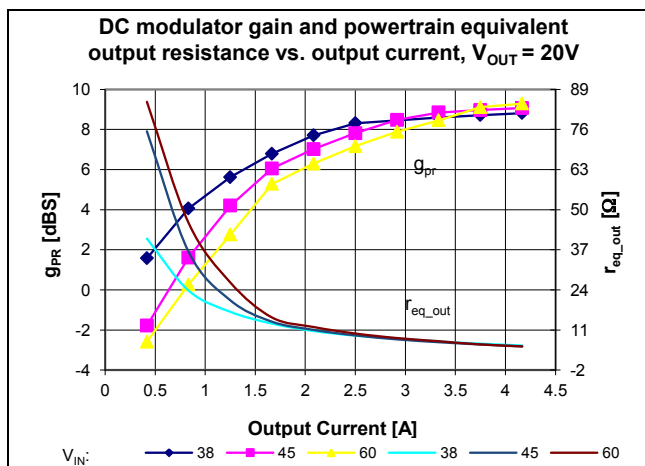


Figure 18 – Powertrain characteristics vs.  $I_{OUT}$ ; Resistive load,  $V_{OUT} = 20V$ , various  $V_{IN}$

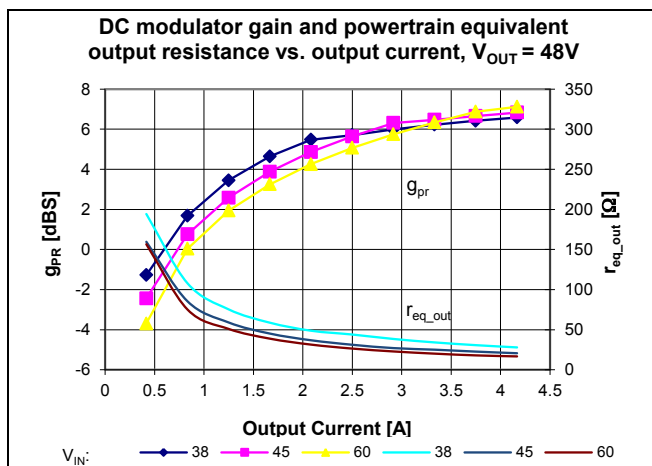


Figure 19 – Powertrain characteristics vs.  $I_{OUT}$ ; Resistive load,  $V_{OUT} = 48V$ , various  $V_{IN}$

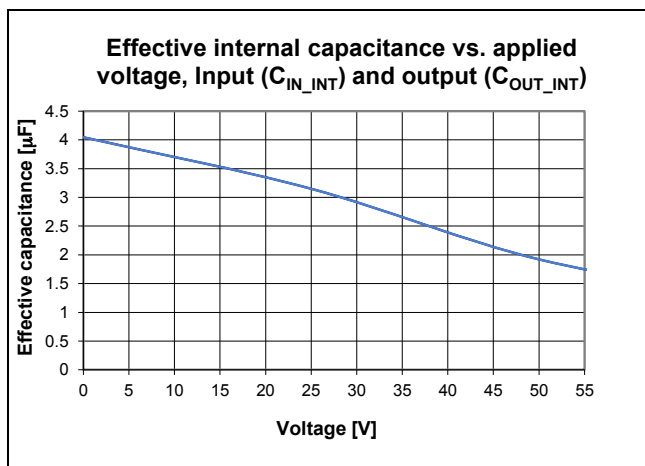


Figure 20 – Effective internal input and output capacitance vs. voltage – ceramic type

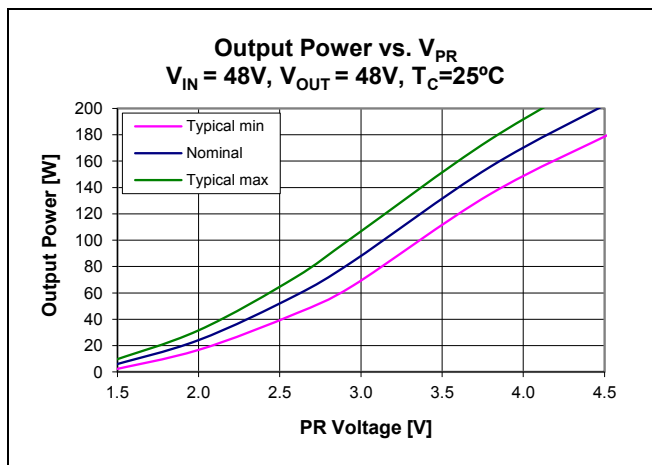


Figure 21 – Output Power vs.  $V_{PR}$ ;  $V_{IN} = 48V$ ,  $V_{OUT} = 48V$ ,  $T_{CASE} = 25^{\circ}C$

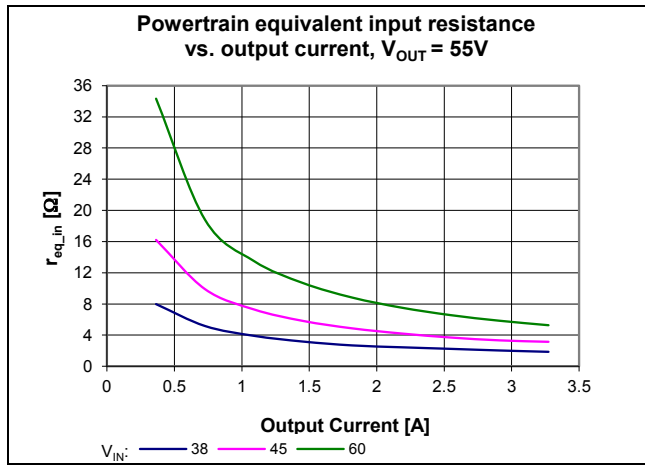


Figure 22 – Magnitude of powertrain dynamic input impedance vs.  $V_{IN}$ ,  $I_{OUT}$ ;  $V_{OUT} = 55V$

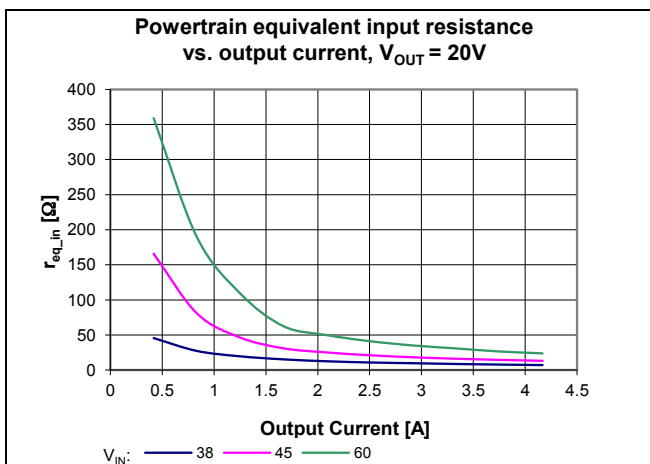


Figure 23 – Magnitude of powertrain dynamic input impedance vs.  $V_{IN}$ ,  $I_{OUT}$ ;  $V_{OUT} = 20V$

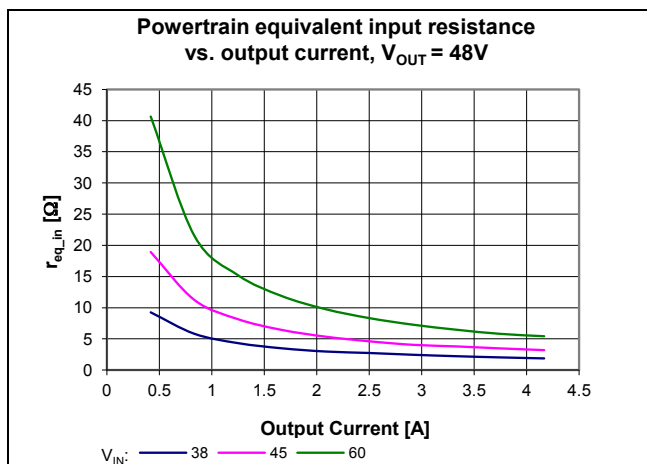


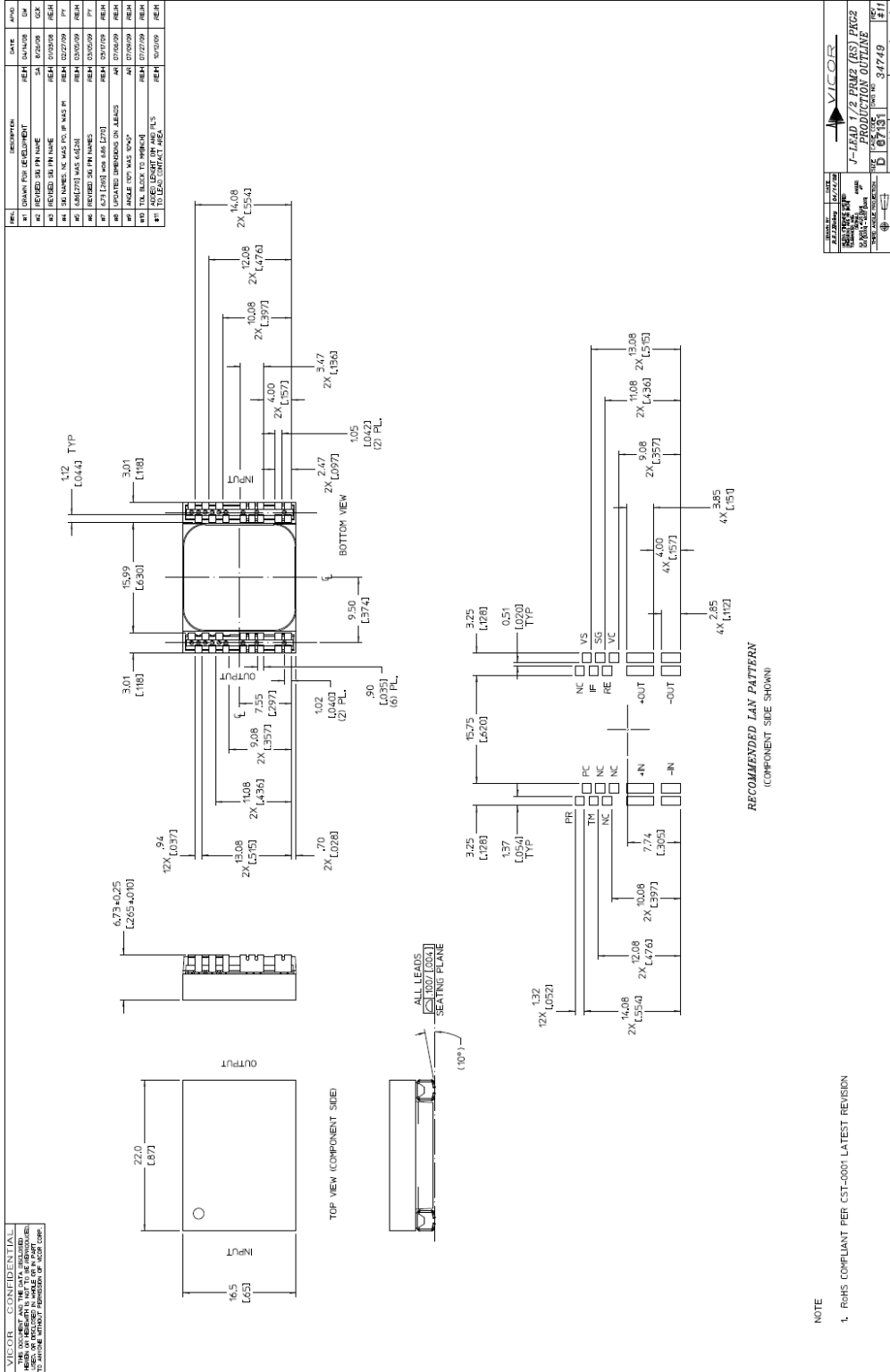
Figure 24 – Magnitude of powertrain dynamic input impedance vs.  $V_{IN}$ ,  $I_{OUT}$ ;  $V_{OUT} = 48V$

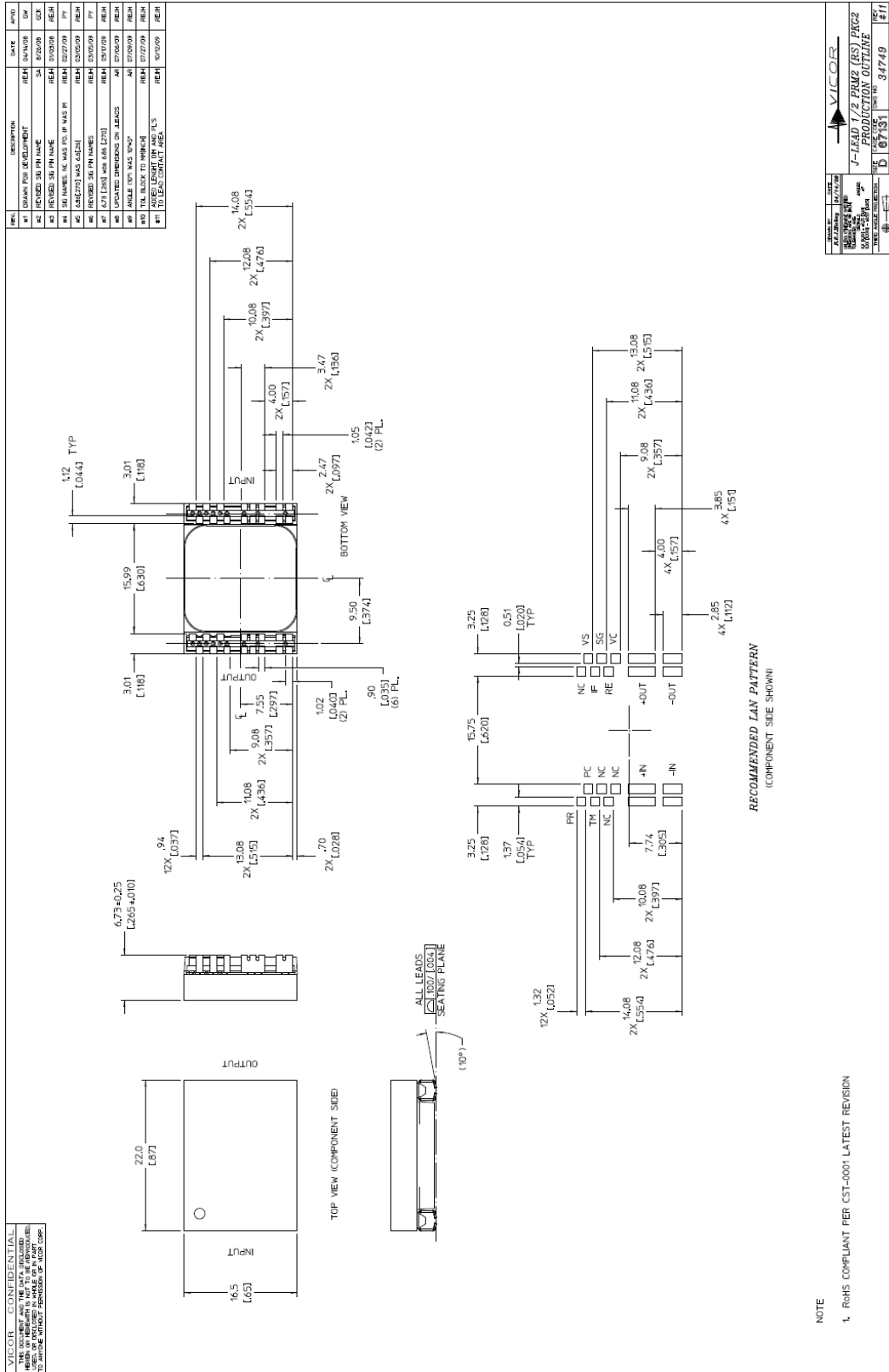
7.0 GENERAL CHARACTERISTICS

Specifications apply over all line and load conditions,  $T_J = 25\text{ °C}$  and Output Voltage from 20V to 55V, unless otherwise noted. **Boldface specifications apply over the temperature range of  $0\text{ °C} < T_J < 125\text{ °C}$ .**

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
<b>MECHANICAL</b>						
Length	L		21.8 / [0.86]	22.0 / [0.87]	22.3 / [0.88]	mm / [in]
Width	W		16.3 / [0.64]	16.5 / [0.65]	16.8 / [0.66]	mm / [in]
Height	H		6.48 / [0.255]	6.73 / [0.265]	6.98 / [0.275]	mm / [in]
Volume	Vol	No Heatsink		2.44 / [0.15]		cm <sup>3</sup> / [in <sup>3</sup> ]
Weight	W			7		g
Lead Finish		Nickel	0.51		2.03	μm
		Palladium	0.02		0.15	
		Gold	0.003		0.050	
<b>THERMAL</b>						
Operating Temperature	$T_J$		0		125	°C
Operating Case Temperature	$T_C$	Any operating condition	0		100	°C
Thermal Capacity				5		Ws/°C
<b>ASSEMBLY</b>						
Peak Compressive Force Applied to Case (Z-axis)		Supported by J-Lead only			3	lbs
Storage Temperature	$T_{ST}$		-40		125	°C
Moisture Sensitivity Level		MSL 6, four hours out of bag maximum MSL 5				
ESD Rating	ESD <sub>HBM</sub>	Human Body Model, "JEDEC JESD 22-A114C.01"	1000			V
	ESD <sub>CDM</sub>	Charged Device Model, "JEDEC JESD 22-C101D"	400			
<b>SOLDERING</b>						
Peak Temperature During Reflow		Under MSL 6 conditions above Under MSL 5 conditions above			245	°C
Maximum Time Above [217] °C					150	s
Peak Heating Rate During Reflow				1.5	2	°C / s
Peak Cooling Rate Post Reflow				2.5	3	°C / s
<b>SAFETY and RELIABILITY</b>						
MTBF		Telcordia Issue 2 - Method I Case 1; Ground Benign, Controlled		5.41		Mhrs
		MIL-HDBK-217Plus Parts Count - 25C Ground Benign, Stationary, Indoors / Computer Profile		6.22		
Agency Approvals / Standards		cTUV <sub>US</sub> CE Mark CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

8.0 PRODUCT OUTLINE DRAWING AND RECOMMENDED PCB FOOTPRINT





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**VICOR**

1-LEAD 1/2 PRM2 (AS) PKG2  
PRODUCTION OUTLINE

DATE: 07/13/09  
REV: 34749

SCALE: 4:1  
SHEET: 1 OF 1

## 9.0 PRODUCT DETAILS AND DESIGN GUIDELINES

### 9.1 Control pins description and characteristics

**Control node (PR)** is the input to the control node which determines the powertrain timing and ultimately the module output power (Figure 21). An internal 0.5mA current sink is always active. The bi-directional buffer between PR and the control node has two states. In normal operation, PR will be above the 0.79V switching threshold, and will drive the control node through the buffer. An internal 7.4V clamp determines the maximum output power that can be requested of the modulator.

When PR falls below 0.79 V, the converter will stop switching. An internal circuit clamps the modulator input control node to 0.79 V, and a buffer will source up to 2.5 mA out of the pin at that clamp level. For this reason, the output impedance of the amplifier driving PR must be taken into account. A rail-to-rail operational amplifier with low output impedance is always recommended.

The powertrain small signal (plant) response consists of a single pole determined by the load resistance, the powertrain equivalent output resistance, and the total output capacitance (internal and external to the module). Both the modulator gain and the equivalent output resistance vary as a function of line, load and output voltage, as shown in Figures 17, 18 and 19. As the load increases, the powertrain pole moves to higher frequency. As a result, the closed loop crossover frequency will be the

highest at full load and lowest at minimum load. Figure 25 shows a reference AC small-signal model.

**Current feedback (IF)** is the input for the module output overcurrent protection and current limit features (see functional block diagram in section 4.0). A voltage proportional to the powertrain output current must be applied to IF in order for overcurrent protection to operate properly.

If the IF voltage exceeds the IF pin's overcurrent protection threshold, the powertrain will stop switching. If the IF voltage falls below the overcurrent protection threshold within  $T_{BLANK}$  time, then the powertrain will immediately resumes switching. Otherwise a fault is latched.

The current limit threshold for the IF pin is set lower than the protection threshold. When the IF pin average voltage exceeds the current limit threshold, an internal integrator will activate a clamp amplifier which overrides the modulator input maximum level. This causes the powertrain to maintain a constant output current.

The bandwidth of this current limit integrator is significantly slower than that of the PR control node input. Therefore this current limit can not be used in lieu of properly compensating the (external) PR control loop to avoid exceeding maximum current or power ratings for the device.

If the IF pin is not driven, it must be resistively terminated to SG. A 1k $\Omega$  resistor to SG is recommended in this case.

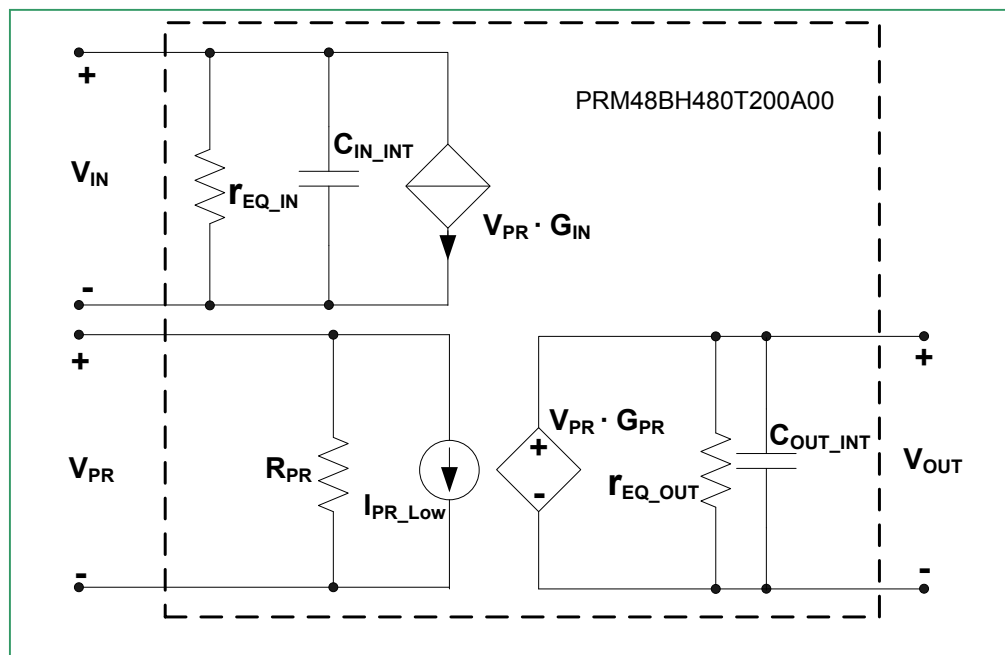


Figure 25 – PRM48BH480T200A00 AC small signal model



**VTM Control (VC)** pin supplies an initial  $V_{CC}$  voltage to downstream VTMs, enabling them and synchronizing their startup with the PRM. The  $V_{CC}$  voltage is a pulse, typically 10 ms duration at 14 V.

If VC is not loaded by a VTM, it must be terminated with a 1 k $\Omega$  resistor to  $-V_{Out}$ .

**Primary Control (PC)** is both an input and an output. It can provide the following features:

- Delayed start: upon application of voltage ( $>UVLO$ ) to the module power input and after  $T_{OFF}$ , the PC pin will source a constant 90  $\mu A$  current.
- Output disable: PC may be pulled down externally in order to disable the module. Pull down resistance should be less than 300  $\Omega$  to SG.
- Fault detection flag: The PC 5 V voltage source is internally turned off when a fault condition is latched. Note that aside from the Short Circuit fault condition, PC does not have significant current sinking capability. Therefore in the case of an array of PRMs with interconnected PC pins, PC does not in general reflect the fault state of all PRMs. The common PC line will not disable neighboring modules when a fault is detected except for a latched Output Short Circuit fault. Conversely any unit in the array latching a Short Circuit fault will disable the array for  $T_{SCR}$ .

**Temperature Monitor (TM)** pin outputs a voltage proportional to the absolute temperature of the converter analog control IC. It can be used to accomplish the following functions:

- Monitor the control IC temperature: The gain and setpoint of TM are such that the temperature, in Kelvin, of the PRM controller IC is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27  $^{\circ}C$ ).
- Closed loop thermal management at the system level (e.g. variable speed fans or coolant flow)
- Fault detection flag: The TM voltage source is turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM.

**Reference Enable (RE)** pin outputs a regulated 3.3 V, 8 mA voltage source. It is enabled only after successful startup of the PRM powertrain (see chapters 5.0 and 6.0.) RE is intended to power the output current transducer and also the voltage reference for the control loop. Powering the reference generator with RE helps provide a controlled startup, since the output voltage of the system is able to track the reference level as it comes up.

**Voltage Source (VS)** pin outputs a gated (e.g. mirrors PC status), non-isolated, regulated 9 V, 5 mA voltage source. It can be used to power external control circuitry; it always leads RE.

**Signal Ground (SG)** pin provides a Kelvin connection to the PRM's internal signal ground. It should be used as the reference for PR, TM, IF, and should return all PC, VS and RE pin currents. In array configurations with common ground control circuits, a series resistor ( $\sim 1 \Omega$ ) is recommended in order to decouple power and signal current returns.

## 9.2 Control circuit requirements and design procedure

The PRM48BH480T200A00 is an intelligent powertrain module designed to fully exploit external output voltage feedback and current sensing sub-circuits. These two external circuits are illustrated in Figure 26, which shows an example of the PRM in a standalone application with local voltage feedback and high side current sensing. In general, these circuits include a precision voltage reference, an operational amplifier which provides closed loop feedback compensation, and a high side current sense circuit which includes a shunt and current sense IC.

The following design procedures refer to the circuit shown in Figure 26.

### 9.2.1 Setting the output voltage level

The output voltage setpoint is a function of the voltage reference and the output voltage sense ratio. With reference to Fig. 26, R1 and R2 form the output voltage sensing divider which provides the scaled output voltage to the negative input of the error amplifier; a dedicated reference IC provides the reference voltage to the positive input of the error amplifier. Under normal operation, the error amplifier will keep the voltages at the inverting and non-inverting inputs equal, and therefore the output voltage is defined by:

$$V_{OUT} = V_{ref} \cdot \frac{R1 + R2}{R2}$$

Note that the component R1 will also factor into the compensation as described in a later section.

It is important to apply proper slew rate to the reference voltage rise when the control loop is initially enabled. The recommended range for reference rise time is 1 ms to 9 ms. The lower rise time limit will ensure optimized modulator timing performance during startup, and to allow the current limit feature (through IF pin) to fully protect the device during power-up. The upper rise time limit is needed to guarantee a sufficient factorized bus voltage is provided to any downstream VTM input before the end of the VC pulse.

### 9.2.2 Setting the output current limit and overcurrent protection level

The current limit and overcurrent protection set points are linked, and scale together against the current sense shunt, and the gain of the current sense amplifier. The output of the current sense IC provides the IF voltage which has  $V_{IF\_IL}$  and  $V_{IF\_OC}$  thresholds for the two functions respectively. The set points are therefore defined by:

$$I_{IL} = \frac{V_{IF\_IL}}{R_S \cdot G_{CS}}$$

and

$$I_{OC} = \frac{V_{IF\_OC}}{R_S \cdot G_{CS}}$$

where  $G_{CS}$  is the gain of the current sense amplifier.

### 9.2.3 Control loop compensation requirements

In order to properly compensate the control loop, all components which contribute to the closed loop frequency response should be identified and understood. Figure 25 shows the AC small signal model for the module. Modulator DC gain  $G_{PR}$  and powertrain equivalent resistance  $r_{EQ\_OUT}$  are shown. These modeling parameters will support a design cut-off frequency up to 50 kHz.

Standard Bode analysis should be used for calculating the error amplifier compensation and analyzing the closed loop stability. The recommended stability criteria are as follows:

- 1) Phase Margin > 45° : for the closed loop response, the phase should be greater than 45° where the gain crosses 0dB.
- 2) Gain Margin > 10dB : The closed loop gain should be lower than -10dB where the phase crosses 0°.
- 3) Gain Slope = -20dB / decade : The closed loop gain should have a slope of -20dB / decade at the crossover frequency.

The compensation characteristics must be selected to meet these stability criteria. Refer to Figure 27 for a local sense, voltage-mode control example based on the configuration in Figure 26. In this example, it is assumed that the maximum crossover frequency ( $F_{C\_MAX}$ ) has been selected to occur between B and C. Type-2 compensation (Curve IJKL) is sufficient in this case.

The following data must be gathered in order to proceed:

- Modulator Gain  $G_{PR}$ : See Figures 17, 18, 19
- Powertrain equivalent resistance  $r_{EQ}$ : See Figures 17, 18, 19
- Internal output capacitance: see Figure 20
- External output capacitance value

In the case of ceramic capacitors, the ESR can be considered low enough to push the associated zero well above the frequency of interest. Applications with high ESR capacitor may require a different type of compensation, or cascade control.

The system poles and zeros of the closed loop can then be defined as follows:

- Powertrain pole, assuming the external capacitor ESR can be neglected:

$$R_{C_{OUT\_EXT}} \ll \frac{r_{EQ\_OUT} \cdot R_{LOAD}}{r_{EQ\_OUT} + R_{LOAD}}$$

- Main pole frequency:

$$F_P \approx \frac{1}{2\pi \cdot \frac{r_{EQ\_OUT} \cdot R_{LOAD}}{r_{EQ\_OUT} + R_{LOAD}} \cdot (C_{OUT\_INT} + C_{OUT\_EXT})}$$

- Compensation Mid-Band Gain:

$$G_{MB} = 20 \log \frac{R_3}{R_1} \quad [1]$$

- Compensation Zero:

$$F_{Z1} = \frac{1}{2\pi \cdot R_3 \cdot C_1} \quad [2]$$

- Compensation Pole:

$$F_{P2} = \frac{1}{2\pi \cdot \frac{R_3 \cdot C_1 \cdot C_2}{C_1 + C_2}}$$

and for  $F_{P2} \gg F_{Z1}$  ( $C_1 + C_2 \approx C_1$ ):

$$F_{P2} \approx \frac{1}{2\pi \cdot R_3 \cdot C_2} \quad [3]$$

## 9.2.4 Midband Gain Design (R1,R3):

With reference to Figure 27: curve ABC is the:

- minimum output voltage in the application
- maximum input voltage expected in the application
- maximum load

PRM open loop response, and is where the maximum crossover frequency occurs. In order for the maximum crossover frequency to occur at the design choice  $F_{CMAX}$ , the compensation gain must be equal and opposite of the powertrain gain at this frequency. For stability purposes, the compensation should be in the Mid-band (J-K) at the crossover. Using Equation [1], the mid-band gain can be selected appropriately.

## 9.2.5 Compensation Zero Design (C1):

With reference to Figure 27: curve EFG is the:

- maximum output voltage in the application
- minimum input voltage expected in the application
- minimum load in the application

PRM open loop response, and is where the minimum crossover frequency  $F_{CMIN}$  occurs. Based on stability criteria, the compensation must be in the mid-band at the minimum crossover frequency, therefore  $F_{CMIN}$  will occur where EFG is equal and opposite of  $G_{MB}$ . C1 can be selected using Equation [2] so that  $F_{Z1}$  occurs prior to  $F_{CMIN}$ .

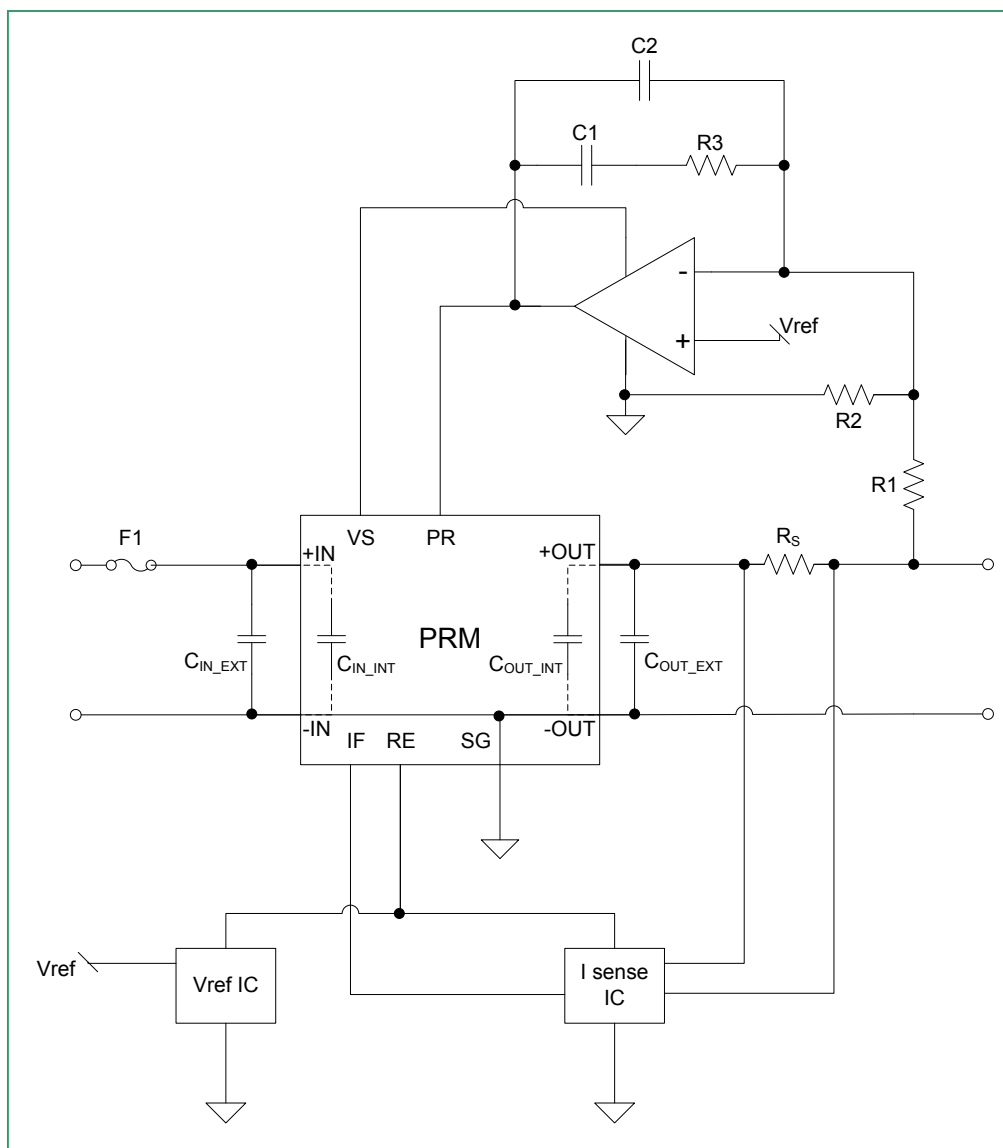


Figure 26 – Control circuit example

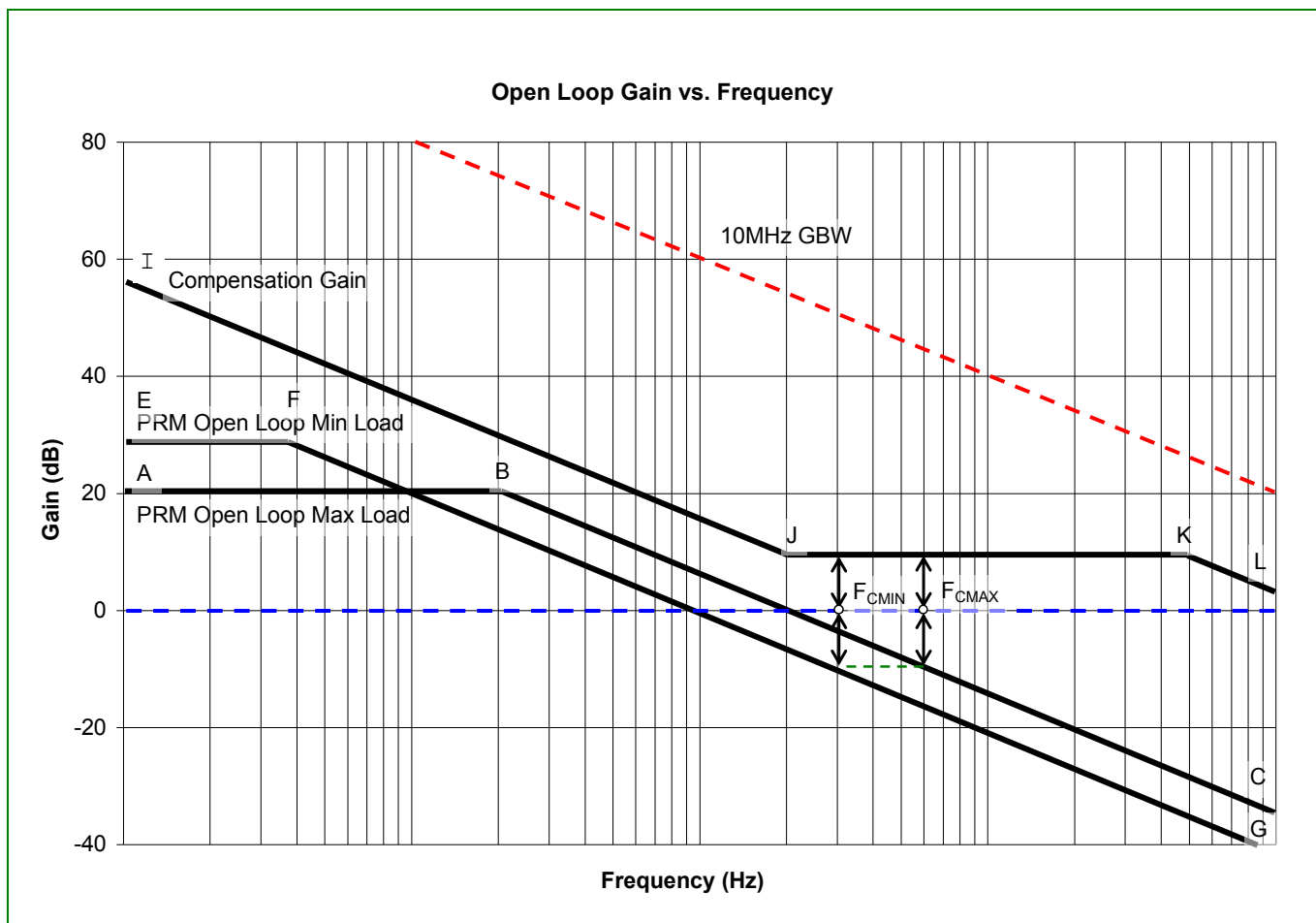


Figure 27 – reference asymptotic Bode plot for the considered system

9.2.6 High Frequency Pole Design (C2):

Using Equation [3], C2 should be selected so that  $F_{P2}$  is at least one decade above  $F_{CMAX}$  and prior to the gain bandwidth product of the operational amplifier (10MHz for this example). For applications with a higher desired crossover frequency the use of a high gain bandwidth product amplifier may be necessary to ensure that the real pole can be set at least one decade above the maximum crossover frequency.

9.2.7 Verifying Stability:

The preferred method for verifying stability is to use a network analyzer, measuring the closed loop response across various lines and load conditions. In the absence of a network analyzer, a load step transient response can be used in order to estimate stability. Figure 28 illustrates an example of a load step response. Equation [4] can be used to predict the phase margin

based on the ratio of the “kick” to “droop” (as defined in Fig. 28).

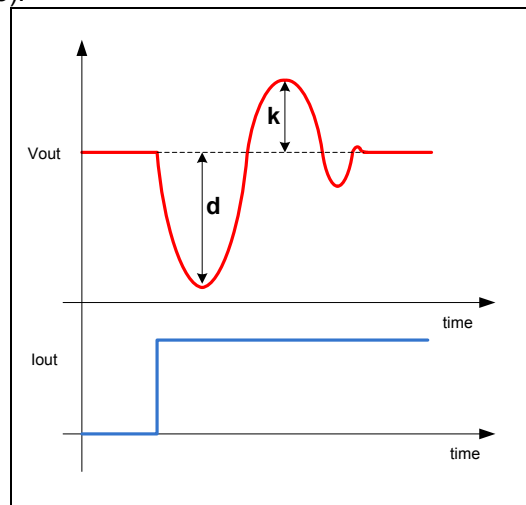


Figure 28 – load step response example and “droop” vs. “kick” definition

$$\Phi_m \approx 100 \sqrt{\frac{\left(\ln \frac{k}{d}\right)^2}{\left(\ln \frac{k}{d}\right)^2 + \pi^2}} \quad [4]$$

### 9.3 Burst Mode Operation:

At light loads, the PRM will operate in a burst mode due to minimum timing constraints. An example burst operation waveform is illustrated in Figure 29.

For very light loads, and also for higher input voltages, the minimum time power switching cycle from the powertrain will exceed the power required by the load. In this case the external error amplifier will periodically drive PR below the switching threshold in order to maintain regulation. Switching will cease momentarily until the error amplifier once again drives PR voltage above the threshold.

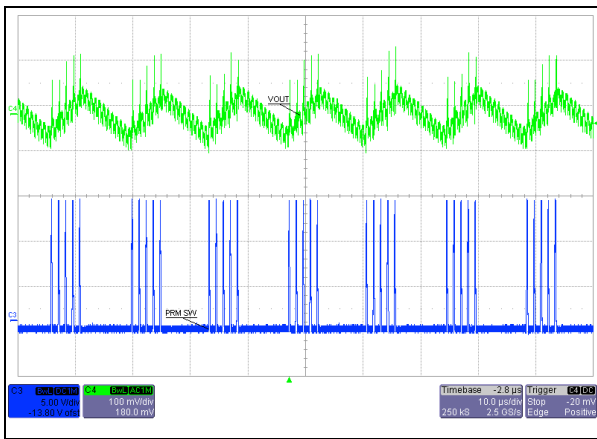


Figure 29 – light load burst mode of operation

Note that during the bursts of switching, the powertrain frequency is constant, but the number of pulses as well as the time between bursts is variable. The variability depends on many factors including input voltage, output voltages, load impedance, and external error amplifier output impedance.

In burst mode, the gain of the PR input to the plant which is modeled in the previous sections is time varying. Therefore the small signal analysis can not be directly applied to burst mode operation.

### 9.4 Input and Output filter design

Figures 14 and 15 provide the total input and output charge per cycle, as well as switching frequency, of the PRM at full load under various input and output voltages conditions.

Figure 20 provides the effective internal capacitance of the module. A conservative estimate of input and output peak-peak voltage ripple at nominal line and trim is provided by equation [5]:

$$\Delta V = \frac{Q_{TOT} - I_{FL} \cdot 0.4}{C_{INT} + C_{EXT}} \quad [5]$$

$Q_{TOT}$  is the total input (Fig. 15) or output (Fig. 14) charge per switching cycle at full load, while  $C_{INT}$  is the module internal effective capacitance at the considered voltage (Fig. 20) and  $C_{EXT}$  is the external effective capacitance at the considered voltage.

### 9.5 Input filter stability

The PRM can provide very high dynamic transients. It is therefore very important to verify that the voltage supply source as well as the interconnecting line are stable and do not oscillate. For this purpose, the converter dynamic input impedance magnitude  $|r_{EQ\_IN}|$  is provided in Figures 22, 23, 24. It is recommended to provide adequate design margin with respect to the stability conditions illustrated in 10.5.1 and 10.5.2.

9.5.1 Inductive source and local, external input decoupling capacitance with negligible ESR (i.e.: ceramic type)

The voltage source impedance can be modeled as a series  $R_{line}L_{line}$  circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{(C_{IN\_INT} + C_{IN\_EXT}) \cdot |r_{EQ\_IN}|} \quad [6]$$

$$R_{line} \ll |r_{EQ\_IN}| \quad [7]$$

It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, [7]. However,  $R_{line}$  cannot be made arbitrarily low otherwise equation [6] is violated and the system will show instability, due to under-damped RLC input network.

9.5.2 Inductive source and local, external input decoupling capacitance with significant  $R_{C_{IN\_EXT}}$  ESR (i.e.: electrolytic type)

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor  $L_{line}$ . Notice that, the high performance ceramic capacitors  $C_{IN\_INT}$  within the PRM should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be

$$\left| r_{EQ\_IN} \right| > R_{C_{IN\_EXT}} \quad [8]$$

$$\frac{L_{line}}{C_{IN\_EXT} \cdot R_{C_{IN\_EXT}}} < \left| r_{EQ\_IN} \right| \quad [9]$$

Equation [9] shows that if the aggregate ESR is too small – for example by using very high quality input capacitors ( $C_{IN\_EXT}$ ) – the system will be under-damped and may even become destabilized. Again, an octave of design margin in satisfying [8] should be considered the minimum.

## 9.6 Arrays

Up to ten PRMs of the same type may be placed in parallel to expand the power capacity of the system. The following high-level guidelines must be followed in order for the resultant system to start up and operate properly, and to avoid overstress or exceeding any absolute maximum ratings.

- –IN pins of all PRMs must be connected together. Both inductance and resistance from the common power source to each PRM should be minimized, and matched.
- Input voltage to all PRMs must be the same. Independent fuses for each PRM are recommended.
- PC pins must be connected together for synchronization and proper fault response.
- Reference supply to the control loop voltage reference and current sense circuitry must be enabled when all modules' RE pins have reached their operational voltage levels.
- There must be one single external voltage control loop. The control loop must drive each PR pin relative to each module's SG pin, and the local PR voltage must be the same across all modules.
- Each PRM must have its own local current shunt and current sense circuitry to drive its IF pin.
- The number of PRMs required to achieve a given array capacity must consider all sources of mismatch to avoid overstress of any PRM in the array. Imbalances in sharing are not only due to current sharing accuracy specifications, but also

temperature differences among PRMs,  $V_{in}$  variations, and error terms in the buffering of the error amplifier output to the PR pins.

- Control loop compensation procedures above will hold for an array, in general, although many parameters must be scaled against the number of PRMs in the system.

Please contact Vicor Applications for assistance.

## 9.7 Input Fuse Recommendations

A fuse should be incorporated at the input to each PRM, in series with the +IN pin. A 10 A or smaller input fuse (Littelfuse® NANO<sup>2</sup>® 451/453 Series, or equivalent) is required to safety agency conditions of acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

## 9.8 Layout considerations

Application Note AN:005 details board layout using V•I Chip components. Additional consideration must be given to the external control circuit components.

The current sense shunt signal voltage is highly sensitive to noise. As such, current sensing circuitry should be located close to the shunt to minimize the length of the sense signals. A Kelvined connection at the shunt is recommended for best results.

The control signal from a remote voltage sense circuit to the PRM should be shielded. Avoid routing this, or other control signals directly underneath the PRM, if possible. Components that tie directly to the PRM should be located close to their respective pins. It is also critical that all control components be referenced to SG, and that SG not be tied to any other ground in the system, including –IN or –OUT of the PRM.

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## JONHON

«JONHON» (основан в 1970 г.)

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«FORSTAR» (основан в 1998 г.)

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