

PSMN6R0-30YL

N-channel 30 V 6 mΩ logic level MOSFET in LFPAK Rev. 04 — 10 March 2011 Product

Product data sheet

Product profile 1.

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- Class-D amplifiers
- DC-to-DC converters

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	30	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	-	-	79	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	55	W
Tj	junction temperature		-55	-	175	°C
Static chara	acteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}$	-	4.26	6	mΩ
Dynamic ch	naracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A};$	-	3.08	-	nC
$Q_{G(tot)}$	total gate charge	V _{DS} = 12 V; see <u>Figure 14;</u> see <u>Figure 15</u>	-	11	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 73 A; $V_{sup} \le 30$ V; R_{GS} = 50 Ω; unclamped	-	-	26	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source	mb	D
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 S
			SOT669 (LFPAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R0-30YL	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	30	V
V_{DSM}	peak drain-source voltage	$t_p \le 25 \text{ ns}; f \le 500 \text{ kHz}; E_{DS(AL)} \le 110 \text{ nJ};$ pulsed	-	35	V
V_{DGR}	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	-	56	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{}$	-	79	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 3	-	292	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	55	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drain	diode				
Is	source current	T _{mb} = 25 °C	-	73	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	292	Α
Avalanche ru	ggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 73 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; unclamped	-	26	mJ

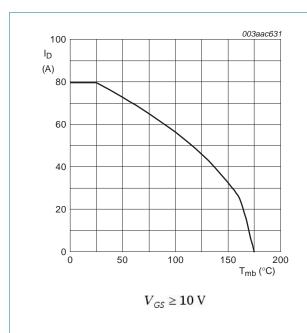


Fig 1. Continuous drain current as a function of mounting base temperature

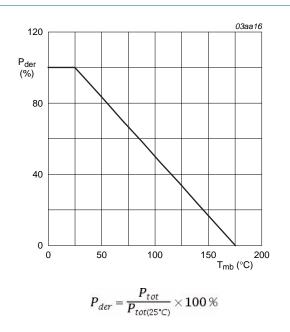


Fig 2. Normalized total power dissipation as a function of mounting base temperature

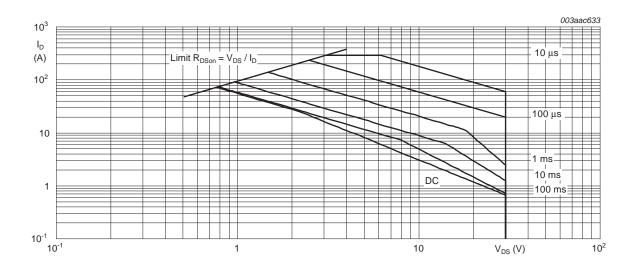


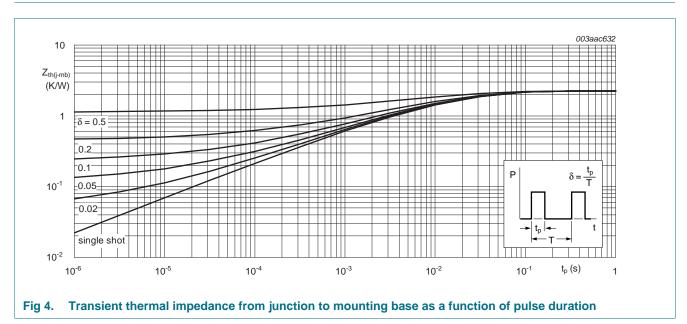
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25 \,^{\circ}C; I_{DM}$ is single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1.4	2.25	K/W



6. Characteristics

Table 6. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^{\circ}C$	27	-	-	V
V _{GS(th)} gate-source thre voltage	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	1.3	1.7	2.15	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 150$ °C; see Figure 12	0.65	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see <u>Figure 12</u>	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
R _{DSon} drain-source or resistance	drain-source on-state	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}$	-	6.18	7.87	$m\Omega$
	resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 ^{\circ}\text{C};$ see Figure 13	-	-	10.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}$	-	4.26	6	mΩ
R _G	gate resistance	f = 1 MHz	-	0.63	1.5	Ω
Dynamic ch	naracteristics					
Q _{G(tot)} total gate charge	total gate charge	$I_D = 10 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; see Figure 14; see Figure 15	-	11	-	nC
		$I_D = 10 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	24	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	22	-	nC
Q_{GS}	gate-source charge	$I_D = 10 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 4.5 \text{ V}$;	-	4.2	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.4	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	1.8	-	nC
Q_{GD}	gate-drain charge		-	3.08	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	V _{DS} = 12 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.6	-	V
C _{iss}	input capacitance	V _{DS} = 12 V; V _{GS} = 0 V; f = 1 MHz;	-	1425	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	313	-	pF
C _{rss}	reverse transfer capacitance		-	155	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 4.5 \text{ V};$	-	25	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	43	-	ns
t _{d(off)}	turn-off delay time		-	31	-	ns
t _f	fall time		-	11	-	ns

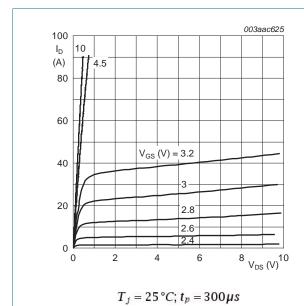
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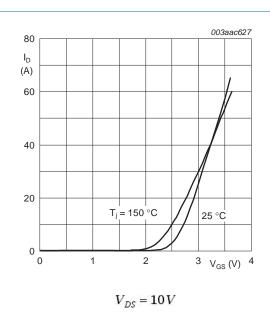
Characteristics ...continued Table 6.

Tested to JEDEC standards where applicable.

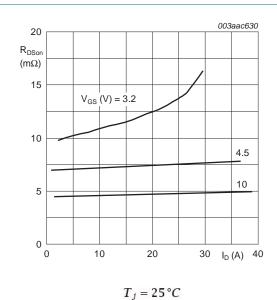
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drai	n diode					
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 17</u>	-	0.88	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	32	-	ns
Q_r	recovered charge	$V_{DS} = 20 \text{ V}$	-	25	-	nC



Output characteristics: drain current as a Fig 5. function of drain-source voltage; typical values



Transfer characteristics: drain current as a Fig 6. function of gate-source voltage; typical values



Drain-source on-state resistance as a function Fig 7. of drain current; typical values

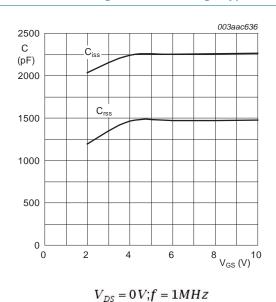


Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

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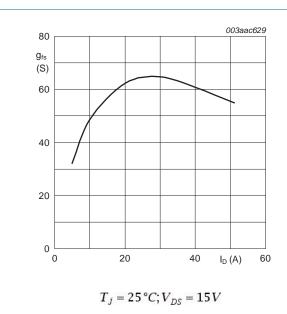
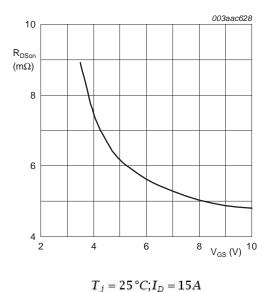
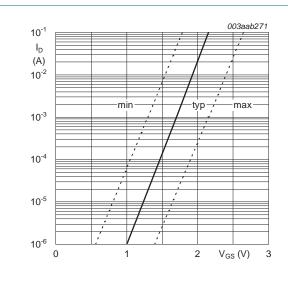


Fig 9. Forward transconductance as a function of drain current; typical values



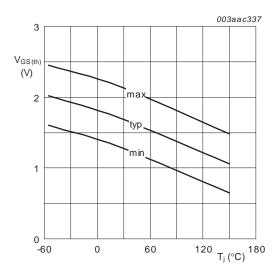
 $I_j = 25$ C, $I_D = 15$ A

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $T_j = 25 \,^{\circ}C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



 $I_D = 1mA; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature

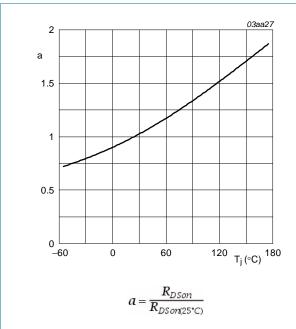


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

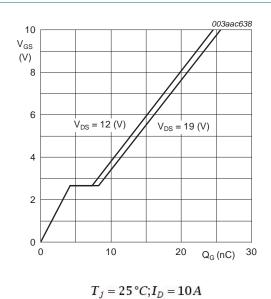


Fig 15. Gate-source voltage as a function of gate charge; typical values

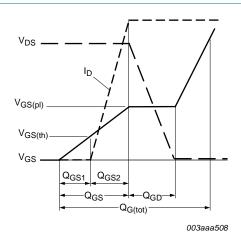
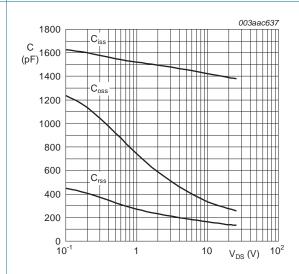


Fig 14. Gate charge waveform definitions



$$V_{GS} = 0V; f = 1MHz$$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

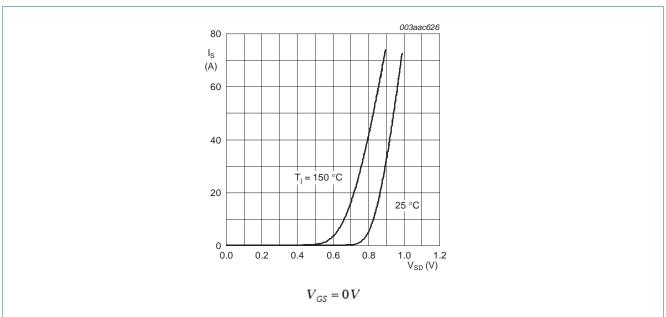


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669

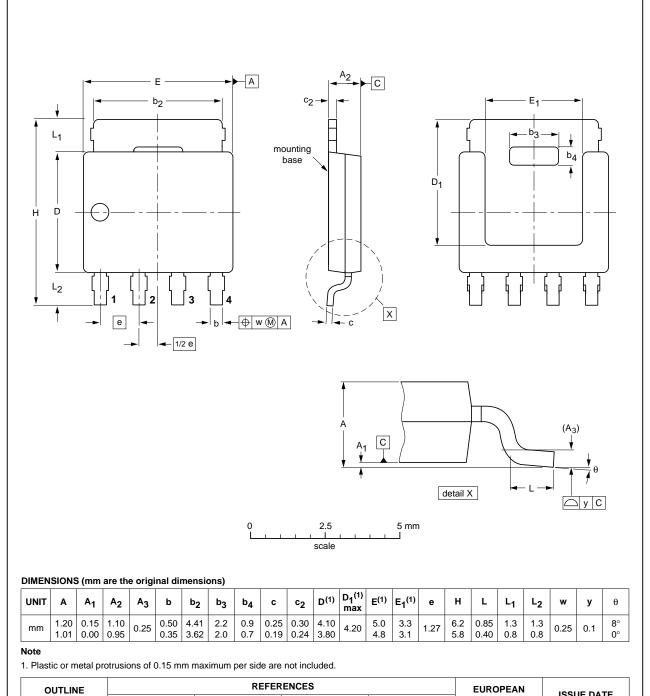


Fig 18. Package outline SOT669 (LFPAK)

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ISSUE DATE

04-10-13

06-03-16

PROJECTION

VERSION

SOT669

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN6R0-30YL v.4	20110310	Product data sheet	-	PSMN6R0-30YL v.3
Modifications:	 Various change 	es to content.		
PSMN6R0-30YL v.3	20100104	Product data sheet	-	PSMN6R0-30YL v.2

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9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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N-channel 30 V 6 mΩ logic level MOSFET in LFPAK

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