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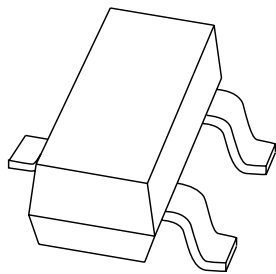
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Kind regards,

Team Nexperia

DATA SHEET



PBSS5320T

20 V, 3 A

PNP low V_{CEsat} (BISS) transistor

Product data sheet
Supersedes data of 2002 Aug 08

2004 Jan 15

20 V, 3 A PNP low V_{CEsat} (BISS) transistor

PBSS5320T

FEATURES

- Low collector-emitter saturation voltage V_{CEsat} and corresponding low R_{CEsat}
- High collector current capability
- High collector current gain
- Improved efficiency due to reduced heat generation.

APPLICATIONS

- Power management applications
- Low and medium power DC/DC convertors
- Supply line switching
- Battery chargers
- Linear voltage regulation with low voltage drop-out (LDO).

DESCRIPTION

PNP low V_{CEsat} transistor in a SOT23 plastic package.
NPN complement: PBSS4320T.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS5320T	ZH*

Note

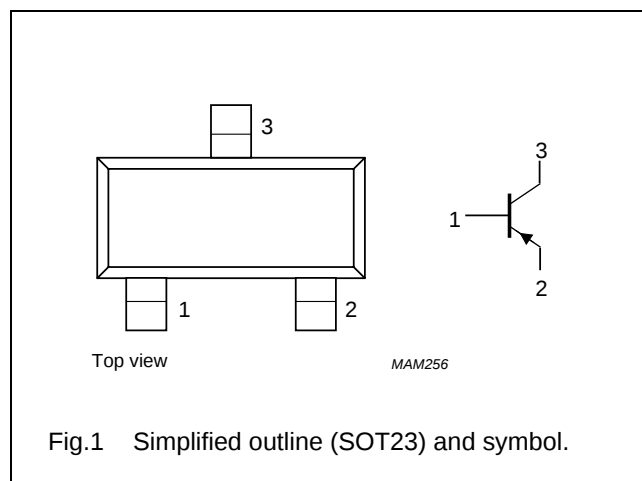
- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	-20	V
I_C	collector current (DC)	-2	A
I_{CRP}	repetitive peak collector current	-3	A
R_{CEsat}	equivalent on-resistance	105	mΩ

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5320T	–	plastic surface mounted package; 3 leads	SOT23

20 V, 3 A PNP low V_{CEsat} (BISS) transistor

PBSS5320T

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–20	V
V_{CEO}	collector-emitter voltage	open base	–	–20	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–2	A
I_{CRP}	repetitive peak collector current	note 1	–	–3	A
I_{CM}	peak collector current	single peak	–	–5	A
I_B	base current (DC)		–	–0.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 2	–	300	mW
		$T_{amb} \leq 25\text{ °C}$; note 3	–	480	mW
		$T_{amb} \leq 25\text{ °C}$; note 4	–	540	mW
		$T_{amb} \leq 25\text{ °C}$; notes 1 and 2	–	1.2	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Operated under pulsed conditions: pulse width $t_p \leq 100\text{ ms}$; duty cycle $\delta \leq 0.25$.
2. Device mounted on a printed-circuit board; single sided copper; tin plated; standard footprint.
3. Device mounted on a printed-circuit board; single sided copper; tin plated; mounting pad for collector 1 cm^2 .
4. Device mounted on a printed-circuit board; single sided copper; tin plated; mounting pad for collector 6 cm^2 .

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	417	K/W
		in free air; note 2	260	K/W
		in free air; note 3	230	K/W
		in free air; notes 1 and 4	104	K/W

Notes

1. Device mounted on a printed-circuit board; single sided copper; tin plated; standard footprint.
2. Device mounted on a printed-circuit board; single sided copper; tin plated; mounting pad for collector 1 cm^2 .
3. Device mounted on a printed-circuit board; single sided copper; tin plated; mounting pad for collector 6 cm^2 .
4. Operated under pulsed conditions: pulse width $t_p \leq 100\text{ ms}$; duty cycle $\delta \leq 0.25$.

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CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

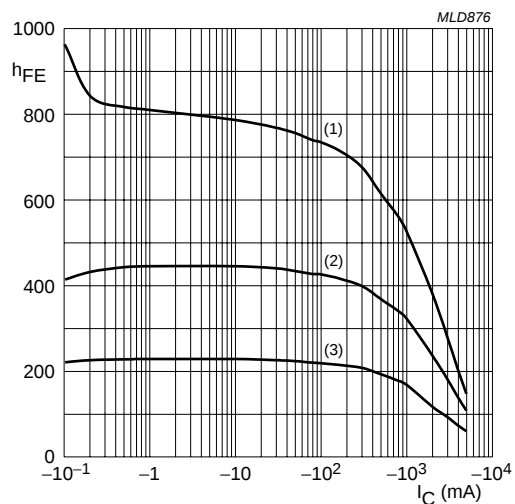
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -20\text{ V}; I_E = 0$	—	—	−100	nA
		$V_{CB} = -20\text{ V}; I_E = 0; T_j = 150\text{ }^{\circ}\text{C}$	—	—	−50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	—	—	−100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	220	—	—	
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	220	—	—	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	200	—	—	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}; \text{note 1}$	150	—	—	
		$V_{CE} = -2\text{ V}; I_C = -3\text{ A}; \text{note 1}$	100	—	—	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	—	—	−70	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	—	—	−130	mV
		$I_C = -2\text{ A}; I_B = -100\text{ mA}; \text{note 1}$	—	—	−230	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	—	—	−210	mV
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	—	—	−300	mV
R_{CEsat}	equivalent on-resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	—	75	105	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -100\text{ mA}; \text{note 1}$	—	—	−1.1	V
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	—	—	−1.2	V
$V_{BE(on)}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	−1.2	—	—	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	100	—	—	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	—	—	50	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

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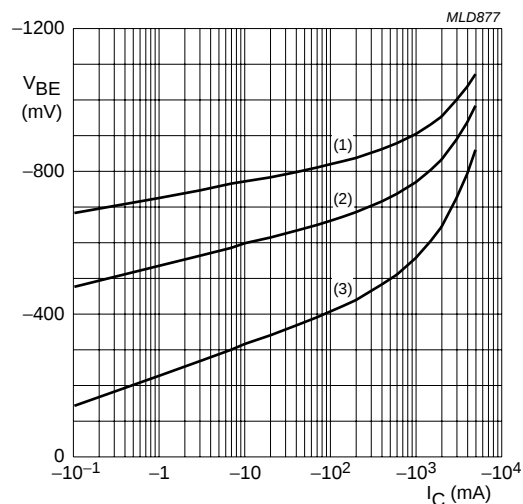
$V_{CE} = -2$ V.

(1) $T_{amb} = 150$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -55$ °C.

Fig.2 DC current gain as a function of collector current; typical values.



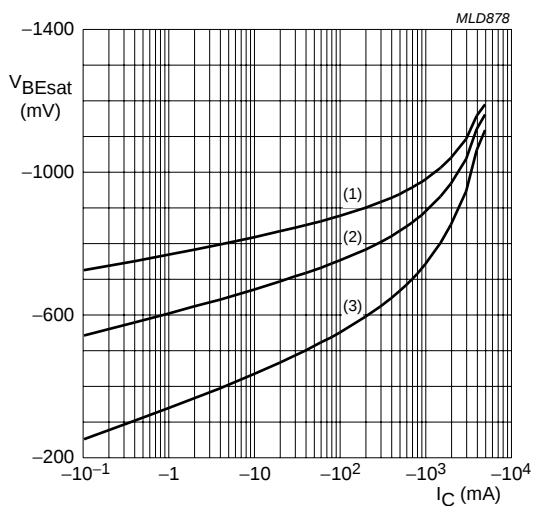
$V_{CE} = -2$ V.

(1) $T_{amb} = -55$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 150$ °C.

Fig.3 Base-emitter voltage as a function of collector current; typical values.



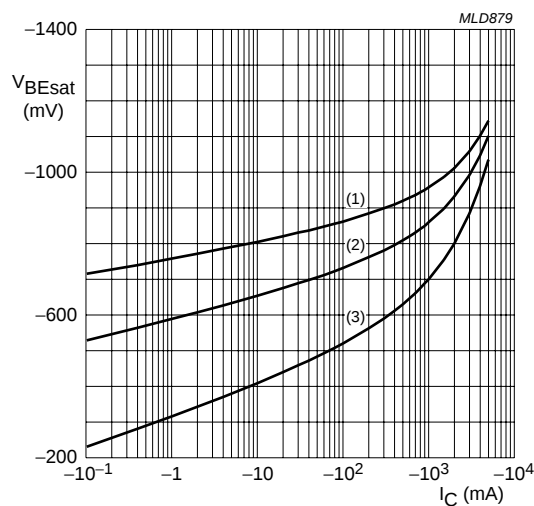
$I_C/I_B = 10$.

(1) $T_{amb} = -55$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 150$ °C.

Fig.4 Base-emitter saturation voltage as a function of collector current; typical values.



$I_C/I_B = 20$.

(1) $T_{amb} = -55$ °C.

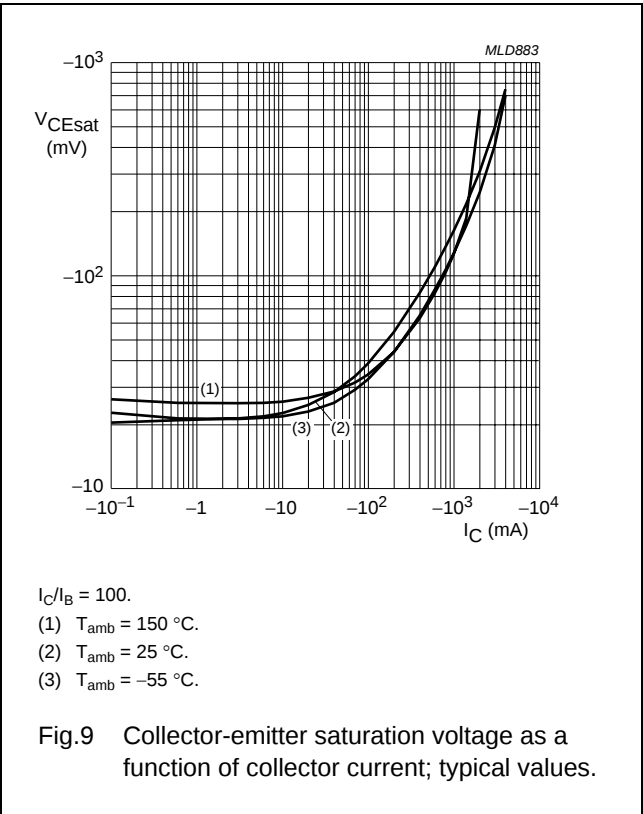
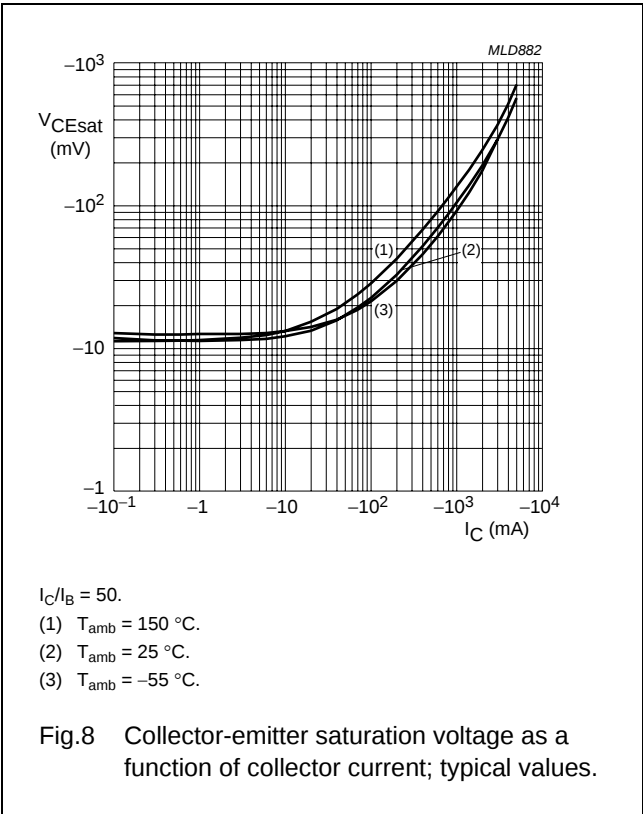
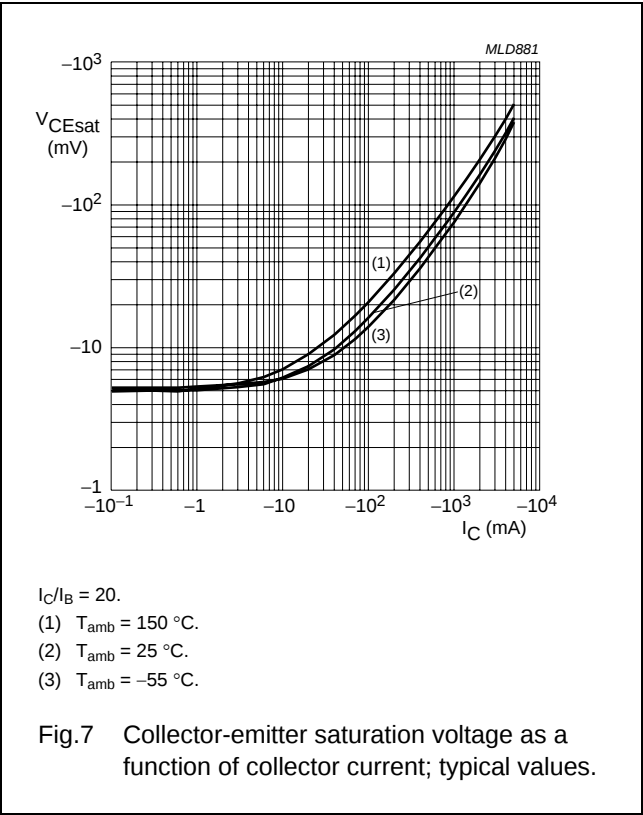
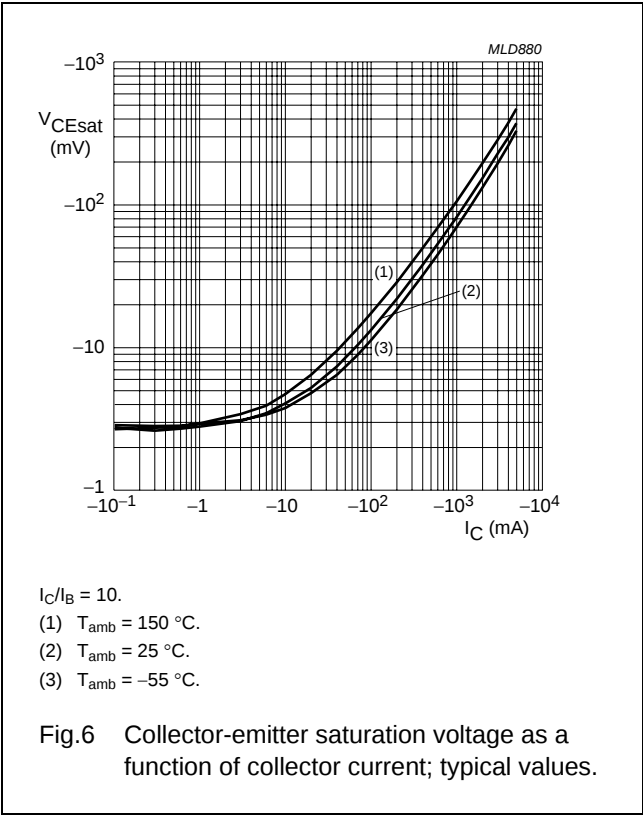
(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 150$ °C.

Fig.5 Base-emitter saturation voltage as a function of collector current; typical values.

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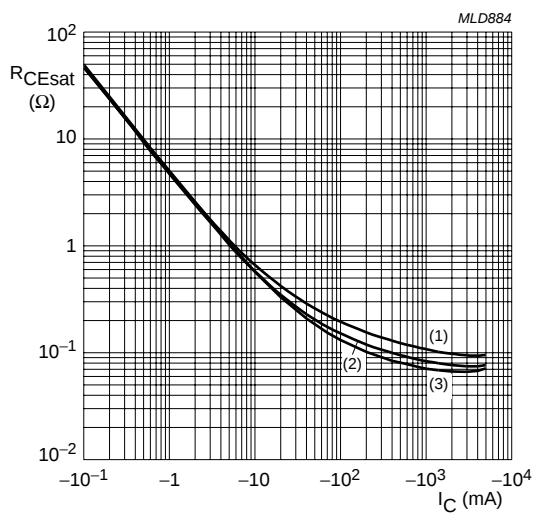
 $I_C/I_B = 20$.(1) $T_{amb} = 150^\circ\text{C}$.(2) $T_{amb} = 25^\circ\text{C}$.(3) $T_{amb} = -55^\circ\text{C}$.

Fig.10 Equivalent on-resistance as a function of collector current; typical values.

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PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads

SOT23

The diagrams illustrate the SOT23 package dimensions. The top view shows the overall width D and lead spacing e. The side view shows the maximum height A, lead height A1, and lead thickness c. The bottom view shows the lead pitch e1 and the distance from the lead center to the package edge b_p. A detail X shows the lead profile with dimensions L_p and Q. A scale bar indicates 0 to 2 mm.

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				04-11-04 06-03-16

20 V, 3 A

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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