SY55859L

3.3V, 3.2Gbps Dual 2X2 Crosspoint Switch

General Description

The SY55859L is a dual CML 2x2 crosspoint switch optimized for high-speed data and/or clock applications (up to 3.2Gbps or 2.7GHz) where low jitter and skew are critical. This device is pin-for-pin, plug-in compatible to the MAX3840. Each 2x2 of the SY55859L routes any input to any output, and thus can distribute or multiplex a clock or data stream. The I/O architecture is fully differential and CML compatible. Both inputs and outputs are optimized for 50Ω transmission lines. The inputs (DA 0-1 and DB 0-1) are internally terminated with 50Ω, thus eliminating external termination, and the outputs (QA0-1 and QB0-1) include 50Ω source termination. Furthermore, a power-saving output enable feature is provided which powers-down unused outputs.

The SY5859L operates from a +3.3V ±10% supply, and is guaranteed over the industrial (–40°C to +85°C) temperature range. It is available in a 32-pin (5mm x 5mm) QFN package.

For applications that require either lower voltage operation or a more flexible input interface (for applications such as AC–coupled LVPECL inputs), consider the SY55858U.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

SuperLite™

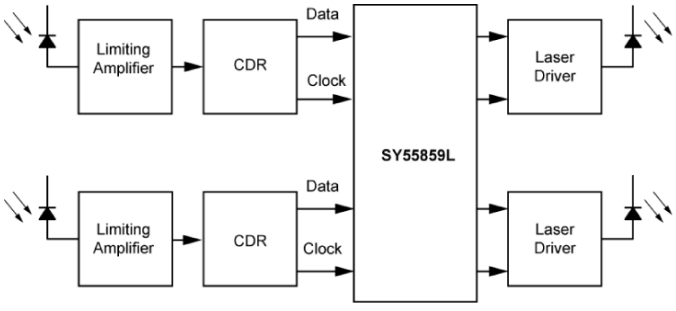
Features

- Pin-for-pin, plug-in compatible to the MAX3840
- Supply voltage operation: +3.3V±10%
- Low Jitter:
  - -2ps$_{RMS}$ random jitter
  - -5ps$_{PP}$ deterministic jitter
- Power saving output disable feature
- 15ps channel-to-channel skew
- Fast CML outputs: <100ps t_r/t_f
- Available in a small (5mm x 5mm) 32-pin EPAD-QFN package

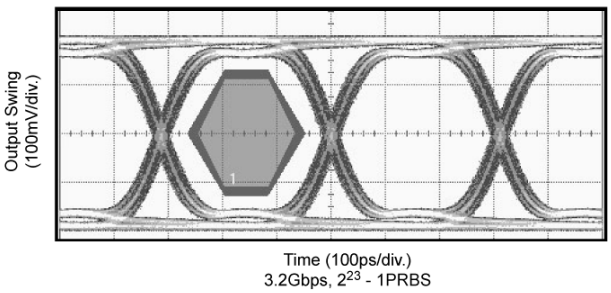
Applications

- SONET/SDH optical transport
- High-speed backplane redundancy
- Add-drop multiplexers

Typical Applications



Typical Performance



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Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY55859LMI	H32-1	Industrial	SY55859LMI	Sn-Pb
SY55859LMITR[2]	H32-1	Industrial	SY55859LMI	Sn-Pb
SY55859LMG[3]	H32-1	Industrial	SY55859LMG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY55859LMGTR[2,3]	H32-1	Industrial	SY55859LMG with Pb-Free bar-line indicator	Pb-Free NiPdAu

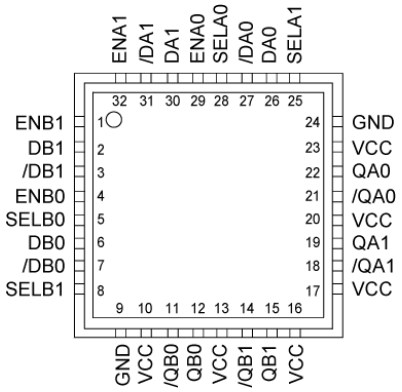
Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

Cross Reference Table

Micrel Semiconductor	Maxim
SY55859LMI	MAX3840EGJ

Pin Configuration



32-Pin EPAD-QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	ENB1	TTL Input. Channel B1 Output Enable. Setting this pin inactive low powers down QB1 and /QB1. Do not leave floating.
2	DB1	CML Input. Channel B1 true input.
3	/DB1	CML Input. Channel B1 complement input.
4	ENB0	TTL Input. Channel B0 Output Enable. Setting this pin inactive low powers down QB0 and /QB. Do not leave floating.
5	SELB0	TTL Input. Channel B0 output select. Please refer to Table 2. Do not leave floating.
6	DB0	CML Input. Channel B0 true input.
7	/DB0	CML Input. Channel B0 complement input.
8	SELB1	TTL Input. Channel B1 output select. Please refer to Table 2. Do not leave floating.
9, 24	GND	Supply ground. Most negative supply voltage.
10, 13, 16, 17, 20, 23	VCC	Positive Supply.
11	/QB0	CML Output. Channel B0 complement output.
12	QB0	CML Output. Channel B0 true output.
14	/QB1	CML Output. Channel B1 complement output.
15	QB1	CML Output. Channel B1 true output.
18	/QA1	CML Output. Channel A1 complement output.
19	QA1	CML Output. Channel A1 true output.
21	/QA0	CML Output. Channel A0 complement output.
22	QA0	CML Output. Channel A0 true output.
25	SELA1	TTL Input. Channel A1 output select. Please refer to Table 1. Do not leave floating.
26	DA0	CML Input. Channel A0 true input.
27	/DA0	CML Input. Channel A0 complement input.
28	SELA0	TTL Input. Channel A0 output select. Please refer to Table 1. Do not leave floating.
29	ENA0	TTL Input. Channel A0 output enable. Setting this pin inactive low powers down QA0 and /QA0. Do not leave floating.
30	DA1	CML Input. Channel A1 true input.
31	/DA1	CML Input. Channel A1 complement input.
32	ENA1	TTL Input. Channel A1 output enable. Setting this pin inactive low powers down QA1 and / QA1. Do not leave floating.
EP	Exposed Pad	Ground. This must be soldered to circuit board ground for proper electrical and thermal operation.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... -0.5V to +6.0V
CML Input Voltage (V_{IN}). ..... -0.5V to +6.0V
TTL Control Input Voltage (V_{IN}). ..... -0.5V to V_{CC} +0.5V
CML Output Voltage (V_{OUT}) ..... V_{CC} -1.0V to V_{CC} +0.5V
CML Output Current (I_{OUT}) 22mA
Lead Temperature (soldering, 20sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0 to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... 160°C
Package Thermal Resistance
QFN (θ_{JA})
Still-air ..... 28°C/W
500lfpm ..... 20°C/W
QFN (θ_{JC}) ..... 4°C/W

DC Electrical Characteristics

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No Load, Over Supply Voltage; All Outputs Enabled		160	190	mA

CML DC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C [Note 3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	CML Differential Output Swing	R_L = 50Ω to V_{CC}, Figure 3	640	800	1000	mV_{PP}
R_{OUT}	Differential Output Impedance	Figure 2	85	100	115	Ω
V_{OCM}	CML Output Common Mode Voltage	R_L = 50Ω to V_{CC}, Figure 3		V_{CC}-0.2		V
V_{IS}	CML Input Voltage Range	Figure 4	V_{CC}-0.8		V_{CC}+0.4	V
V_{DIFF}	CML Differential Input Voltage Swing	Figure 5	300		1600	mV_{PP}
	CML Single-ended Input Impedance	Figure 1	42.5	50	57.5	Ω

TTL Control Electrical Characteristics

V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C [Note 3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	TTL Input HIGH Voltage		2.0			V
V_{IL}	TTL Input LOW Voltage				0.8	V
I_{IH}	TTL Input HIGH Current		-10		+10	µA
I_{IL}	TTL Input LOW Current		-10		+10	µA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. The device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500lfpm is maintained.

AC Electrical Characteristics

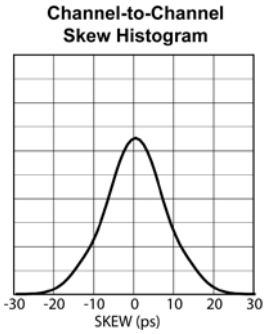
V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C (Note 1)

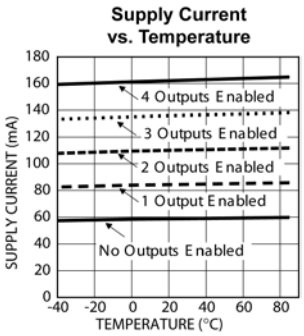
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum NRZ Data Rate			3.2		Gbps
f_{MAX}	Maximum Clock Rate			2.7		GHz
t_{PD}	Propagation Delay from Input-to-Output			275		ps
R_J	Random Jitter	**Note 2**		2		ps_{RMS}
D_J	Deterministic Jitter	**Note 3**		5	20	ps_{PP}
t_{SKDIFF}	CML Output Differential Skew	Any Differential Pair- Duty Cycle Distortion		7	25	ps
t_{SKEW}	CML Output Channel-to-Channel	**Note 4**, Any Two Outputs		15	40	ps
t_r, t_f	CML Output Rise/Fall Times	(20% to 80%)		80	135	ps

Notes:

1. AC characteristics are guaranteed by design and characterization. Tested using environment of Figure 6, 50Ω equivalent load.
2. Measured with 100mVp-p noise (f ≤ 2MHz) on the power supply.
3. Deterministic jitter (D_J) is the arithmetic sum of pattern-dependent jitter pulse width distortion.
4. This represents the skew on a QA and QB output with their inputs receiving the same signal.

Typical Operating Characteristics





Typical Characteristics

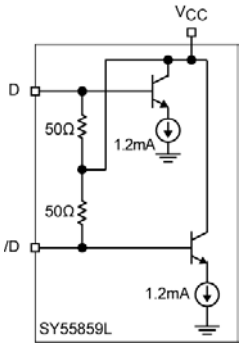


Figure 1. Input Structure

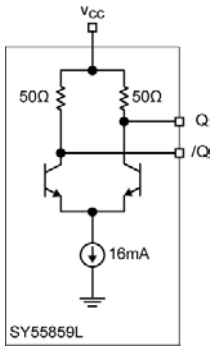


Figure 2. Output Structure

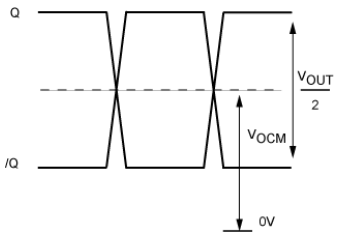


Figure 3a. Output Levels

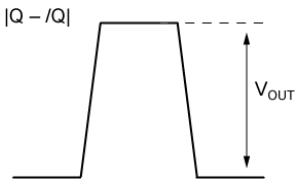


Figure 3b. Output Levels

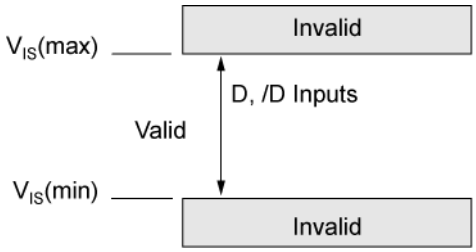


Figure 4. Input Range

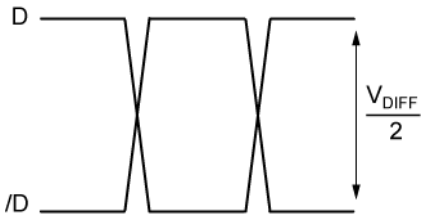


Figure 5a. Input Levels

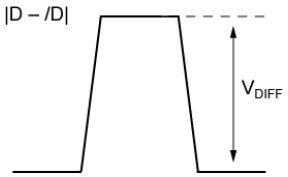


Figure 5b. Input Levels

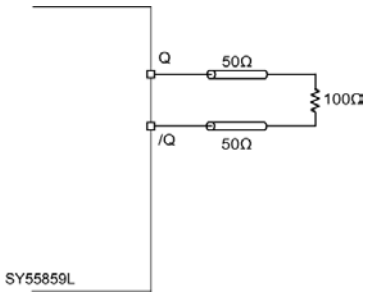


Figure 6. Output Interface

hbwhelp@micrel.com or (408) 955-1690

Functional Characteristics

SY55859L is a dual cross point with excellent pin-to-pin and part-to-part skew matching. As shown in table 1, based on the logic value at TTL input SELA0, output QA0 replicates either input DA0 or DA1. TTL input SELA1 selects whether output QA1 replicates input DA0 or DA1. As shown in table 2, TTL inputs SELB0 and SELB1 perform similarly for outputs QB0 and QB1 respectively, choosing between inputs DB0 or DB1.

If the two control inputs are tied together, SY55859L behaves as a redundant distribution device. Depending on the state of the combined control inputs, QA0 and QA1 will both replicate either DA0 or DA1. If the two control inputs are made the logical complement of each other, the SY55859L functions as a crosspoint, either sending DA0 to QA0 and DA1 to QA1, or sending DA0 to QA1 and DA1 to QA0. The same applies to channel B.

SY85859L's CML outputs are source terminated to 50Ω individually, 100Ω differentially. The CML inputs are parallel terminated, also to 50Ω. This improves signal integrity. With all terminations on chip, high-speed interfacing is greatly simplified, eliminating the need for external termination passive components. Figures 1 and 2 show the input and output structures.

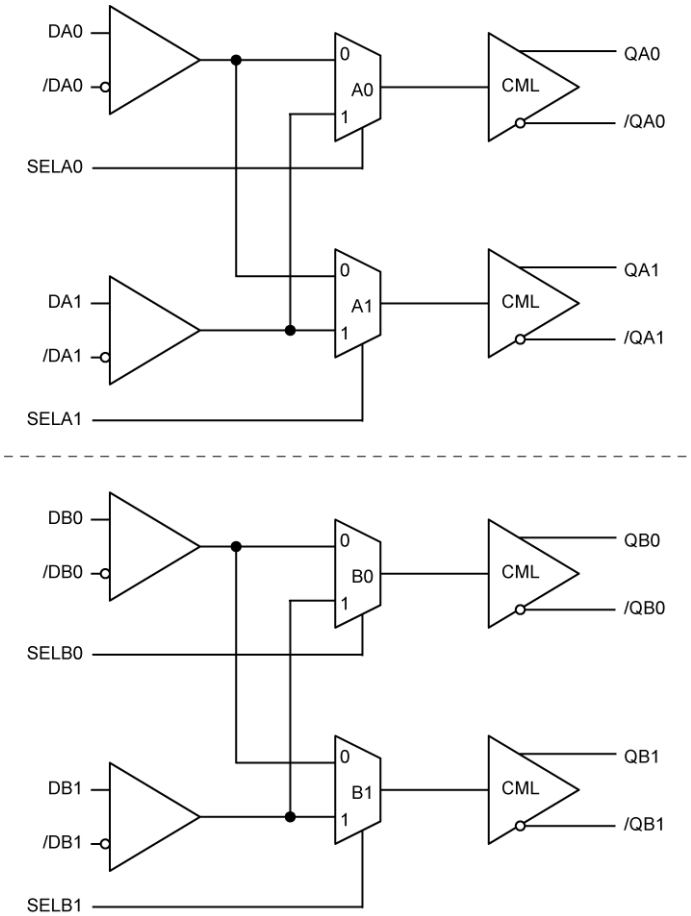
SELA0	SELA1	QA0	QA1	Function
0	0	DA0	DA0	Fanout Buffer
0	1	DA0	DA1	Dual Buffer
1	0	DA1	DA0	Dual Buffer
1	1	DA1	DA1	Fanout Buffer
CTL	CTL	Same	Same	Redundant Distribution
CTL	/CTL	Opposite	Opposite	Crosspoint

Table 1. Input to Output Connectivity, Crosspoint A

SELA0	SELA1	QA0	QA1	Function
0	0	DA0	DA0	Fanout Buffer
0	1	DA0	DA1	Dual Buffer
1	0	DA1	DA0	Dual Buffer
1	1	DA1	DA1	Fanout Buffer
CTL	CTL	Same	Same	Redundant Distribution
CTL	/CTL	Opposite	Opposite	Crosspoint

Table 2. Input to Output Connectivity, Crosspoint B

Functional Block Diagram



Application Information

The eight TTL compliant inputs to SY55859L are ENA0, ENA1, ENB0 ENB1, SELA0, SELA1, SELB0 and SELB1. These high impedance inputs do not default to a stable logic state when left unconnected. Therefore, these TTL compliant inputs cannot be left floating. Connect these inputs to a valid control signal, or hardwire to V_{CC} or GND.

The four enable TTL inputs, when driven low, disable the corresponding output stage. This reduces power consumption. Disabled output stages do not go into a high impedance state. Rather, each pin of a disabled output stage pair goes high through its respective 50Ω source termination.

The delay from a logic transition on an enable input to the corresponding effect on the CML output is not defined in the tables of this data sheet. This delay is 3ns typical, and 10ns maximum. Please note that, for cases where highly capacitive lines are being driven, the RC effects of the line may make this delay longer.

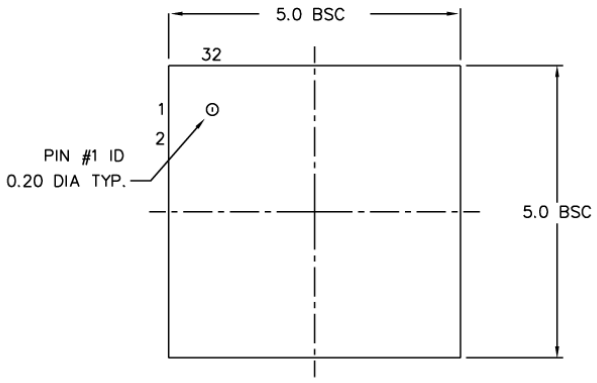
The delay from a logic transition on a select input to the corresponding CML output is also not defined in the tables. It is 300psec typical, 500psec maximum.

For best performance, use good high frequency layout techniques, filter V_{CC} supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the SY55859L data inputs and outputs.

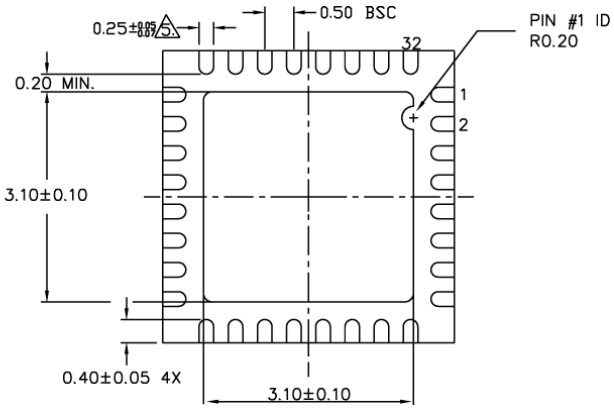
Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY55854U	2x2 CML Crosspoint	www.micrel.com/product-info/products/sy55854u.shtml
SY55858U	Dual 2x2 CML Crosspoint	www.micrel.com/product-info/products/sy55858u.shtml

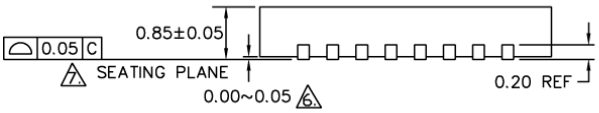
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

32-Pin EPAD-QFN

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