USB3290

Small Footprint Hi-Speed USB 2.0 Device PHY with UTMI Interface

PRODUCT FEATURES

Datasheet

- Available in a 40 ball lead-free RoHS compliant (4 x 4 x 0.9mm) VFBGA package
- Interface compliant with the UTMI specification (60MHz, 8-bit bidirectional interface)
- Only one required power supply (+3.3V)
- Supports 480Mbps Hi-Speed (HS) and 12Mbps Full Speed (FS) serial data transmission rates
- Integrated 45Ω and 1.5kΩ termination resistors reduce external component count
- Internal short circuit protection of DP and DM lines
- On-chip oscillator operates with low cost 24MHz crystal
- Latch-up performance exceeds 150mA per EIA/JESD 78, Class II
- ESD protection levels of 5kV HBM without external protection devices
- SYNC and EOP generation on transmit packets and detection on receive packets
- NRZI encoding and decoding
- Bit stuffing and unstuffing with error detection
- Supports the USB suspend state, HS detection, HS Chirp, Reset and Resume
- Support for all test modes defined in the USB 2.0 specification
- 55mA Unconfigured Current (typical) - ideal for bus powered applications.
- 83uA suspend current (typical) - ideal for battery powered applications.
- Industrial Operating Temperature -40^{o}C to +85^{o}C

Applications

The USB3290 is the ideal companion to any ASIC, SoC or FPGA solution designed with a UTMI Hi-Speed USB device (peripheral) core.

The USB3290 is well suited for:

- Cell Phones
- MP3 Players
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers

ORDER NUMBER(S):

USB3290-FH FOR 40 BALL, VFBGA LEAD-FREE ROHS COMPLIANT PACKAGE

USB3290-FH-TR FOR 40 BALL, VFBGA LEAD-FREE ROHS COMPLIANT PACKAGE (TAPE AND REEL)

Reel Size is 4000 pieces.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Table of Contents

List of Figures

List of Tables

Chapter 1 General Description

The USB3290 provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The IC is available in a 40 ball lead-free RoHS compliant VFBGA package. The small footprint package makes the USB3290 ideal for portable consumer electronics applications.

1.1 Product Description

The USB3290 is an industrial temperature USB 2.0 physical layer transceiver (PHY) integrated circuit. SMSC's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY uses an 8-bit bidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports 480Mbps transfer rate, while remaining backward compatible with USB 1.1 legacy protocol at 12Mbps.

All required termination and 5.25V short circuit protection of the DP/DM lines are internal to the chip. The USB3290 also has an integrated 1.8V regulator so that only a 3.3V supply is required.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

Chapter 2 Functional Block Diagram

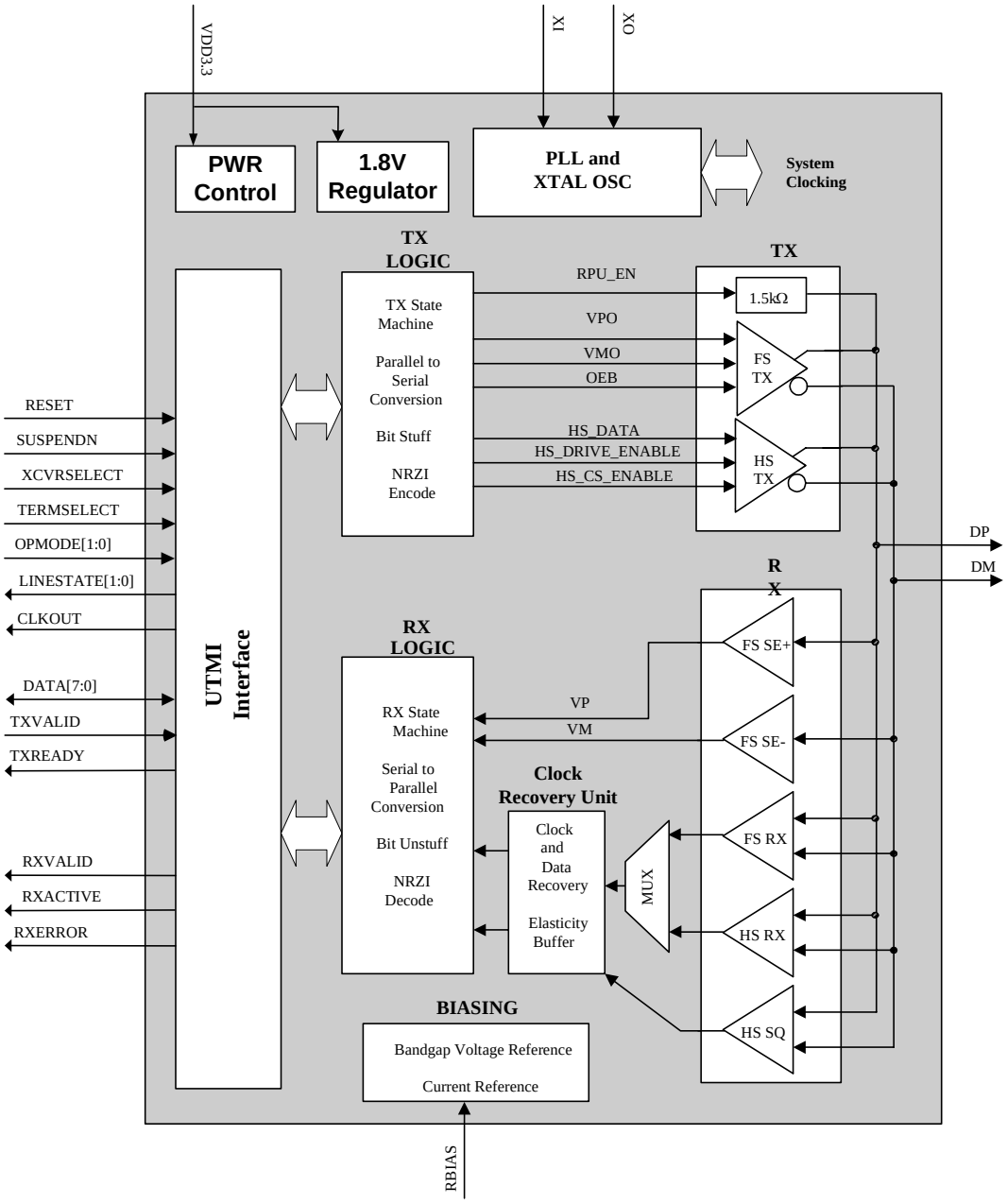


Figure 2.1 USB3290 Block Diagram

Chapter 3 Pinout

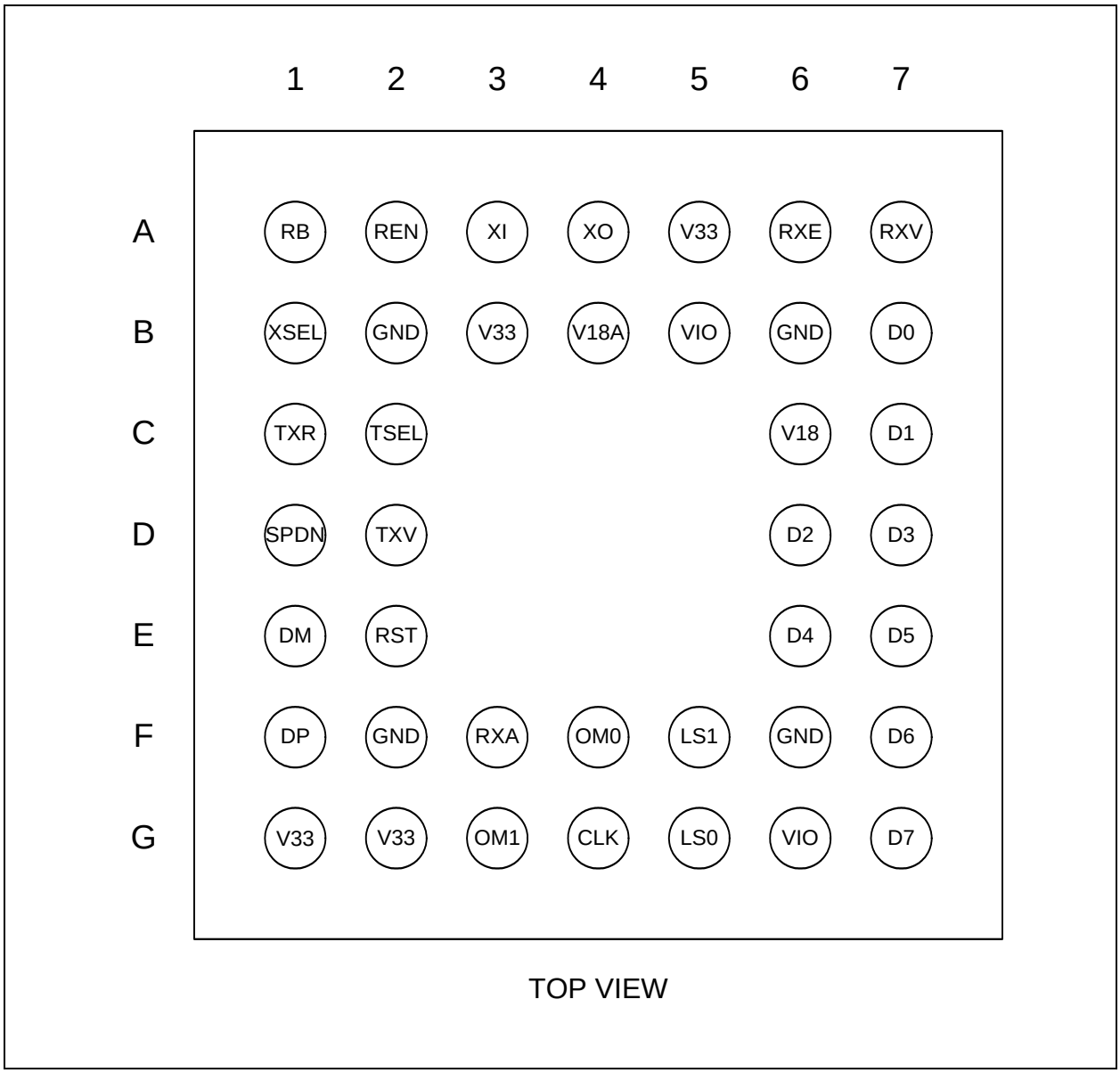


Figure 3.1 USB3290 Pinout - Top View

Chapter 4 Interface Signal Definition

Table 4.1 System Interface Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RESET (RST)	Input	High	**Reset.** Reset all state machines. After coming out of reset, must wait 5 rising edges of clock before asserting TXValid for transmit. See Section 7.8.3
XCVRSELECT (XSEL)	Input	N/A	**Transceiver Select.** This signal selects between the FS and HS transceivers: 0: HS transceiver enabled 1: FS transceiver enabled.
TERMSELECT (TSEL)	Input	N/A	**Termination Select.** This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SUSPENDN (SPDN)	Input	Low	**Suspend.** Places the transceiver in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, TERMSELECT must always be in FS mode to ensure that the 1.5kΩ pull-up on DP remains powered. 0: Transceiver circuitry drawing suspend current 1: Transceiver circuitry drawing normal current
CLKOUT (CLK)	Output	Rising Edge	**System Clock**. This output is used for clocking receive and transmit parallel data at 60MHz.
OPMODE[1:0] (OM1) (OM0)	Input	N/A	**Operational Mode.** These signals select between the various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-driving (all terminations removed) 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved
LINESTATE[1:0] (LS1) (LS0)	Output	N/A	**Line State**. These signals reflect the current state of the USB data bus in FS mode, with [0] reflecting the state of DP and [1] reflecting the state of DM. When the device is suspended or resuming from a suspended state, the signals are combinatorial. Otherwise, the signals are synchronized to CLKOUT. [1] [0] Description 0 0 0: SE0 0 1 1: J State 1 0 2: K State 1 1 3: SE1

Table 4.2 Data Interface Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
DATA[7:0] (D7) . . . (D0)	Bidirectional	High	**Data bus. 8-bit Bidirectional mode.** **TXVALID** | **DATA[7:0]** 0 | output 1 | input
TXVALID (TXV)	Input	High	**Transmit Valid.** Indicates that the DATA bus is valid for transmit. The assertion of TXVALID initiates the transmission of SYNC on the USB bus. The negation of TXVALID initiates EOP on the USB. Control inputs (OPMODE[1:0], TERMSELECT,XCVRSELECT) must not be changed on the de-assertion or assertion of TXVALID. The PHY must be in a quiescent state when these inputs are changed.
TXREADY (TXR)	Output	High	**Transmit Data Ready.** If TXVALID is asserted, the SIE must always have data available for clocking into the TX Holding Register on the rising edge of CLKOUT. TXREADY is an acknowledgement to the SIE that the transceiver has clocked the data from the bus and is ready for the next transfer on the bus. If TXVALID is negated, TXREADY can be ignored by the SIE.
RXVALID (RXV)	Output	High	**Receive Data Valid.** Indicates that the DATA bus has received valid data. The Receive Data Holding Register is full and ready to be unloaded. The SIE is expected to latch the DATA bus on the rising edge of CLKOUT.
RXACTIVE (RXA)	Output	High	**Receive Active.** Indicates that the receive state machine has detected Start of Packet and is active.
RXERROR (RXE)	Output	High	**Receive Error**. 0: Indicates no error. 1: Indicates a receive error has been detected. This output is clocked with the same timing as the receive DATA lines and can occur at anytime during a transfer.

Table 4.3 USB I/O Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
DP	I/O	N/A	**USB Positive Data Pin.**
DM	I/O	N/A	**USB Negative Data Pin.**

Table 4.4 Biasing and Clock Oscillator Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RBIAS (RB)	Input	N/A	**External 1% bias resistor.** Requires a 12kΩ resistor to ground. Used for setting HS transmit current level and on-chip termination impedance.
XI/XO	Input	N/A	**External crystal.** 24MHz crystal connected from XI to XO.

Table 4.5 Power and Ground Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
VDD3.3 (V33) (VIO)	N/A	N/A	**3.3V Supply.** Provides power for USB 2.0 Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
REG_EN (REN)	Input	High	**On-Chip 1.8V regulator enable.** Connect to ground to disable both of the on chip (VDDA1.8 and VDD1.8) regulators. When regulators are disabled: ▪ External 1.8V must be supplied to VDDA1.8 and VDD1.8 pins. When the regulators are disabled, VDDA1.8 may be connected to VDD1.8 and a bypass capacitor (0.1μF recommended) should be connected to each pin. ▪ The voltage at VDD3.3 must be at least 2.64V (0.8 * 3.3V) before voltage is applied to VDDA1.8 and VDD1.8.
VDD1.8 (V18)	N/A	N/A	**1.8V Digital Supply.** Supplied by On-Chip Regulator when REG_EN is active. Low ESR 4.7uF minimum capacitor requirement when using internal regulators. Do not connect VDD1.8 to VDDA1.8 when using internal regulators. When the regulators are disabled, VDD1.8 may be connected to VDD1.8A.
VSS (GND)	N/A	N/A	**Common Ground.**
VDDA1.8 (V18A)	N/A	N/A	**1.8V Analog Supply.** Supplied by On-Chip Regulator when REG_EN is active. Low ESR 4.7uF minimum capacitor requirement when using internal regulators. Do not connect VDD1.8A to VDD1.8 when using internal regulators. When the regulators are disabled, VDD1.8A may be connected to VDD1.8.

Chapter 5 Limiting Values

Table 5.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum DP and DM voltage to Ground	V_{MAX_5V}		-0.3		5.5	V
Maximum VDD1.8 and VDDA1.8 voltage to Ground	$V_{MAX\_1.8V}$		-0.3		2.5	V
Maximum 3.3V Supply Voltage to Ground	$V_{MAX\_3.3V}$		-0.3		4.0	V
Maximum I/O Voltage to Ground	V_I		-0.3		4.0	V
Storage Temperature	T_{STG}		-55		150	^oC
ESD PERFORMANCE						
All Pins	V_{HBM}	Human Body Model	±5			kV
LATCH-UP PERFORMANCE						
All Pins	I_{LTCH_UP}	EIA/JESD 78, Class II	150			mA

Note: In accordance with the Absolute Maximum Rating system (IEC 60134)

Table 5.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	$V_{DD3.3}$		3.0	3.3	3.6	V
Input Voltage on Digital Pins	V_I		0.0		$V_{DD3.3}$	V
Input Voltage on Analog I/O Pins (DP, DM)	$V_{I(I/O)}$		0.0		$V_{DD3.3}$	V
Ambient Temperature	T_A		-40		85	^oC

Table 5.3 Recommended External Clock Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Frequency		XO driven by the external clock; and no connection at XI		24 (±100ppm)		MHz
System Clock Duty Cycle		XO driven by the external clock; and no connection at XI	45	50	55	%

Chapter 6 Electrical Characteristics

Table 6.1 Electrical Characteristics: Supply Pins (Note 6.1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Unconfigured Current	$I_{AVG(UCFG)}$	Device Unconfigured		55		mA
FS Idle Current	$I_{AVG(FS)}$	FS idle not data transfer		55		mA
FS Transmit Current	$I_{AVG(FSTX)}$	FS current during data transmit		60.5		mA
FS Receive Current	$I_{AVG(FSRX)}$	FS current during data receive		57.5		mA
HS Idle Current	$I_{AVG(HS)}$	HS idle not data transfer		60.6		mA
HS Transmit Current	$I_{AVG(HSTX)}$	HS current during data transmit		62.4		mA
HS Receive Current	$I_{AVG(HSRX)}$	HS current during data receive		61.5		mA
Low Power Mode	$I_{DD(LPM)}$	VBUS 15kΩ pull-down and 1.5kΩ pull-up resistor currents not included.		83		uA

Note 6.1 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.2 DC Electrical Characteristics: Logic Pins (Note 6.2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		2.0		$V_{DD3.3}$	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	$V_{DD3.3}$ - 0.5			V
Input Leakage Current	I_{LI}				± 1	uA
Pin Capacitance	Cpin				4	pF

Note 6.2 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.3 DC Electrical Characteristics: Analog I/O Pins (DP/DM) (Note 6.3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to $V_{DD3.3}$			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive (See Figure 6.1)	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	TX, RPU disabled	10			MΩ
Pull-up Resistor Impedance	Z_{PU}	Bus Idle	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	Z_{PURX}	Device Receiving	1.425	2.26	3.09	kΩ
Termination Voltage For Pull-up Resistor On Pin DP	V_{TERM}		3.0		3.6	V
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	Squelch Threshold			100	mV
		Unsquelch Threshold	150			mV
Output Levels						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV

Table 6.3 DC Electrical Characteristics: Analog I/O Pins (DP/DM) (Note 6.3) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				± 1	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 6.3 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.4 Dynamic Characteristics: Analog I/O Pins (DP/DM) (Note 6.4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS Output Driver Timing						
Rise Time	T_{FSR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Fall Time	T_{FFF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	FRFM	Excluding the first transition from IDLE state	90		111.1	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification			See Figure 6.2	
High Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6.2	
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6.2	

Note 6.4 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.5 Dynamic Characteristics: Digital UTMI Pins (Note 6.5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UTMI Timing						
DATA[7:0]	T_{PD}	Output Delay. Measured from PHY output to the rising edge of CLKOUT	2		5	ns
RXVALID						
RXACTIVE						
RXERROR						
LINESTATE[1:0]						
TXREADY						
DATA[7:0]	T_{SU}	Setup Time. Measured from PHY input to the rising edge of CLKOUT.	5			ns
TXVALID						
OPMODE[1:0]						
XCVRSELECT						
TERMSELECT						
DATA[7:0]	T_H	Hold time. Measured from the rising egde of CLKOUT to the PHY input signal edge.	0			ns
TXVALID						
OPMODE[1:0]						
XCVRSELECT						
TERMSELECT						

Note 6.5 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

6.1 Driver Characteristics of Full-Speed Drivers in High-Speed Capable Transceivers

The USB3290 uses a differential output driver to drive the USB data signal onto the USB cable. Figure 6.1 Full-Speed Driver VOH/IOH Characteristics for High-speed Capable Transceiveron page 17 shows the V/I characteristics for a full-speed driver which is part of a high-speed capable transceiver. The normalized V/I curve for the driver must fall entirely inside the shaded region. The V/I region is bounded by the minimum driver impedance above (40.5 Ohm) and the maximum driver impedance below (49.5 Ohm). The output voltage must be within 10mV of ground when no current is flowing in or out of the pin.

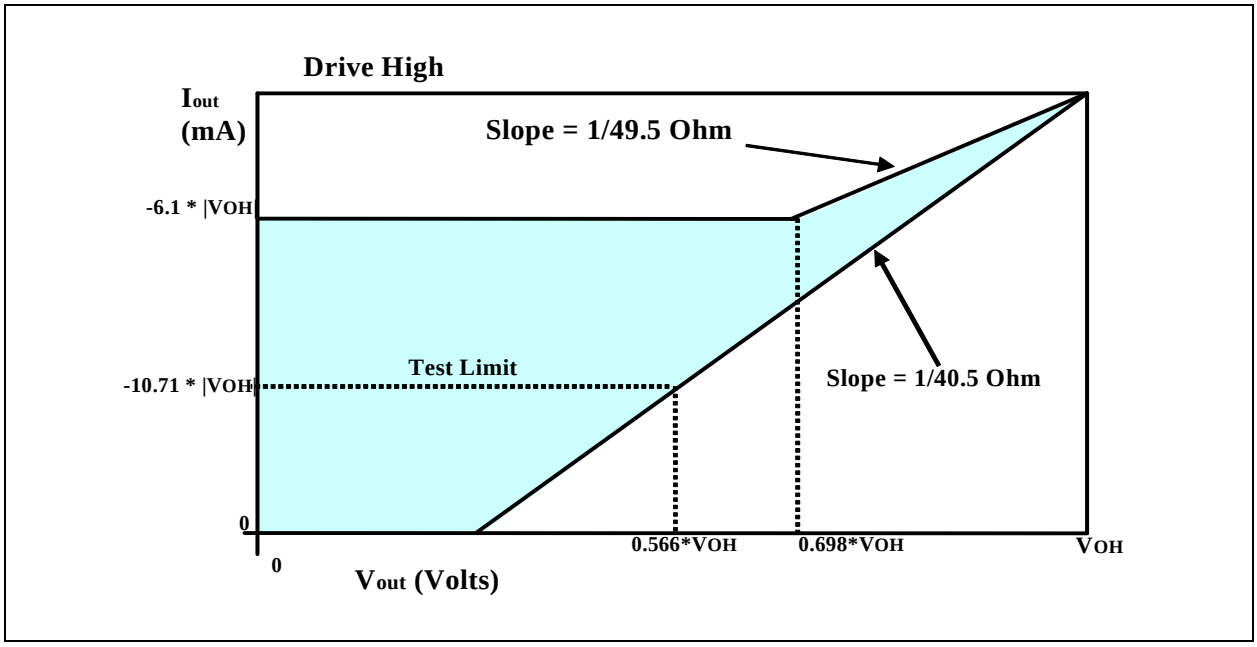


Figure 6.1 Full-Speed Driver VOH/IOH Characteristics for High-speed Capable Transceiver

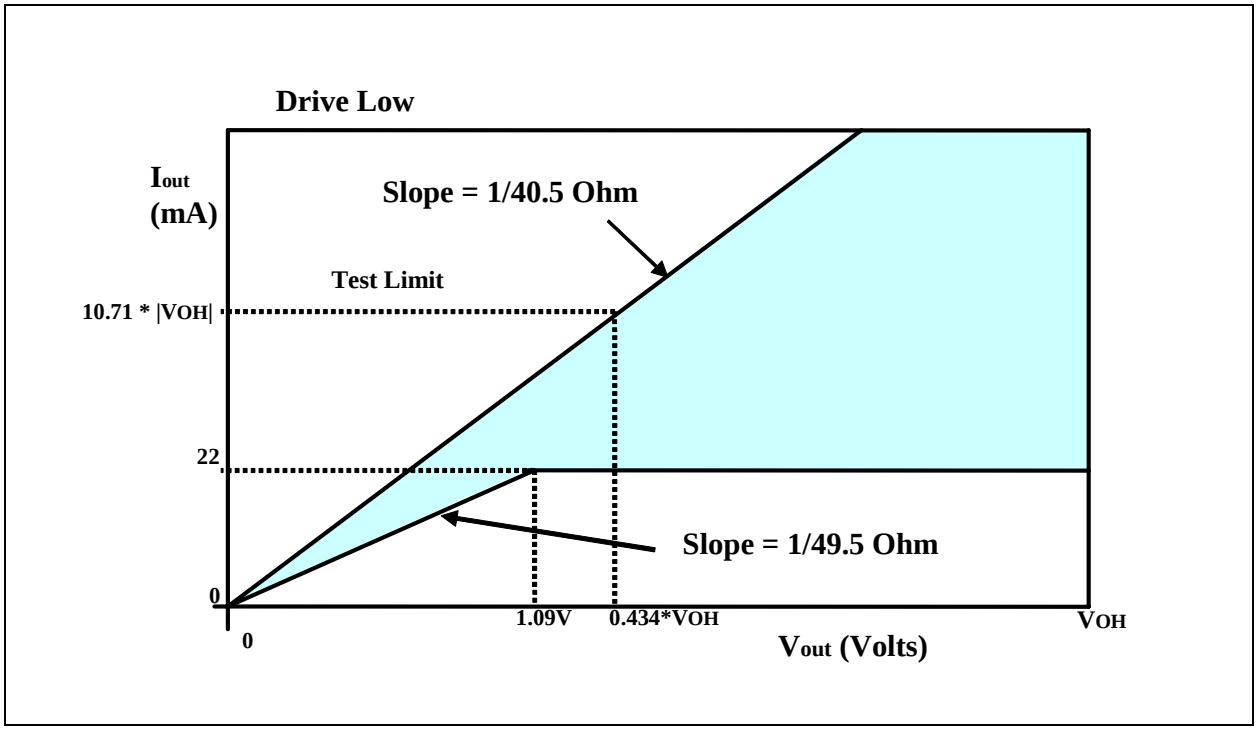


Figure 6.2 Full-Speed Driver VOL/IOL Characteristics for High-speed Capable Transceiver

6.2 High-speed Signaling Eye Patterns

High-speed USB signals are characterized using eye patterns. For measuring the eye patterns 4 points have been defined (see Figure 6.3). The Universal Serial Bus Specification Rev.2.0 defines the eye patterns in several 'templates'. The two templates that are relevant to the PHY are shown below.

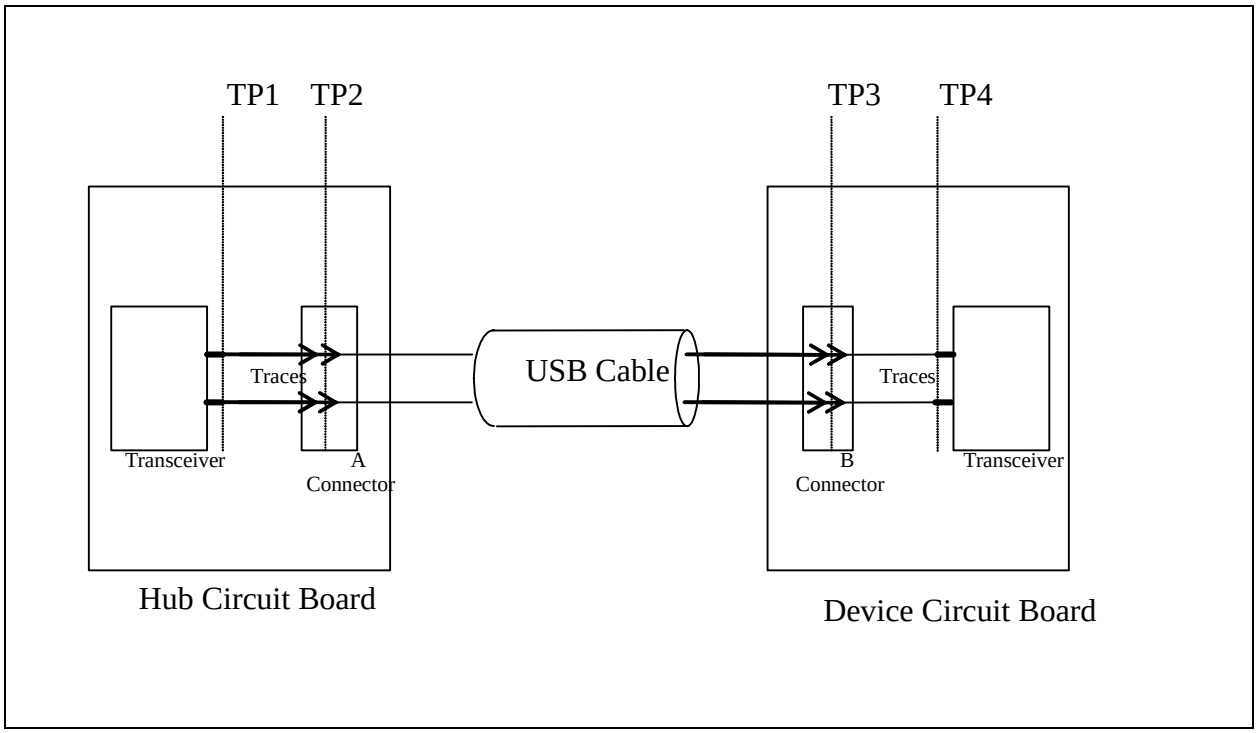


Figure 6.3 Eye Pattern Measurement Planes

The eye pattern in Figure 6.4 defines the transmit waveform requirements for a hub (measured at TP2 of Figure 6.3) or a device without a captive cable (measured at TP3 of Figure 6.3). The corresponding signal levels and timings are given in table below. Time is specified as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

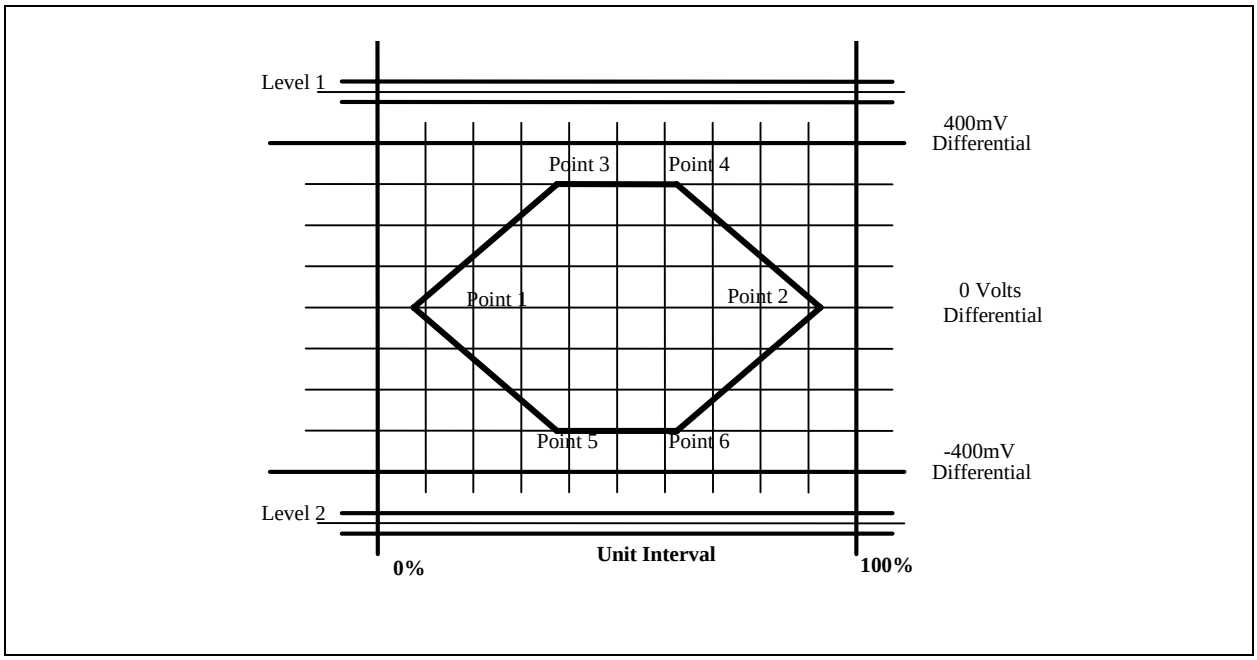


Figure 6.4 Eye Pattern for Transmit Waveform and Eye Pattern Definition

	VOLTAGE LEVEL (D+, D-)	TIME (% OF UNIT INTERVAL)
Level 1	525mV in UI following a transition, 475mV in all others	N/A
Level 2	-525mV in UI following a transition, -475mV in all others	N/A
Point 1	0V	7.5% UI
Point 2	0V	92.5% UI
Point 3	300mV	37.5% UI
Point 4	300mV	62.5% UI
Point 5	-300mV	37.5% UI
Point 6	-300mV	62.5% UI

The eye pattern in Figure 6.5 defines the receiver sensitivity requirements for a hub (signal applied at test point TP2 of Figure 6.3) or a device without a captive cable (signal applied at test point TP3 of Figure 6.3). The corresponding signal levels and timings are given in the table below. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

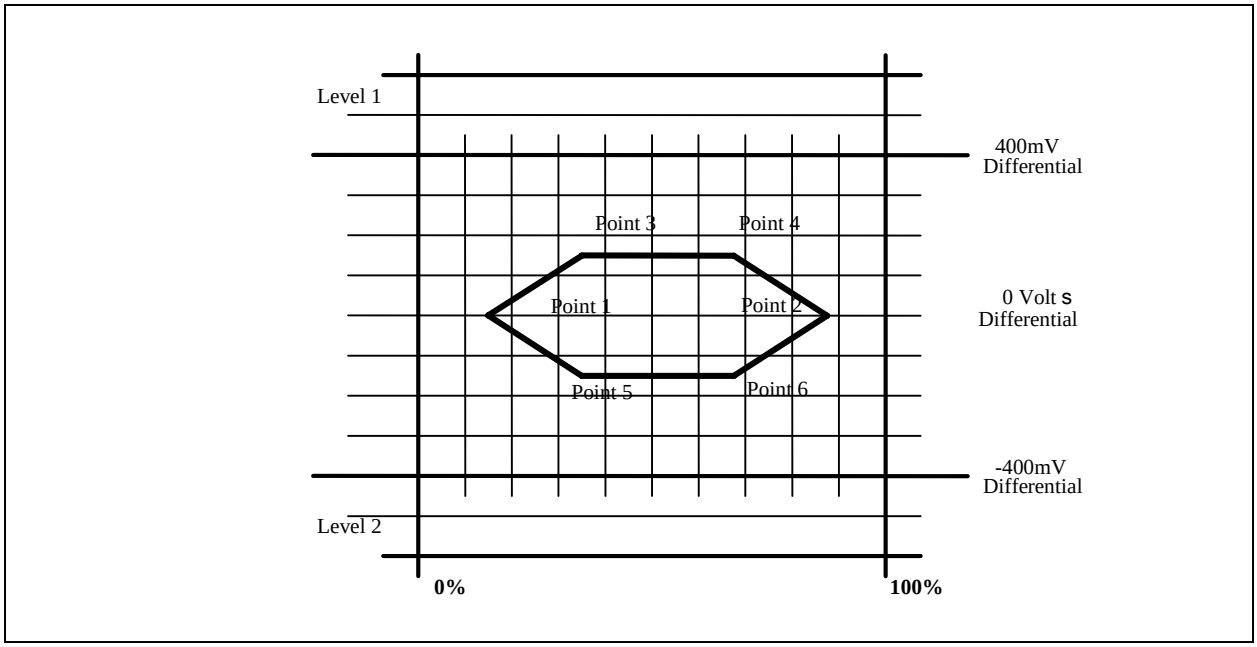


Figure 6.5 Eye Pattern for Receive Waveform and Eye Pattern Definition

	VOLTAGE LEVEL (D+, D-)	TIME (% OF UNIT INTERVAL)
Level 1	575mV	N/A
Level 2	-575mV	N/A
Point 1	0V	15% UI
Point 2	0V	85% UI
Point 3	150mV	35% UI
Point 4	150mV	65% UI
Point 5	-150mV	35% UI
Point 6	-150mV	65% UI

Chapter 7 Functional Overview

Figure 2.1 on page 7 shows the functional block diagram of the USB3290. Each of the functions is described in detail below.

7.1 Modes of Operation

The USB3290 supports an 8-bit bi-directional parallel interface.

- CLKOUT runs at 60MHz
- The 8-bit data bus (DATA[7:0]) is used for transmit when TXVALID = 1
- The 8-bit data bus (DATA[7:0]) is used for receive when TXVALID = 0

7.2 System Clocking

This block connects to either an external 24MHz crystal or an external clock source and generates a 480MHz multi-phase clock. The clock is used in the CRC block to over-sample the incoming received data, resynchronize the transmit data, and is divided down to 60MHz (CLKOUT) which acts as the system byte clock. The PLL block also outputs a clock valid signal to the other parts of the transceiver when the clock signal is stable. All UTMI signals are synchronized to the CLKOUT output. The behavior of the CLKOUT is as follows:

- Produce the first CLKOUT transition no later than 5.6ms after negation of SUSPENDN. The CLKOUT signal frequency error is less than 10% at this time.
- The CLKOUT signal will fully meet the required accuracy of ±500ppm no later than 1.4ms after the first transition of CLKOUT.

In HS mode there is one CLKOUT cycle per byte time. The frequency of CLKOUT does not change when the PHY is switched between HS to FS modes. In FS mode there are 5 CLKOUT cycles per FS bit time, typically 40 CLKOUT cycles per FS byte time. If a received byte contains a stuffed bit then the byte boundary can be stretched to 45 CLKOUT cycles, and two stuffed bits would result in a 50 CLKOUT cycles.

Figure 7.1 shows the relationship between CLKOUT and the transmit data transfer signals in FS mode. TXREADY is only asserted for one CLKOUT per byte time to signal the SIE that the data on the DATA lines has been read by the PHY. The SIE may hold the data on the DATA lines for the duration of the byte time. Transitions of TXVALID must meet the defined setup and hold times relative to CLKOUT.

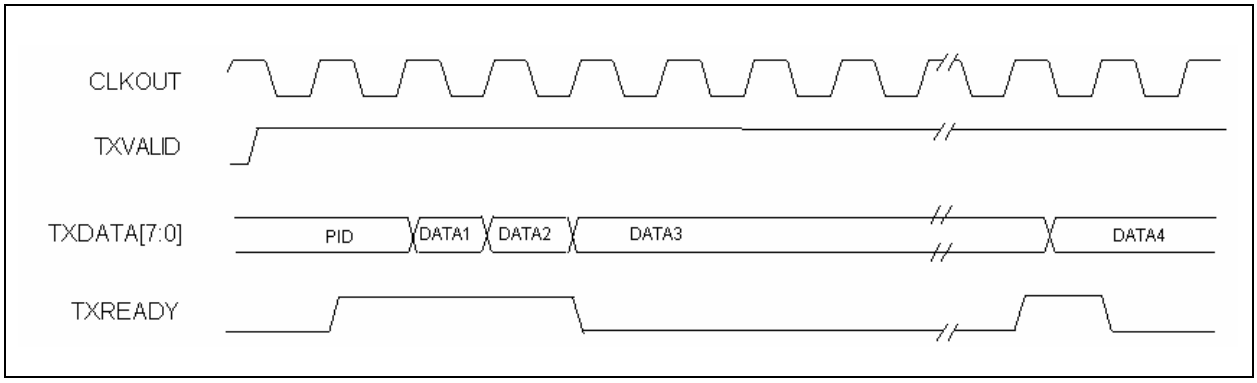


Figure 7.1 FS CLK Relationship to Transmit Data and Control Signals

Figure 7.2 shows the relationship between CLKOUT and the receive data control signals in FS mode. RXACTIVE "frames" a packet, transitioning only at the beginning and end of a packet. However transitions of RXVALID may take place any time 8 bits of data are available. Figure 7.1 also shows how RXVALID is only asserted for one CLKOUT cycle per byte time even though the data may be presented for the full byte time. The XCVRSELECT signal determines whether the HS or FS timing relationship is applied to the data and control signals.

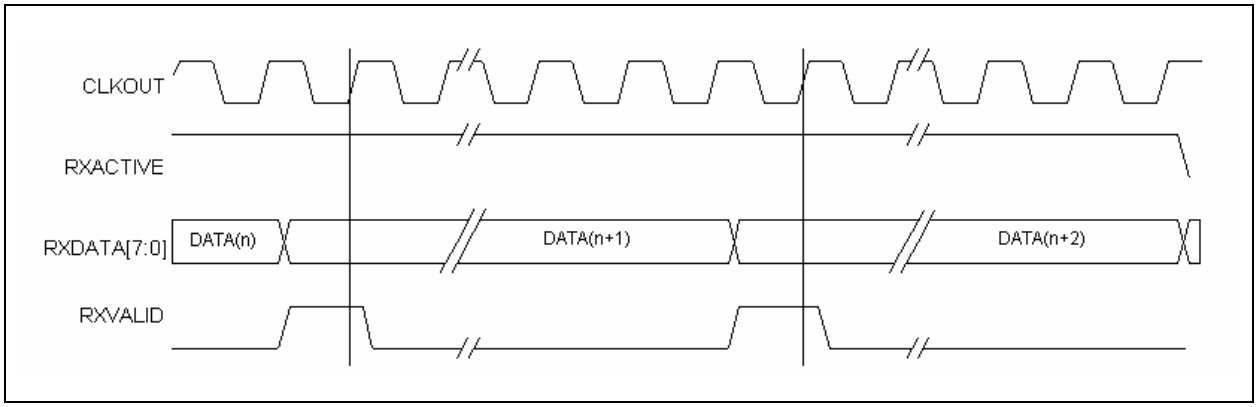


Figure 7.2 FS CLK Relationship to Receive Data and Control Signals

7.3 Clock and Data Recovery Circuit

This block consists of the Clock and Data Recovery Circuit and the Elasticity Buffer. The Elasticity Buffer is used to compensate for differences between the transmitting and receiving clock domains. The USB 2.0 specification defines a maximum clock error of ±1000ppm of drift.

7.4 TX Logic

This block receives parallel data bytes placed on the DATA bus and performs the necessary transmit operations. These operations include parallel to serial conversion, bit stuffing and NRZI encoding. Upon valid assertion of the proper TX control lines by the SIE and TX State Machine, the TX LOGIC block will synchronously shift, at either the FS or HS rate, the data to the FS/HS TX block to be transmitted on the USB cable. Data transmit timing is shown in Figure 7.3.

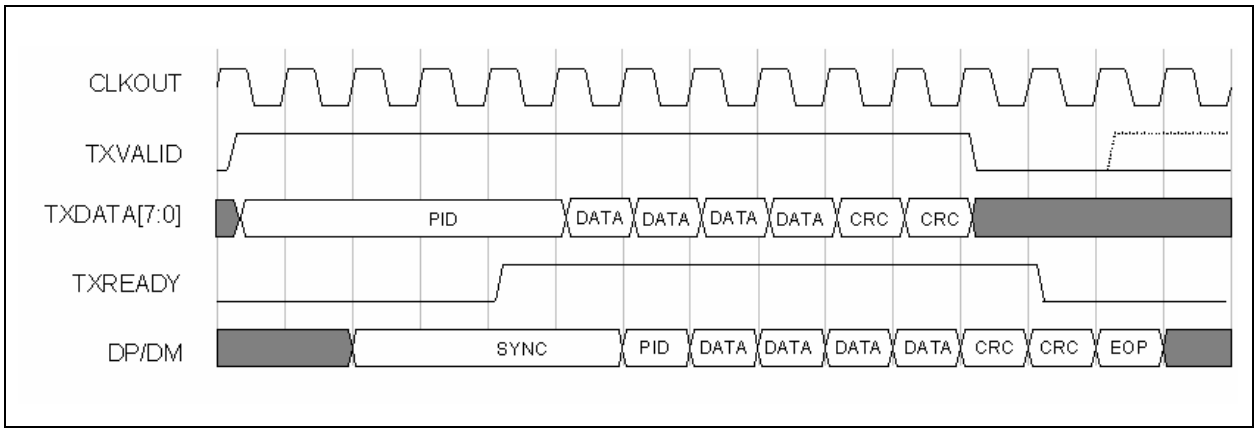


Figure 7.3 Transmit Timing for a Data Packet

The behavior of the Transmit State Machine is described below.

- Asserting a RESET forces the transmit state machine into the Reset state which negates TXREADY. When RESET is negated the transmit state machine will enter a wait state.
- The SIE asserts TXVALID to begin a transmission.
- After the SIE asserts TXVALID it can assume that the transmission has started when it detects TXREADY has been asserted.
- The SIE must assume that the USB3290 has consumed a data byte if TXREADY and TXVALID are asserted on the rising edge of CLKOUT.
- The SIE must have valid packet information (PID) asserted on the DATA bus coincident with the assertion of TXVALID.
- TXREADY is sampled by the SIE on the rising edge of CLKOUT.
- The SIE negates TXVALID to complete a packet. Once negated, the transmit logic will never reassert TXREADY until after the EOP has been generated. (TXREADY will not re-assert until TXVALD asserts again.
- The USB3290 is ready to transmit another packet immediately, however the SIE must conform to the minimum inter-packet delays identified in the USB 2.0 specification.

7.5 RX Logic

This block receives serial data from the CRC block and processes it to be transferred to the SIE on the DATA bus. The processing involved includes NRZI decoding, bit unstuffing, and serial to parallel conversion. Upon valid assertion of the proper RX control lines by the RX State Machine, the RX Logic block will provide bytes to the DATA bus as shown in the figures below. The behavior of the Receive State Machine is described below.

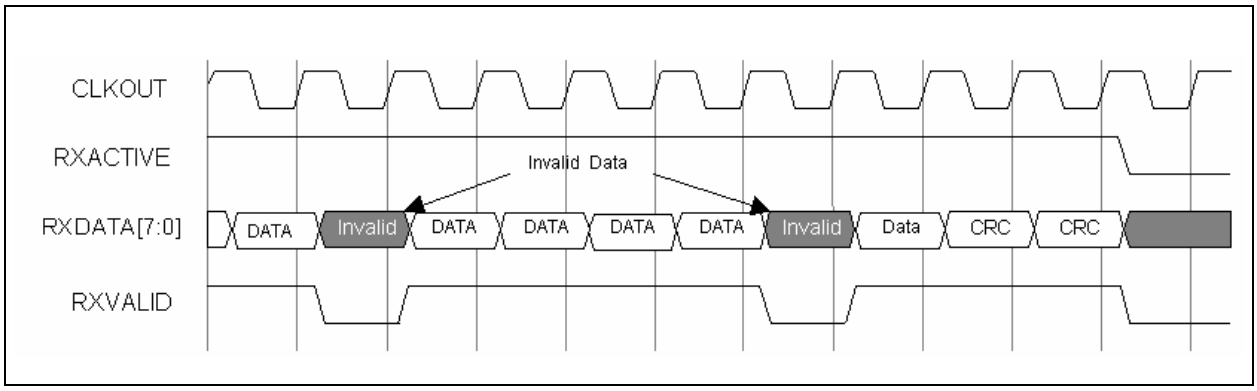


Figure 7.4 Receive Timing for Data with Unstuffed Bits

The assertion of RESET will force the Receive State Machine into the *Reset* state. The *Reset* state deasserts RXACTIVE and RXVALID. When the RESET signal is deasserted the Receive State Machine enters the *RX Wait* state and starts looking for a SYNC pattern on the USB. When a SYNC pattern is detected the state machine will enter the *Strip SYNC* state and assert RXACTIVE. The length of the received Hi-Speed SYNC pattern varies and can be up to 32 bits long or as short as 12 bits long when at the end of five hubs. As a result, the state machine may remain in the *Strip SYNC* state for several byte times before capturing the first byte of data and entering the *RX Data* state.

After valid serial data is received, the state machine enters the *RX Data* state, where the data is loaded into the RX Holding Register on the rising edge of CLKOUT and RXVALID is asserted. The SIE must clock the data off the DATA bus on the next rising edge of CLKOUT. If OPMODE = Normal, then stuffed bits are stripped from the data stream. Each time 8 stuffed bits are accumulated the state machine will enter the *RX Data Wait* state, negating RXVALID thus skipping a byte time.

When the EOP is detected the state machine will enter the *Strip EOP* state and negate RXACTIVE and RXVALID. After the EOP has been stripped the Receive State Machine will reenter the *RX Wait* state and begin looking for the next packet.

The behavior of the Receive State Machine is described below:

- RXACTIVE and RXREADY are sampled on the rising edge of CLKOUT.
- In the RX Wait state the receiver is always looking for SYNC.
- The USB3290 asserts RXACTIVE when SYNC is detected (Strip SYNC state).
- The USB3290 negates RXACTIVE when an EOP is detected and the elasticity buffer is empty (Strip EOP state).
- When RXACTIVE is asserted, RXVALID will be asserted if the RX Holding Register is full.
- RXVALID will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXACTIVE and RXVALID are asserted (RX Data state).
- Figure 7.5 shows the timing relationship between the received data (DP/DM), RXVALID, RXACTIVE, RXERROR and DATA signals.

Notes:

- The USB 2.0 Transceiver does NOT decode Packet ID's (PIDs). They are passed to the SIE for decoding.
- Figure 7.5, Figure 7.6 and Figure 7.7 are timing examples of a HS/FS PHY when it is in HS mode. When a HS/FS PHY is in FS Mode there are approximately 40 CLKOUT cycles every byte time. The Receive State Machine assumes that the SIE captures the data on the DATA bus if RXACTIVE and RXVALID are asserted. In FS mode, RXVALID will only be asserted for one CLKOUT per byte time.
- In Figure 7.5, Figure 7.6 and Figure 7.7 the SYNC pattern on DP/DM is shown as one byte long. The SYNC pattern received by a device can vary in length. These figures assume that all but the last 12 bits have been consumed by the hubs between the device and the host controller.

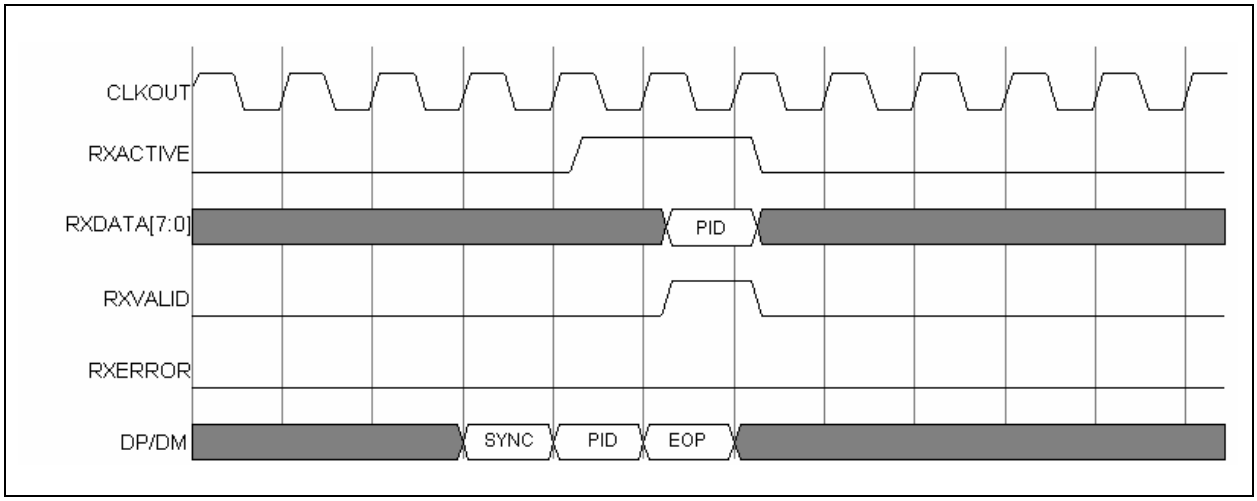


Figure 7.5 Receive Timing for a Handshake Packet (no CRC)

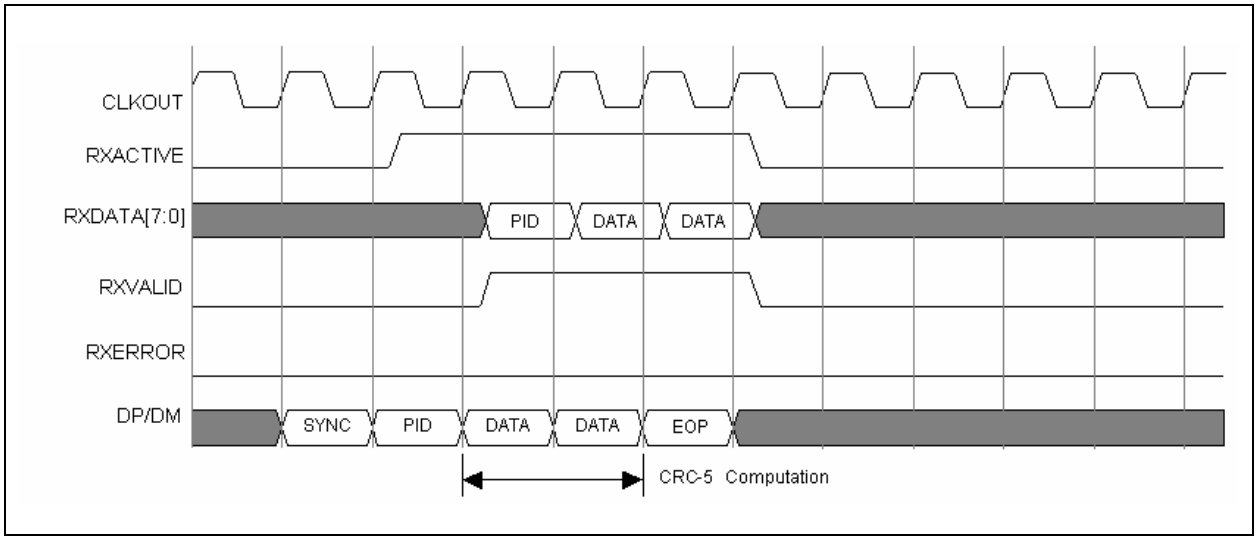


Figure 7.6 Receive Timing for Setup Packet

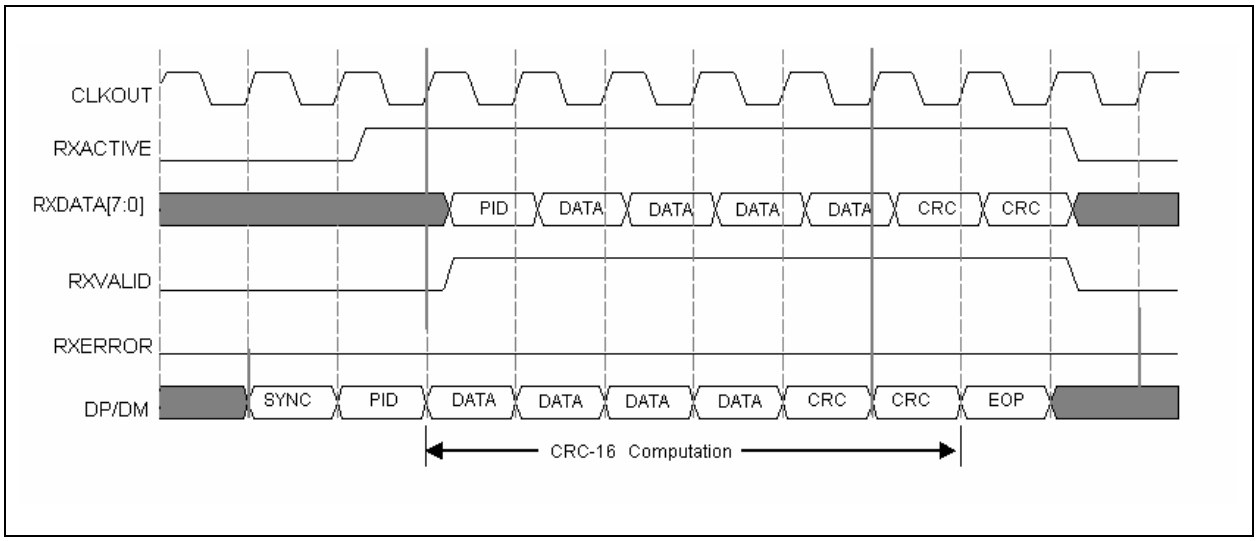


Figure 7.7 Receive Timing for Data Packet (with CRC-16)

The receivers connect directly to the USB cable. The block contains a separate differential receiver for HS and FS mode. Depending on the mode, the selected receiver provides the serial data stream through the mulitplexer to the RX Logic block. The FS mode section of the FS/HS RX block also consists of a single-ended receiver on each of the data lines to determine the correct FS LINESTATE. For HS mode support, the FS/HS RX block contains a squelch circuit to insure that noise is never interpreted as data.

7.6 USB 2.0 Transceiver

The SMSC Hi-Speed USB 2.0 Transceiver consists of the High Speed and Full Speed Transceivers, and the Termination resistors.

7.6.1 High Speed and Full Speed Transceivers

The USB3290 transceiver meets all requirements in the USB 2.0 specification.

The receivers connect directly to the USB cable. This block contains a separate differential receiver for HS and FS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. The FS mode section of the FS/HS RX block also consists of a single-ended receiver on each of the data lines to determine the correct FS linestate. For HS mode support, the FS/HS RX block contains a squelch circuit to insure that noise is never interpreted as data.

The transmitters connect directly to the USB cable. The block contains a separate differential FS and HS transmitter which receive encoded, bit stuffed, serialized data from the TX Logic block and transmit it on the USB cable.

7.6.2 Termination Resistors

The USB3290 transceiver fully integrates all of the USB termination resistors. The USB3290 includes the 1.5kΩ pull-up resistor on DP. In addition the 45Ω high speed termination resistors are also integrated. These integrated resistors require no tuning or trimming. The state of the resistors is determined by the operating mode of the PHY. The possible valid resistor combinations are shown in Table 7.1.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- HSTERM_EN activates the 45Ω DP and DM high speed termination resistors

Table 7.1 DP/DM Termination vs. Signaling Mode

SIGNALING MODE	UTMI+ INTERFACE SETTINGS			RESISTOR SETTINGS	
	XCVRSELECT	TERMSELECT	OPMODE[1:0]	RPU_DP_EN	HSTERM_EN
Tri-State Drivers	Xb	Xb	01b	0b	0b
Power-up	1b	0b	00b	0b	0b
Peripheral Chirp	0b	1b	10b	1b	0b
Peripheral HS	0b	0b	00b	0b	1b
Peripheral FS	1b	1b	00b	1b	0b
Peripheral HS/FS Suspend	1b	1b	00b	1b	0b
Peripheral HS/FS Resume	1b	1b	10b	1b	0b
Peripheral Test J/Test K	0b	0b	10b	0b	1b

7.6.3 Bias Generator

This block consists of an internal bandgap reference circuit used for generating the high speed driver currents and the biasing of the analog circuits. This block requires an external 12kΩ, 1% tolerance, external reference resistor connected from RBIAS to ground.

7.7 Crystal Oscillator and PLL

The USB3290 uses an internal crystal driver and PLL sub-system to provide a clean 480MHz reference clock that is used by the PHY during both transmit and receive. The USB3290 requires a clean 24MHz crystal or clock as a frequency reference. If the 24MHz reference is noisy or off frequency the PHY may not operate correctly.

The USB3290 can use either a crystal or an external clock oscillator for the 24MHz reference. The crystal is connected to the XI and XO pins as shown in the application diagram, Figure 8.10. If a clock oscillator is used the clock should be connected to the XI input and the XO pin left floating. When a external clock is used the XI pin is designed to be driven with a 0 to 3.3 volt signal. When using an external clock the user needs to take care to ensure the external clock source is clean enough to not degrade the high speed eye performance.

Once, the 480MHz PLL has locked to the correct frequency it will drive the CLKOUT pin with a 60MHz clock.

7.8 Internal Regulators and POR

The USB3290 includes an integrated set of built in power management functions. These power management features include a POR generation and allow the USB3290 to be powered from a single 3.3 volt power supply. This reduces the bill of materials and simplifies product design.

7.8.1 Internal Regulators

The USB3290 has two integrated 3.3 volt to 1.8 volt regulators. These regulators require an external 4.7uF +/-20% low ESR bypass capacitor to ensure stability. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower than 0.1 ohm at frequencies greater than 10kHz.

The two regulator outputs, which require bypass capacitors, are the pins labeled VDDA1.8 and VDD1.8. Each pin requires a 4.7uF bypass capacitor placed as close to the pin as possible.

Note: The USB3290 regulators are designed to generate a 1.8 volt supply for the USB3290 only. Using the regulators to provide current for other circuits is not recommended and SMSC does not guarantee USB performance or regulator stability.

7.8.2 Power On Reset (POR)

The USB3290 provides an internal POR circuit that generates a reset pulse once the PHY supplies are stable.

7.8.3 Reset Pin

The UTMI+ Digital can be reset at any time with the RESET pin. The RESET pin of the USB3290 may be asynchronously asserted and de-asserted so long as it is held in the asserted state continuously for a duration greater than one CLKOUT cycle. The RESET input may be asserted when the USB3290 CLKOUT signal is not active (i.e. in the suspend state caused by asserting the SUSPENDN input) but reset must only be de-asserted when the USB3290 CLKOUT signal is active and the RESET has been held asserted for a duration greater than one CKOUT clock cycle. No other PHY digital input signals may change state for two CLKOUT clock cycles after the de-assertion of the reset signal.

Chapter 8 Application Notes

The following sections consist of select functional explanations to aid in implementing the USB3290 into a system. For complete description and specifications consult the *USB 2.0 Transceiver Macrocell Interface Specification* and *Universal Serial Bus Specification Revision 2.0.*

8.1 Linestate

The voltage thresholds that the LINESTATE[1:0] signals use to reflect the state of DP and DM depend on the state of XCVRSELECT. LINESTATE[1:0] uses HS thresholds when the HS transceiver is enabled (XCVRSELECT = 0) and FS thresholds when the FS transceiver is enabled (XCVRSELECT = 1). There is not a concept of variable single-ended thresholds in the USB 2.0 specification for HS mode.

The HS receiver is used to detect Chirp J or K, where the output of the HS receiver is always qualified with the Squelch signal. If squelched, the output of the HS receiver is ignored. In the USB3290, as an alternative to using variable thresholds for the single-ended receivers, the following approach is used.

Table 8.1 Linestate States

		STATE OF DP/DM LINES		
LINESTATE[1:0]		**FULL SPEED XCVRSELECT =1 TERMSELECT=1**	**HIGH SPEED XCVRSELECT =0 TERMSELECT=0**	**CHIRP MODE XCVRSELECT =0 TERMSELECT=1**
LS[1]	**LS[0]**			
0	0	SE0	Squelch	Squelch
0	1	J	!Squelch	!Squelch & HS Differential Receiver Output
1	0	K	Invalid	!Squelch & !HS Differential Receiver Output
1	1	SE1	Invalid	Invalid

In HS mode, 3ms of no USB activity (IDLE state) signals a reset. The SIE monitors LINESTATE[1:0] for the IDLE state. To minimize transitions on LINESTATE[1:0] while in HS mode, the presence of !Squelch is used to force LINESTATE[1:0] to a J state.

8.2 OPMODES

The OPMODE[1:0] pins allow control of the operating modes.

Table 8.2 Operational Modes

MODE[1:0]	STATE#	STATE NAME	DESCRIPTION
00	0	Normal Operation	Transceiver operates with normal USB data encoding and decoding
01	1	Non-Driving	Allows the transceiver logic to support a soft disconnect feature which tri-states both the HS and FS transmitters, and removes any termination from the USB making it appear to an upstream port that the device has been disconnected from the bus
10	2	Disable Bit Stuffing and NRZI encoding	Disables bitstuffing and NRZI encoding logic so that 1's loaded from the DATA bus become 'J's on the DP/DM and 0's become 'K's
11	3	Reserved	N/A

The OPMODE[1:0] signals are normally changed only when the transmitter and the receiver are quiescent, i.e. when entering a test mode or for a device initiated resume.

When using OPMODE[1:0] = 10 (state 2), OPMODES are set, and then 5 60MHz clocks later, TXVALID is asserted. In this case, the SYNC and EOP patterns are not transmitted.

The only exception to this is when OPMODE[1:0] is set to state 2 while TXVALID has been asserted (the transceiver is transmitting a packet), in order to flag a transmission error. In this case, the USB3290 has already transmitted the SYNC pattern so upon negation of TXVALID the EOP must also be transmitted to properly terminate the packet. Changing the OPMODE[1:0] signals under all other conditions, while the transceiver is transmitting or receiving data will generate undefined results.

Under no circumstances should the device controller change OPMODE while the DP/DM lines are still transmitting or unpredictable changes on DP/DM are likely to occur. The same applies for TERMSELECT and XCVRSELECT.

8.3 Test Mode Support

Table 8.3 USB 2.0 Test Modes

USB 2.0 TEST MODES	USB3290 **SETUP**		
	OPERATIONAL MODE	**SIE TRANSMITTED DATA**	**XCVRSELECT & TERMSELECT**
SE0_NAK	State 0	No transmit	HS
J	State 2	All '1's	HS
K	State 2	All '0's	HS
Test_Packet	State 0	Test Packet data	HS

8.4 SE0 Handling

For FS operation, IDLE is a J state on the bus. SE0 is used as part of the EOP or to indicate reset. When asserted in an EOP, SE0 is never asserted for more than 2 bit times. The assertion of SE0 for more than 2.5us is interpreted as a reset by the device operating in FS mode.

For HS operation, IDLE is a SE0 state on the bus. SE0 is also used to reset a HS device. A HS device cannot use the 2.5us assertion of SE0 (as defined for FS operation) to indicate reset since the bus is often in this state between packets. If no bus activity (IDLE) is detected for more than 3ms, a HS device must determine whether the downstream facing port is signaling a suspend or a reset. The following section details how this determination is made. If a reset is signaled, the HS device will then initiate the HS Detection Handshake protocol.

8.5 Reset Detection

If a device in HS mode detects bus inactivity for more than 3ms (T1), it reverts to FS mode. This enables the FS pull-up on the DP line in an attempt to assert a continuous FS J state on the bus. The SIE must then check LINESTATE for the SE0 condition. If SE0 is asserted at time T2, then the upstream port is forcing the reset state to the device (i.e., a Driven SE0). The device will then initiate the HS detection handshake protocol.

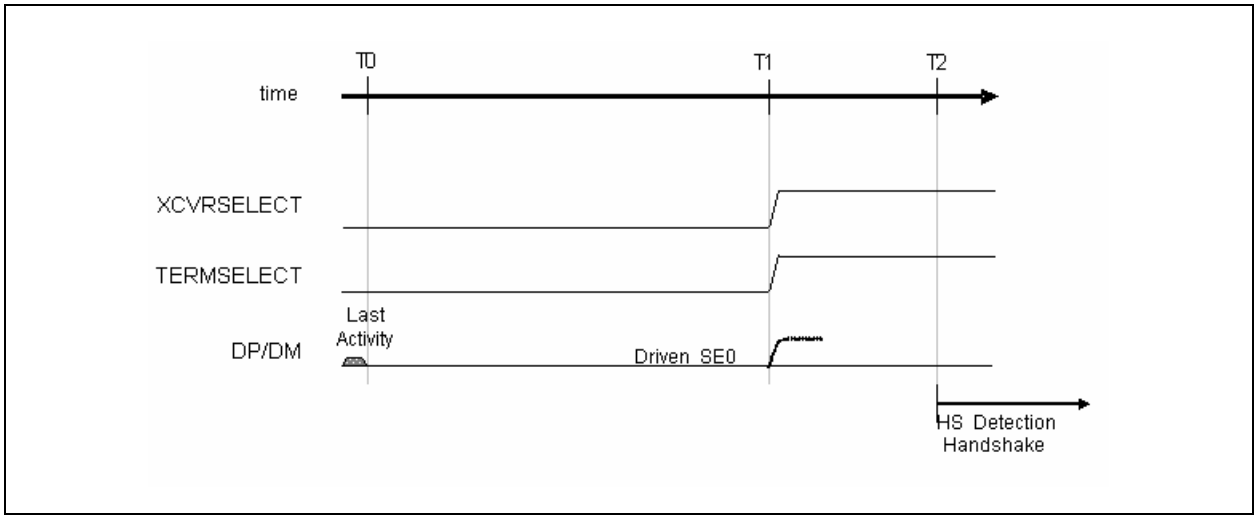


Figure 8.1 Reset Timing Behavior (HS Mode)

Table 8.4 Reset Timing Values (HS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
HS Reset T0	Bus activity ceases, signaling either a reset or a SUSPEND.	0 (reference)
T1	Earliest time at which the device may place itself in FS mode after bus activity stops.	HS Reset T0 + 3. 0ms < T1 < HS Reset T0 + 3.125ms
T2	SIE samples LINESTATE. If LINESTATE = SE0, then the SE0 on the bus is due to a Reset state. The device now enters the HS Detection Handshake protocol.	T1 + 100µs < T2 < T1 + 875µs

8.6 Suspend Detection

If a HS device detects SE0 asserted on the bus for more than 3ms (T1), it reverts to FS mode. This enables the FS pull-up on the DP line in an attempt to assert a continuous FS J state on the bus. The SIE must then check LINESTATE for the J condition. If J is asserted at time T2, then the upstream port is asserting a soft SE0 and the USB is in a J state indicating a suspend condition. By time T4 the device must be fully suspended.

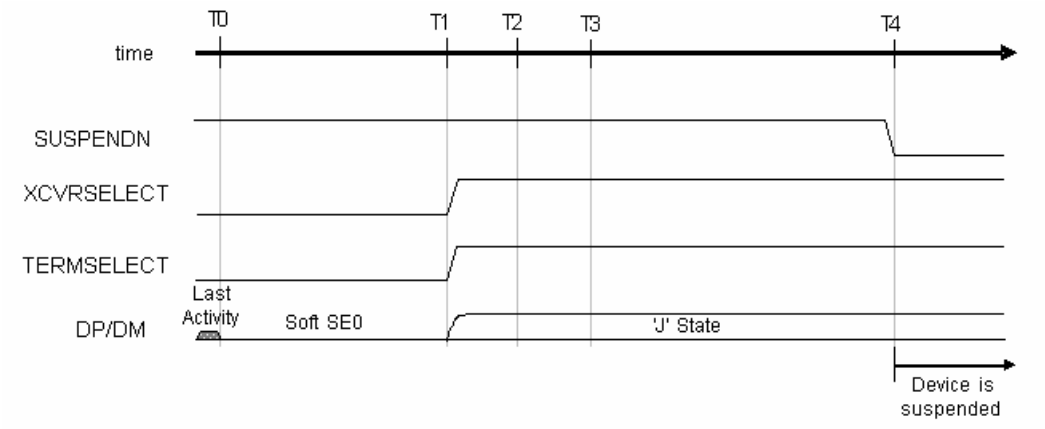


Figure 8.2 Suspend Timing Behavior (HS Mode)

Table 8.5 Suspend Timing Values (HS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
HS Reset T0	End of last bus activity, signaling either a reset or a SUSPEND.	0 (reference)
T1	The time at which the device must place itself in FS mode after bus activity stops.	HS Reset T0 + 3. 0ms < T1 < HS Reset T0 + 3.125ms
T2	SIE samples LINESTATE. If LINESTATE = 'J', then the initial SE0 on the bus (T0 - T1) had been due to a Suspend state and the SIE remains in HS mode.	T1 + 100 µs < T2 < T1 + 875µs
T3	The earliest time where a device can issue Resume signaling.	HS Reset T0 + 5ms
T4	The latest time that a device must actually be suspended, drawing no more than the suspend current from the bus.	HS Reset T0 + 10ms

8.7 HS Detection Handshake

The High Speed Detection Handshake process is entered from one of three states: suspend, active FS or active HS. The downstream facing port asserting an SE0 state on the bus initiates the HS Detection Handshake. Depending on the initial state, an SE0 condition can be asserted from 0 to 4 ms before initiating the HS Detection Handshake. These states are described in the USB 2.0 specification.

There are three ways in which a device may enter the HS Handshake Detection process:

1. If the device is suspended and it detects an SE0 state on the bus it may immediately enter the HS handshake detection process.
2. If the device is in FS mode and an SE0 state is detected for more than 2.5µs. it may enter the HS handshake detection process.
3. If the device is in HS mode and an SE0 state is detected for more than 3.0ms. it may enter the HS handshake detection process. In HS mode, a device must first determine whether the SE0 state is signaling a suspend or a reset condition. To do this the device reverts to FS mode by placing XCVRSELECT and TERMSELECT into FS mode. The device must not wait more than 3.125ms before the reversion to FS mode. After reverting to FS mode, no less than 100µs and no more than 875µs later the SIE must check the LINESTATE signals. If a J state is detected the device will enter a suspend state. If an SE0 state is detected, then the device will enter the HS Handshake detection process.

In each case, the assertion of the SE0 state on the bus initiates the reset. The minimum reset interval is 10ms. Depending on the previous mode that the bus was in, the delay between the initial assertion of the SE0 state and entering the HS Handshake detection can be from 0 to 4ms.

This transceiver design pushes as much of the responsibility for timing events on to the SIE as possible, and the SIE requires a stable CLKOUT signal to perform accurate timing. In case 2 and 3 above, CLKOUT has been running and is stable, however in case 1 the USB3290 is reset from a suspend state, and the internal oscillator and clocks of the transceiver are assumed to be powered down. A device has up to 6ms after the release of SUSPENDN to assert a minimum of a 1ms Chirp K.

8.8 HS Detection Handshake – FS Downstream Facing Port

Upon entering the HS Detection process (T0) XCVRSELECT and TERMSELECT are in FS mode. The DP pull-up is asserted and the HS terminations are disabled. The SIE then sets OPMODE to *Disable Bit Stuffing and NRZI encoding*, XCVRSELECT to HS mode, and begins the transmission of all 0's data, which asserts a HS K (chirp) on the bus (T1). The device chirp must last at least 1.0ms, and must end no later than 7.0ms after HS Reset T0. At time T1 the device begins listening for a chirp sequence from the host port.

If the downstream facing port is not HS capable, then the HS K asserted by the device is ignored and the alternating sequence of HS Chirp K's and J's is not generated. If no chirps are detected (T4) by the device, it will enter FS mode by returning XCVRSELECT to FS mode.

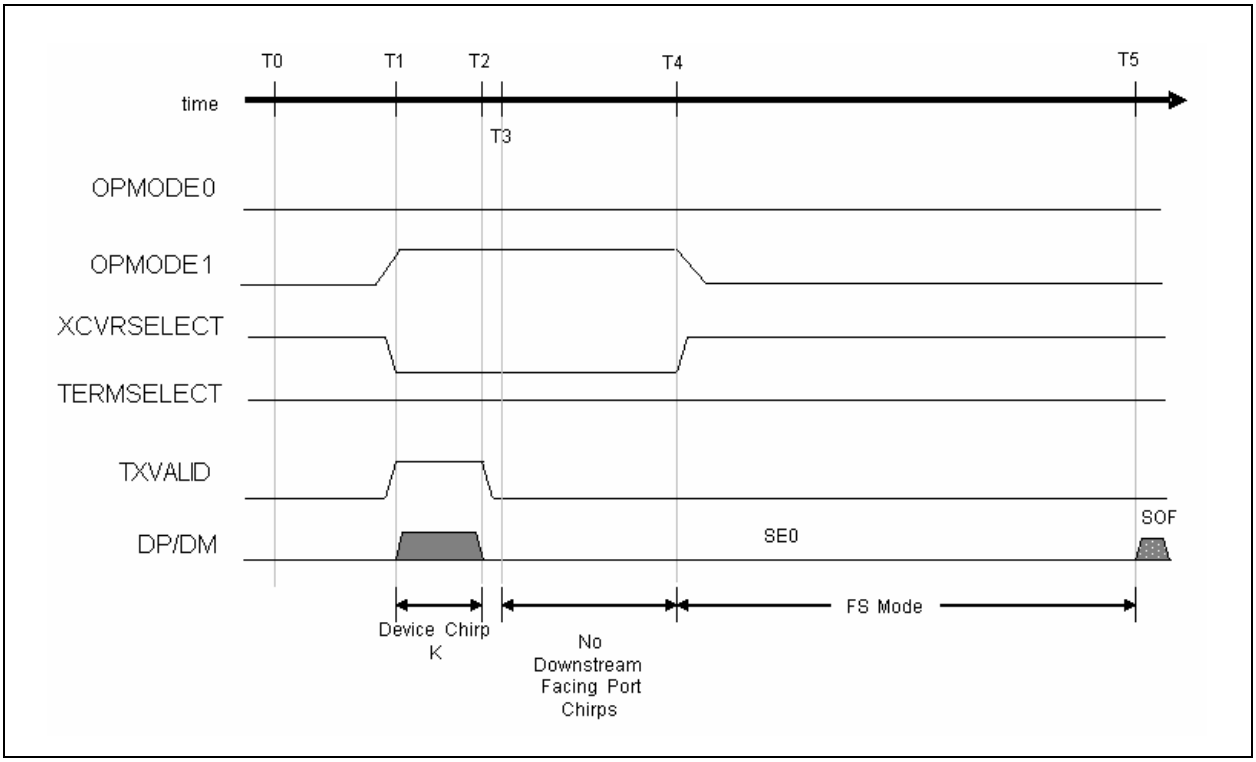


Figure 8.3 HS Detection Handshake Timing Behavior (FS Mode)

Table 8.6 HS Detection Handshake Timing Values (FS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
T0	HS Handshake begins. DP pull-up enabled, HS terminations disabled.	0 (reference)
T1	Device enables HS Transceiver and asserts Chirp K on the bus.	T0 < T1 < HS Reset T0 + 6.0ms
T2	Device removes Chirp K from the bus. 1ms minimum width.	T1 + 1.0 ms < T2 < HS Reset T0 + 7.0ms
T3	Earliest time when downstream facing port may assert Chirp KJ sequence on the bus.	T2 < T3 < T2+100µs
T4	Chirp not detected by the device. Device reverts to FS default state and waits for end of reset.	T2 + 1.0ms < T4 < T2 + 2.5ms
T5	Earliest time at which host port may end reset	HS Reset T0 + 10ms

Notes:

- T0 may occur to 4ms after HS Reset T0.
- The SIE must assert the Chirp K for 66000 CLKOUT cycles to ensure a 1ms minimum duration.

8.9 HS Detection Handshake – HS Downstream Facing Port

Upon entering the HS Detection process (T0) XCVRSELECT and TERMSELECT are in FS mode. The DP pull-up is asserted and the HS terminations are disabled. The SIE then sets OPMODE to *Disable Bit Stuffing and NRZI encoding*, XCVRSELECT to HS mode, and begins the transmission of all 0's data, which asserts a HS K (chirp) on the bus (T1). The device chirp must last at least 1.0ms, and must end no later than 7.0ms after HS Reset T0. At time T1 the device begins listening for a chirp sequence from the downstream facing port. If the downstream facing port is HS capable then it will begin generating an alternating sequence of Chirp K's and Chirp J's (T3) after the termination of the chirp from the device (T2). After the device sees the valid chirp sequence Chirp K-J-K-J-K-J (T6), it will enter HS mode by setting TERMSELECT to HS mode (T7).

Figure 8.4 provides a state diagram for Chirp K-J-K-J-K-J validation. Prior to the end of reset (T9) the device port must terminate the sequence of Chirp K's and Chirp J's (T8) and assert SE0 (T8-T9). Note that the sequence of Chirp K's and Chirp J's constitutes bus activity.

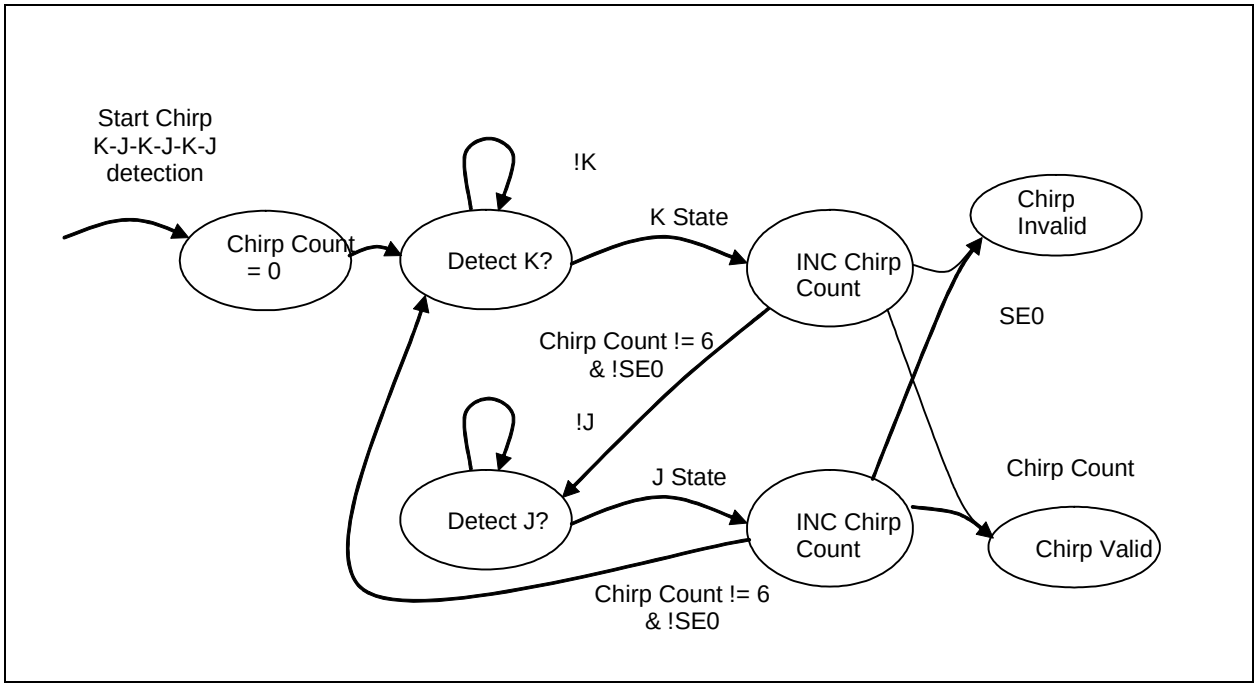


Figure 8.4 Chirp K-J-K-J-K-J Sequence Detection State Diagram

The Chirp K-J-K-J-K-J sequence occurs too slow to propagate through the serial data path, therefore LINESTATE signal transitions must be used by the SIE to step through the Chirp K-J-K-J-K-J state diagram, where "K State" is equivalent to LINESTATE = K State and "J State" is equivalent to LINESTATE = J State. The SIE must employ a counter (Chirp Count) to count the number of Chirp K and Chirp J states. Note that LINESTATE does not filter the bus signals so the requirement that a bus state must be "continuously asserted for 2.5µs" must be verified by the SIE sampling the LINESTATE signals.

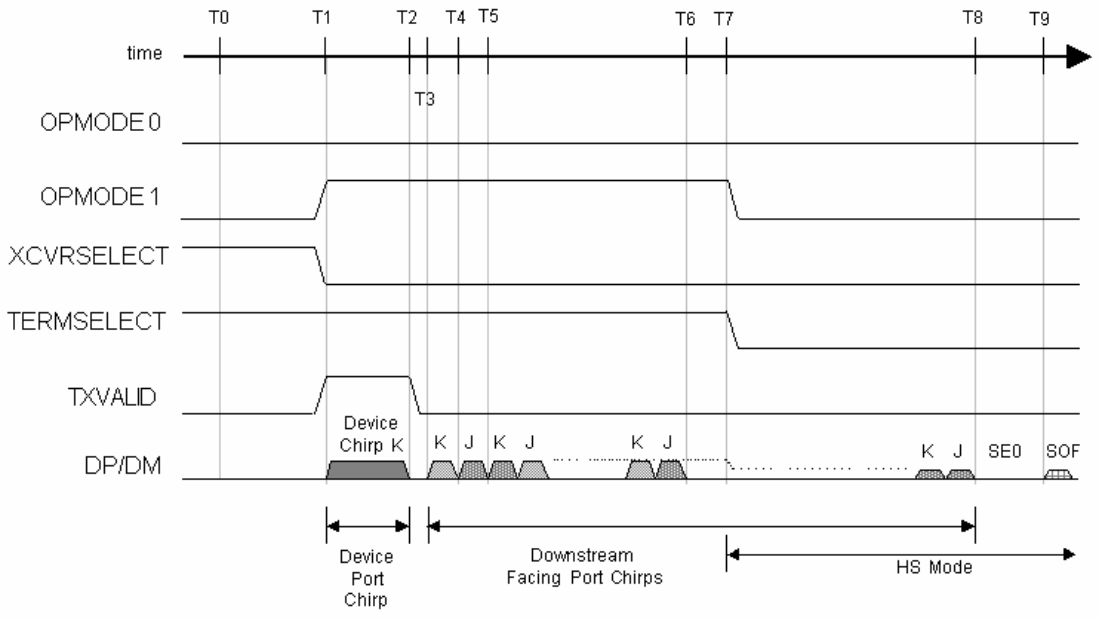


Figure 8.5 HS Detection Handshake Timing Behavior (HS Mode)

Table 8.7 Reset Timing Values

TIMING PARAMETER	DESCRIPTION	VALUE
T0	HS Handshake begins. DP pull-up enabled, HS terminations disabled.	0 (reference)
T1	Device asserts Chirp K on the bus.	T0 < T1 < HS Reset T0 + 6.0ms
T2	Device removes Chirp K from the bus. 1 ms minimum width.	T0 + 1.0ms < T2 < HS Reset T0 + 7.0ms
T3	Downstream facing port asserts Chirp K on the bus.	T2 < T3 < T2+100µs
T4	Downstream facing port toggles Chirp K to Chirp J on the bus.	T3 + 40µs < T4 < T3 + 60µs
T5	Downstream facing port toggles Chirp J to Chirp K on the bus.	T4 + 40µs < T5 < T4 + 60µs
T6	Device detects downstream port chirp.	T6
T7	Chirp detected by the device. Device removes DP pull-up and asserts HS terminations, reverts to HS default state and waits for end of reset.	T6 < T7 < T6 + 500µs
T8	Terminate host port Chirp K-J sequence (Repeating T4 and T5)	T9 - 500µs < T8 < T9 - 100µs
T9	The earliest time at which host port may end reset. The latest time, at which the device may remove the DP pull-up and assert the HS terminations, reverts to HS default state.	HS Reset T0 + 10ms

Notes:

- T0 may be up to 4ms after HS Reset T0.
- The SIE must use LINESTATE to detect the downstream port chirp sequence.
- Due to the assertion of the HS termination on the host port and FS termination on the device port, between T1 and T7 the signaling levels on the bus are higher than HS signaling levels and are less than FS signaling levels.

8.10 HS Detection Handshake – Suspend Timing

If reset is entered from a suspended state, the internal oscillator and clocks of the transceiver are assumed to be powered down. Figure 8.6 shows how CLKOUT is used to control the duration of the chirp generated by the device.

When reset is entered from a suspended state (J to SE0 transition reported by LINESTATE), SUSPENDN is combinatorially negated at time T0 by the SIE. It takes approximately 5 milliseconds for the transceiver's oscillator to stabilize. The device does not generate any transitions of the CLKOUT signal until it is "usable" (where "usable" is defined as stable to within ±10% of the nominal frequency and the duty cycle accuracy 50±5%).

The first transition of CLKOUT occurs at T1. The SIE then sets OPMODE to *Disable Bit Stuffing and NRZI encoding*, XCVRSELECT to HS mode, and must assert a Chirp K for 66000 CLKOUT cycles to ensure a 1ms minimum duration. If CLKOUT is 10% fast (66MHz) then Chirp K will be 1.0ms. If CLKOUT is 10% slow (54 MHz) then Chirp K will be 1.2ms. The 5.6ms requirement for the first CLKOUT transition after SUSPENDN, ensures enough time to assert a 1ms Chirp K and still complete before T3. Once the Chirp K is completed (T3) the SIE can begin looking for host chirps and use CLKOUT to time the process. At this time, the device follows the same protocol as in Section 8.9, "HS Detection Handshake – HS Downstream Facing Port" for completion of the High Speed Handshake.

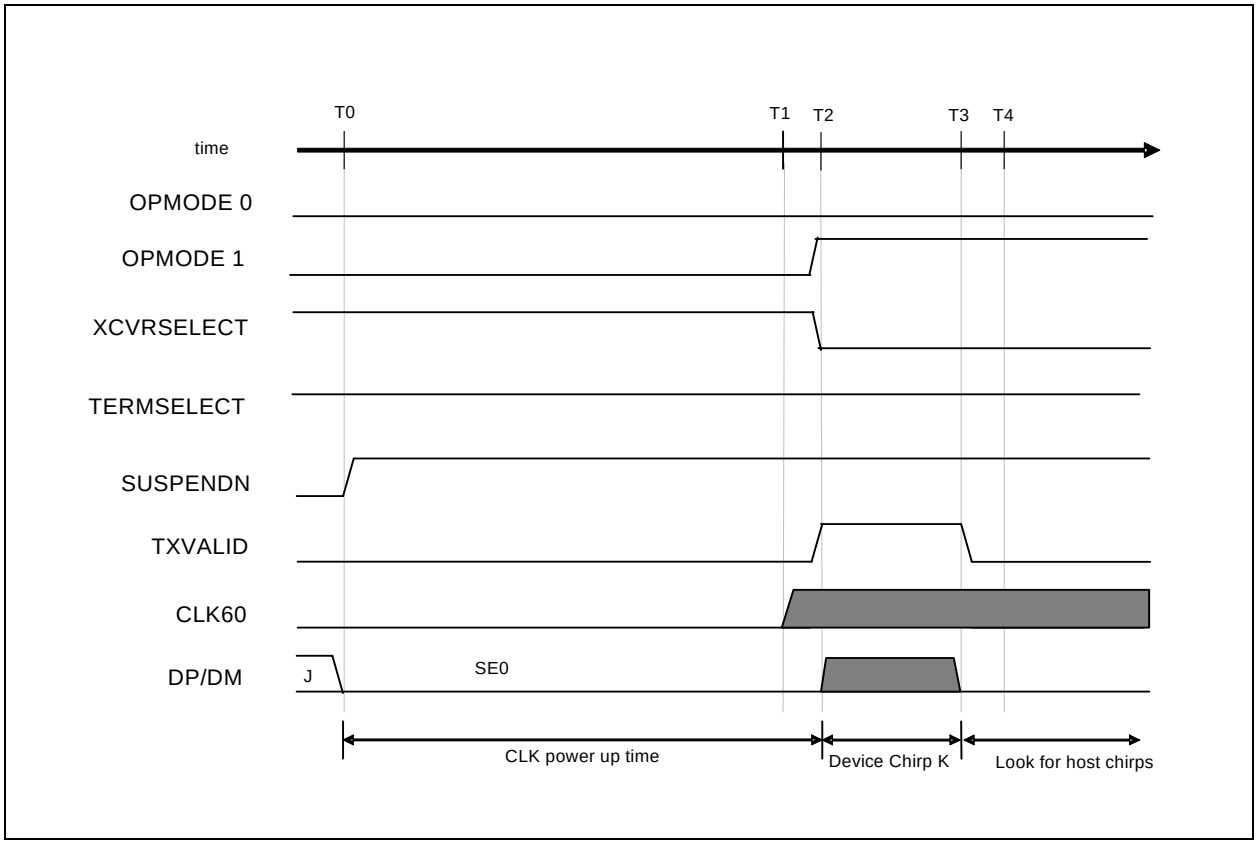


Figure 8.6 HS Detection Handshake Timing Behavior from Suspend

To detect the assertion of the downstream Chirp K's and Chirp J's for 2.5us {T_{FILT}}, the SIE must see the appropriate LINESTATE signals asserted continuously for 165 CLKOUT cycles.

Table 8.8 HS Detection Handshake Timing Values from Suspend

TIMING PARAMETER	DESCRIPTION	VALUE
T0	While in suspend state an SE0 is detected on the USB. HS Handshake begins. D+ pull-up enabled, HS terminations disabled, SUSPENDN negated.	0 (HS Reset T0)
T1	First transition of CLKOUT. CLKOUT "Usable" (frequency accurate to ±10%, duty cycle accurate to 50±5).	T0 < T1 < T0 + 5.6ms
T2	Device asserts Chirp K on the bus.	T1 < T2 < T0 + 5.8ms
T3	Device removes Chirp K from the bus. (1 ms minimum width) and begins looking for host chirps.	T2 + 1.0 ms < T3 < T0 + 7.0 ms
T4	CLK "Nominal" (CLKOUT is frequency accurate to ±500 ppm, duty cycle accurate to 50±5).	T1 < T3 < T0 + 20.0ms

8.11 Assertion of Resume

In this case, an event internal to the device initiates the resume process. A device with remote wake-up capability must wait for at least 5ms after the bus is in the idle state before sending the remote wake-up resume signaling. This allows the hubs to get into their suspend state and prepare for propagating resume signaling.

The device has 10ms where it can draw a non-suspend current before it must drive resume signaling. At the beginning of this period the SIE may negate SUSPENDN, allowing the transceiver (and its oscillator) to power up and stabilize.

Figure 8.7 illustrates the behavior of a device returning to HS mode after being suspended. At T4, a device that was previously in FS mode would maintain TERMSELECT and XCVRSELECT high.

To generate resume signaling (FS 'K') the device is placed in the "Disable Bit Stuffing and NRZI encoding" Operational Mode (OPMODE [1:0] = 10), TERMSELECT and XCVRSELECT must be in FS mode, TXVALID asserted, and all 0's data is presented on the DATA bus for at least 1ms (T1 - T2).

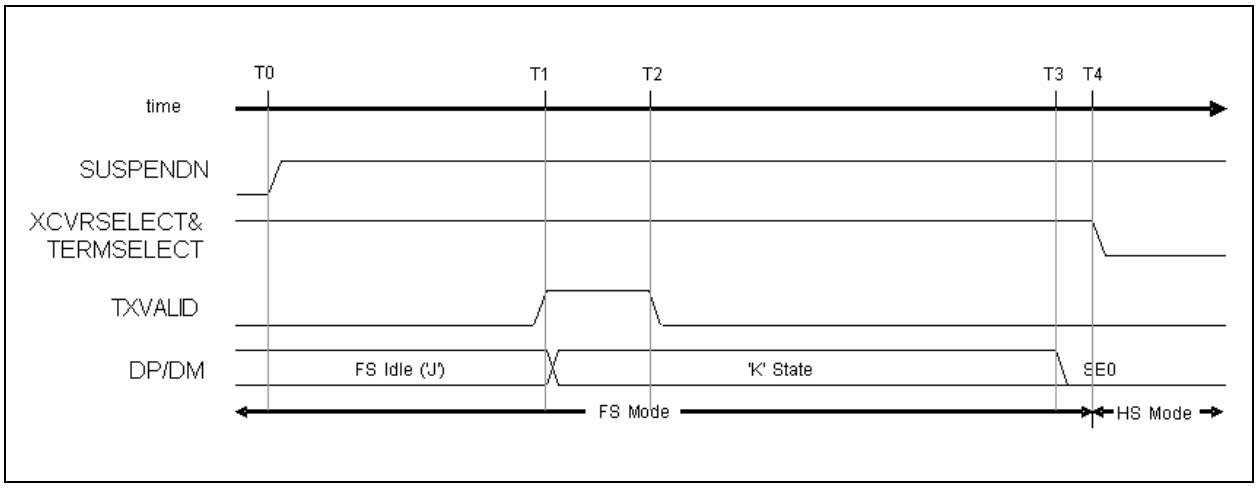


Figure 8.7 Resume Timing Behavior (HS Mode)

Table 8.9 Resume Timing Values (HS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
T0	Internal device event initiating the resume process	0 (reference)
T1	Device asserts FS 'K' on the bus to signal resume request to downstream port	T0 < T1 < T0 + 10ms.
T2	The device releases FS 'K' on the bus. However by this time the 'K' state is held by downstream port.	T1 + 1.0ms < T2 < T1 + 15ms
T3	Downstream port asserts SE0.	T1 + 20ms
T4	Latest time at which a device, which was previously in HS mode, must restore HS mode after bus activity stops.	T3 + 1.33µs {2 Low-speed bit times}

8.12 Detection of Resume

Resume signaling always takes place in FS mode (TERMSELECT and XCVRSELECT = FS enabled), so the behavior for a HS device is identical to that of a FS device. The SIE uses the LINESTATE signals to determine when the USB transitions from the 'J' to the 'K' state and finally to the terminating FS EOP (SE0 for 1.25us-1.5µs.).

The resume signaling (FS 'K') will be asserted for at least 20ms. At the beginning of this period the SIE may negate SUSPENDN, allowing the transceiver (and its oscillator) to power up and stabilize.

The FS EOP condition is relatively short. SIEs that simply look for an SE0 condition to exit suspend mode do not necessarily give the transceiver's clock generator enough time to stabilize. It is recommended that all SIE implementations key off the 'J' to 'K' transition for exiting suspend mode (SUSPENDN = 1). And within 1.25µs after the transition to the SE0 state (low-speed EOP) the SIE must enable normal operation, i.e. enter HS or FS mode depending on the mode the device was in when it was suspended.

If the device was in FS mode: then the SIE leaves the FS terminations enabled. After the SE0 expires, the downstream port will assert a J state for one low-speed bit time, and the bus will enter a FS Idle state (maintained by the FS terminations).

If the device was in HS mode: then the SIE must switch to the FS terminations before the SE0 expires (< 1.25µs). After the SE0 expires, the bus will then enter a HS IDLE state (maintained by the HS terminations).

8.13 HS Device Attach

Figure 8.8 demonstrates the timing of the USB3290 control signals during a device attach event. When a HS device is attached to an upstream port, power is asserted to the device and the device sets XCVRSELECT and TERMSELECT to FS mode (time T1).

V_{BUS} is the +5V power available on the USB cable. Device Reset in Figure 8.8 indicates that V_{BUS} is within normal operational range as defined in the USB 2.0 specification. The assertion of Device Reset (T0) by the upstream port will initialize the device. By monitoring LINESTATE, the SIE state machine knows to set the XCVRSELECT and TERMSELECT signals to FS mode (T1).

The standard FS technique of using a pull-up resistor on DP to signal the attach of a FS device is employed. The SIE must then check the LINESTATE signals for SE0. If LINESTATE = SE0 is asserted at time T2 then the upstream port is forcing the reset state to the device (i.e. Driven SE0). The device will then reset itself before initiating the HS Detection Handshake protocol.

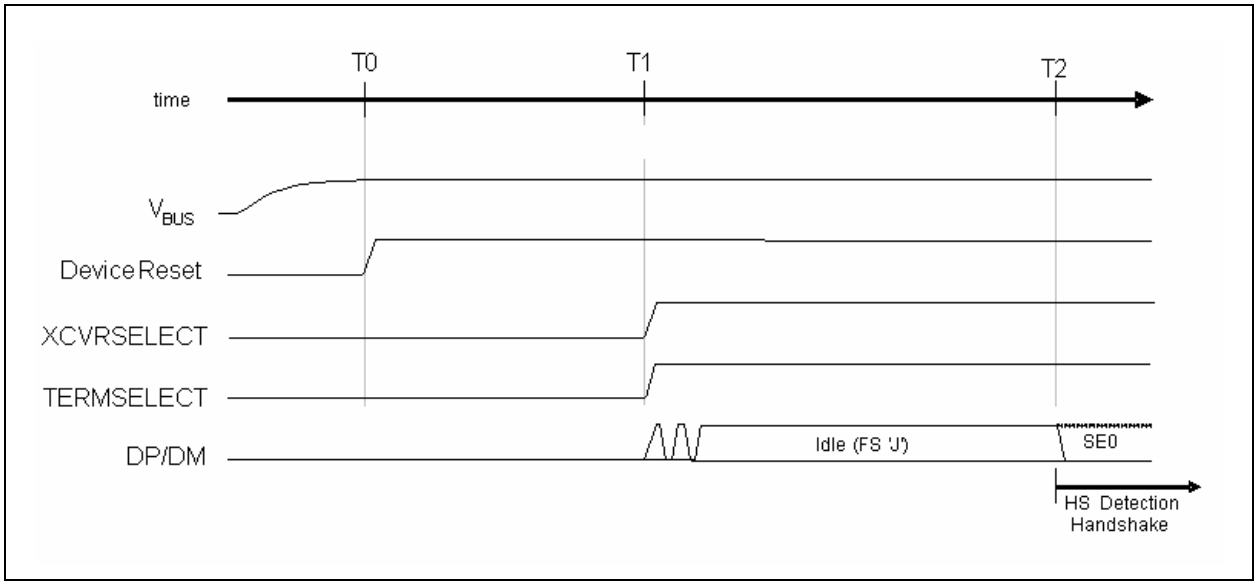


Figure 8.8 Device Attach Behavior

Table 8.10 Attach and Reset Timing Values

TIMING PARAMETER	DESCRIPTION	VALUE
T0	Vbus Valid.	0 (reference)
T1	Maximum time from Vbus valid to when the device must signal attach.	T0 + 100ms < T1
T2 (HS Reset T0)	Debounce interval. The device now enters the HS Detection Handshake protocol.	T1 + 100ms < T2

8.14 Application Diagram

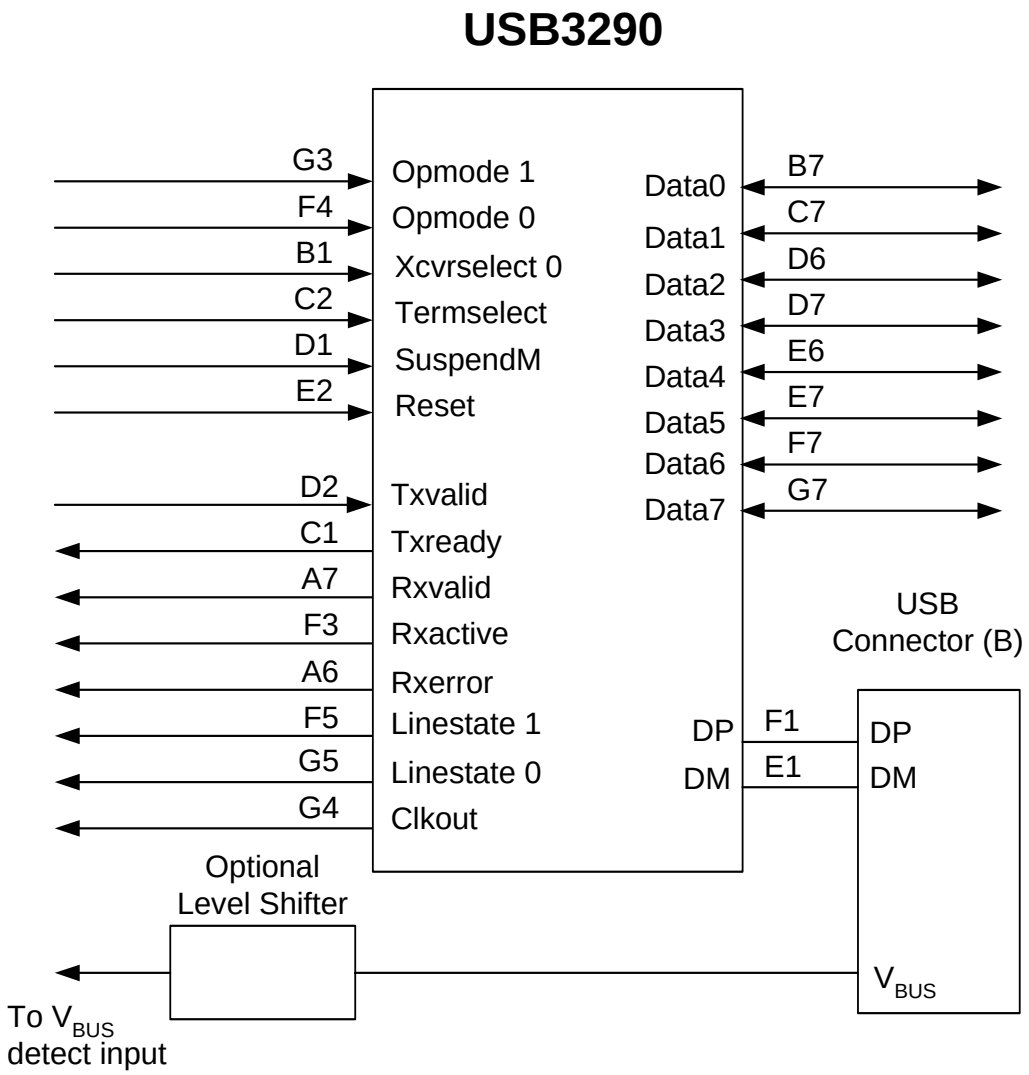


Figure 8.9 USB3290 Application Diagram showing USB related signals

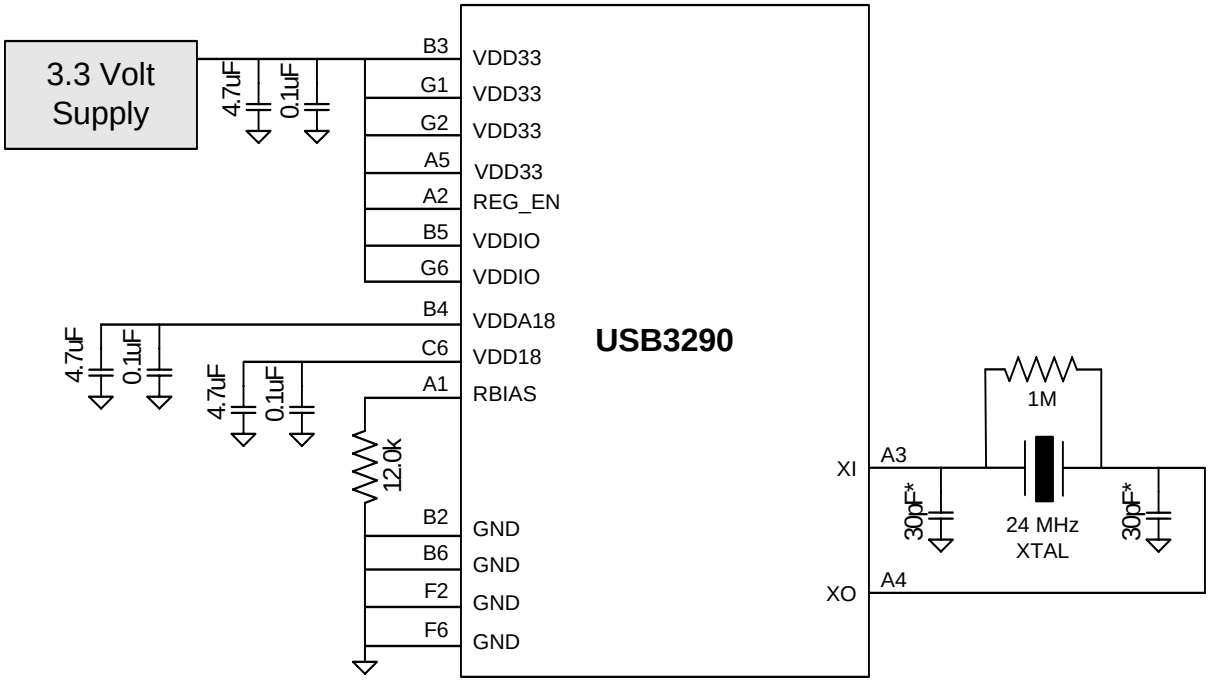
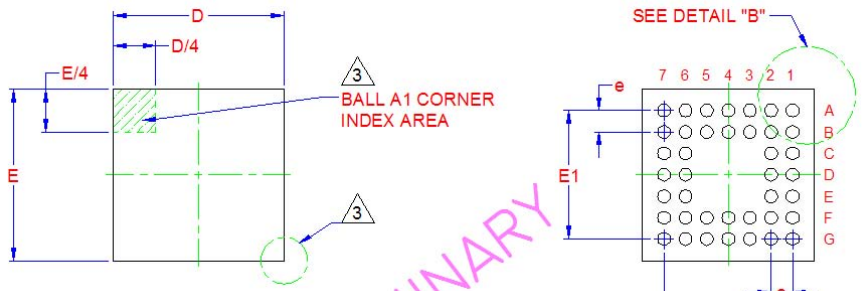
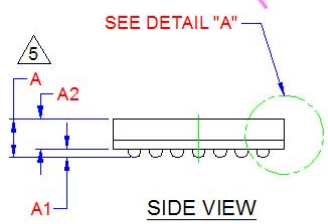
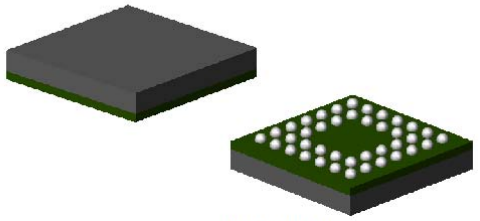


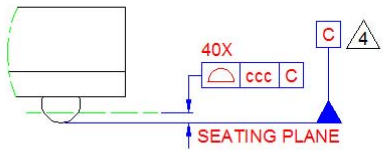
Figure 8.10 USB3290 Application Diagram showing power and miscellaneous signals

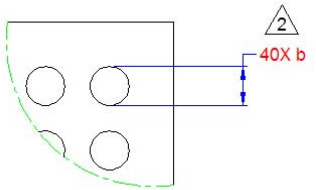
Chapter 9 Package Outline







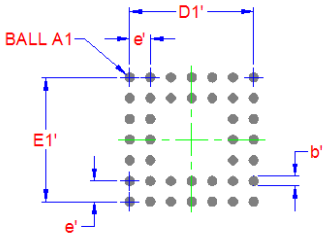




COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	-	-	1.00	5	OVERALL PACKAGE HEIGHT
A1	0.15	-	-	-	STANDOFF
A2	0.65	-	-	-	PKG BODY THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D1/E1	3.00 BSC			-	X/Y END BALLS DISTANCE
b	0.25	0.30	0.35	2	BALL DIAMETER
e	0.50 BSC			-	BALL PITCH
ccc	0	-	0.08	4	COPLANARITY

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAXIMUM RADIAL TRUE POSITION TOLERANCE OF EACH BALL IS ± 0.075mm AT MAXIMUM MATERIAL CONDITION. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM "C".
3. THE BALL "A1" CORNER MUST BE IDENTIFIED IN THE INDICATED AREA OF THE TOP PACKAGE SURFACE BY USING A CORNER CHAMFER, INK/LASER/METALIZED MARKING, INDENTATION, OR OTHER FEATURE OF PACKAGE BODY. EXACT SHAPE OF EACH CORNER IS OPTIONAL, BUT TERMINAL "A1" CORNER MUST BE UNIQUE.
4. PRIMARY DATUM "C" AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT SOLDER BALLS.
5. DIMENSION "A" DOES NOT INCLUDE ATTACHED EXTERNAL FEATURES, SUCH AS HEAT SINK OR CHIP CAPACITORS.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1'/E1'	-	3.00	-
b'	0.20	-	0.25
e'	-	0.50	-

THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

Figure 9.1 USB3290-FH 40 Ball, VFBGA Package Outline & Parameters 4x4x0.9mm Body, Lead-Free RoHS Compliant

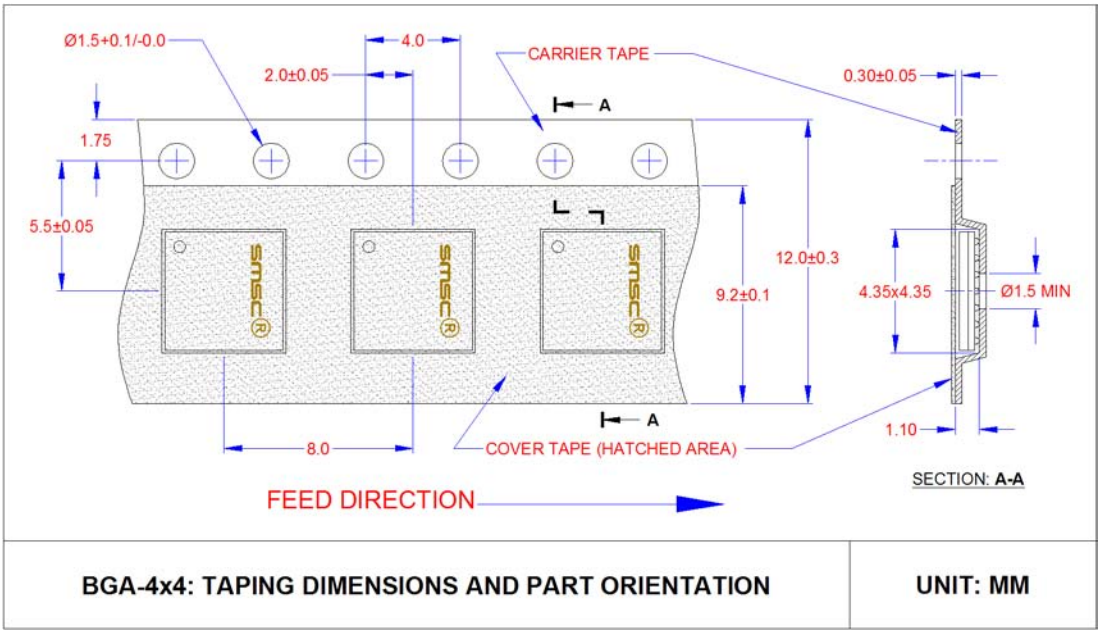
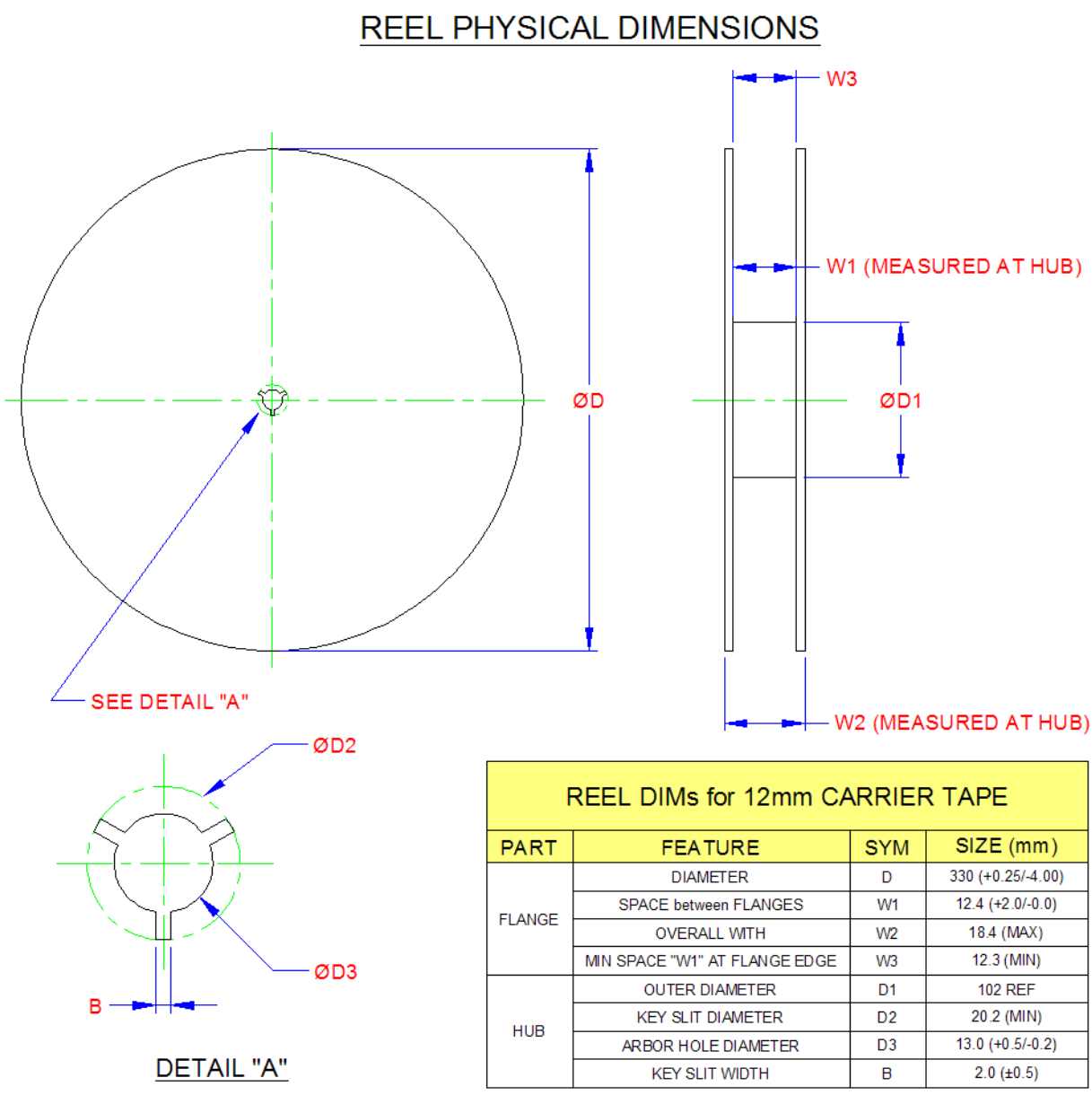
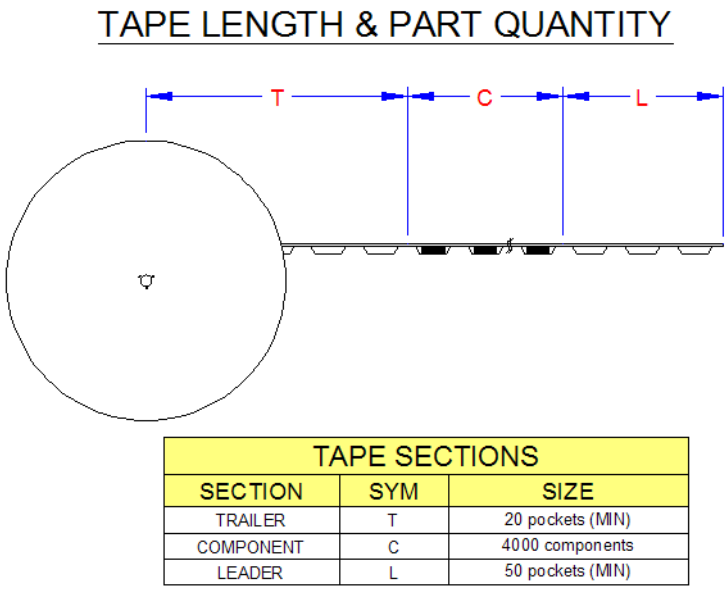


Figure 9.2 BGA, 4x4 Taping Dimensions and Part Orientation



REEL DIMs for 12mm CARRIER TAPE			
PART	FEATURE	SYM	SIZE (mm)
FLANGE	DIAMETER	D	330 (+0.25/-4.00)
	SPACE between FLANGES	W1	12.4 (+2.0/-0.0)
	OVERALL WITH	W2	18.4 (MAX)
	MIN SPACE "W1" AT FLANGE EDGE	W3	12.3 (MIN)
HUB	OUTER DIAMETER	D1	102 REF
	KEY SLIT DIAMETER	D2	20.2 (MIN)
	ARBOR HOLE DIAMETER	D3	13.0 (+0.5/-0.2)
	KEY SLIT WIDTH	B	2.0 (±0.5)

Figure 9.3 Reel Dimensions for 12mm Carrier Tape



TAPE SECTIONS		
SECTION	SYM	SIZE
TRAILER	T	20 pockets (MIN)
COMPONENT	C	4000 components
LEADER	L	50 pockets (MIN)

Figure 9.4 Tape Length and Part Quantity

Note: Standard reel size is 4000 pieces per reel.

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