

Multifunction LCD Segment Driver

BU97931FV MAX 112 segments (SEG28×COM4)

Features

- Integrated RAM for display data (DDRAM): 28 x 4 bit (Max 112 Segment)
- LCD drive output:
- 4 Common output, Max 28 Segment output
- Integrated 1ch LED driver circuit
- Segment/GPO (Max 5port) output mode selectable Support PWM generation from ext. or internal clock
- (Resolution: 8bit)
- Support standby mode
- Integrated Power-on-Reset circuit (POR)
- Integrated Oscillator circuit
- No external component
- Low power consumption design
- Independent power supply for LCD driving
- Support Blink function (Blink frequency 1.6, 2.0, 2.6, 4.0Hz selectable)

Applications

- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment

etc.

Typical Application Circuit

LED/GPO using case

Key Specifications

- Supply Voltage Range: +1.8V to +3.6V LCD drive power supply Range: +2.7V to +5.5V **Operating Temperature Range:** -40°C to +85°C Max Segments: 112 Segments Display Duty: Static, 1/3, 1/4 selectable Bias: Static. 1/3
 - Interface:

3wire serial interface

Package

W (Typ.) x D (Typ.) x H (Max.)



13.60mm x 7.80mm x 2.00mm





OProduct structure : Silicon monolithic integrated circuit OThis product is not designed for protection against radioactive rays.

Block Diagram / Pin Configuration / Pin Description





Figure 2. Block Diagram

Figure 3. Pin Configuration (TOP VIEW)

Terminal	Terminal number	I/O	Unused case	Function
CSB	26	Ι	-	Chip select: "L" active
SCL	27	I	-	Serial data transfer clock
SD	28	Ι	-	Input serial data
VDD	29	-	-	Power supply for LOGIC
CLKIN	30	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable); Support Hi-Z input mode at internal clock mode
VSS	25	-	-	GND
VLCD	31	-	-	Power supply for LCD
COM0 to 3	32 to 35	0	OPEN	COMMON output for LCD
SEG0 to 22	36 to 40 1 to 18	0	OPEN	SEGMENT output for LCD
SEG23 to 27	19 to 23	0	OPEN	SEGMENT output for LCD/GPO
LED	24	0	OPEN	LED driver output

Table 1 Pin Description

Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remarks
Power supply voltage 1	VDD	-0.3 to +4.5	V	Power supply
Power supply voltage 2	VLCD	-0.5 to +7.0	V	Power supply for LCD
Power Dissipation	Pd	0.8* ¹	W	
Input voltage range	VIN	-0.5 to VDD+0.5	V	
Operational temperature range	Topr	-40 to +85	°C	
Storage temperature range	Tstg	-55 to +125	°C	
	lout1	5	mA	SEG output
Output ourropt	lout2	5	mA	COM output
	lout3	10	mA	GPO output
	lout4	50	mA	LED output

*1 When operated more than Ta=25[°]C, subtract 8.0mW per degree. (using ROHM standard board) (board size:74.2mm×74.2mm×1.6mm material: FR4 board copper foil: land pattern only).

Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)

Paramotor	Symbol		Ratings		Llnit	Pomarka		
Faranielei	Symbol	MIN	TYP	MAX	Unit	Nemains		
Power supply voltage 1	VDD	1.8	-	3.6	V	Power supply		
Power supply voltage 2	VLCD	2.7	-	5.5	V	Power supply for LCD		
Output current	lout4	-	-	20	mA	Per LED port 1ch		

Electrical Characteristics

DC characteristics (Ta= -40°C to +85°C, VDD=1.8V to 3.6V, VLCD=3.3V to 5.5V, VSS=0)

Deremeter	Sympol	Limits				Conditions		
Falameter	Symbol	MIN	TYP	MAX	Unit	Conditions		
"H" level input voltage	VIH	0.8VDD	-	VDD	V	SD, SCL, CSB, CLKIN		
"L" level input voltage	VIL	VSS	-	0.2VDD	V	SD, SCL, CSB, CLKIN		
Hysteresis width	VH	-	0.2	-	V	SCL, VDD=3.3V, Ta=25°C		
"H" level input current	IIH1	-	-	5	μA	SD, SCL, CSB, CLKIN, VI=3.6V		
"L" level input current	IIL1	-5	-	-	μA	SD, SCL, CSB, CLKIN, VI=0V		
	VOH1	VLCD -0.4	-	-	V	lload=-50μA, VLCD=5.0V SEG0 to SEG27		
"H" level output voltage (*2)	VOH2	VLCD -0.4	-	-	V	Iload=-50µA, VLCD=5.0V, COM0 to COM3		
	VOH3	VLCD -0.6	-	-	V	Iload=-1mA,VLCD=5.0V, SEG23 to SEG27(GPO mode)		
	VOL1	-	-	0.4	V	lload= 50μA, VLCD=5.0V, SEG0 to SEG27		
"L" level output voltage	VOL2	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, COM0 to COM3		
(*2)	VOL3			0.5	V	Iload=1mA, VLCD=5.0V, SEG23 to SEG27(GPO mode)		
	VOL4	-	0.11	0.5	V	Iload=20mA, VLCD=5.0V,		

*1 Power save mode 1 and frame inversion setting

*2 Iload: In this case, load current from only one port

Electrical Characteristics – continued

DC characteristics (Ta= -40°C to +85°C, VDD=1.8V to 3.6V, VLCD=3.3V to 5.5V, VSS=0)

Deremeter	Symbol	Limits				Conditiona		
Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions		
	IstVDD	-	3	10	μA	Input terminal ALL'L', Display off, Oscillation off		
	IstVLCD	-	0.5	5	μA	Input terminal ALL'L', Display off, Oscillation off		
	IVDD1	-	8	15	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM generate off, All output pin open		
Current consumption (*1)	IVDD2	-	30	45	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open		
	IVLCD1	-	10	15	μA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, LED generate off, All output pin open		
	IVLCD2	-	30	48	μA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open		

*1 Power save mode 1 and frame inversion setting

*2 Iload: In case, load current from only one port

Oscillation Frequency Characteristics (Ta= -40°C to +85°C, VDD=1.8V to 3.6V, VLCD=2.7V to 5.5V, VSS=0)

Baramatar	Symbol		Limits		Llnit	Conditions			
Faidilielei	Symbol	MIN	MIN	MIN	Unit	Conditions			
Frame frequency 1	fFR1	57.6	64	70.4	Hz	VDD=3.3V, Ta=25°C, fFR=64Hz setting			
Frame frequency 2	fFR2	51.2	64	73.0	Hz	VDD=2.5V to 3.6V fFR=64Hz setting			
Frame frequency 3	fFR3	45.0	-	64	Hz	VDD=1.8V to 2.5V fFR=64Hz setting			

About detail function, please refer to the frame frequency setting of DISCTL command.

MPU interface Characteristics (Ta= -40°C to +85°C, VDD=1.8V to 3.6V, VLCD=2.7V to 5.5V, VSS=0)

Deremeter	Symbol		Limits		unit	Conditions	
Parameter	MIN TYP MAX		Conditions				
Input rise time	tr	-	-	50	ns		
Input fall time	tf	-	-	50	ns		
SCL cycle time	tSCYC	250	-	-	ns		
"H" SCL pulse width	tSHW	50	-	-	ns		
"L" SCL pulse width	tSLW	50	-	-	ns		
SD setup time	tSDS	50	-	-	ns		
SD hold time	tSDH	50	-	-	ns		
CSB setup time	tCSS	50	-	-	ns		
CSB hold time	tCSH	50	-	-	ns		
"H" CSB pulse width	tCHW	50	-	-	ns		



Figure 4. Serial Interface Timing

●I/O equivalent circuit



Figure 5. I/O equivalent circuit

•Example of recommended circuit

1) LED/GPO using case



2) SEG output only case



Figure 6. BU97931FV E.g. of recommended circuit

Function description

OCommand and data transfer method

O3-SPI (3-wire serial interface)

This device is controlled by a 3-wire signal (CSB, SCL, and SD).

First, Interface counter is initialized with CSB="H".

Setting CSB="L" enables SD and SCL inputs.

The protocol of 3-SPI transfer is as follows.

Each command starts with Command or Data judgment bit (D/C) as MSB data, followed by data D6 to D0 (this is when CSB ="L").

(Internal data is latched at the rising edge of SCL then it is converted to an 8-bit parallel data at the falling edge of the 8th CLK.)

When CSB changes from "L" to "H", and at this time sending commands are less than 8 bits, command and data transfer are cancelled. To start sending command again, please set CSB="L" and send command continuously.

After sending RAMWR or BLKWR or GPOSET command, this device is in the RAM data input mode. Under this mode, device can not accept new commands.

In this case, please execute a "H" to "L" transition at CSB, after this sequence the device is released from RAM data input mode, and can accept new command.



Figure 7. 3-SPI Data transfer Format

* 8-bit data, sending after RAMWR command, are display RAM data

* 8-bit data, sending after BLKWR command, are blink RAM data

* SCL and SD can be set to "H" or cleared to "L" during CSB="H"

OWrite display data and transfer method

This device has Display Data RAM (DDRAM) of 28×4=112bit. The relationship between data input and display data, DDRAM data and address are as follows.

1st Byte Command	2nd Byte Command	Command																	
10000011	00000000	10100000	a	b	с	d	е	f	g	h	i	j	k	I	m	n	0	р	
Addr	ess set	RAM Write		→[) Disp	lay	RA	M d	ata	I		1	I						

According to this command, an 8-bit binary data will be written to DDRAM. The starting address of the DDRAM where data will be written is specified by "ADSET" command, and is automatically incremented after every 4 bits of data received.

Writing data to DDRAM can be done by continuously sending data. (In case data is sent continuously after write date at 1Bh (SEG27), address return to address 00h (SEG0) automatically.)

In case SEG port assigned to GPO port by OUTSET command, corresponding SEG address do not change and is used as a dummy address.



Display data write to DDRAM every 4bits. In case CSB changes from "L" to "H" before 4 bits of data transfer was finished, RAM write is cancelled.



Figure 8. Display Data Transfer Method

OBlink function

This device has Blink function. Blink function can set each segment port individually. Blink ON/OFF and Blink frequency are set by the BLKSET command. Blink frequency varies according to fCLK characteristics. Blink setup of each segment is controlled by BLKWR command.

The write start address is specified by "BLKADSET" command. And this address will automatically increment after receiving every 4 bits of blink data. The relation of BLKWR command, blink ram data, and blinking segment port is below.

In case data is "1", segment will blink, on the other hand when data is "0", segment will not blink. (In case data is written continuously after write data at 1Bh (SEG27), address will return to 00h (SEG0) automatically.)

Please refer to the following figures about Blink operation of each segment.

In case SEG port assigned to GPO port by OUTSET command, corresponding SEG address does not change and is used as a dummy address.



Figure 9. Blink Operation

OLCD Driver Bias/Duty Circuit

BU97931FV generates LCD driving voltage using an on-chip Buffer AMP.

Also, it can drive LCD with low power consumption

*Line and frame inversion can be set in MODESET command.

*1/4duty, 1/3duty and static mode can be set DISCTL command.

About each LCD driving waveform, please refer to "LCD driving waveform" descriptions.

OInitial state

Initial state after SWRST command input

Display off

oAll command register values are in Reset state.

oDDRAM address data and Blink address data are initialized

(If DDRAM data and Blink RAM data are not initialized, write DDRAM data and Blink RAM data before Display on.)

Command / Function list

Function description table

NO	Command	Function
1	Mode Set (MODESET)	Sets LCD drive mode (display on/off, current mode)
2	Display control (DISCTL)	Sets LCD drive mode (frame freq., line/frame inversion)
3	Address set (ADSET)	Sets display data RAM address for RAMWR command
4	Blink set (BLKSET)	Sets Blink mode on/off
5	Blink address set (BLKADSET)	Sets Blink data RAM address for BLKWR command
6	SEG/GPO port change (OUTSET)	Selects segment output/general purpose output (GPO)
7	LED drive control (PWMSET) (H piece adjustment of PWM)	Sets PWM1 signal "H" width for LED driving
8	RAM WRITE (RAMWR)	Writes display data to display data RAM
9	Blink RAM WRITE (BLKWR)	Writes Blink data to BLINK data RAM
10	All Pixel ON (APON)	Sets all Pixel display on
11	All Pixel OFF (APOFF)	Sets all Pixel display off
12	All Pixel On/Off mode off (NORON)	Sets normal display mode (APON/APOFF cancel)
13	Software Reset (SWRST)	Software Reset
14	OSC external input (OSCSET)	Enables External clock input
15	GPO output set (GPOSET)	Sets GPO output data

Detailed Command Descriptions

D/C, Data / Command judgment bit (MSB) For details, please refer to 3-wire serial I/F

OMode Set (MODESET)

	MSB		LSB							
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte command	1	0	0	0	0	0	0	1	81h	-
2nd byte command	0	0	0	0	P3	P2	P1	P0	-	00h

Display Set

Condition	P3	Reset state
Display OFF	0	0
Display ON	1	

Display OFF: No LCD driving mode (Output: VSS Level)

Turn off OSC circuit and LCD power supply circuit. (Synchronized with frame freq) Display ON: LCD driving mode

Turn on OSC circuit and LCD power supply circuit. Read data from DDRAM and display to LCD.

LED port and GPO port output states are not influenced by a Display on/off state Output state is decided by command setup (OUTSET, GPOSET, PWMSET). For more details, please refer to each command description.

LCD drive mode set

Condition	P2	Reset state
Frame inversion	0	0
Line inversion	1	

Current mode set

Condition	P1	P0	Reset state
Power save mode1	0	0	0
Power save mode2	0	1	
Normal mode	1	0	
High power mode	1	1	

(Reference data of consumption current)

Condition	Current consumption
Power save mode 1	×1.0
Power save mode 2	×1.7
Normal mode	×2.7
High power mode	×5.0

* The value changes according to the panel load.

ODisplay control (DISCTL)

MSB					LSB					
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte Command	1	0	0	0	0	0	1	0	82h	-
2nd byte Command	0	0	0	0	P3	P2	P1	P0	-	02h

Duty set

Condition	P3	P2	Reset state
1/4duty (1/3bias)	0	0	0
1/3duty (1/3bias)	0	1	
Static (1/1bias)	1	*	

*: Don't care

In 1/3duty, Display data and Blink data of COM3 are ineffective. COM1 and COM3 output are same data.

Please be careful in transmitting display data and blink data. The examples of SEG/COM output waveform, under each Bias/Duty set up, are shown at "LCD Driver Bias/Duty Circuit" description.

Frame frequency set

Condition (1/4,1/3,1/1duty)	P1	P0	Reset state
(128Hz, 130Hz, 128Hz)	0	0	
(85Hz, 86hz, 64Hz)	0	1	
(64Hz, 65Hz, 48Hz)	1	0	0
(51Hz, 52Hz, 32Hz)	1	1	

Relation table, between Frame freque	encies (FR), integrated oscillator	circuit (OSC) and Divide number.
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		Divide		FR [Hz] (* 1)				
DISCTL	Di	uty set (P3,P	2)	Dı	uty set (P3,P2	2)		
(P1,P0)	(0,0) 1/4duty	(0,1) 1/3duty	(1, *) 1/1duty	(0,0) 1/4duty	(0,1) 1/3duty	(1, *) 1/1duty		
(0,0)	160	156	160	128	131.3	128		
(0,1)	240	237	320	85.3	86.4	64		
(1,0)	320	315	428	64	65	47.9		
(1,1)	400	393	640	51.2	52.1	32		

*1: FR is frame frequency, in case OSC frequency = 20.48KHz (typ).

The Formula, to calculate OSC frequency from Frame frequency is shown below.

" OSC frequency = Frame frequency (measurement value) x Divide number " Divide number: Determined by using the value of Frame Frequency Set (P1,P0) and duty setting (P3,P2).

Ex) (P1,P0) = (0,1) ,(P3,P2) = (0,1) => Divide number= 237

OAddress set (ADSET)

	MSB							LSB		
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte Command	1	0	0	0	0	0	1	1	83h	-
2nd byte Command	0	0	0	P4	P3	P2	P1	P0	-	00h

Sets start address to write DDRAM data.

The address can be set from 00h to 1Bh.

Do not set other address. (Except 00h to 1Bh address is not acceptable.)

In case writing data to DDRAM, make sure to send RAMWR command.

OBlink set (BLKSET)

MSB						LSB				
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1 st byte Command	1	0	0	0	0	1	0	0	84h	-
2 nd byte Command	0	0	0	0	0	P2	P1	P0	-	00h

Set Blink ON/OFF.

For more details, please refer to "Blink function".

Blink set

Blink mode(Hz)	P2	P1	P0	Reset state
OFF	0	0 / *	0 / *	0
1.6	1	0	0	
2.0	1	0	1	
2.6	1	1	0	
4.0	1	1	1	
*· Don't care		•		

*: Don't care

OBlink address set (BLKADSET)

/ISB	3
/	1SE

LSB

	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte Command	1	0	0	0	0	1	1	1	87h	-
2nd byte Command	0	0	0	P4	P3	P2	P1	P0	-	00h

Sets RAM start address to write Blink data.

The address can be set from 00h to 1Bh.

Do not set other addresses. (Except 00h to 1Bh address is not acceptable)

In case writing data to Blink RAM, make sure to send BLKWR command.

OSEG/GPO port change (OUTSET)

	LSB									
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte Command	1	0	0	0	1	0	0	0	88h	-
2nd byte Command	0	0	0	0	0	P2	P1	P0	-	00h

Set output mode, Segment output or GPO output.

P2 to P0: Select changing port number. (SEG23 to SEG27 ports are SEG mode/GPO mode selectable)

In case GPO output is selected, terminal output data is set by GPOSET command.

Ex) In case SEG 26 port is assigned to GPO,

If GPO1 data is "H", GPO1 (SEG26) port outputs "H" (VLCD Level). If GPO1 data is "L", GPO1 (SEG26) port outputs "L" (VSS level).

Output terminal state under the P2 to P0 set condition is listed below.

Output Terminal state Condition SEG Terminal state (SEG output/GPO output) P2 P1 P0 SEG23 port SEG24 port SEG25 port SEG26 port SEG27 port 0 0 0 SEG23 SEG24 SEG25 SEG26 SEG27 0 0 SEG23 SEG24 SEG25 SEG26 GPO0 1 0 1 0 SEG23 SEG24 SEG25 GPO1 GPO0 0 SEG24 GPO2 GPO1 GPO0 1 1 SEG23 1 0 0 SEG23 GPO3 GPO2 GPO1 GPO0 1 0 1 GPO4 GPO3 GPO2 GPO1 GPO0 1 (OUTSET command will be canceled) 1

In case the SEG port is switched to the GPO port, DDRAM address and Blink RAM address do not change. In case DDRAM address and Blink RAM address, selected GPO output mode is dummy address.

	MSB				LSB						
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset	
1st byte Command	1	0	0	0	1	0	1	0	8Ah	-	
2nd byte Command	0	0	0	0	0	0	P7	P6	-	00h	
3rd byte Command	0	0	P5	P4	P3	P2	P1	P0	-	00h	

OLED drive-control (PWM "H" width control) command (PWMSET)

2nd and 3rd byte command data can be set from 00h to 3Fh (described as 8-bit binary data).

In case other value is selected, sending command is ignored and 2nd and 3rd byte command data are set to 3Fh. In reset state, 2nd and 3rd byte command data are set to 00h.

In case the command is less than 3 byte, sending command is cancelled.

According to PWMSET command, LED driving signal is adjustable. PWM "H" width is adjustable by 8-bit resolution.

Explanation about P7 to P6 data of 2nd byte command and P5 to P0 data of 3rd byte command are as follows: (The 2nd byte data are used as upper 2bit, and 3rd byte data are used as lower 6 bits.)

8bit mode : P7 data is used as MSB of 8 bits, and P0 data is used LSB.

LED driving period is determined by the "H" width of PWM signal, generated by PWM generator circuit (resolution : 8bit).

Ex)

In case external PWM clock is 125KHz, parameter setting value is 127 (7Fh) 1-bit resolution : 8us ALL HI set : PWM signal frequency about 500Hz, H width about 2.00msec ALL LOW set : PWM signal frequency about 500Hz, H width 0usec (in case 8bit resolution)

This command is reflected, synchronizing with a next PWM frame head. And, LED port output is as follows. LED port operation does not affect Display ON/OFF state.



(*)PWM frequency and PWM "H" width calculation.

PWM cycle and PWM "H" width, decided by PWM clock cycle are described as follows. (PWM clock cycle is a minimum unit of PWM "H" width)

PWM frequency = PWM clock cycle × (Number of the steps (8bit =256) - 1) PWM H width = PWM clock cycle × Parameter set value (8bit: 0 to 255) PWM Duty = PWM H width/PWM cycle = Parameter set value / Number of the steps

In case PWM is generated from the internal clock, the PWM cycle varies depending on the OSC frequency.

In case LED is used as back light of LCD panel and PWM is generated from internal clock, there is a possibility that the display will flicker. For such cases, please use under the PWM width ALL "L" or ALL "H" setting only.

ORAM WRITE (RAMWR)

	MSB				LSB						
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset	
1st byte Command	1	0	1	0	0	0	0	0	A0h	-	
2nd byte Command				Displa	iy data					Random	
				• •	•••						
n byte Command				Displa	ıy data					Random	

Input data, sending after 1st byte command, are used as Display data. And display data are sent every 4 bits. Please set this command after the ADSET command.

OBlink RAM WRITE (BLKWR)

	MSB				LSB						
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset	
1st byte Command	1	1	0	0	0	0	0	0	C0h	-	
2nd byte Command				Blink	data					Random	
n byte Command				Random							

Input data, sending after 1st byte command, are used as Display data. And display data are sent every 4 bits. Please set this command after the BLKADSET command.

OAll Pixel ON (APON)

	MSB					LSB					
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset	
1st byte Command	1	0	0	1	0	0	0	1	91h	-	

After sending the command, all SEG outputs set display on state regardless of the DDRAM data. (This command affect to the SEG output terminal only (except GPO and LED output))

OAll Pixel OFF (APOFF)

	LSB									
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte Command	1	0	0	1	0	0	0	0	90h	-

After sending the command, all SEG outputs set display off state regardless of the DDRAM data. (This command affects the SEG output terminals only (except GPO and LED outputs))

OAll Pixel ON/OFF mode off (NORON)

	LSB									
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte Command	1	0	0	1	0	0	1	1	93h	-

After sending the command, all SEG outputs are released from APON/APOFF state. And SEG port outputs signal follows DDRAM data.

(This command affects the SEG output terminals only (except GPO and LED output))

After reset sequence or SWRESET, all outputs are set to NORON state.

OSoftware Reset (SWRST)

	MSB							LSB					
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset			
1st byte Command	1	0	0	1	0	0	1	0	92h	-			

After sending the command, device is set to the default state.

OOSC external input command (OSCSET)

	MSB				LSB						
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset	
1st byte Command	1	0	0	1	1	0	0	0	98h	-	
2nd byte Command	0	0	0	0	0	P2	P1	P0	-	00h	

Sets the type of clock mode. There are 4 selectable modes including external clock input mode. Details of this command function are as follows.

Condition	P2	P1	P0	Reset state
Internal CLK (PWM generation OFF)	0	0	0	0
External CLK input for PWM (PWM generation OFF)	0	0	1	
Internal CLK (PWM generation ON)	0	1	0	
External CLK input for PWM (PWM generation ON)	0	1	1	
External CLK input for Display (ROHM use only)	1	*	*	

(*: Don't care)

(P2,P1,P0)=(0,0,1): External PWM input mode

CLKIN: external PWM input available. PWMOUT: "L" Output

*under the (P2,P1,P0)=(0,0,0) condition PWMOUT into same state

(P2,P1,P0)=(0,1,0) : PWM is generated from an internal oscillating frequency

(P2,P1,P0)=(0,1,1) : PWM is generated from an External CLK input from CLKIN PWM width is set up by PWMSET and PWMSET command.

In case LED is used as back light of LCD panel and PWM is generated from internal clock, display flickering will occur. In this case, please use under the PWM width ALL "L" or ALL "H"setting only.

The relation of OSC function control by each command is as follows:



Figure 10. OSC External Input

OGPO output set command (GPOSET)

	MSB						LSB					
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset		
1st byte Command	1	0	0	1	1	0	1	0	9Ah	-		
2nd byte Command	0	0	0	P4	P3	P2	P1	P0	-	00h		

Set GPO output data. The relation between SEG port (GPO port) and data is shown below.

GPOSET data	GPO port	SEG port
P0	GPO0	SEG27
P1	GPO1	SEG26
P2	GPO2	SEG25
P3	GPO3	SEG24
P4	GPO4	SEG23

GPO data output is asynchronous from frame cycle. GPO output is not affectedby Display ON/OFF state.

LCD driving waveform



Figure 11. Waveform of Line Inversion

Figure 12. Waveform of Frame Inversion



Figure 13. Waveform of Line Inversion

Figure 14. Waveform of Frame Inversion

Datasheet







●initialize Sequence

Recommended input sequence is listed below, before starting LCD driving. (Refer to Power ON/OFF sequence)

* Before initializing sequence, DDRAM address, DDRAM data, Blink address and Blink data are random.

Cautions on Power-On/ Power-Off condition

OPOR circuit

BU97931FV has "P.O.R" (Power-On Reset) circuit and Software Reset function. Please follow the recommended Power-On conditions in order to power up properly.

1, Please set power up conditions, follow the recommended tR, tF, tOFF, and Vbot specification below in order to ensure P.O.R operation.

(*The detection voltage of POR varies because of environment etc. To operate POR properly, please satisfy Vbot lower than 0.5V condition.)



Recommended condition of tR, tF, tOFF, Vbot

tR	tOFF	Vbot	VDET
less than	Over	less than	TYP
10ms	1ms	0.5V	1.2V

* VDET : POR detect level

Figure 17. Power ON/OFF Waveform

2, If it is difficult to meet the above conditions, execute the following sequence after Power-On.

(1) CSB="L" \rightarrow "H" condition

(2) After CSB"H"→"L", execute SWRST command

In addition, in order to the Software reset command certainly, please wait 1ms after a VDD level reaches to 90% and CSB="L" \rightarrow "H".

*Before SWRST command input device will be in unstable state, since SWRST command does not operate perfect substitution of a POR function.



Figure 18. SWRST Command Sequence

Power ON / OFF sequence





Attention about input port pull down

Satisfy the following sequence if input terminals are pulled down by external resistors (In case MPU output Hi-Z).

BU97931FUV adopts a 5V tolerant I/O for the digital input. This circuit includes a bus-hold function to keep HIGH level. A pull down resistor of below $10K\Omega$ shall be connected to the input terminals for transitions from HIGH to LOW because the bus-hold transistor turns on during the input's HIGH level. (Refer to the Figure 5; I/O Equivalent Circuit)

A higher resistor than $10K\Omega$ (approximate) causes input terminals being steady by intermediate potential between HIGH and LOW level so unexpected current is consumed by the system.

The potential depends on the pull down resistance and bus-hold transistor's resistance.

As the bus-hold transistor turns off upon the input level is cleared to LOW, a higher resistor can be used as a pull down resistor if MPU sets SD and SCL lines to LOW before it releases the lines.

The LOW period preceding MPU's bus release shall be at least 50ns as same as a minimum CLK width (tSLW).

Operational Notes

(1) Absolute maximum ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(2) Recommended operating conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(4) Power supply lines

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(5) Ground Voltage

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(6) Short between pins and mounting errors Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

- (7) Operation under strong electromagnetic field Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- (8) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage

(9) Regarding input pins of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the GND voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input terminals have voltages within the values specified in the electrical characteristics of this IC.

(10) Ground wiring pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(11) External Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

(12) Unused input terminals

Input terminals of an IC are often connected to the gate of a CMOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or ground line.

(13) Rush current

When power is first supplied to the IC, rush current may flow instantaneously. It is possible that the charge current to the parastic capacitance of internal photo diode or the internal logic may be unstable. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

Marking Diagram

Revision History

Date	Revision	Changes	
14.Mar.2012	001	New Release	
8.Jan.2013	002	Improved the statement in all pages. Deleted "Status of this document" in page 26. Changed format of Physical Dimension, Tape and Reel Information	
26.Jan.2015	003	Add the condition when power supply in page 24.	
10.Apr.2015	004	No modification. Updated the revision number only to match the Japanese version.	

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