

TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 12, 19, 21, 35, 49, 53, 56	V_{SS}	Ground
2, 13, 20, 32, 36, 39, 52, 68	V_{CC}	Positive Power Supply
3-11, 18, 22-31, 33, 34, 37, 38, 40, 41, 64-67	D4-D12, D15, D16-25, D26, D27, D28, D29, D30, D31, D0-D3	Data Bus
42	CKM	Clock Mode
43	386CLK2	386 CPU Clock 2
44	387CLK2	387 MCP Clock 2
45	RESETIN	System Reset
46	NC	Not Connected
47 59	Tie High	Tie High
48	$\overline{\text{READY}}$	Bus Ready Input
50	$\overline{\text{CMD0}}$	Command
51	$\overline{\text{ADS}}$	Address Strobe
54	NPS2	MCP Select #2
55	$\overline{\text{NPS1}}$	MCP Select #1
57	$\overline{\text{W/R}}$	Write/Read
58	STEN	Status Enable
60	$\overline{\text{READYO}}$	Ready Output
61	$\overline{\text{BUSY}}$	Busy Status
62	$\overline{\text{ERROR}}$	Error Status
63	PEREQ	Processor Extension Request

TABLE 2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage, any pin, with respect to Ground	V_{CC}	-0.5	$V_{CC}+0.5$	V
Power Dissipation	P_D	--	1.5	W
Storage Temperature Range	T_S	-65	150	°C
Operating Temperature Range	T_A	-55	125	°C
Lead Temperature (soldering 10 seconds)		--	260	°C

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{LI}	$\pm 1.5 \mu\text{A}$
I_{LO}	$\pm 1.5 \mu\text{A}$
I_{CC} CLK2 = 32 MHz	$\pm 25 \text{ mA}$
I_{CC} CLK2 = 50 MHz	$\pm 39 \text{ mA}$

TABLE 4. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	4.75	5.25	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input High Voltage	V_{IH}	2.0	$V_{CC} + 0.3$	V
Operating Temperature	T_A	-55	125	$^{\circ}\text{C}$

TABLE 5. 80387DX DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 4.75\text{V TO } 5.25\text{V}; T_A = -55 \text{ TO } +125^{\circ}\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Input Low Voltage	V_{IL}^1		--	0.8	V
Input High Voltage	V_{IH}^1		2.0	--	V
386 CLK2 Input Low Voltage	V_{CL}		--	0.8	V
386 CLK2 Input High Voltage	V_{CH}		3.7	--	V
Output Low Voltage	V_{OL}	$I_{OL} = 4 \text{ mA}, \text{D0-D31}, I_{OL} = 2.5 \text{ mA}$ READYO, ERROR, BUSY, PEREQ	--	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -1 \text{ mA}, \text{D0-D31}, I_{OH} = -0.6 \text{ mA}$ READYO, READYO, ERROR, BUSY, PEREQ	2.4	--	V
Input Leakage Current	I_{LI}	$0\text{V} \leq V_{IN} \leq V_{CC}$		± 15	μA
Output Leakage Current	I_{LO}	$0.45\text{V} \leq V_{OUT} \leq V_{CC}$	--	± 15	μA
Power Supply Current	I_{CC}	CLK2 = 32 MHz CLK2 = 40 MHz CLK2 = 50 MHz ²	--	250 310 390	mA
Input Capacitance ³	C_{IN}	$F_C = 1 \text{ MHz}$	--	10	pF
Output Capacitance ³	C_O	$F_C = 1 \text{ MHz}$	--	12	pF
CLK2 Capacitance ³	C_{CLK}	$F_C = 1 \text{ MHz}$	--	20	pF

1. This parameter is for all inputs, including 387CLK2 but excluding 386CLK2.
2. I_{CC} is measured at steady state, maximum capacitive loading on the outputs, and worst-case DC level at the inputs; 386CLK2 at the same frequency as 387CLK2.
3. Guaranteed By Design

TABLE 6. 80387DX COMBINATIONS OF BUS INTERFACE AND EXECUTION SPEEDS
($V_{CC} = 4.75V$ TO $5.25V$; $T_A = -55$ TO $+125^{\circ}C$, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Bus Interface Unit					MHz
-16			16	--	
-20			20	--	
-25			25	--	
Execution Unit					MHz
-16			16	--	
-20			20	--	
-25			25	--	

TABLE 7. 80387DX TIMING REQUIREMENTS OF THE EXECUTION UNIT
($V_{CC} = 4.75V$ TO $5.25V$; $T_A = -55$ TO $+125^{\circ}C$, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
387CLK2 Period ¹	t_1	At 2V			ns
-16			31	125	
-20			25	125	
-25			20	125	
387CLK2 High Time	t_{2a}	At 2V			ns
-16			9	--	
-20			8	--	
-25			7	--	
387CLK2 High Time ¹	t_{2b}	At 3.7V			ns
-16			5	--	
-20			5	--	
-25			4	--	
387CLK2 Low Time	t_{3a}	At 2V			ns
-16			9	--	
-20			8	--	
-25			7	--	
387CLK2 Low Time ¹	t_{3b}	At 0.8V			ns
-16			7	--	
-20			6	--	
-25			5	--	
387CLK2 Fall Time ¹	t_4	At 3.7V to 0.8V			ns
-16			--	8	
-20			--	8	
-25			--	7	
387CLK2 Rise Time ¹	t_5	At 0.8V to 3.7V			ns
-16			--	8	
-20			--	8	
-25			--	7	

1. Guaranteed By Design

TABLE 8. 80387DX TIMING REQUIREMENTS OF THE BUS INTERFACE UNIT (OUTPUT TRIP LEVEL = 1.5V)
 ($V_{CC} = 4.75V$ TO $5.25V$; $T_A = -55$ TO $+125^\circ C$, UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
386CLK2 Period ¹ -16 -20 -25	At 2.0V	t_1	31 25 20	125 125 125	ns
386CLK2 High Time -16 -20 -25	At 2.0V	t_{2a}	9 8 7	-- -- --	ns
386CLK2 High Time1 -16 -20 -25	At 3.7V	t_{2b}	5 5 4	-- -- --	ns
386CLK2 Low Time -16 -20 -25	At 2V	t_{3a}	9 8 7	-- -- --	ns
386CLK2 Low Time ¹ -16 -20 -25	At 0.8V	t_{3b}	7 6 5	-- -- --	ns
386CLK2 Fall Time ¹ -16 -20 -25	At 3.7V to 0.8V	t_4	-- -- --	8 8 7	ns
386CLK2 Rise Time ¹ -16 -20 -25	At 0.8V to 3.7V	t_5	-- -- --	8 8 7	ns
386 CLK2/387CLK2 Ratio		--	10/16	14/10	--
READYO Out Delay -16 -20 -25	$C_L = 50$ pF	t_7	4 3 3	34 31 24	ns
PEREQ, ERROR Out Delay -16 -20 -25	$C_L = 50$ pF	t_7	5 5 4	34 34 33	ns
BUSY Out Delay -16 -20 -25	$C_L = 50$ pF	t_7	5 5 4	34 29 29	ns

TABLE 8. 80387DX TIMING REQUIREMENTS OF THE BUS INTERFACE UNIT (OUTPUT TRIP LEVEL = 1.5V)
 ($V_{CC} = 4.75V$ TO $5.25V$; $T_A = -55$ TO $+125^\circ C$, UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
D31 - D0 Out Delay -16 -20 -25	$C_L = 50$ pF	t_8	1 1 0	54 54 50	ns
D31 - D0 Setup Time		t_{10}	11		ns
D31 - D0 Hold Delay		t_{11}	11		ns
D31 - D0 Float Time -16 -20 -25	$C_L = 50$ pF ²	t_{12}	6 6 5	33 27 24	ns
PEREQ, BUSY, ERROR, READYO Float Time ¹ -16 -20 -25	$C_L = 50$ pF ¹	t_{13}	1 1 1	60 50 40	ns
ADS, $\overline{W/R}$ Setup Time -16 -20 -25		t_{14}	26 21 16	-- -- --	ns
ADS, $\overline{W/R}$ Hold Time -16 -20 -25		t_{15}	5 5 4	-- -- --	ns
READY Setup Time -16 -20 -25		t_{16}	21 12 9	-- -- --	ns
READY Hold Time -16 -20 -25		t_{17}	4 4 4	-- -- --	ns
CMDO Setup Time -16 -20 -25		t_{16}	21 19 16	-- -- --	ns
CMDO Hold Time -16 -20 -25		t_{17}	2 4 4	-- -- --	ns
NPS1, NPS2 Setup Time -16 -20 -25		t_{16}	21 19 16	-- -- --	ns

TABLE 8. 80387DX TIMING REQUIREMENTS OF THE BUS INTERFACE UNIT (OUTPUT TRIP LEVEL = 1.5V)
($V_{CC} = 4.75V$ TO $5.25V$; $T_A = -55$ TO $+125^\circ C$, UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
NPS1, NPS2 Hold Time -16 -20 -25		t_{17}	2 2 4	-- -- --	ns
STEN Setup Time -16 -20 -25		t_{16}	21 21 15	-- -- --	ns
STEN Hold Time -16 -20 -25		t_{17}	2 2 4	-- -- --	ns
RESETIN Setup Time -16 -20 -25		t_{18}	13 12 10	-- -- --	ns
RESETIN Hold Time -16 -20 -25		t_{19}	4 4 3	-- -- --	ns

1. Guaranteed By Design

2. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float Delay is not tested.

TABLE 9. 80387DX TIMING REQUIREMENT OF OTHER PARAMETER

PARAMETER	SYMBOL	MIN	MAX	UNIT
RESETIN Duration	t_{30}	40		(387 CLK2)
RESETIN Inactive to First Opcode Write	t_{31}	50		(387 CLK2)
BUSY Duration	t_{32}	6		(386 CLK2)
ERROR Inactive to BUSY Inactive	t_{33}	6		(386 CLK2)
PEREQ Inactive to ERROR Active	t_{34}	6		(386 CLK2)
READY Active to Busy Active	t_{35}	4	4	(386 CLK2)
READY Minimum Time from Opcode Write to Opcode to Opcode/ Operand Write	t_{36}	6		(386 CLK2)
READY Minimum Time from Operand Write to Operand Write	t_{37}	8		(386 CLK2)

FIGURE 1. TIMING DIAGRAMS - FAST TRANSITIONS TO AND FROM PIPELINED CYCLES

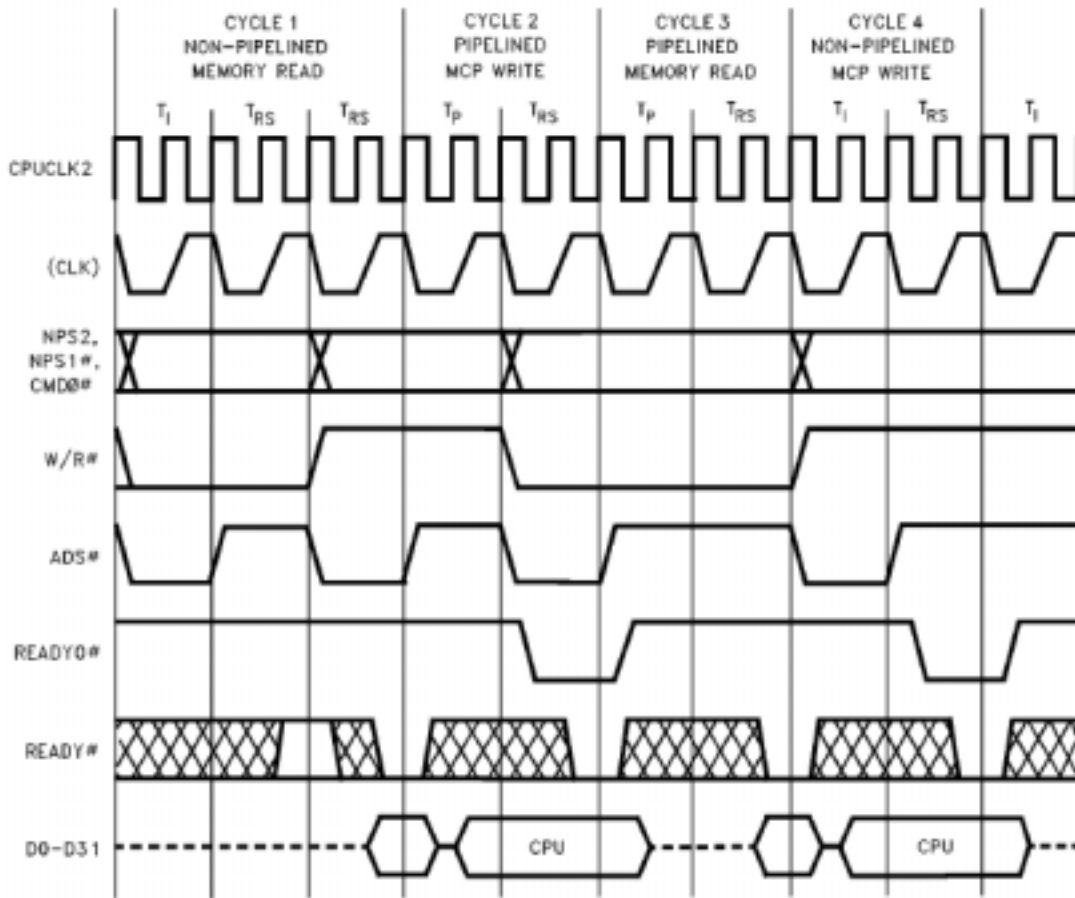
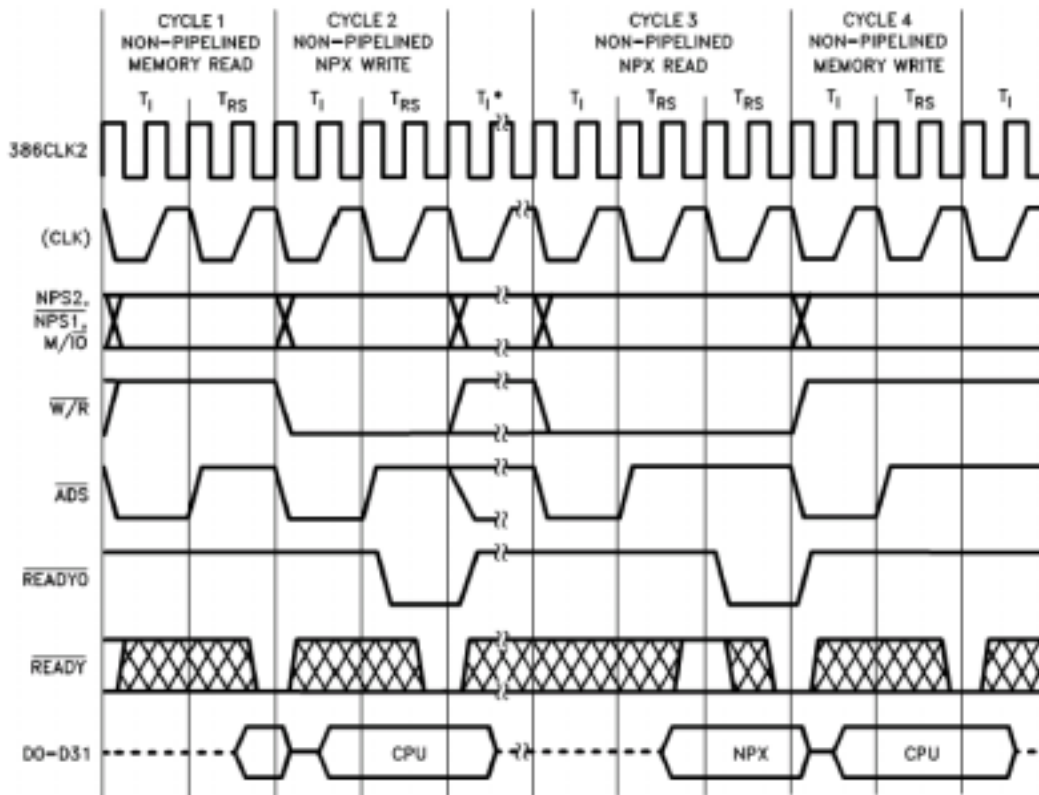
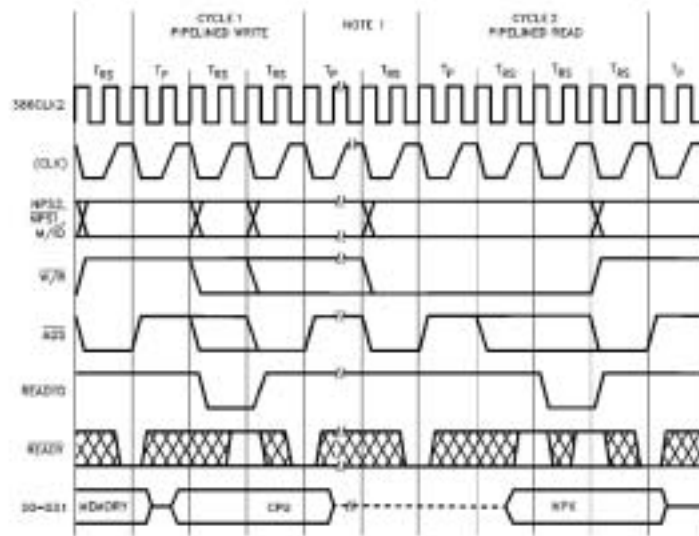


FIGURE 2. TIMING DIAGRAM – NON-PIPELINED READ AND WRITE CYCLES



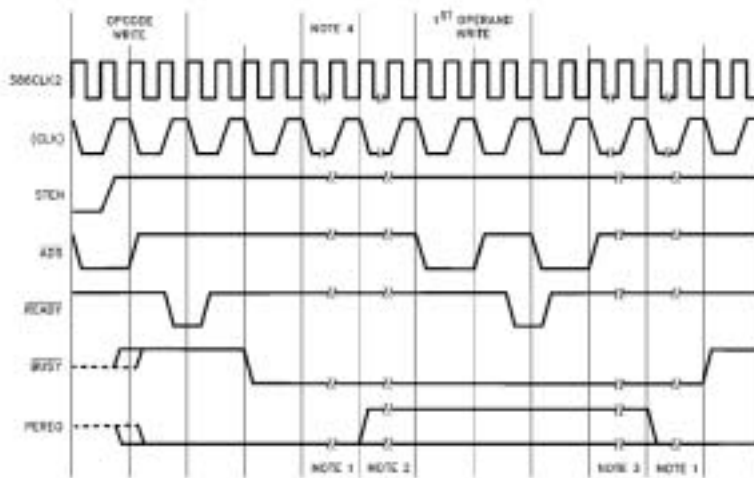
Cycles 1 & 2 represent part of the operand transfer cycle for instructions involving either 4-byte or 8-byte operand loads.
 Cycles 3 & 4 represent part of the operand transfer cycle for a store operation.
 *Cycles 1 & 2 could repeat here or T_1 states for various non-operand transfer cycles and overhead.

FIGURE 3. TIMING DIAGRAM – PIPELINED CYCLES WITH WAIT STATES



NOTE:
1. Cycles between operand write to the NPX and storing result.

FIGURE 4. TIMING DIAGRAM – STEN, BUSY, AND PEREQ TIMING RELATIONSHIP



NOTES:
1. Instruction dependent.
2. PEREQ is an asynchronous input to the 387 processor; it may not be asserted (instruction dependent).
3. More operand transfers.
4. Memory read (operand) cycle is not shown.

FIGURE 5. TIMING DIAGRAM – 386CLK2/387CLK2 WAVEFORM AND MEASUREMENT POINTS FOR INPUT/OUTPUT AC SPECIFICATIONS

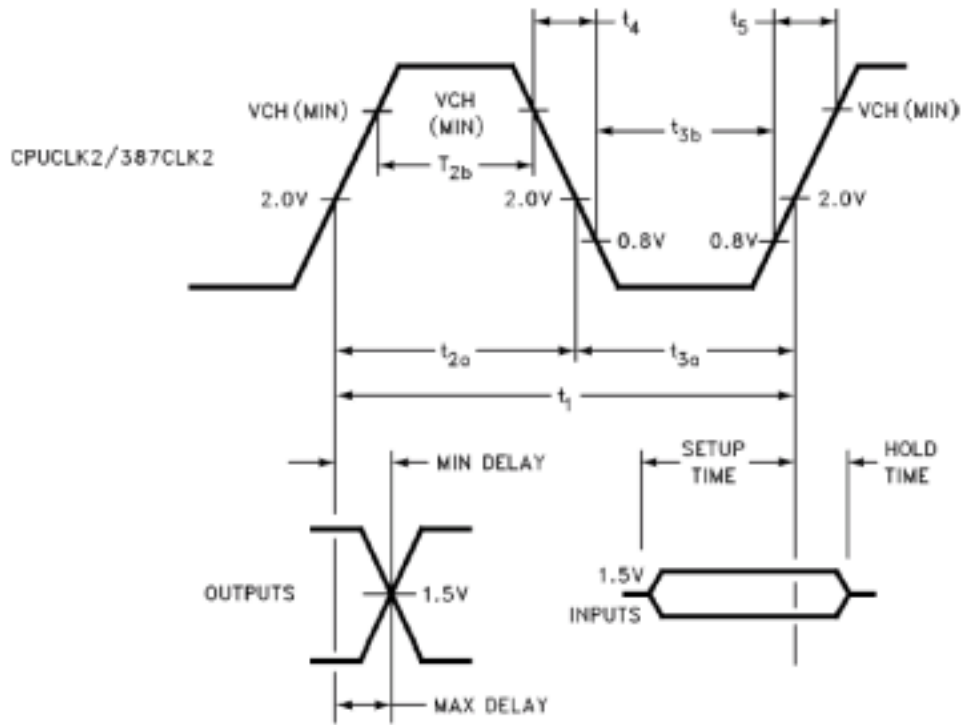


FIGURE 6. TIMING DIAGRAM – TEST CIRCUIT

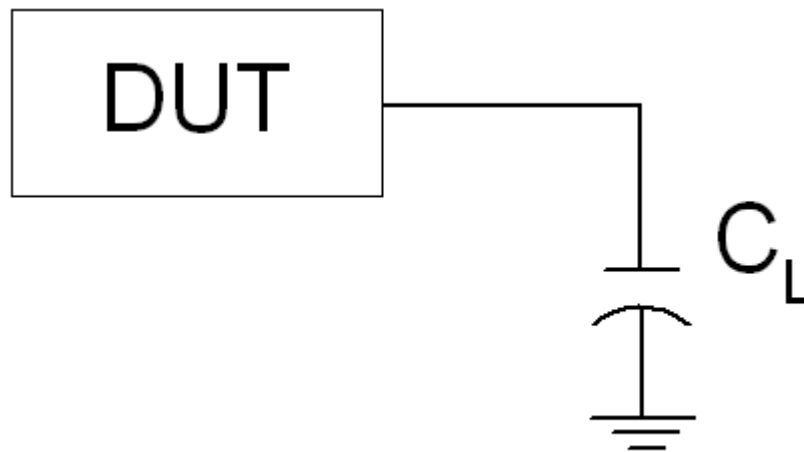
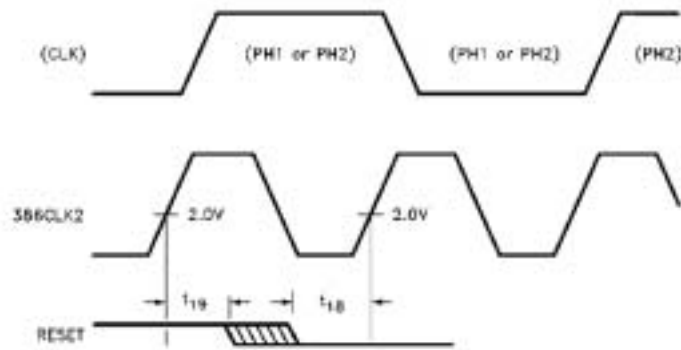
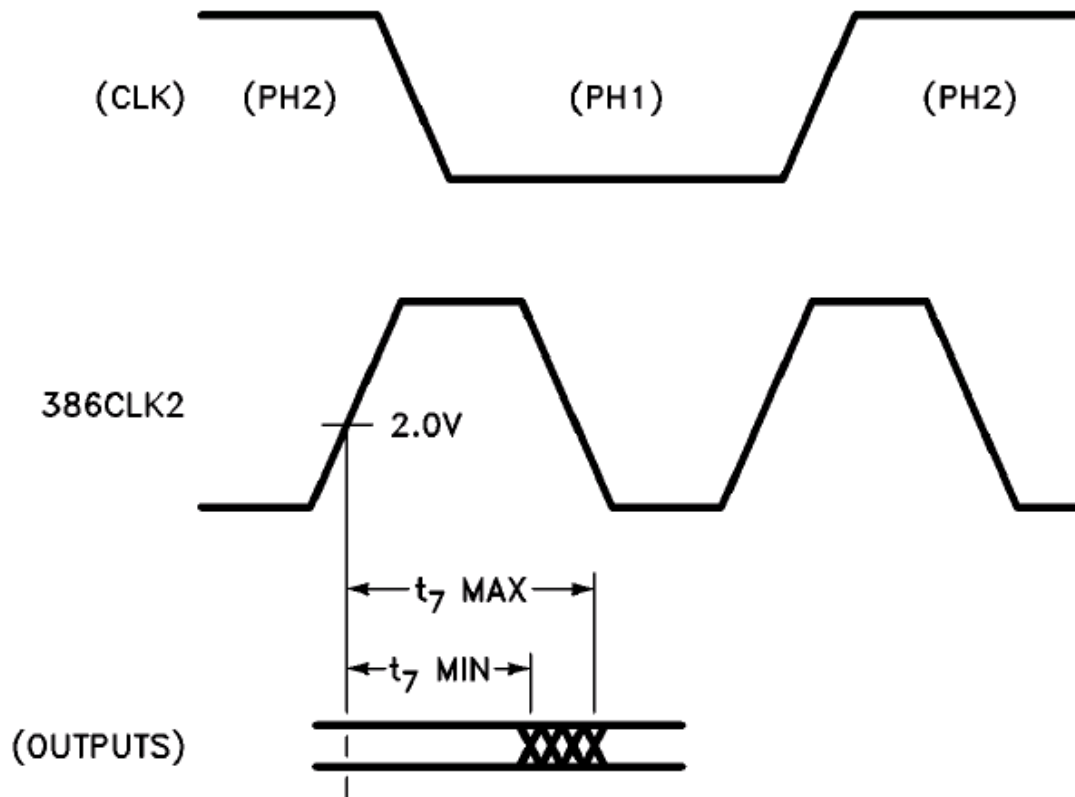


FIGURE 7. TIMING DIAGRAM – RESET



NOTE: The second internal processor phase following RESET high to low transition is PH2.

FIGURE 8. TIMING DIAGRAM – OUTPUT



(ERROR REFERENCED TO 387CLK2)

FIGURE 9. TIMING DIAGRAM – INPUT AND I/O SIGNALS

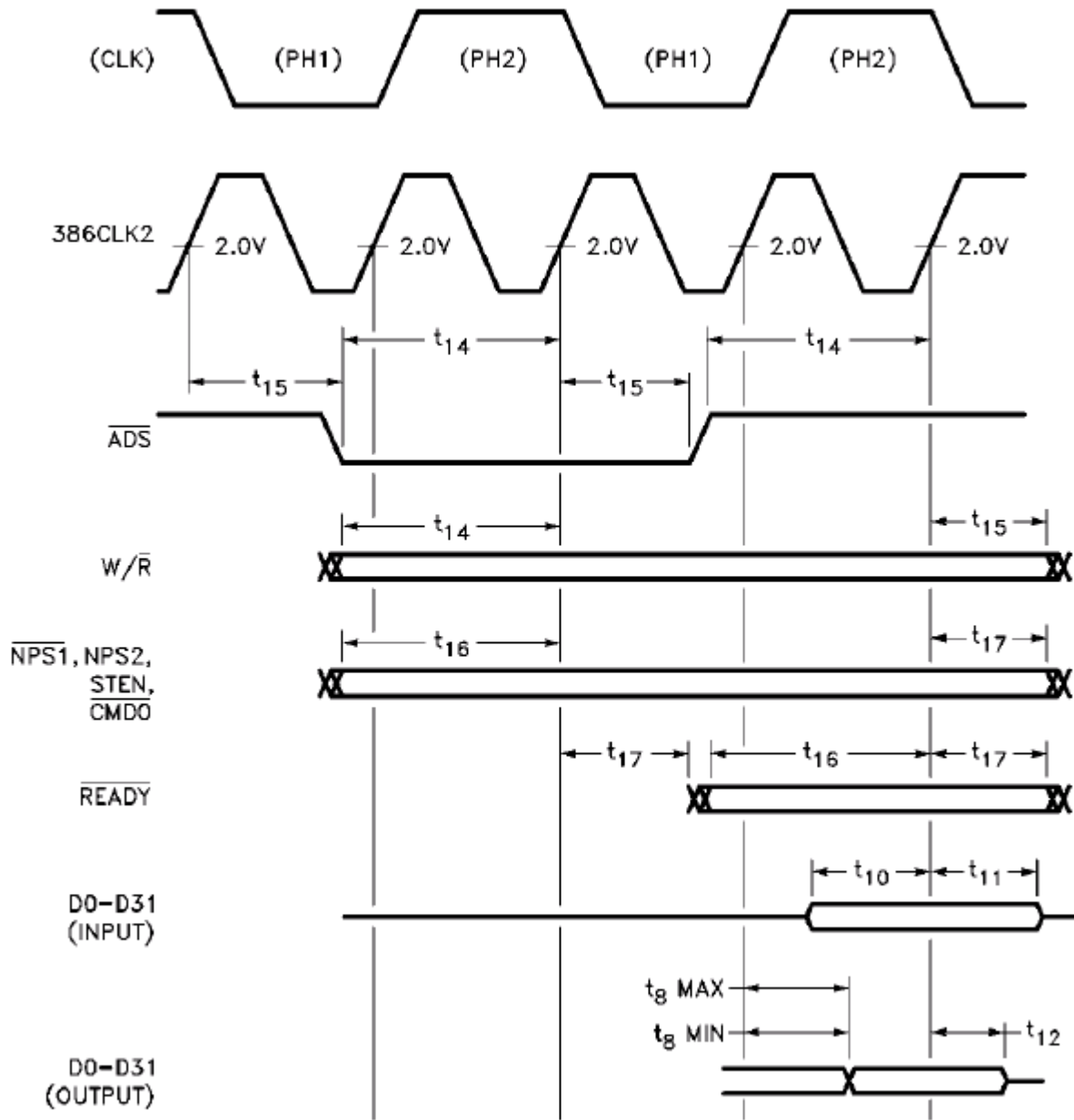


FIGURE 10. TIMING DIAGRAM – FLOAT FROM STEN

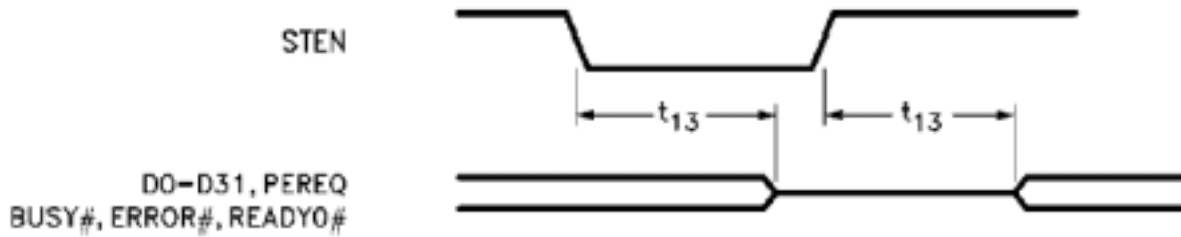
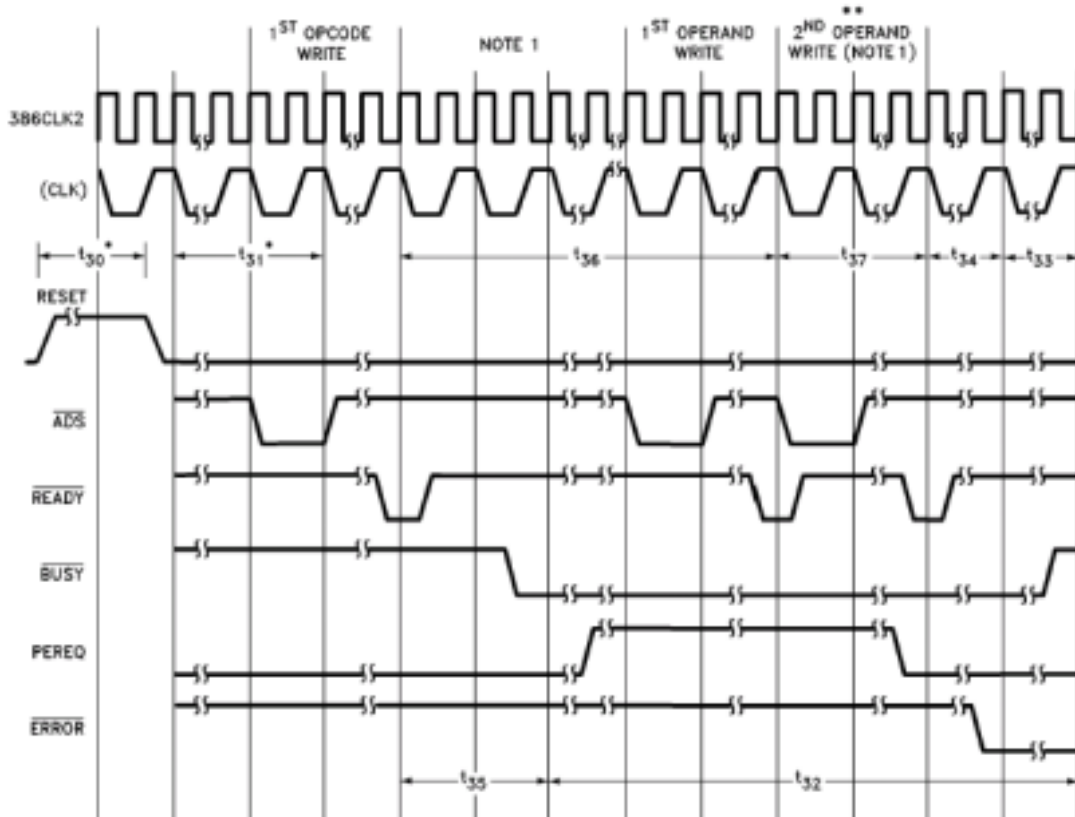
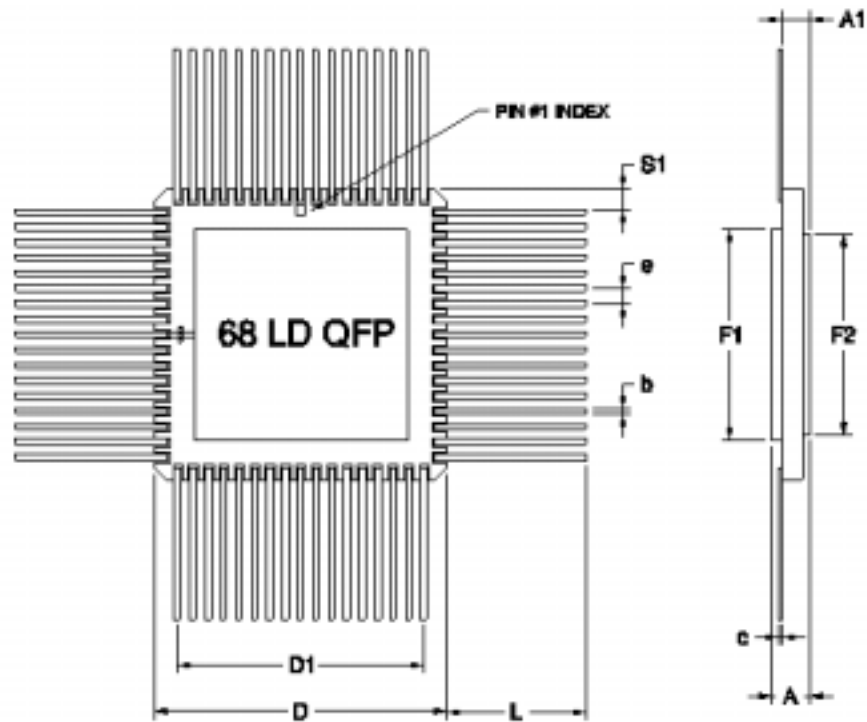


FIGURE 11. TIMING DIAGRAM – OTHER PARAMETERS



* In 387CLK2's
 ** or last operand

NOTE:
 1. Memory read (operand) cycle is not shown.



14 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.121	0.135	0.145
b	0.016	0.018	0.020
c	0.008	0.010	0.012
D	0.940	0.950	0.960
D1	0.800 BSC		
e	0.050 BSC		
S1	0.013	0.066	--
F1	0.645	0.650	0.655
F2	0.645	0.650	0.655
L	0.477	0.487	0.497
A1	0.080	0.090	0.100
N	68		

Note: All dimensions in inches.
Q68-01

Important Notice:

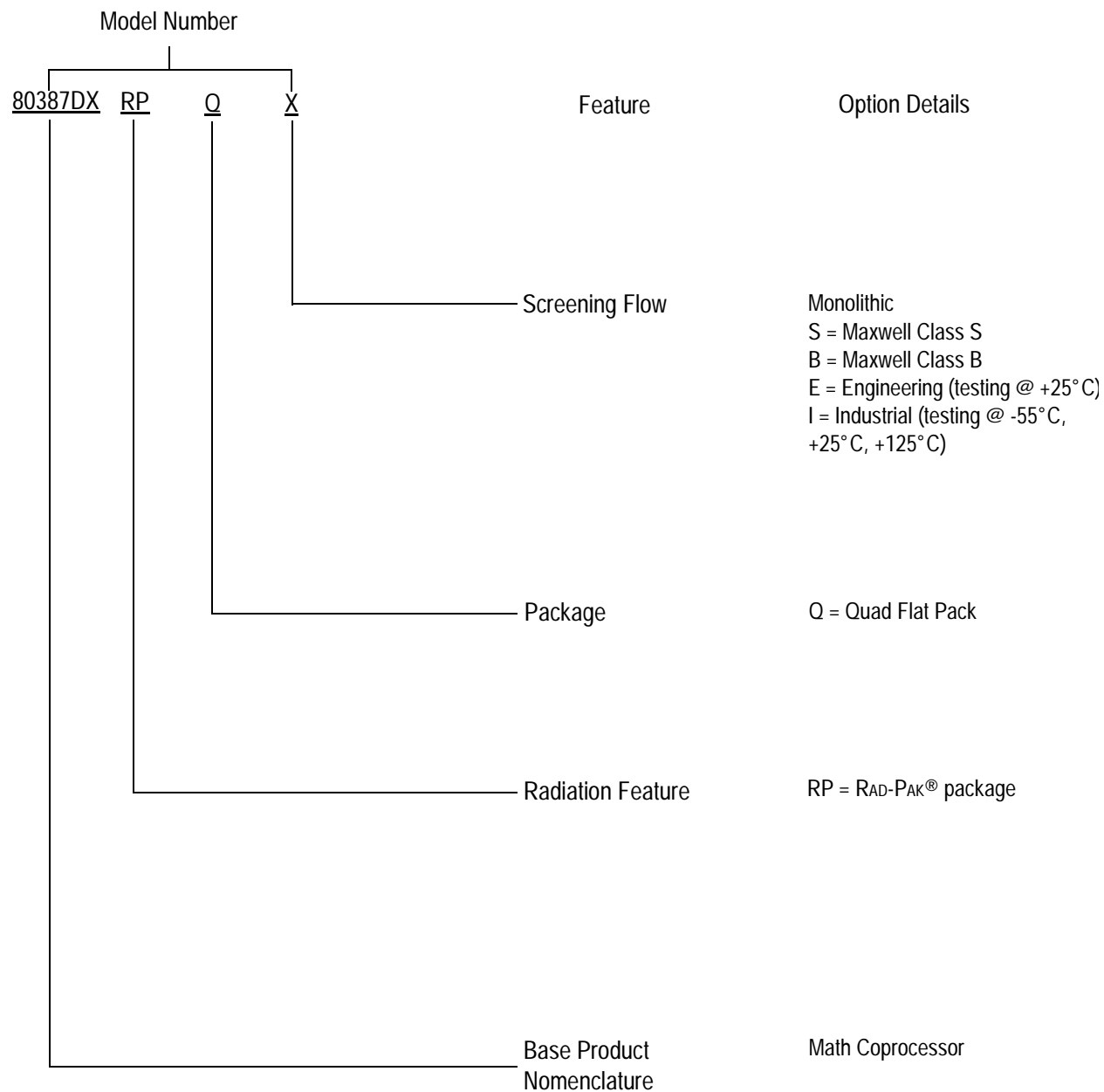
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