

MAX5113

9-Channel, 14-Bit Current DAC with SPI Interface

General Description

The MAX5113 is a 14-bit, 9-channel, current-output digital-to-analog converter (DAC). The device operates from a low +3.0V power supply and provides 14-bit performance without any adjustment.

The device's output ranges are optimized to bias a high-power tunable laser source. Each of the 9 channels provides a current source. Channels 1 and 2 provide 10mA current. An internal multiplexer switches the outputs of each channel to one of four external nodes. Channel 3 provides a selectable current of 2mA or 20mA. Channel 4 provides 90mA. Channel 5 provides 180mA. Channel 6 provides a selectable current of -60mA or +300mA. Channel 7 provides 90mA. Channels 8 and 9 provide a selectable current of 15mA or 35mA. Connect DAC outputs in parallel to obtain additional current or to achieve higher resolution. The device contains an internal reference.

An SPI interface drives the device with clock rates of up to 25MHz. An active-high asynchronous CLR input resets DAC codes to zero independent of the serial interface. The device provides a separate power-supply input for driving the interface logic.

The MAX5113 is specified over the -40°C to +105°C temperature range, and is available in 3mm x 3mm, 36-bump WLP and 5mm x 5mm, 32-pin TQFN packages.

Features

- ◆ **Low 3.0V Supply**
- ◆ **Integrated Multiplexers for Outputs 1 and 2**
- ◆ **Increased Current or Resolution with Outputs Connected in Parallel**
- ◆ **SPI-Compatible Serial Interface**
- ◆ **Internal Reference**
- ◆ **Overtemperature Protection**
- ◆ **Operates Over the -40°C to +105°C Temperature Range**
- ◆ **Available in 36-Bump WLP or 32-Pin TQFN Packages**

Applications

Tunable Laser Diode Biasing

Ordering Information

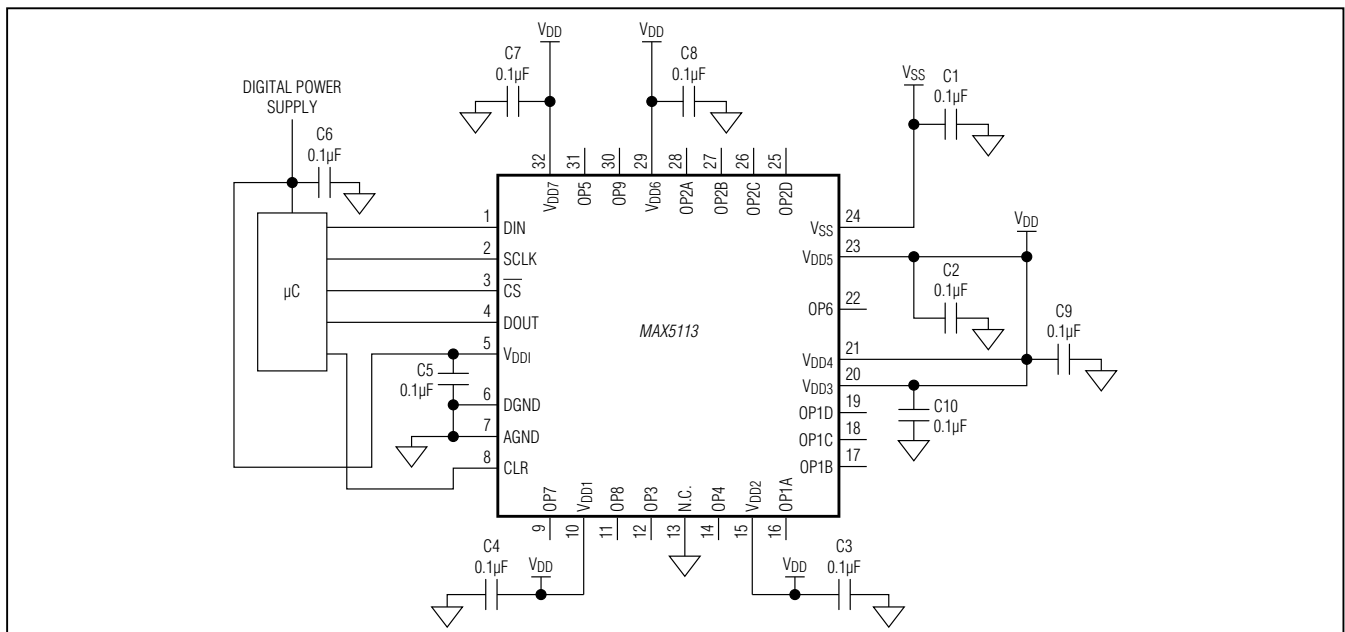
| PART | INTERFACE | PIN-PACKAGE |
|--------------|-----------|-------------|
| MAX5113GWX+T | SPI | 36 WLP |
| MAX5113GTJ+ | SPI | 32 TQFN-EP* |

Note: All devices are specified over the -40°C to +105°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

| | |
|--------------------------|---|
| VDD to AGND | -0.3V to +4.0V |
| VSS to AGND | -6.0V to +0.3V |
| VDDI to AGND | -0.3V to +6.0V |
| OP6 to AGN | the higher of (VDD - 9V), (VSS - 0.3V) and -6.0V to the lower of (VDD + 0.3V) and +4.0V |
| OP1 to OP5 and OP7, OP8, | |
| OP9 to AGND | -0.3V to the lower of (VDD + 0.3V) and +4.0V |
| DOUT to DGND | -0.3V to the lower of (VDDIO + 0.3V) and +6.0V |
| N.C. to AGND | -0.3V to the lower of (VDD + 0.3V) and +4.0V |
| Digital I/Os to DGND | -0.3V to +6.0V |

| | |
|--|-----------------|
| AGND to DGND | -0.3V to +0.3V |
| All Other Pins to AGND | -0.3V to +4.0V |
| Continuous Power Dissipation (TA = +70°C) | |
| WLP (derate at 26.3mW/°C above +70°C) | 2104mW |
| TQFN (derate at 34.5mW/°C above +70°C) | 2758mW |
| Maximum Current Into Any Pin | 380mA |
| Operating Temperature Range | -40°C to +105°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (TQFN only, soldering, 10s) | +300°C |
| Soldering Temperature (reflow) | +260°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

| | | | | | |
|------|--|---------|-----|--|--------|
| TQFN | Junction-to-Ambient Thermal Resistance (θ_{JA}) | 29°C/W | WLP | Junction-to-Ambient Thermal Resistance (θ_{JA}) | 38°C/W |
| | Junction-to-Case Thermal Resistance (θ_{JC}) | 1.7°C/W | | | |

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

(VDD = +2.6V to +3.3V, VSS = -4.75V to -5.46V, VDDI = +1.8V to +5.25V, AGND = DGND, TA = -40°C to +105°C, VOP1–VOP5 = VOP6 sourcing = VOP7, VOP8, and VOP9 = VDD - 1V, VOP6 sinking = VSS + 1V, unless otherwise noted. Typical specifications are at VDD = +3.0V, VSS = -5.2V, TA = +25°C. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|--------|-------------------------------|---------------|------------------|------|--------|
| STATIC PERFORMANCE | | | | | | |
| Resolution | N | | 14 | | | Bits |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | ±0.5 | ±1.0 | LSB |
| Integral Nonlinearity | INL | OP1–OP6 source and OP9 | | ±2 | ±8 | LSB |
| | | OP6 sink | | ±8 | | |
| Ideal Gain | IGAIN | | | $I_{MAX}/2^{14}$ | | mA/LSB |
| Gain Error (Note 3) | GE | All but OP3, 2mA and OP6 sink | | | ±1.3 | %FS |
| | | OP3, 2mA | | | ±1.5 | |
| | | OP6 sink | | | ±5 | |
| Gain Error Tempco (Note 4) | GETC | All but OP6 sink | | | ±50 | ppm/°C |
| | | OP6 sink | | | ±15 | |
| Full-Scale Output | IMAX | OP1 and OP2 | | | 10 | mA |
| | | OP3 | 2mA FS range | | 2 | |
| | | | 20mA FS range | | 20 | |
| | | OP4 | | | 90 | |
| | | OP5 | | | 180 | |
| | | OP6 current source | | | 300 | |
| | | OP6 current sink | | | -60 | |
| | | OP7 | | | 90 | |
| | | OP8 and OP9 | 15mA FS range | | 15 | |
| 35mA FS range | | | 35 | | | |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.6V$ to $+3.3V$, $V_{SS} = -4.75V$ to $-5.46V$, $V_{DDI} = +1.8V$ to $+5.25V$, $AGND = DGND$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$, $V_{OP1}-V_{OP5} = V_{OP6}$ sourcing = V_{OP7} , V_{OP8} , and $V_{OP9} = V_{DD} - 1V$, V_{OP6} sinking = $V_{SS} + 1V$, unless otherwise noted. Typical specifications are at $V_{DD} = +3.0V$, $V_{SS} = -5.2V$, $T_A = +25^{\circ}C$. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|------------------------------|---------------|--------------------|---------------|------------|--------------|----------------|---|
| Offset Error (Note 3) | OE | OP1 and OP2 | -120 | -60 | 0 | μA | |
| | | OP3 | 2mA FS range | -24 | -12 | | 0 |
| | | | 20mA FS range | -240 | -120 | | 0 |
| | | OP4 | -1080 | -540 | 0 | | |
| | | OP5 | -2160 | -1080 | 0 | | |
| | | OP6 current source | -3600 | -1800 | 0 | | |
| | | OP6 current sink | 0 | +360 | +720 | | |
| | | OP7 | -1080 | -540 | 0 | | |
| OP8 and OP9 | 15mA FS range | -180 | -90 | 0 | | | |
| | 35mA FS range | -420 | -210 | 0 | | | |
| Offset Error Tempco (Note 4) | OETC | OP1 and OP2 | | | ± 250 | $nA/^{\circ}C$ | |
| | | OP3 | 2mA FS range | | ± 50 | | |
| | | | 20mA FS range | | ± 500 | | |
| | | OP4 | | ± 2250 | | | |
| | | OP5 | | ± 4500 | | | |
| | | OP6 current source | | ± 7500 | | | |
| | | OP6 current sink | | ± 1500 | | | |
| | | OP7 | | ± 2250 | | | |
| OP8 and OP9 | 15mA FS range | | ± 375 | | | | |
| | 35mA FS range | | ± 875 | | | | |
| Output Compliance Range | V_{OR} | All but OP6 sink | V_{GND} | | $V_{DD} - 1$ | V | |
| | | OP6 sink | $V_{SS} + 1$ | | V_{DD} | | |
| DYNAMIC PERFORMANCE | | | | | | | |
| Output Resistance | R_{OUT} | OP1 and OP2 | | 2 | | $M\Omega$ | |
| | | OP3 | 2mA FS range | | 10 | | |
| | | | 20mA FS range | | 1 | | |
| | | OP4 | | 0.2 | | | |
| | | OP5 | | 0.1 | | | |
| | | OP6 current source | | 0.06 | | | |
| | | OP6 current sink | | 0.04 | | | |
| | | OP7 | | 0.2 | | | |
| OP8 and OP9 | 15mA FS range | | 1.3 | | | | |
| | 35mA FS range | | 0.56 | | | | |
| Current-Output Slew Rate | SR | OP1 and OP2 | | 5 | | $mA/\mu s$ | |
| | | OP3 | 2mA FS range | | 1 | | |
| | | | 20mA FS range | | 10 | | |
| | | OP4 | | 45 | | | |
| | | OP5 | | 90 | | | |
| | | OP6 current source | | 150 | | | |
| | | OP6 current sink | | 30 | | | |
| | | OP7 | | 45 | | | |
| OP8 and OP9 | 15mA FS range | | 7.5 | | | | |
| | 35mA FS range | | 17.5 | | | | |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.6V$ to $+3.3V$, $V_{SS} = -4.75V$ to $-5.46V$, $V_{DDI} = +1.8V$ to $+5.25V$, $AGND = DGND$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$, $V_{OP1}-V_{OP5} = V_{OP6}$ sourcing = V_{OP7} , V_{OP8} , and $V_{OP9} = V_{DD} - 1V$, V_{OP6} sinking = $V_{SS} + 1V$, unless otherwise noted. Typical specifications are at $V_{DD} = +3.0V$, $V_{SS} = -5.2V$, $T_A = +25^{\circ}C$. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|--------------------|---------------|-------|-------|-----------------|
| Output Settling Time | t_{OS} | $t_O \pm 0.1\%$ | | 15 | | μs |
| Noise at Full Scale (10kHz) | INO | OP1 and OP2 | | 1.6 | | nA/ \sqrt{Hz} |
| | | OP3 | 2mA FS range | 0.4 | | |
| | | | 20mA FS range | 3.4 | | |
| | | OP4 | | 16 | | |
| | | OP5 | | 31 | | |
| | | OP6 current source | | 56 | | |
| | | OP6 current sink | | 11 | | |
| | | OP7 | | 16 | | |
| | | OP8 and OP9 | 15mA FS range | 2.8 | | |
| 35mA FS range | 6.5 | | | | | |
| DAC Glitch Impulse Major-Carry Transition | IOGE | OP1 and OP2 | | 60 | | μC |
| | | OP3, 20mA | | 120 | | |
| | | OP4 | | 540 | | |
| | | OP5 | | 1080 | | |
| | | OP6 current source | | 1800 | | |
| | | OP6 current sink | | 360 | | |
| | | OP7 | | 540 | | |
| | | OP8 and OP9 | 15mA FS range | 90 | | |
| | | | 35mA FS range | 210 | | |
| DAC Output GND Switch Resistance | R_{GSW} | At 0.7V | | | 50 | Ω |
| DAC Output GND Switch Current | I_{GSW} | At 0.7V | 14 | | | mA |
| OVERTEMPERATURE DETECTORS | | | | | | |
| Overtemperature Disable Threshold | T_{OVTD} | | | +160 | | $^{\circ}C$ |
| Overtemperature Warning Threshold | T_{OVTW} | | | +150 | | $^{\circ}C$ |
| POWER REQUIREMENTS | | | | | | |
| Power-Supply Range | V_{DD} | | 2.6 | | 3.3 | V |
| Interface Power-Supply Range | V_{DDI} | | 1.8 | | 5.25 | V |
| Negative Supply Range | V_{SS} | | -5.46 | -5.2 | -4.75 | V |
| Supply Current | I_{DD} | No load, no I/O | | 500 | 600 | μA |
| Negative Supply Current | I_{SS} | | -20 | -11 | | μA |
| POWER-ON RESET (POR) | | | | | | |
| POR Threshold | V_{POR} | | | 1.6 | | V |
| POR Threshold Hysteresis | V_{PORH} | | | 0.025 | | V |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.6V to +3.3V, V_{SS} = -4.75V to -5.46V, V_{DDI} = +1.8V to +5.25V, AGND = DGND, T_A = -40°C to +105°C, V_{OP1}–V_{OP5} = V_{OP6} sourcing = V_{OP7}, V_{OP8}, and V_{OP9} = V_{DD} - 1V, V_{OP6} sinking = V_{SS} + 1V, unless otherwise noted. Typical specifications are at V_{DD} = +3.0V, V_{SS} = -5.2V, T_A = +25°C. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|--|------------------------|-------|------------------------|-------|
| DIGITAL INPUT CHARACTERISTICS (DIN, SCLK, $\overline{\text{CS}}$, CLR) | | | | | | |
| Input Low Voltage | V _{IL} | V _{DDI} = 2.2V to 5.25V | | | 0.3 x V _{DDI} | V |
| | | V _{DDI} = 1.8V to 2.2V | | | 0.2 x V _{DDI} | V |
| Input High Voltage | V _{IH} | V _{DDI} = 2.2V to 5.25V | 0.7 x V _{DDI} | | | V |
| | | V _{DDI} = 1.8V to 2.2V | 0.8 x V _{DDI} | | | V |
| Input Hysteresis | V _{HYS} | | | 250 | | mV |
| Input Capacitance | C _{IN} | | | 10 | | pF |
| Input Leakage Current | I _{IN} | Input = 0V or V _{DDI} | | | ±10 | µA |
| DIGITAL OUTPUT CHARACTERISTICS (DOUT) | | | | | | |
| Output Low Voltage | V _{OL} | V _{DDI} = 2.2V to 5.5V, I _{SINK} = 5mA | | | 0.40 | V |
| | | V _{DDI} = 1.8V to 2.2V, I _{SINK} = 2mA | | | 0.25 | |
| Output High Voltage | V _{OH} | V _{DDI} = 2.2V to 5.5V, I _{SOURCE} = 5mA | V _{DDI} - 0.5 | | | V |
| | | V _{DDI} = 1.8V to 2.2V, I _{SOURCE} = 2mA | V _{DDI} - 0.3 | | | V |
| Output Three-State Leakage | I _{OZ} | BHEN = 0 | | ±0.01 | ±1 | µA |
| Output Bus Hold Sinking Current | I _{BHK} | DOUT low, BHEN = 1 | | -12 | | µA |
| Output Bus Hold Sourcing Current | I _{BHC} | DOUT high, BHEN = 1 | | +5 | | µA |
| Output Three-State Capacitance | C _{OZ} | | | 11 | | pF |
| Output Short-Circuit Current | I _{OSS} | V _{DDI} = 5.25V | | ±100 | | mA |
| TIMING CHARACTERISTICS (Note 5) | | | | | | |
| Serial Clock Frequency | f _{SCLK} | | 0 | | 25 | MHz |
| SCLK Period | t _{CP} | V _{DDI} = 1.8V to 5.25V | 40 | | | ns |
| SCLK Pulse Width Low | t _{CL} | V _{DDI} = 1.8V to 5.25V, 60% duty cycle | 16 | | | ns |
| SCLK Pulse Width High | t _{CH} | V _{DDI} = 1.8V to 5.25V, 40% duty cycle | 16 | | | ns |
| $\overline{\text{CS}}$ Fall to SCLK Fall Setup Time | t _{CSS0} | To first SCLK falling edge | 16 | | | ns |
| $\overline{\text{CS}}$ Fall to SCLK Fall Hold Time | t _{CSh0} | Applies to inactive FE preceding first FE | 0 | | | ns |
| $\overline{\text{CS}}$ Rise to SCLK Fall Hold Time | t _{CSh1} | Applies to 24th FE | 0 | | | ns |
| DIN-to-SCLK Fall Setup Time | t _{DS} | | 8 | | | ns |
| DIN-to-SCLK Fall Hold Time | t _{DH} | | 8 | | | ns |
| SCLK Fall to DOUT Settling Time | t _{DOT} | V _{DDI} = 2.2V to 5.5V, C _{LOAD} = 20pF | | | 30 | ns |
| | | V _{DDI} = 1.8V to 2.2V, C _{LOAD} = 20pF | | | 60 | |
| SCLK Fall to DOUT Hold Time | t _{DOH} | C _{LOAD} = 0pF | 2 | | | ns |
| SCLK Fall to DOUT Disable | t _{DOZ} | 24th active FE deassertion | 2 | | 30 | ns |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.6V$ to $+3.3V$, $V_{SS} = -4.75V$ to $-5.46V$, $V_{DDI} = +1.8V$ to $+5.25V$, $AGND = DGND$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$, $V_{OP1}\text{--}V_{OP5} = V_{OP6}$ sourcing = V_{OP7} , V_{OP8} , and $V_{OP9} = V_{DD} - 1V$, V_{OP6} sinking = $V_{SS} + 1V$, unless otherwise noted. Typical specifications are at $V_{DD} = +3.0V$, $V_{SS} = -5.2V$, $T_A = +25^{\circ}C$. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|--------|---|-----|-----|-----|-------|
| \overline{CS} Fall to DOUT Enable | tDOE | $V_{DDI} = 2.2V$ to $5.5V$, asynchronous | 1 | | 30 | ns |
| | | $V_{DDI} = 1.8V$ to $2.2V$, asynchronous | 1 | | 40 | |
| \overline{CS} Rise to DOUT Disable | tCSDOZ | Stand alone, aborted sequence | | | 35 | ns |
| \overline{CS} Rise to SCLK Fall | tCSA | Applies to 24th FE, aborted sequence | | | 20 | ns |
| \overline{CS} Pulse-Width High | tCSPW | Stand alone | 20 | | | ns |
| SCLK Fall to \overline{CS} Fall | tCSF | Applies to 24th active FE | 100 | | | ns |
| CLR Fall to \overline{CS} Fall | tCLRCS | Applies to DACs in reset mode only | 20 | | | ns |
| CLR Pulse-Width High | tCLRPW | No DAC is in shutter or gate mode | 40 | | | ns |
| | | Any DAC is in shutter or gate mode (Note 6) | 500 | | | |

Note 2: Specifications are 100% production tested at $T_A \geq +25^{\circ}C$. Specifications for $T_A < +25^{\circ}C$ are guaranteed by design and characterization.

Note 3: Configuration register write operation required following power-up for output offset adjustment. See the *DAC Outputs* section in the *Detailed Description*. All gain and offset errors include the effect of the internal reference and are guaranteed over temperature. Gain error = (measured gain - I_{GAIN})/I_{GAIN}. Measured gain = (code 16383 DAC output - code 500 DAC output)/15883. Offset error = code 500 DAC output - (500 x measured gain). The device is trimmed such that offset error is negative, ensuring linear operation down to zero current output.

Note 4: Guaranteed by design and characterization. Not production tested. All gain and offset temperature coefficients include the effect of the internal reference. Temperature coefficients are calculated by the “box” method. For additional information, refer to Maxim Application Note 4300: *Calculating the error budget in precision digital-to-analog converter (DAC) applications*.

Note 5: Timing characteristics are tested and guaranteed with digital input conditions $V_{IH} = V_{DDI}$ and $V_{IL} = 0V$.

Note 6: Minimum pulse width required to realize functionally useful DAC transitions. Not production tested. See Shutter Mode Settling Time Down and Shutter Mode Settling Time Up graphs in the *Typical Operating Characteristics* section.

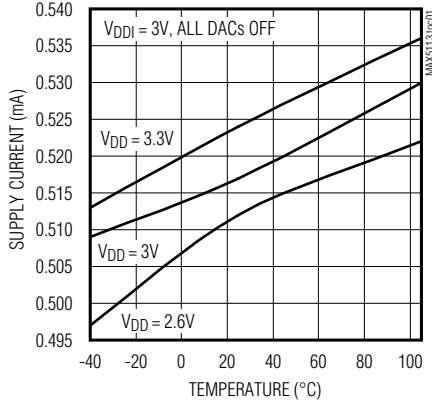
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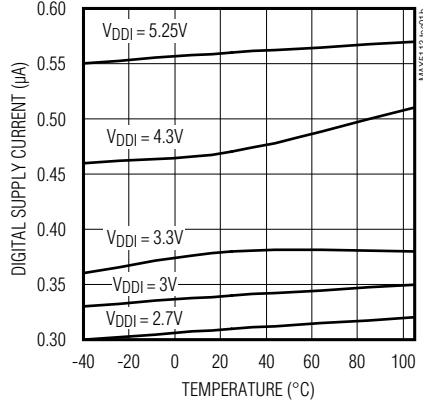
Typical Operating Characteristics

($V_{DD} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

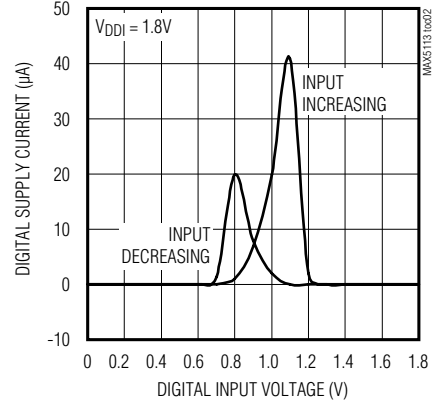
ANALOG SUPPLY CURRENT vs. TEMPERATURE



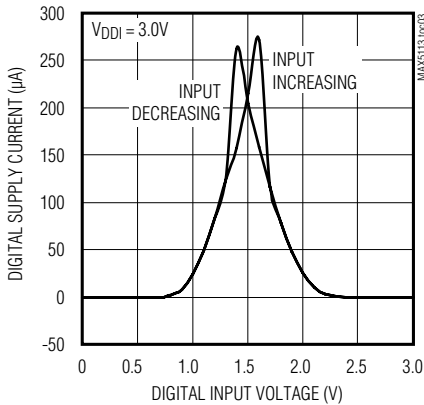
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



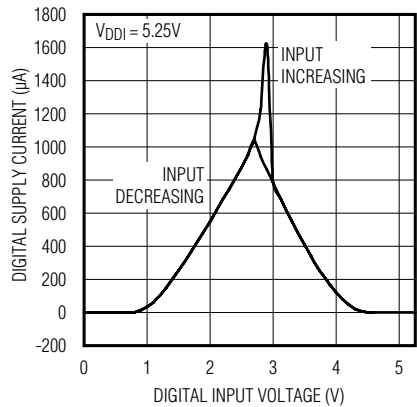
DIGITAL SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



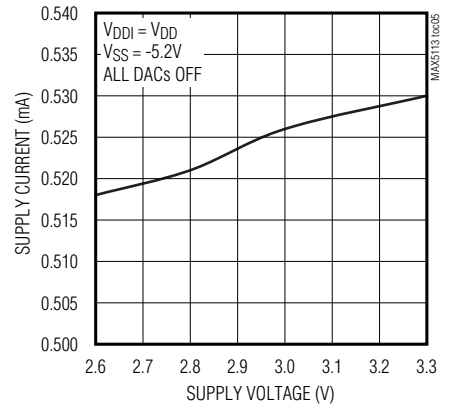
DIGITAL SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



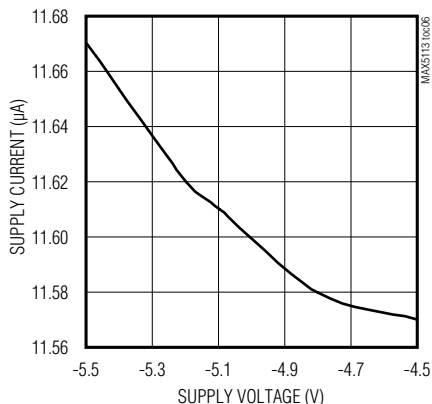
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



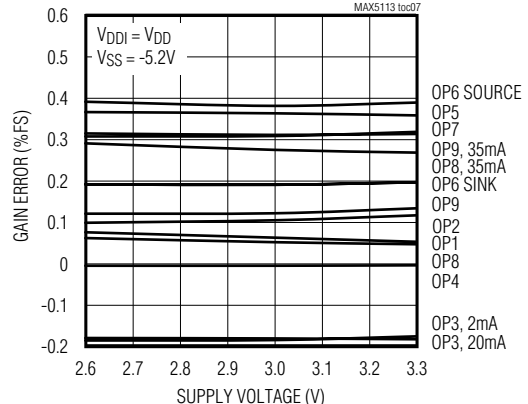
POSITIVE ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



NEGATIVE ANALOG SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE



GAIN ERROR vs. ANALOG SUPPLY VOLTAGE

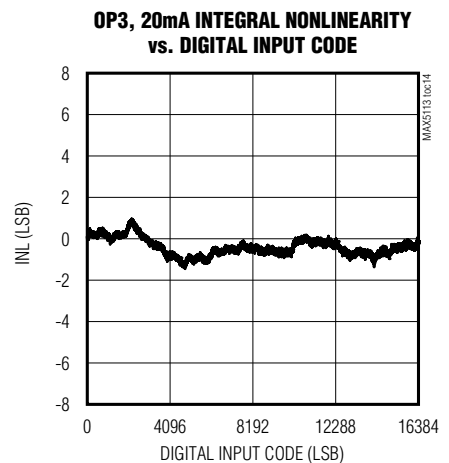
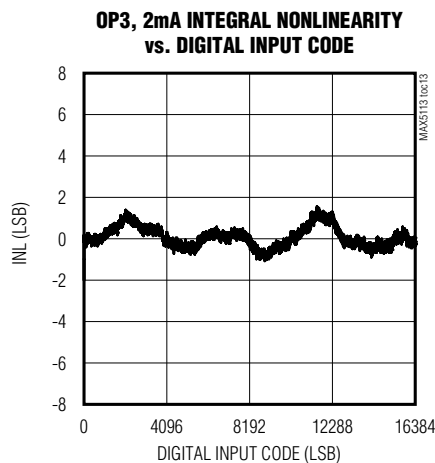
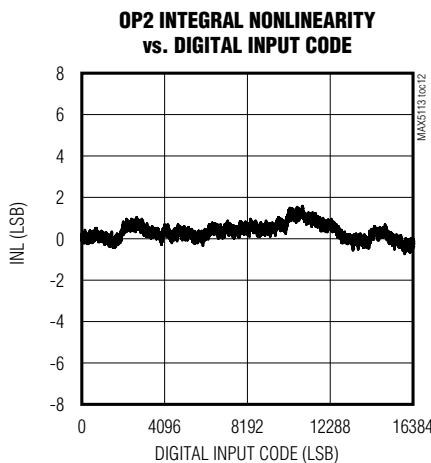
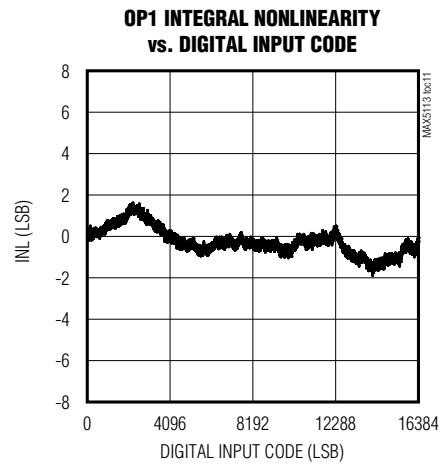
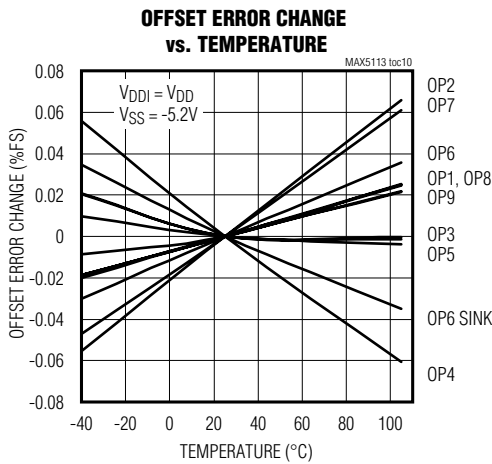
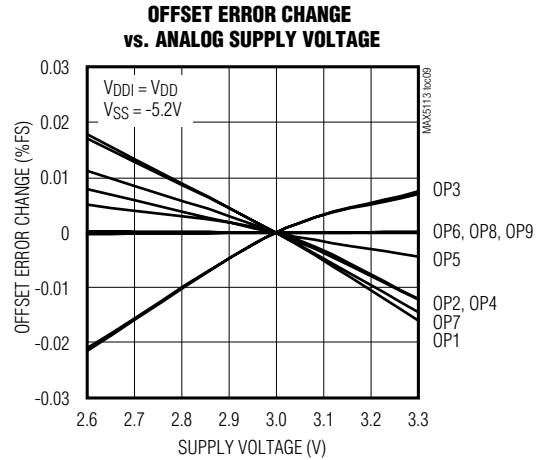
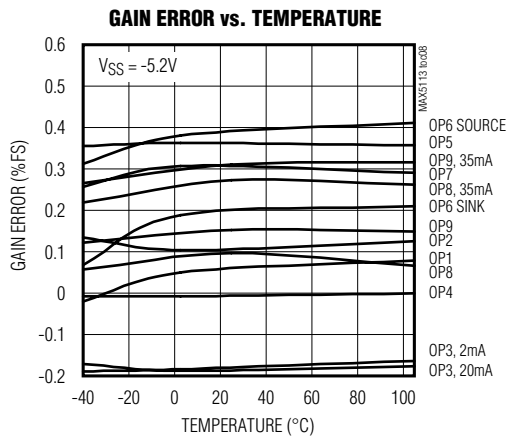


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Typical Operating Characteristics (continued)

($V_{DD} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

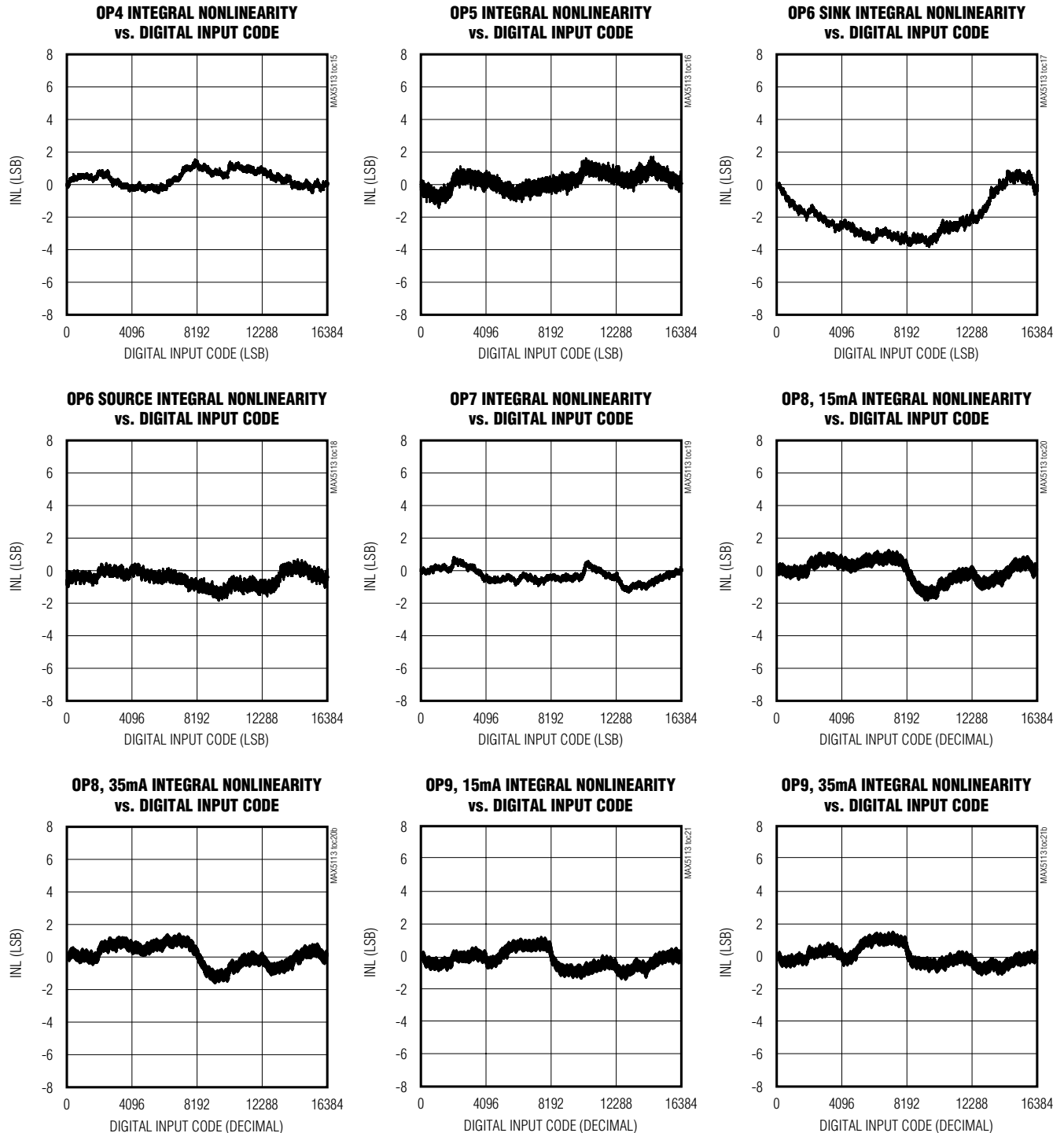


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9-Channel, 14-Bit Current DAC with SPI Interface

Typical Operating Characteristics (continued)

($V_{DD} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

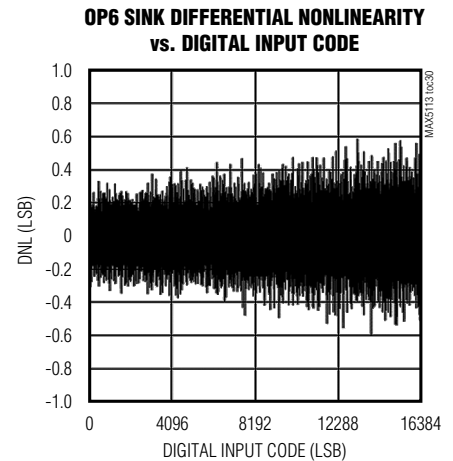
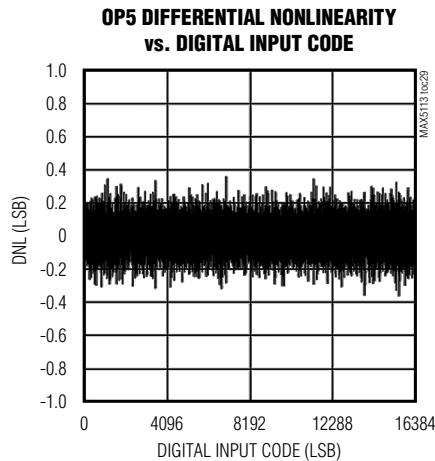
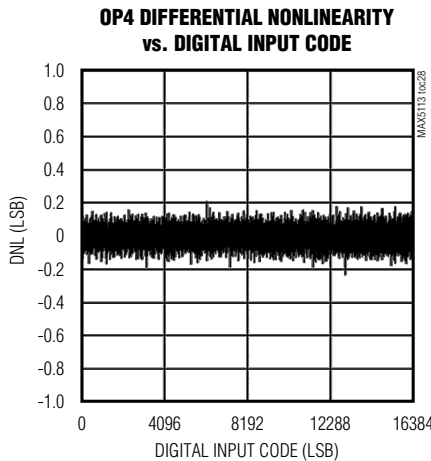
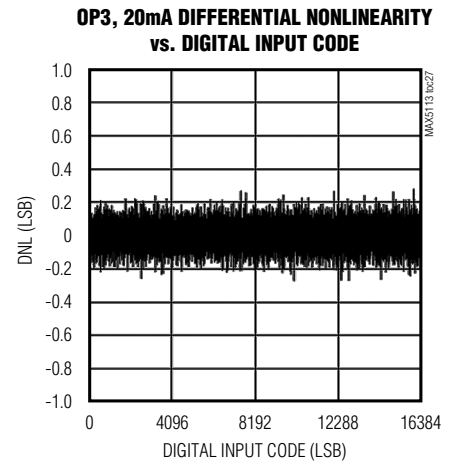
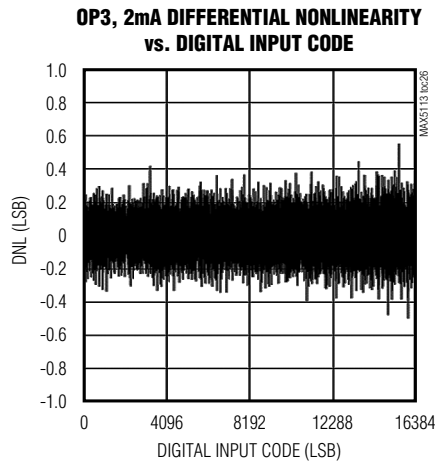
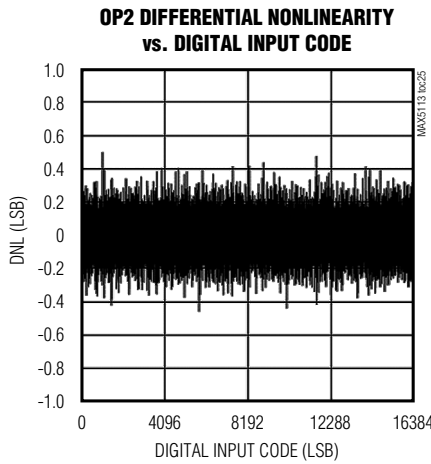
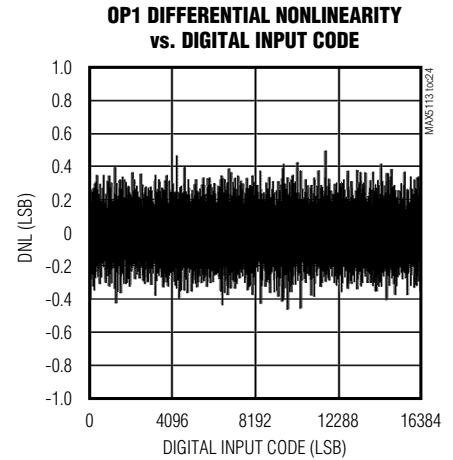
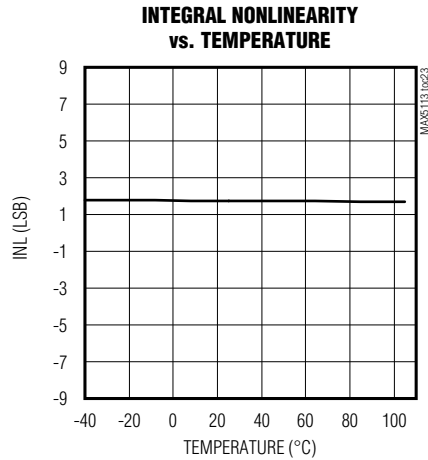
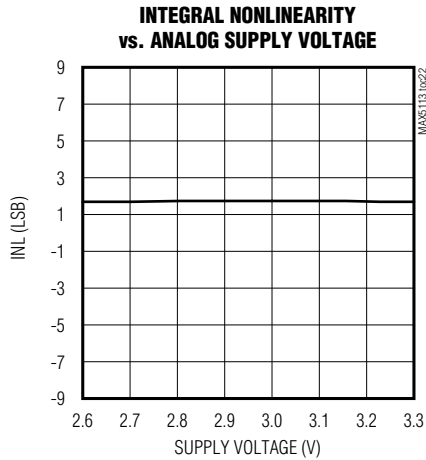


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9-Channel, 14-Bit Current DAC with SPI Interface

Typical Operating Characteristics (continued)

($V_{DD} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

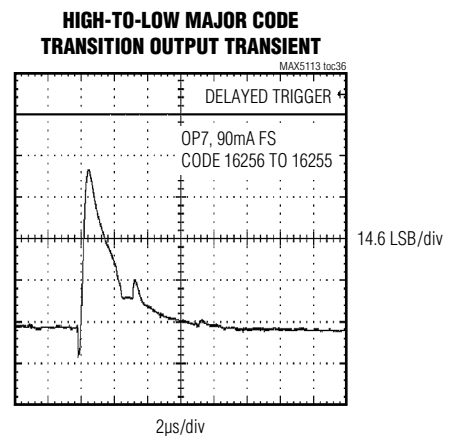
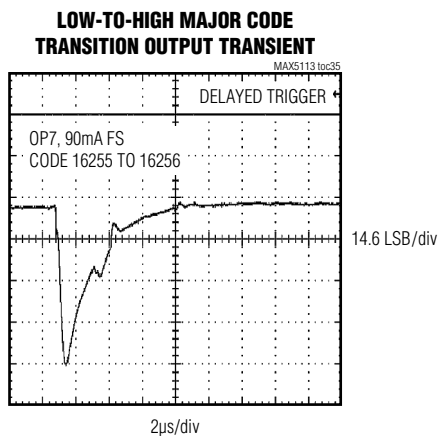
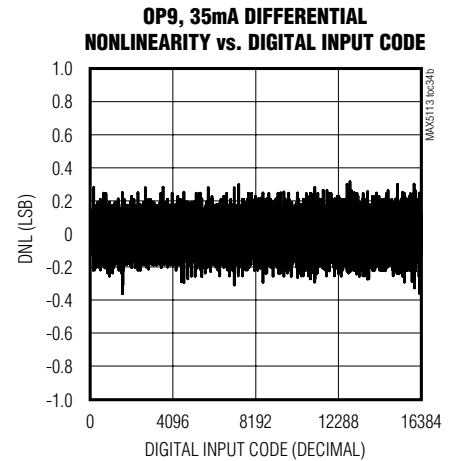
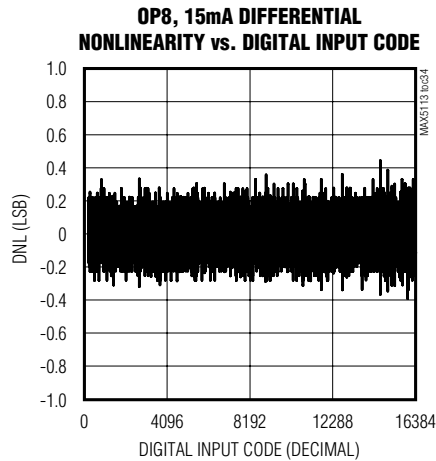
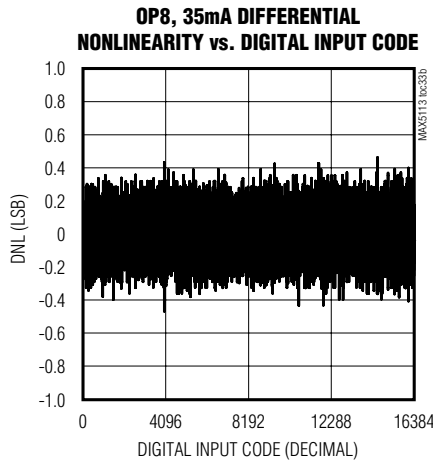
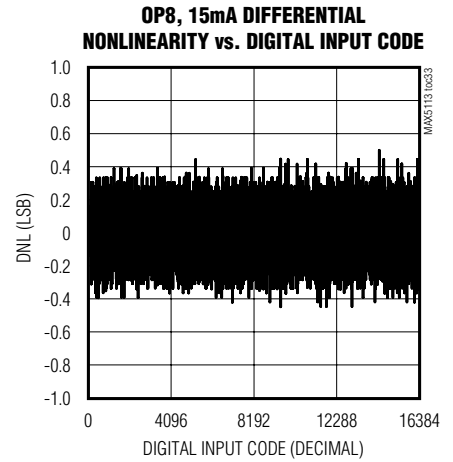
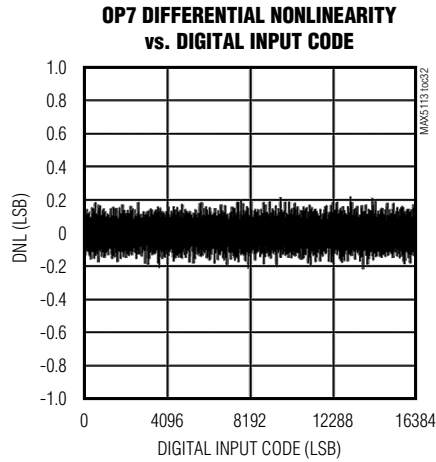
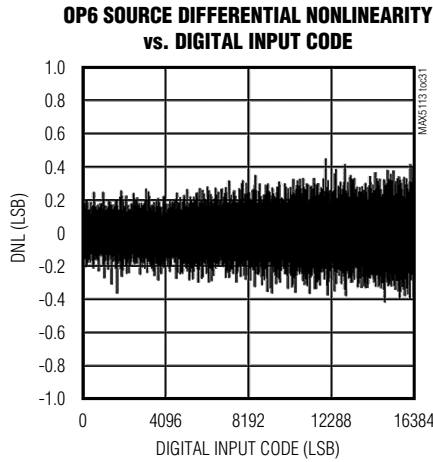


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9-Channel, 14-Bit Current DAC with SPI Interface

Typical Operating Characteristics (continued)

($V_{DD} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



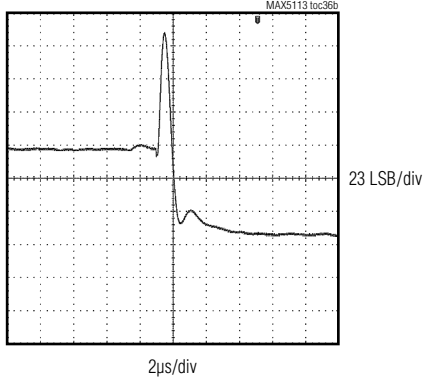
MAX5113

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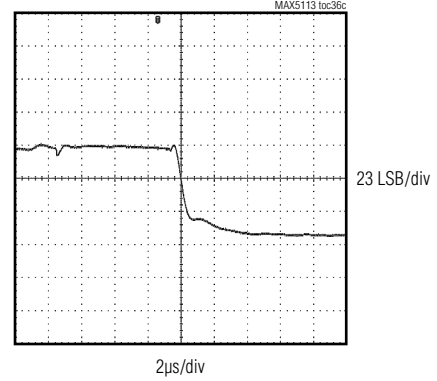
Typical Operating Characteristics (continued)

(VDD = 3.0V, TA = +25°C, unless otherwise noted.)

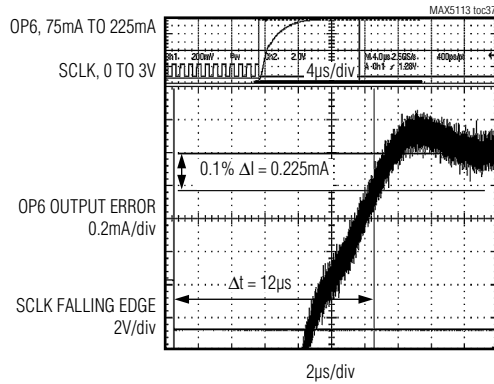
**MULTICODE TRANSITION TRANSIENT
OP8 CODE 9690 TO 9630 (T/H OFF)**



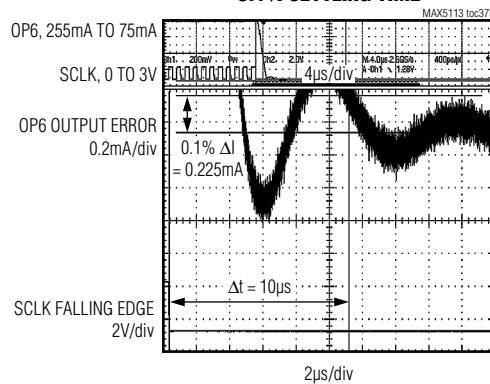
**MULTICODE TRANSITION TRANSIENT
OP8 CODE 9690 TO 9630 (T/H ON)**



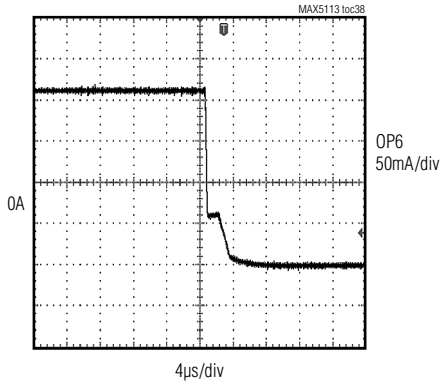
**OUTPUT 6 LOW TO HIGH CODE
0.1% SETTling TIME**



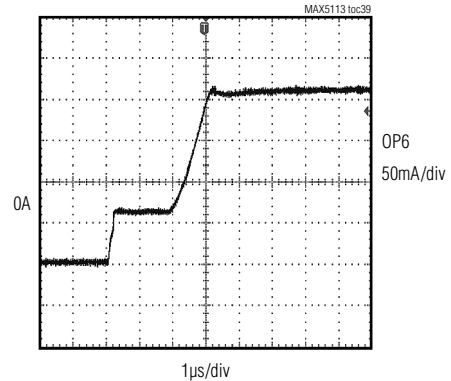
**OUTPUT 6 HIGH TO LOW CODE
0.1% SETTling TIME**



SHUTTER MODE SETTling TIME DOWN



SHUTTER MODE SETTling TIME UP

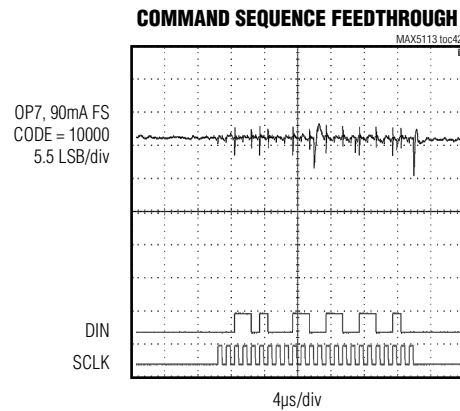
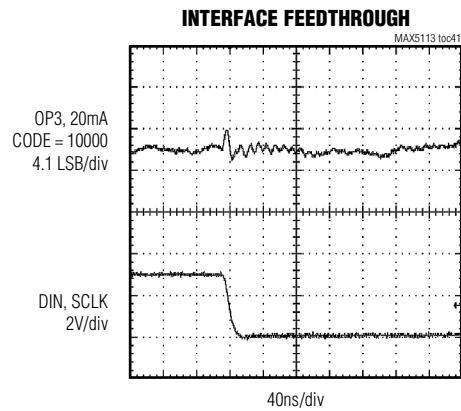
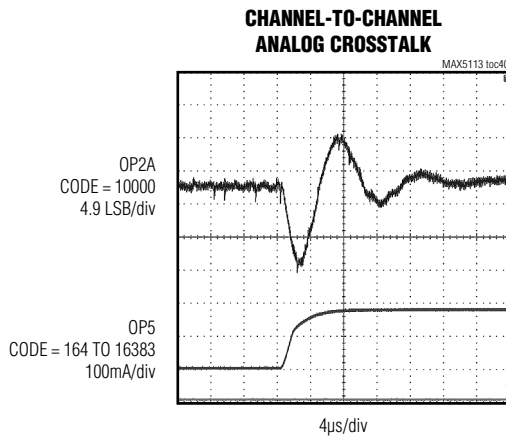


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9-Channel, 14-Bit Current DAC with SPI Interface

Typical Operating Characteristics (continued)

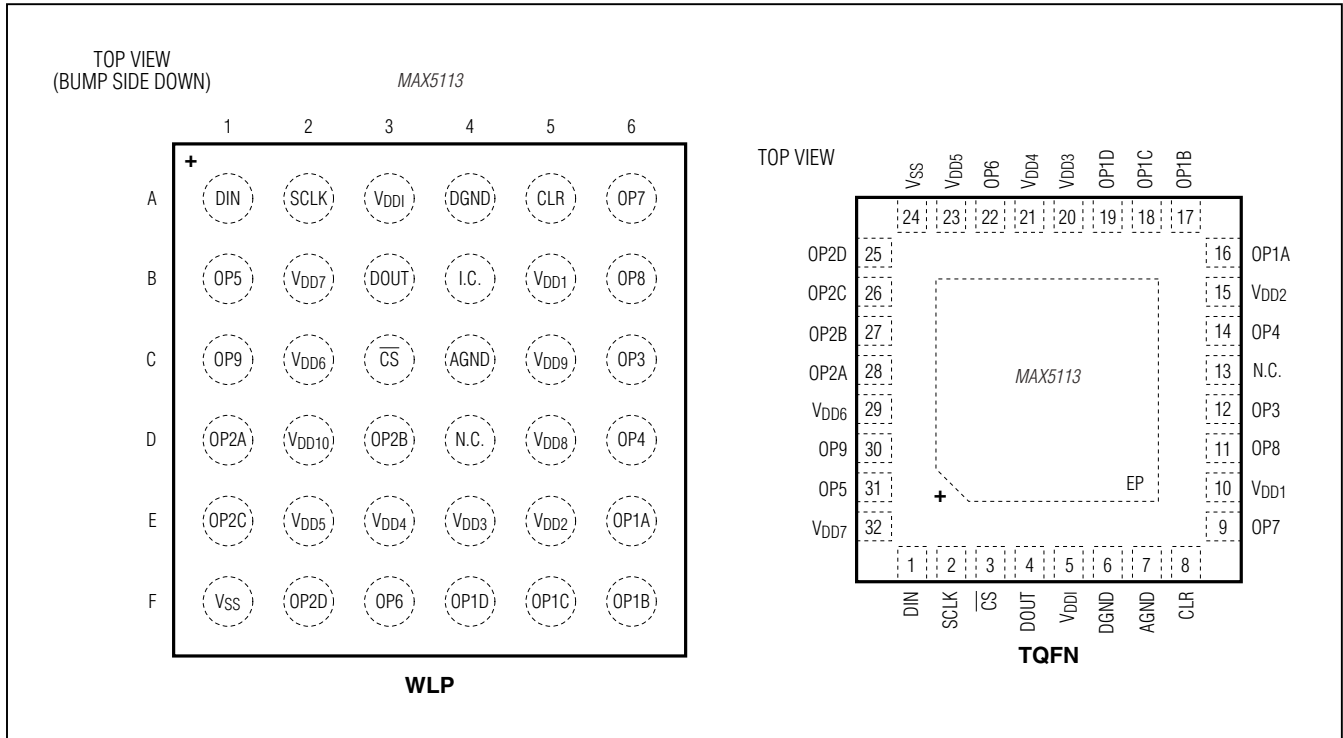
(VDD = 3.0V, TA = +25°C, unless otherwise noted.)



MAX5113

9-Channel, 14-Bit Current DAC with SPI Interface

Pin Configurations



Pin Description

| PIN | | NAME | FUNCTION |
|-----|---------|-------|---|
| WLP | TQFN-EP | | |
| A1 | 1 | DIN | SPI Data In |
| B1 | 31 | OP5 | DAC 5 Output, 180mA Full Scale |
| C1 | 30 | OP9 | DAC 9 Output, 15mA or 35mA Full Scale |
| D1 | 28 | OP2A | DAC 2 Multiplexer Output A, 10mA Full Scale |
| E1 | 26 | OP2C | DAC 2 Multiplexer Output C, 10mA Full Scale |
| F1 | 24 | VSS | Negative Power Supply |
| A2 | 2 | SCLK | SPI Clock Input |
| B2 | 32 | VDD7 | DAC 5 Output Positive Power Supply. Internally connected to VDD6 and VDD10. |
| C2 | 29 | VDD6 | DAC 5 Output Positive Power Supply (WLP). Internally connected to VDD7 and VDD10. |
| | | | DAC 5 Output and DAC 2 Output Positive Power Supply (TQFN). Internally connected to VDD7 and VDD10. |
| D2 | — | VDD10 | DAC 2 Output and DAC 9 Output Positive Power Supply. Internally connected to VDD6 and VDD7. |
| E2 | 23 | VDD5 | DAC 6 Output Positive Power Supply. Internally connected to VDD3 and VDD4. |
| F2 | 25 | OP2D | DAC 2 Multiplexer Output D, 10mA Full Scale |

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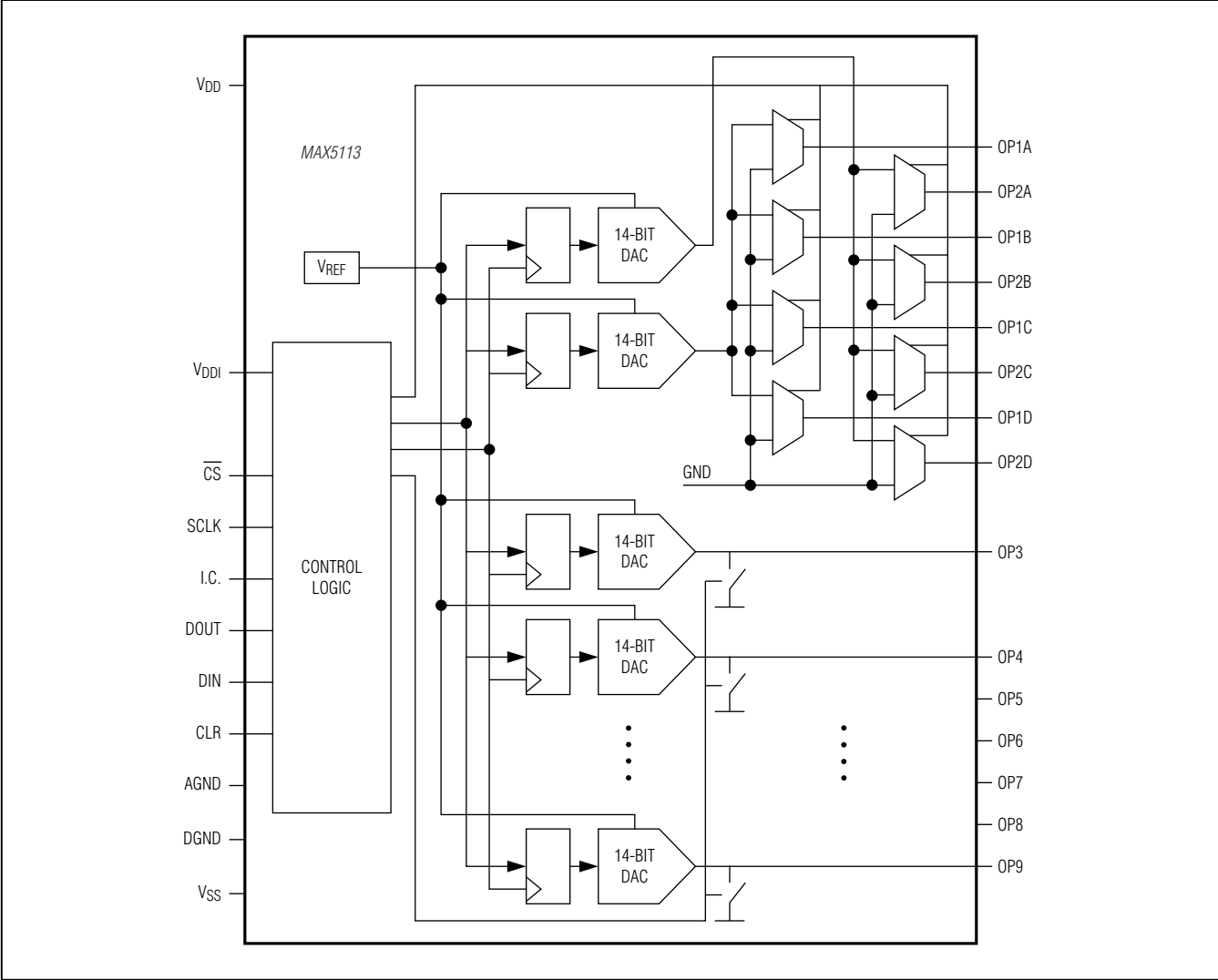
Pin Description (continued)

| PIN | | NAME | FUNCTION |
|-----|---------|------------------------|--|
| WLP | TQFN-EP | | |
| A3 | 5 | V _{DDI} | Interface Power Supply. Connect to V _{DD} or to a separate supply to allow for a different interface voltage. |
| B3 | 4 | DO _{UT} | SPI Data Out |
| C3 | 3 | $\overline{\text{CS}}$ | Active-Low SPI Chip Select |
| D3 | 27 | OP _{2B} | DAC 2 Multiplexer Output B, 10mA Full Scale |
| E3 | 21 | V _{DD4} | DAC 6 Output Positive Power Supply. Internally connected to V _{DD5} and V _{DD3} . |
| F3 | 22 | OP ₆ | DAC 6 Output, -60mA or 300mA Full Scale |
| A4 | 6 | DGND | Digital Ground |
| B4 | — | I.C. | Internally Connected. Connect to DGND. |
| C4 | 7 | AGND | Analog Ground |
| D4 | 13 | N.C. | No Internal Connection. Must obey <i>Absolute Maximum Ratings</i> . |
| E4 | 20 | V _{DD3} | DAC6 Output Positive Power Supply. Internally connected to V _{DD5} and V _{DD4} . |
| F4 | 19 | OP _{1D} | DAC 1 Multiplexer Output D, 10mA Full Scale |
| A5 | 8 | CLR | Active-High Clear |
| B5 | 10 | V _{DD1} | DAC 7 Output Positive Power Supply (WLP) |
| | | | DAC 3 Output and DAC 7 Output and DAC8 Output Positive Power Supply (TQFN) |
| C5 | — | V _{DD9} | DAC 3 Output and DAC 8 Output Positive Power Supply |
| D5 | — | V _{DD8} | DAC 4 Output Positive Power Supply |
| E5 | 15 | V _{DD2} | DAC 1 Output Positive Power Supply (WLP) |
| | | | DAC 1 Output and DAC 4 Output Positive Power Supply (TQFN) |
| F5 | 18 | OP _{1C} | DAC 1 Multiplexer Output C, 10mA Full Scale |
| A6 | 9 | OP ₇ | DAC 7 Output, 90mA Full Scale |
| B6 | 11 | OP ₈ | DAC 8 Output, 15mA or 35mA Full Scale |
| C6 | 12 | OP ₃ | DAC 3 Output, 2mA or 20mA Full Scale |
| D6 | 14 | OP ₄ | DAC 4 Output, 90mA Full Scale |
| E6 | 16 | OP _{1A} | DAC 1 Multiplexer Output A, 10mA Full Scale |
| F6 | 17 | OP _{1B} | DAC 1 Multiplexer Output B, 10mA Full Scale |
| — | — | EP | Exposed Pad (TQFN only). Internally connected to AGND. Connect to a ground plane to enhance thermal dissipation. |

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9-Channel, 14-Bit Current DAC with SPI Interface

Functional Diagram



9-Channel, 14-Bit Current DAC with SPI Interface

Detailed Description

The MAX5113 output ranges are optimized to bias a high-power tunable laser source. See Table 1 for the output current range available on each DAC output.

The DACs and highly stable internal reference are factory trimmed to ensure the outputs are within the specifications. Connect DACs in parallel to increase current drive or resolution.

DAC Outputs

The DAC configuration registers (01h–09h) control the configuration of each DAC. The Individual Configuration Register for each channel must be written to after a power-up event, even if the default values are written. This ensures the device will meet guaranteed offset performance specifications. DACs 1 and 2 drive four 2:1 multiplexers. The multiplexers route each DAC output to one of four outputs. Configure unused outputs as high impedance or connect to AGND. DAC 3 full-scale output is selectable between 2mA and 20mA.

DAC 6 provides 300mA full-scale output when selected as a current source. When selected as a current sink, the full 14 bits are available between 0 and -60mA. A typical application for DAC 6 is to drive an optical amplifier where a current source is varied to set the gain or where a current sink is varied to set the attenuation.

All other DACs are positive current source DACs. DACs 8 and 9 full-scale outputs are selectable between 15mA and 35mA. The output range of DACs 3, 8 and 9 is selected using the RNG bit in the Individual Configuration

Table 1. Typical Full-Scale Output Currents

| OUTPUT | OUTPUT-CURRENT RANGE CAPABILITY (mA) | |
|--------|--------------------------------------|------------|
| | LOW RANGE (DEFAULT) | HIGH RANGE |
| OP1 | 0 to 10 | Reserved |
| OP2 | 0 to 10 | Reserved |
| OP3 | 0 to 2 | 0 to 20 |
| OP4 | 0 to 90 | Reserved |
| OP5 | 0 to 180 | Reserved |
| OP6 | -60 to 0 or 0 to 300 | Reserved |
| OP7 | 0 to 90 | Reserved |
| OP8 | 0 to 15 | 0 to 35 |
| OP9 | 0 to 15 | 0 to 35 |

registers. The DAC 6 polarity and full-scale output is set by the SW_POL bit in the DAC 6 register.

Output Track and Hold

All channels feature a track-and-hold circuit to improve glitch performance. In common with all DACs of this type, the MAX5113 DACs will glitch when in transition from one code to another. The size of the glitch is defined by the size of the transition and where in the overall range the transition occurs. In general, a small transition results in a small glitch. However, this is not absolute. The track-and-hold circuit may be enabled to reduce the glitch size to close to zero. The track and hold can be enabled independently for each channel by setting bit 12 in the Individual DAC Configuration registers (01h–09h).

When enabled, the track and hold will engage after the 24th SCLK in the SPI frame, setting a new DAC code. This will hold the output level until the DAC section has settled. There is a small negative offset present in the output level while the track and hold is engaged. Approximately 10 LSB. The track and hold is engaged for 6μs, typical. It then disengages and the channel will transition to its new level with no glitch.

DAC Ground Switch

All DACs include a programmable switch to connect the output to ground when the DAC code is set to zero. The switch is open when the configuration bit is set to 0 and code zero is programmed. In this case, the output drivers are disabled, and the outputs set to high impedance. The DAC switch configuration is set for each individual DAC; see the *01h–09h: Individual DAC (1 to 9) Configuration Registers* section. The global DAC switch-override bits (GSWG[1:0]) in the General Configuration register (00h) override all switch selections when applied.

Clear Function (CLR)

The clear function allows the access of modes of operation through a single active-high input, CLR. The behavior of each DAC with CLR asserted is independently configurable. See the *CLR Interaction* section.

The clear function can also be asserted in software by setting the SW_CLR bit in the Software Reset Command register; see the *0Fh: Software Reset Command Register* section.

The clear function for each DAC is programmed through the CLR_CFG[1:0] bits in the Individual DAC Configuration registers (01h–09h) as shown in the following:

- **00 (Ignore):** The assertion of CLR does not affect the DAC.

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- **01 (Shutter):** Shutter mode applies to OP6 only. For all other DACs, shutter mode produces the same effect as ignore. For OP6, the output polarity stays negative for as long as CLR is asserted (level sensitive). The current sink level is defined by the DAC 6 Shutter Mode Code register (1Bh). Once CLR releases, the DAC output returns to the previously programmed value as set in the DAC 6 Source Mode Code register (16h).
- **10 (Gate):** The DAC is held at code zero (with ground switches engaged if enabled) as long as CLR is asserted (level sensitive). Once CLR releases, the DAC output returns to the previously programmed value as set in the DAC 1–9 Code register (10h–1Ah).
- **11 (Reset):** The DAC is set to code zero (with ground switches engaged if enabled) when CLR is asserted and remains at code zero after CLR is released (edge sensitive).

While the clear operation is in effect, DAC channels configured in ignore, shutter, or gate mode continue to accept new code settings. DAC channels configured in reset mode do not accept code changes until the clear operation is terminated.

Software Clear Interactions

The device provides a software-accessible version of the clear function (SW_CLR), which allows access to the clear functionality directly through the SPI interface (see the *0Fh: Software Reset Command Register* section). When the command 0Fh is used to launch a clear operation, the affected DAC outputs are held in the clear position, determined by the clear configuration settings. This happens from the time when the 0Fh command requesting a clear operation is completed until a second 0Fh command requesting removal of the clear operation is completed. The software- and pin-based clear operations are independently controlled and can be used individually or together without conflict. The devices provide an internal logic-OR circuitry.

Power-On Reset (POR), Power Brownout

The device contains a POR circuit with a threshold of 1.6V (typ) and a hysteresis of 0.025V (typ). POR ensures that the device resets all registers to default conditions as V_{DD} rises through the upper POR threshold. The default condition of all DAC registers is code zero with ground switches engaged, ensuring that no large output current transients damage the load during initial power-up.

In a V_{DD} brownout situation, V_{DD} must fall below the lower POR threshold before a POR is issued when V_{DD} rises again. As V_{DD} falls, the device eventually loses

regulation. However, the device is designed to avoid any large output current transients that could damage the load.

Software Reset and Standby Functions

The device contains a software reset function. The software reset function resets all code and configuration registers to default conditions. Write a 1 to the RST bit in the Software Reset Command register (0Fh) to initiate reset. The RST bit is not persistent, so writing a 0 to reset the bit is not required.

The device includes a software standby function that causes all DAC code registers (10h–1Bh) to be set to code zero. Write a 1 to the STDBY bit in the Software Reset Command register (0Fh) to initiate the standby function. STDBY bit is not persistent, so writing a 0 to reset the bit is not required.

The software standby function is a subset of the software reset function. The software reset function takes effect when both functions are issues.

Overtemperature Error Handling

The device features an on-chip temperature protection circuit to prevent the device from overheating when all DACs output the maximum programmed current. When the die temperature rises above the threshold temperature, +160°C, the PRO_TEMP bit in the Status/Revision Readback Command register (0Eh) is set and the device enters an overtemperature shutdown mode. All DACs are set to code zero, but the control interface remains active, thereby allowing the host processor to read back the device status. The PRO_TEMP bit is latched and, therefore, the device can only be reset by a software reset command, a software standby command, or by cycling the power.

The device features an overtemperature status bit, OVR_TEMP. The OVR_TEMP bit is not latched, and is set if the device temperature is above the protection threshold. The OVR_TEMP bit allows the host processor to determine if the device is too hot to reset. If a software reset is attempted while the device is above the protection threshold, the command is ignored. Similarly, above the threshold die temperature, the device immediately enters shutdown mode when power is cycled.

The device features a warning bit, HI_TEMP. The warning bit is not latched and serves as a high-temperature status indicator bit. The HI_TEMP bit is set when the die temperature is typically 10°C below the overtemperature protection threshold.

See the *Applications Information* section for more detail on calculating die temperature and heat-sinking requirements.

9-Channel, 14-Bit Current DAC with SPI Interface

User Configuration Registers

Table 2 shows a summary of the register map.

Table 2. User Register/Command Summary

| REGISTER ADDRESS (hex) | ACCESS | PAIRABLE | REGISTER NAME |
|---------------------------|--------|----------|------------------------------|
| 00h | W | Y | General Configuration |
| 01h | W | Y | DAC 1 Configuration |
| 02h | W | Y | DAC 2 Configuration |
| 03h | W | Y | DAC 3 Configuration |
| 04h | W | Y | DAC 4 Configuration |
| 05h | W | Y | DAC 5 Configuration |
| 06h | W | Y | DAC 6 Configuration |
| 07h | W | Y | DAC 7 Configuration |
| 08h | W | Y | DAC 8 Configuration |
| 09h | W | Y | DAC 9 Configuration |
| 0Ah | — | — | Reserved |
| 0Bh | — | — | Reserved |
| 0Ch | — | — | Reserved |
| 0Dh | — | — | Reserved |
| 0Eh | R | N | Status Feedback and Part ID |
| 0Fh | W | Y | Software Reset/Standby/Clear |
| 10h | W | Y | DAC 1–9 Code |
| 11h | W | Y | DAC 1 Code |
| 12h | W | Y | DAC 2 Code |
| 13h | W | Y | DAC 3 Code |
| 14h | W | Y | DAC 4 Code |
| 15h | W | Y | DAC 5 Code |
| 16h | W | Y | DAC 6 Source Mode Code |
| 17h | W | Y | DAC 7 Code |
| 18h | W | Y | DAC 8 Code |
| 19h | W | Y | DAC 9 Code |
| 1Ah | W | Y | DAC 6 Sink Mode Code |
| 1Bh | W | Y | DAC 6 Shutter Mode Code |
| 1Ch | — | — | Reserved |
| 1Dh | — | — | Reserved |
| 1Eh | — | — | Reserved |
| 1Fh | W | Y | DAC 6 Polarity Control |

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Register Details

00h: General Configuration Register

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|-----------|----|------|----|----|----|---|---|
| NAME | GSWG[1:0] | | BHEN | X | X | X | X | X |
| DEFAULT | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| NAME | X | X | X | X | X | X | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|-------|-----------|--|
| 15:14 | GSWG[1:0] | Global GSW Configuration Override 00: Individual DAC GSW settings are unaltered 01: Individual DAC GSW settings are set to 0 (ground switches disabled) 10: Individual DAC GSW settings are set to 1 (ground switches enabled) 11: Individual DAC GSW settings are unaltered |
| 13 | BHEN | DOUT Bus Hold Enable 0: Bus hold circuit is disabled 1: Bus hold circuit is enabled |
| 12:0 | X | Reserved |

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01h–09h: Individual DAC (1 to 9) Configuration Registers

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|-----|--------------|----|--------|-----|----------|---|---|
| NAME | GSW | CLR_CFG[1:0] | | T/H_EN | RNG | MUX[3:1] | | |
| DEFAULT | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|---|---|---|---|---|---|---|
| NAME | MUX0 | X | X | X | X | X | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|-------|--------------|---|
| 15 | GSW | Ground Switch Control 0: Output is left open when DAC code = 0000h 1: Output is connected to ground when DAC code = 0000h. For DACs 1 and 2, this setting applies to the active mux output. |
| 14:13 | CLR_CFG[1:0] | Clear Configuration Settings (determine how CLR pin affects each DAC) 00 (Ignore): The DAC is not affected by the CLR pin (default) 01 (Shutter): DAC output polarity is held negative (current level determined by 1Bh) as long as the CLR pin is asserted (level sensitive, applies to DAC 6 only; otherwise, implements the ignore function) 10 (Gate): DAC output is held at zero scale (with ground switches engaged if enabled) as long as the CLR pin is asserted (level sensitive) 11 (Reset): DAC output is set to zero scale (with ground switches engaged if enabled) when CLR is asserted and remains valid after CLR is removed (edge sensitive) |
| 12 | T/H_EN | Track and Hold Enable 0: Track and Hold disabled 1: Track and Hold enabled |
| 11 | RNG | Range (DAC 3, 8, and 9) 0: DAC full-scale output level is set to high range. 1: DAC full-scale output level is set to low range. Note: For all DACs not supporting RNG settings, this bit is reserved and should be set to 1 (default). |
| 10:7 | MUX[3:0] | Output Mux Settings for DAC (mux settings are only supported for DAC 1 and DAC 2) 0000: Output A active, all others high impedance 0001: Output B active, all others high impedance 0010: Output C active, all others high impedance 0011: Output D active, all others high impedance 01XX: All outputs high impedance (open) 1000: Output A active, all others shunted to GND 1001: Output B active, all others shunted to GND 1010: Output C active, all others shunted to GND 1011: Output D active, all others shunted to GND 11XX: All outputs shunted to GND (default) |
| 6:0 | X | Reserved |

Note: Any change to individual DAC configuration settings resets the affected DAC code to 0000h.

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0Eh: Status/Revision Readback Command Register

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|----------|----------|---------|----|--------------|----|---|---|
| NAME | PRO_TEMP | OVR_TEMP | HI_TEMP | X | PART_ID[3:0] | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---|---|---|---|---|---|---|
| NAME | REV_ID[3:0] | | | | X | X | X | X |
| DEFAULT | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|------|--------------|--|
| 15 | PRO_TEMP | Overtemperature Protection Indicator 0: Normal operation 1: Device overtemperature protection engaged |
| 14 | OVR_TEMP | Overtemperature Warning Indicator 0: Normal operation 1: Device temperature is too high (exceeding protection limit) |
| 13 | HI_TEMP | High-Temperature Warning Indicator 0: Normal operation 1: Device temperature is high (nearing protection limit) |
| 12 | X | Reserved |
| 11:8 | PART_ID[3:0] | Part ID Code (0001) |
| 7:4 | REV_ID[3:0] | Revision Code (0100) |
| 3:0 | X | Reserved |

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0Fh: Software Reset Command Register

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|-----|-------|--------|----|----|----|---|---|
| NAME | RST | STDBY | SW_CLR | X | X | X | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| NAME | X | X | X | X | X | X | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|------|--------|---|
| 15 | RST | Global Reset (identical to a POR) 0: No operation 1: Reset: All DAC modes, configurations, and codes are returned to their default settings <i>Not Persistent: The reset operation is contained within the command. It is not necessary to issue a second 0Fh command to remove the reset condition.</i> |
| 14 | STDBY | Global Standby (identical to a global power-down) 0: No operation 1: Standby: All DAC codes are set to zero, but retain all configuration information <i>Not Persistent: The standby operation is contained within the command. It is not necessary to issue a second 0Fh command to remove the standby condition.</i> <i>Exclusive: If RST and STDBY are requested, STDBY is not issued.</i> |
| 13 | SW_CLR | Software Clear 0: No operation/remove SW_CLR 1: Assert SW_CLR <i>Persistent: The status of SW_CLR remains in effect until changed by a later 0Fh command.</i> <i>Exclusive: If SW_CLR and RST and/or STDBY are requested, SW_CLR is not issued.</i> |
| 12:0 | X | Reserved |

Note: A software reset or standby command is required to exit overtemperature-protection mode once engaged (software clear does not qualify for an exit).

10h: Group DAC (1 to 9) Code Command Register

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|-----|-----|-----|-----|----|----|----|----|
| NAME | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|---|---|
| NAME | B5 | B4 | B3 | B2 | B1 | B0 | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|------|---------|---|
| 15:2 | B[13:0] | Group DAC Code Setting in Straight Binary Format. All DACs outputs update to code B[13:0] upon command completion. <i>This command is primarily useful for speeding up testing and qualification.</i> <i>Deglitching circuitry is not activated by group DAC code operations.</i> |
| 1:0 | X | Reserved |

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11h–1Bh: Individual DAC (1 to 9) Code Setting Registers

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|-----|-----|-----|-----|----|----|----|----|
| NAME | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|---|---|
| NAME | B5 | B4 | B3 | B2 | B1 | B0 | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|------|---------|--|
| 15:2 | B[13:0] | DAC Code Settings in Straight Binary Format 3FFFh = Full-scale output 0000h = Zero-scale output (GSW configuration settings apply) |
| 1:0 | X | Reserved |

Note: 11h–19h are DAC code settings for DACs 1–9, respectively. 1Ah is the sink mode setting for DAC 6. 1Bh is the shutter mode setting for DAC 6. See Table 2.

1Fh: DAC 6 Polarity Command Register

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|--------|----|----|----|----|----|---|---|
| NAME | SW_POL | X | X | X | X | X | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| NAME | X | X | X | X | X | X | X | X |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|------|--------|---|
| 15 | SW_POL | Software Polarity Control (to DAC 6 only) 0: Source-mode operation (0 to 300mA determined by 16h code, with GSW operation) 1: Sink-mode operation (0 to -60mA determined by 1Ah code, GSW operation disabled) |
| 14:0 | X | Reserved |

DAC 6 Polarity Operations

Software command 1Fh (SW_POL) or the CLR operation in shutter (01) mode controls the polarity of DAC 6. DAC 6 operates in a sink-current mode (0 to -60mA, determined by register 1Ah in sink mode) when SW_POL is set high. When the software command is used, the requested polarity is held in effect from the time when the 1Fh command requesting a polarity change is completed until a second 1Fh command requesting a polarity change operation is completed. When the shutter mode is used, DAC 6 remains in shutter mode as long as CLR is held high. The software- and CLR-driven polarity operations

are independently controlled and can be used individually or together without conflict. The device provides an internal logic-OR operation. Shutter allows the fast access to a programmable negative code, based on register 1Bh, from either a source or sink mode with a controlled return to the original operating state upon release.

Gate mode is activated by asserting the CLR or through the SW_CLR bit. If gate mode is activated while the DAC is set to sink mode, the DAC remains in sink mode, but the current is reduced to 0mA for the duration of the gating event.

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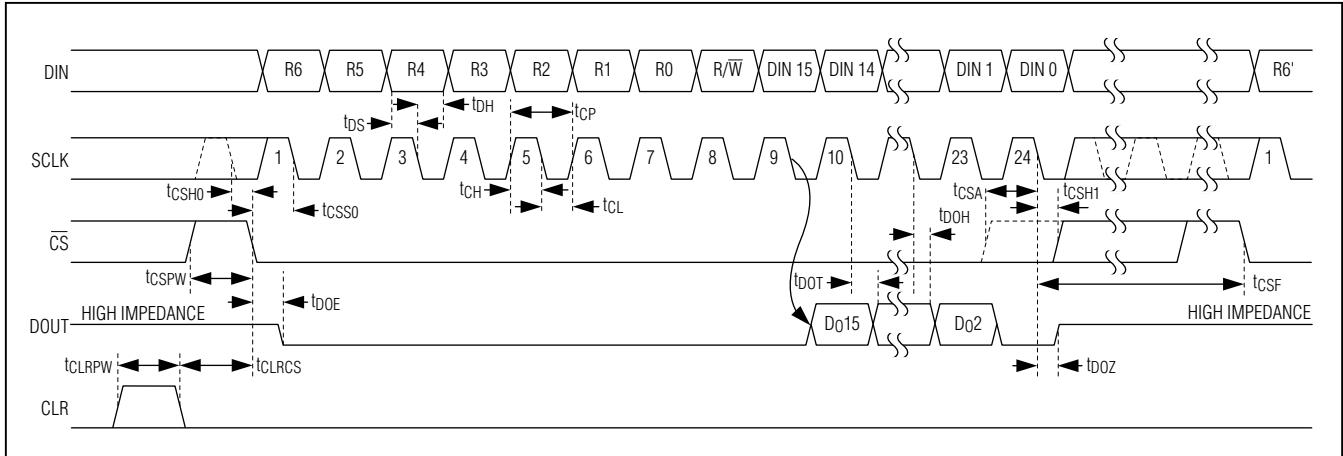


Figure 1. Minimum SPI Programming Operation

Table 3. SPI User Commands and Data Mapping with Clock Falling Edges (24-Bit Frame)

| EDGE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|------|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|--------|
| DIN | R6 | R5 | R4 | R3 | R2 | R1 | R0 | R/W | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DOUT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | 0 | High-Z |

Similarly, when reset mode is set, the DAC remains in sink mode, but the current is reduced to 0mA and remains there during and after the reset event. All source-, sink-, and shutter-mode current settings are reset to zero by this operation. Shutter mode is inaccessible while DAC 6 is configured for reset.

Regardless of polarity/shutter setting, DAC 6 continues to accept updated code settings for either source (16h), sink (1Ah), or shutter mode (1Bh) code registers, provided the DAC is not being held in any reset mode (through CLR or SW_CLR).

SPI Interface

The device features an SPI interface capable of clock speeds up to 25MHz. Figure 1 shows programming operation with 24 SCLK periods, which is the minimum for a valid frame.

For free-running SCLK applications, tCSH0 is shown with respect to the SCLK falling edge preceding the first SCLK falling edge (optional cycles shown in gray). To abort a command sequence, the rise of CS must precede the 24th falling edge of SCLK by tCSA.

Table 3 shows how the contents of the user-command data are mapped into the command registry. The device requires a 1-byte command, also referred to as a register address, R[6:0] paired with a R/W bit, followed by a 2-byte data word, D[15:0]. Set R/W to 0 for a write. Set R/W to 1 for a read. A full 24-bit SPI command sequence is required for all SPI command operations, regardless of the number of data bits actually used for the command. Any commands terminating with less than a full 24-bit sequence are aborted without affecting the operation of the device, subject to tCSA timing requirements. When a command sequence with more than 24 bits is provided, the command is executed on the 24th SCLK falling edge and the remainder of the command is ignored. In addition, the SPI interface elements are disabled to reduce transient current consumption.

All SPI commands cause the device to assume control of the DOUT line from the first SCLK edge through the 24th SCLK edge. Write-mode commands read out all zeros. After relinquishing the DOUT line, the device returns to a high-impedance mode. An optional bus hold circuit can be engaged to prevent leaving the DOUT line unbiased while not interfering with other devices on the bus. This is bit 13 in the General Configuration register (00h).

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CLR Interaction

The device's clear function allows the access of operation modes through a single input, CLR. Each DAC mode can be configured independently. The CLR input interacts with DAC code settings only. The CLR input does not interfere with configurations or readback operations. On-going SPI transfers continue uninterrupted when CLR is driven high. The effect of CLR being driven depends on the clear configurations of the individual DAC channel.

Code changes to any DAC channels configured in ignore (00), shutter (01), or gate (10) mode are recognized, regardless of the status of CLR. In shutter or gate mode, the DACs remain in the shutter or off positions for the duration of the CLR assertion. Once CLR is released, the DACs return to the most recently programmed output values.

Any DAC channels configured in reset (11) mode ignore code changes contained in the SPI commands during when CLR is or has been asserted. These channels do not recognize code-change commands until a subsequent \overline{CS} high condition is recognized, if the removal of the clear condition is observed at least t_{CLRCS} prior to the falling edge of \overline{CS} . In reset mode, the DAC code memories are reset to a zero code state and remain in that state until programmed by a subsequent command.

Applications Information

Thermal Design

To reduce thermal resistance, include V_{DD} and ground planes in the application PCB. Connect the TQFN exposed pad to the ground plane through a large via. Connect the multiple V_{DD} inputs to the V_{DD} plane through multiple vias and bypass each V_{DD} pin with a separate 0.1 μ F capacitor as close as possible to the supply pin. Connect AGND and DGND to the ground plane.

Noise Immunity

Each V_{DD} pin should be bypassed with a separate 0.1 μ F capacitor as close as possible to the supply pin. Pay particular attention to the ESR value of the capacitors and add a 100pF capacitor in parallel to each 100nF capacitor. Noise is particularly important in fiber applications; thus, it may be necessary to add 100pF capacitors to decouple the optional electrodes to ground. This ensures that any crosstalk between the interface and the DAC outputs caused by PCB parasitic is minimized.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|--|
| 36 WLP | W363A3+1 | 21-0024 | Refer to Application Note 1891 |
| 32 TQFN-EP | T3255+4 | 21-0140 | 90-0012 |

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Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0 | 7/12 | Initial release | — |
| 1 | 9/12 | Released the WLP package and revised the <i>Electrical Characteristics</i> , Table 1, and the <i>01h–09h: Individual DAC (1 to 9) Configuration Registers</i> table. | 1, 2, 17, 21 |
| 2 | 5/13 | Updated Note 3 in the <i>Electrical Characteristics</i> and revised the <i>DAC Outputs</i> section. | 6, 17 |



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