

AD574A—SPECIFICATIONS (@ +25°C with $V_{CC} = +15\text{ V}$ or $+12\text{ V}$, $V_{LOGIC} = +5\text{ V}$, $V_{EE} = -15\text{ V}$ or -12 V unless otherwise noted)

| Model | AD574AJ | | | AD574AK | | | AD574AL | | | Units |
|--|---------|----------|---------|---------|----------|---------|---------|----------|---------|--------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | | 12 | | | 12 | | | 12 | Bits |
| LINEARITY ERROR @ +25°C | | | ±1 | | | ±1/2 | | | ±1/2 | LSB |
| T_{MIN} to T_{MAX} | | | ±1 | | | ±1/2 | | | ±1/2 | LSB |
| DIFFERENTIAL LINEARITY ERROR (Minimum Resolution for Which No Missing Codes are Guaranteed) T_{MIN} to T_{MAX} | 11 | | | 12 | | | 12 | | | Bits |
| UNIPOLAR OFFSET (Adjustable to Zero) | | | ±2 | | | ±1 | | | ±1 | LSB |
| BIPOLAR OFFSET (Adjustable to Zero) | | | ±4 | | | ±4 | | | ±2 | LSB |
| FULL-SCALE CALIBRATION ERROR (With Fixed 50 Ω Resistor from REF OUT to REF IN) (Adjustable to Zero) | | | 0.25 | | | 0.25 | | | 0.125 | % of FS |
| TEMPERATURE RANGE | 0 | | +70 | 0 | | +70 | 0 | | +70 | °C |
| TEMPERATURE COEFFICIENTS (Using Internal Reference) T_{MIN} to T_{MAX} | | | | | | | | | | |
| Unipolar Offset | | | ±2 (10) | | | ±1 (5) | | | ±1 (5) | LSB (ppm/°C) |
| Bipolar Offset | | | ±2 (10) | | | ±1 (5) | | | ±1 (5) | LSB (ppm/°C) |
| Full-Scale Calibration | | | ±9 (50) | | | ±5 (27) | | | ±2 (10) | LSB (ppm/°C) |
| POWER SUPPLY REJECTION Max Change in Full-Scale Calibration | | | | | | | | | | |
| $V_{CC} = 15\text{ V} \pm 1.5\text{ V}$ or $12\text{ V} \pm 0.6\text{ V}$ | | | ±2 | | | ±1 | | | ±1 | LSB |
| $V_{LOGIC} = 5\text{ V} \pm 0.5\text{ V}$ | | | ±1/2 | | | ±1/2 | | | ±1/2 | LSB |
| $V_{EE} = -15\text{ V} \pm 1.5\text{ V}$ or $-12\text{ V} \pm 0.6\text{ V}$ | | | ±2 | | | ±1 | | | ±1 | LSB |
| ANALOG INPUT | | | | | | | | | | |
| Input Ranges | | | | | | | | | | |
| Bipolar | -5 | | +5 | -5 | | +5 | -5 | | +5 | Volts |
| | -10 | | +10 | -10 | | +10 | -10 | | +10 | Volts |
| Unipolar | 0 | | +10 | 0 | | +10 | 0 | | +10 | Volts |
| | 0 | | +20 | 0 | | +20 | 0 | | +20 | Volts |
| Input Impedance | | | | | | | | | | |
| 10 Volt Span | 3 | 5 | 7 | 3 | 5 | 7 | 3 | 5 | 7 | kΩ |
| 20 Volt Span | 6 | 10 | 14 | 6 | 10 | 14 | 6 | 10 | 14 | kΩ |
| DIGITAL CHARACTERISTICS ¹ (T_{MIN} - T_{MAX}) | | | | | | | | | | |
| Inputs ² (CE, \overline{CS} , R/ \overline{C} , A ₀) | | | | | | | | | | |
| Logic "1" Voltage | +2.0 | | +5.5 | +2.0 | | +5.5 | +2.0 | | +5.5 | Volts |
| Logic "0" Voltage | -0.5 | | +0.8 | -0.5 | | +0.8 | -0.5 | | +0.8 | Volts |
| Current | -20 | | +20 | -20 | | +20 | -20 | | +20 | μA |
| Capacitance | | 5 | | | 5 | | | 5 | | pF |
| Output (DB11-DB0, STS) | | | | | | | | | | |
| Logic "1" Voltage ($I_{SOURCE} \leq 500\text{ μA}$) | +2.4 | | | +2.4 | | | +2.4 | | | Volts |
| Logic "0" Voltage ($I_{SINK} \leq 1.6\text{ mA}$) | | | +0.4 | | | +0.4 | | | +0.4 | Volts |
| Leakage (DB11-DB0, High-Z State) | -20 | | +20 | -20 | | +20 | -20 | | +20 | μA |
| Capacitance | | 5 | | | 5 | | | 5 | | pF |
| POWER SUPPLIES | | | | | | | | | | |
| Operating Range | | | | | | | | | | |
| V_{LOGIC} | +4.5 | | +5.5 | +4.5 | | +5.5 | +4.5 | | +5.5 | Volts |
| V_{CC} | +11.4 | | +16.5 | +11.4 | | +16.5 | +11.4 | | +16.5 | Volts |
| V_{EE} | -11.4 | | -16.5 | -11.4 | | -16.5 | -11.4 | | -16.5 | Volts |
| Operating Current | | | | | | | | | | |
| I_{LOGIC} | | 30 | 40 | | 30 | 40 | | 30 | 40 | mA |
| I_{CC} | | 2 | 5 | | 2 | 5 | | 2 | 5 | mA |
| I_{EE} | | 18 | 30 | | 18 | 30 | | 18 | 30 | mA |
| POWER DISSIPATION | | 390 | 725 | | 390 | 725 | | 390 | 725 | mW |
| INTERNAL REFERENCE VOLTAGE | | | | | | | | | | |
| Output Current (Available for External Loads) ³ (External Load Should not Change During Conversion) | 9.98 | 10.0 | 10.02 | 9.98 | 10.0 | 10.02 | 9.99 | 10.0 | 10.01 | Volts |
| | | | 1.5 | | | 1.5 | | | 1.5 | mA |
| PACKAGE OPTIONS ⁴ | | | | | | | | | | |
| Ceramic (D-28) | | AD574ASD | | | AD574AKD | | | AD574ALD | | |
| Plastic (N-28) | | AD574AJN | | | AD574AKN | | | AD574ALN | | |
| PLCC (P-28A) | | AD574AJP | | | AD574AKP | | | | | |
| LCC (E-28A) | | AD574AJE | | | AD574AKE | | | | | |

NOTES

¹Detailed Timing Specifications appear in the Timing Section.

²12/8 Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.

³The reference should be buffered for operation on $\pm 12\text{ V}$ supplies.

⁴D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier.

Specifications subject to change without notice.

| Model | AD574AS | | | AD574AT | | | AD574AU | | | Units |
|---|---------|----------|----------|---------|----------|----------|---------|----------|-----------|--------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | | 12 | | | 12 | | | 12 | Bits |
| LINEARITY ERROR @ +25°C | | | ±1 | | | ±1/2 | | | ±1/2 | LSB |
| T_{MIN} to T_{MAX} | | | ±1 | | | ±1 | | | ±1 | LSB |
| DIFFERENTIAL LINEARITY ERROR (Minimum Resolution for Which No Missing Codes are Guaranteed) T_{MIN} to T_{MAX} | 11 | | | 12 | | | 12 | | | Bits |
| UNIPOLAR OFFSET (Adjustable to Zero) | | | ±2 | | | ±1 | | | ±1 | LSB |
| BIPOLAR OFFSET (Adjustable to Zero) | | | ±4 | | | ±4 | | | ±2 | LSB |
| FULL-SCALE CALIBRATION ERROR (With Fixed 50 Ω Resistor from REF OUT to REF IN) (Adjustable to Zero) | | | 0.25 | | | 0.25 | | | 0.125 | % of FS |
| TEMPERATURE RANGE | -55 | | +125 | -55 | | +125 | -55 | | +125 | °C |
| TEMPERATURE COEFFICIENTS (Using Internal Reference) (T_{MIN} to T_{MAX}) | | | | | | | | | | |
| Unipolar Offset | | | ±2 (5) | | | ±1 (2.5) | | | ±1 (2.5) | LSB (ppm/°C) |
| Bipolar Offset | | | ±4 (10) | | | ±2 (5) | | | ±1 (2.5) | LSB (ppm/°C) |
| Full-Scale Calibration | | | ±20 (50) | | | ±10 (25) | | | ±5 (12.5) | LSB (ppm/°C) |
| POWER SUPPLY REJECTION Max Change in Full-Scale Calibration | | | | | | | | | | |
| $V_{CC} = 15\text{ V} \pm 1.5\text{ V}$ or $12\text{ V} \pm 0.6\text{ V}$ | | | ±2 | | | ±1 | | | ±1 | LSB |
| $V_{LOGIC} = 5\text{ V} \pm 0.5\text{ V}$ | | | ±1/2 | | | ±1/2 | | | ±1/2 | LSB |
| $V_{EE} = -15\text{ V} \pm 1.5\text{ V}$ or $-12\text{ V} \pm 0.6\text{ V}$ | | | ±2 | | | ±1 | | | ±1 | LSB |
| ANALOG INPUT | | | | | | | | | | |
| Input Ranges | | | | | | | | | | |
| Bipolar | -5 | | +5 | -5 | | +5 | -5 | | +5 | Volts |
| | -10 | | +10 | -10 | | +10 | -10 | | +10 | Volts |
| Unipolar | 0 | | +10 | 0 | | +10 | 0 | | +10 | Volts |
| | 0 | | +20 | 0 | | +20 | 0 | | +20 | Volts |
| Input Impedance | | | | | | | | | | |
| 10 Volt Span | 3 | 5 | 7 | 3 | 5 | 7 | 3 | 5 | 7 | kΩ |
| 20 Volt Span | 6 | 10 | 14 | 6 | 10 | 14 | 6 | 10 | 14 | kΩ |
| DIGITAL CHARACTERISTICS ¹ (T_{MIN} - T_{MAX}) | | | | | | | | | | |
| Inputs ² (CE, \overline{CS} , R/ \overline{C} , A ₀) | | | | | | | | | | |
| Logic "1" Voltage | +2.0 | | +5.5 | +2.0 | | +5.5 | +2.0 | | +5.5 | Volts |
| Logic "0" Voltage | -0.5 | | +0.8 | -0.5 | | +0.8 | -0.5 | | +0.8 | Volts |
| Current | -20 | | +20 | -20 | | +20 | -20 | | +20 | μA |
| Capacitance | | 5 | | | 5 | | | 5 | | pF |
| Output (DB11-DB0, STS) | | | | | | | | | | |
| Logic "1" Voltage ($I_{SOURCE} \leq 500\text{ μA}$) | +2.4 | | | +2.4 | | | +2.4 | | | Volts |
| Logic "0" Voltage ($I_{SINK} \leq 1.6\text{ mA}$) | | | +0.4 | | | +0.4 | | | +0.4 | Volts |
| Leakage (DB11-DB0, High-Z State) | -20 | | +20 | -20 | | +20 | -20 | | +20 | μA |
| Capacitance | | 5 | | | 5 | | | 5 | | pF |
| POWER SUPPLIES | | | | | | | | | | |
| Operating Range | | | | | | | | | | |
| V_{LOGIC} | +4.5 | | +5.5 | +4.5 | | +5.5 | +4.5 | | +5.5 | Volts |
| V_{CC} | +11.4 | | +16.5 | +11.4 | | +16.5 | +11.4 | | +16.5 | Volts |
| V_{EE} | -11.4 | | -16.5 | -11.4 | | -16.5 | -11.4 | | -16.5 | Volts |
| Operating Current | | | | | | | | | | |
| I_{LOGIC} | | 30 | 40 | | 30 | 40 | | 30 | 40 | mA |
| I_{CC} | | 2 | 5 | | 2 | 5 | | 2 | 5 | mA |
| I_{EE} | | 18 | 30 | | 18 | 30 | | 18 | 30 | mA |
| POWER DISSIPATION | | 390 | 725 | | 390 | 725 | | 390 | 725 | mW |
| INTERNAL REFERENCE VOLTAGE Output Current (Available for External Loads) ³ (External Load Should not Change During Conversion) | 9.98 | 10.0 | 10.02 | 9.98 | 10.0 | 10.02 | 9.99 | 10.0 | 10.01 | Volts mA |
| 1.5 | | | 1.5 | | | 1.5 | | | 1.5 | |
| PACKAGE OPTION ⁴ | | | | | | | | | | |
| Ceramic (D-28) | | AD574ASD | | | AD574ATD | | | AD574AUD | | |

NOTES

¹Detailed Timing Specifications appear in the Timing Section.²12/8 Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.³The reference should be buffered for operation on ±12 V supplies.⁴D = Ceramic DIP.

Specifications subject to change without notice.

THE AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from “zero” through “full scale”. The point used as “zero” occurs 1/2 LSB (1.22 mV for 10 volt span) before the first code transition (all zeros to only the LSB “on”). “Full scale” is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574AK, L, T, and U grades are guaranteed for maximum nonlinearity of $\pm 1/2$ LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574AJ and S grades are guaranteed to ± 1 LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm 1/2$ LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of

full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

FULL-SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05% to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX} .

POWER SUPPLY REJECTION

The standard specifications for the AD574A assume use of +5.00 V and ± 15.00 V or ± 12.00 V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44 mV out of 10 volts for a 12-bit ADC.

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CIRCUIT OPERATION

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574A is shown in Figure 1.

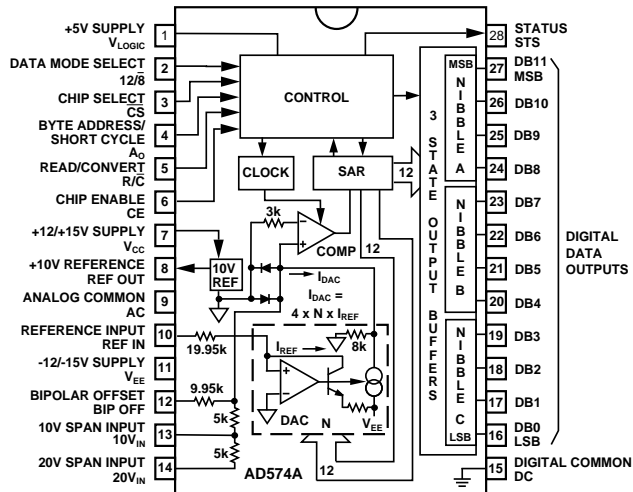


Figure 1. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or restarted and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most significant bit (MSB) to least significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5 k Ω (or 10 k Ω) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within $\pm 1/2$ LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts $\pm 0.2\%$; it can supply up to 1.5 mA to an external load in addition to the requirements of the reference input resistor (0.5 mA) and bipolar offset resistor (1 mA) when the AD574A is powered from ± 15 V supplies. If the AD574A is used with ± 12 V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin-film application resistors are trimmed to match the full-scale output current of the DAC. There are two 5 k Ω input scaling resistors to allow either a 10 volt or 20 volt span. The 10 k Ω bipolar offset resistor is grounded for unipolar operation and connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574 ANALOG INPUT

The internal circuitry of the AD574 dictates that its analog input be driven by a low source impedance. Voltage changes at the current summing node of the internal comparator result in abrupt modulations of the current at the analog input. For accurate 12-bit conversions the driving source must be capable of holding a constant output voltage under these dynamically changing load conditions.

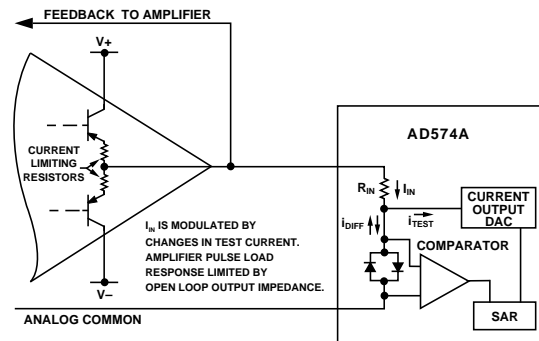


Figure 2. Op Amp - AD574A Interface

The output impedance of an op amp has an open-loop value which, in a closed loop, is divided by the loop gain available at the frequency of interest. The amplifier should have acceptable loop gain at 500 kHz for use with the AD574A. To check whether the output properties of a signal source are suitable, monitor the AD574's input with an oscilloscope while a conversion is in progress. Each of the 12 disturbances should subside in 1 μ s or less.

For applications involving the use of a sample-and-hold amplifier, the AD585 is recommended. The AD711 or AD544 op amps are recommended for dc applications.

SAMPLE-AND-HOLD AMPLIFIERS

Although the conversion time of the AD574A is a maximum of 35 μ s, to achieve accurate 12-bit conversions of frequencies greater than a few Hz requires the use of a sample-and-hold amplifier (SHA). If the voltage of the analog input signal driving the AD574A changes by more than 1/2 LSB over the time interval needed to make a conversion, then the input requires a SHA.

The AD585 is a high linearity SHA capable of directly driving the analog input of the AD574A. The AD585's fast acquisition time, low aperture and low aperture jitter are ideally suited for high-speed data acquisition systems. Consider the AD574A converter with a 35 μ s conversion time and an input signal of 10 V p-p: the maximum frequency which may be applied to achieve rated accuracy is 1.5 Hz. However, with the addition of an AD585, as shown in Figure 3, the maximum frequency increases to 26 kHz.

The AD585's low output impedance, fast-loop response, and low droop maintain 12-bits of accuracy under the changing load conditions that occur during a conversion, making it suitable for use in high accuracy conversion systems. Many other SHAs cannot achieve 12-bits of accuracy and can thus compromise a system. The AD585 is recommended for AD574A applications requiring a sample and hold.

An alternate approach is to use the AD1674, which combines the ADC and SHA on one chip, with a total throughput time of 10 μ s.

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The full-scale trim is done by applying a signal 1/2 LSB below the nominal full scale (9.9963 for a 10 V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50 Ω ± 1% fixed resistor. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale (-4.9988 V for the ±5 V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1/2 LSB below positive full scale (+4.9963 V the ±5 V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).



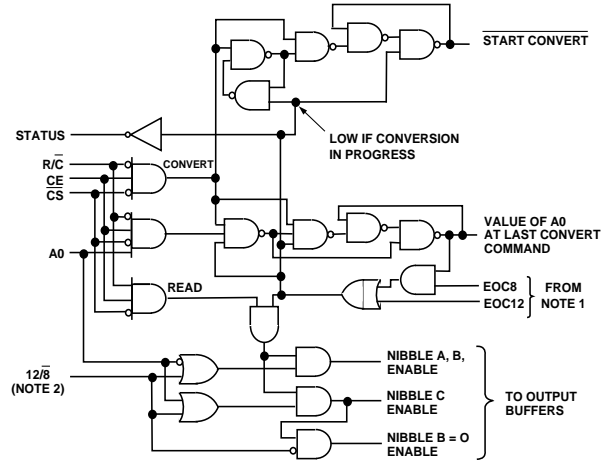
Figure 5. Bipolar Input Connections

CONTROL LOGIC

The AD574A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 6 shows the internal logic circuitry of the AD574A.

The control signals CE, \overline{CS} , and $\overline{R/C}$ control the operation of the converter. The state of $\overline{R/C}$ when CE and \overline{CS} are both asserted determines whether a data read ($\overline{R/C} = 1$) or a convert ($\overline{R/C} = 0$) is in progress. The register control inputs A_0 and $12/\overline{8}$ control conversion length and data format. The A_0 line is usually tied to the least significant bit of the address bus. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result ($A_0 = 0$) or the 4 LSBs ($A_0 = 1$) are enabled. The $12/\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words ($12/\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word ($12/\overline{8}$ tied to V_{LOGIC}). The $12/\overline{8}$ pin is not TTL-compatible and must be hard-wired to either V_{LOGIC} or DIGITAL COMMON. In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

It is not recommended that A_0 change state during a data read operation. Asymmetrical enable and disable times of the three-state buffers could cause internal bus contention resulting in potential damage to the AD574A.



NOTE 1: WHEN START CONVERT GOES LOW, THE EOC (END OF CONVERSION) SIGNALS GO LOW. EOC8 RETURNS HIGH AFTER AN 8-BIT CONVERSION CYCLE IS COMPLETE, AND EOC12 RETURNS HIGH WHEN ALL 12-BITS HAVE BEEN CONVERTED. THE EOC SIGNALS PREVENT DATA FROM BEING READ DURING CONVERSIONS.

NOTE 2: $12/\overline{8}$ IS NOT A TTL-COMPATIBLE INPUT AND SHOULD ALWAYS BE WIRED DIRECTLY TO V_{LOGIC} OR DIGITAL COMMON.

Figure 6. AD574A Control Logic

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

Table I. AD574A Truth Table

| CE | \overline{CS} | $\overline{R/C}$ | $12/\overline{8}$ | A_0 | Operation |
|----|-----------------|------------------|-------------------|-------|-----------------------------------|
| 0 | X | X | X | X | None |
| X | 1 | X | X | X | None |
| 1 | 0 | 0 | X | 0 | Initiate 12-Bit Conversion |
| 1 | 0 | 0 | X | 1 | Initiate 8-Bit Conversion |
| 1 | 0 | 1 | Pin 1 | X | Enable 12-Bit Parallel Output |
| 1 | 0 | 1 | Pin 15 | 0 | Enable 8 Most Significant Bits |
| 1 | 0 | 1 | Pin 15 | 1 | Enable 4 LSBs + 4 Trailing Zeroes |

TIMING

The AD574A is easily interfaced to a wide variety of microprocessors and other digital systems. The following discussion of the timing requirements of the AD574A control signals should provide the system designer with useful insight into the operation of the device.

Table II. Convert Start Timing—Full Control Mode

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|-------------------------------------|-----|-----|-----|-------|
| t_{DSC} | STS Delay from CE | | | 400 | ns |
| t_{HEC} | CE Pulse Width | 300 | | | ns |
| t_{SSC} | \overline{CS} to CE Setup | 300 | | | ns |
| t_{HSC} | \overline{CS} Low During CE High | 200 | | | ns |
| t_{SRC} | $\overline{R/C}$ to CE Setup | 250 | | | ns |
| t_{HRC} | $\overline{R/C}$ Low During CE High | 200 | | | ns |
| t_{SAC} | A_0 to CE Setup | 0 | | | ns |
| t_{HAC} | A_0 Valid During CE High | 300 | | | ns |
| t_C | Conversion Time | | | | |
| | 8-Bit Cycle | 10 | | 24 | μs |
| | 12-Bit Cycle | 15 | | 35 | μs |

Figure 7 shows a complete timing diagram for the AD574A $\overline{\text{convert}}$ start operation. $\overline{\text{R}/\overline{\text{C}}}$ should be low before both CE and $\overline{\text{CS}}$ are asserted; if $\overline{\text{R}/\overline{\text{C}}}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention. Either CE or $\overline{\text{CS}}$ may be used to initiate a conversion; however, use of CE is recommended since it includes one less propagation delay than $\overline{\text{CS}}$ and is the faster input. In Figure 7, CE is used to initiate the conversion.

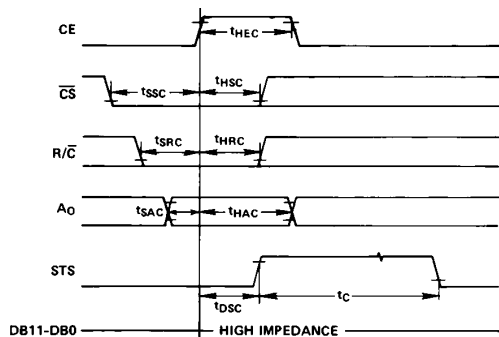


Figure 7. Convert Start Timing

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffers cannot be enabled during conversion.

Figure 8 shows the timing for data read operations. During data read operations, access time is measured from the point where CE and $\overline{\text{R}/\overline{\text{C}}}$ both are high (assuming $\overline{\text{CS}}$ is already low). If $\overline{\text{CS}}$ is used to enable the device, access time is extended by 100 ns.

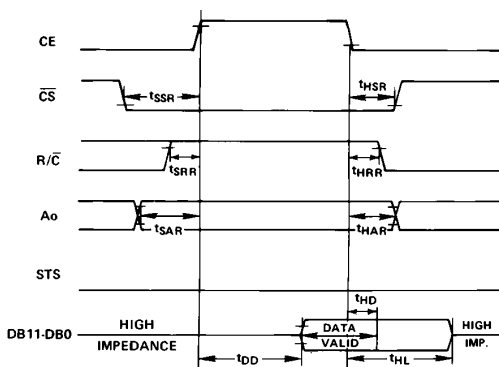


Figure 8. Read Cycle Timing

In the 8-bit bus interface mode ($12/\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_0 , must be stable at least 150 ns prior to $\overline{\text{CE}}$ going high and must remain stable during the entire read cycle. If A_0 is allowed to change, damage to the AD574A output buffers may result.

Table III. Read Timing—Full Control Mode

| Symbol | Parameter | Min | Typ | Max | Units |
|------------|---|-----|-----|-----|-------|
| t_{DD}^1 | Access Time (from CE) | | | 200 | ns |
| t_{HD} | Data Valid After CE Low | 25 | | | ns |
| t_{HL}^2 | Output Float Delay | | | 100 | ns |
| t_{SSR} | $\overline{\text{CS}}$ to CE Setup | 150 | | | ns |
| t_{SRR} | $\overline{\text{R}/\overline{\text{C}}}$ to CE Setup | 0 | | | ns |
| t_{SAR} | A_0 to CE Setup | 150 | | | ns |
| t_{HSR} | $\overline{\text{CS}}$ Valid After CE Low | 50 | | | ns |
| t_{HRR} | $\overline{\text{R}/\overline{\text{C}}}$ High After CE Low | 0 | | | ns |
| t_{HAR} | A_0 Valid After CE Low | 50 | | | ns |

NOTES

¹ t_{DD} is measured with the load circuit of Figure 9 and defined as the time required for an output to cross 0.4 V or 2.4 V.

² t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 10.



a. High-Z to Logic 1 b. High-Z to Logic 0
Figure 9. Load Circuit for Access Time Test



a. Logic 1 to High-Z b. Logic 0 to High-Z
Figure 10. Load Circuit for Output Float Delay Test

“STAND-ALONE” OPERATION

The AD574A can be used in a “stand-alone” mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and $12/\overline{8}$ are wired high, $\overline{\text{CS}}$ and A_0 are wired low, and conversion is controlled by $\overline{\text{R}/\overline{\text{C}}}$. The three-state buffers are enabled when $\overline{\text{R}/\overline{\text{C}}}$ is high and a conversion starts when $\overline{\text{R}/\overline{\text{C}}}$ goes low. This allows two possible control signals—a high pulse or a low pulse. Operation with a low pulse is shown in Figure 11. In this case, the outputs are forced into the high impedance state in response to the falling edge of $\overline{\text{R}/\overline{\text{C}}}$ and return



Figure 11. Low Pulse for $\overline{\text{R}/\overline{\text{C}}}$ —Outputs Enabled After Conversion

AD574A

to valid logic levels after the conversion cycle is completed. The STS line goes high 600 ns after R/C goes low and returns low 300 ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 12, the data lines are enabled during the time when R/C is high. The falling edge of R/C starts the next conversion, and the data lines return to three-state (and remain three-state) until the next high pulse of R/C.



Figure 12. High Pulse for R/C—Outputs Enabled While R/C High, Otherwise High-Z

Table IV. Stand-Alone Mode Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|------------------|----------------------------|-----|------|-----|-------|
| t _{HRL} | Low R/C Pulse Width | 250 | | | ns |
| t _{DS} | STS Delay from R/C | | 600 | | ns |
| t _{HDR} | Data Valid After R/C Low | 25 | | | ns |
| t _{HL} | Output Float Delay | | 150 | | ns |
| t _{HS} | STS Delay After Data Valid | 300 | 1000 | | ns |
| t _{HRH} | High R/C Pulse Width | 300 | | | ns |
| t _{DDR} | Data Access Time | | 250 | | ns |

Usually the low pulse for R/C stand-alone mode will be used. Figure 13 illustrates a typical stand-alone configuration for 8086 type processors. The addition of the 74F/S374 latches improves bus access/release times and helps minimize digital feedthrough to the analog portion of the converter.



Figure 13. 8086 Stand-Alone Configuration

INTERFACING THE AD574A TO MICROPROCESSORS

The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD574A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD574A is only 35 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 35 microseconds to convert, and insert a sufficient number of "do-nothing" instructions to ensure that 35 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD574A includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by connection of the 12/8 input. In 16-bit bus applications (12/8 high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/8 low) is done in a left-justified format. The even address (A0 low) contains the 8 MSBs (DB11 through DB4). The odd address (A0 high) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the AD574A data lines for right justified 8-bit bus interface.

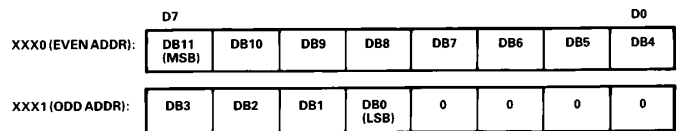


Figure 14. AD574A Data Format for 8-Bit Bus

SPECIFIC PROCESSOR INTERFACE EXAMPLES

Z-80 System Interface

The AD574A may be interfaced to the Z-80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O or mapped configuration. The Z-80 uses address lines A0-A7 to decode the I/O port address.

An interesting feature of the Z-80 is that during I/O operations a single wait state is automatically inserted, allowing the AD574A to be used with Z-80 processors having clock speeds up to 4 MHz. For applications faster than 4 MHz use the wait state generator in Figure 16. In a memory mapped configuration the AD574A may be interfaced to Z-80 processors with clock speeds of up to 2.5 MHz.



Figure 15. Z80—AD574A Interface



Figure 16. Wait State Generator

IBM PC Interface

The AD574A appears in Figure 17 interfaced to the 4 MHz 8088 processor of an IBM PC. Since the device resides in I/O space, its address is decoded from only the lower ten address lines and must be gated with AEN (active low) to mask out internal DMA cycles which use the same I/O address space. This active low signal is applied to CS. IOR and IOW are used to initiate the conversion and read, and are gated together to drive the chip enable, CE. Because the data bus width is limited to 8 bits, the AD574A data resides in two adjacent addresses selected by A0.



Figure 17. IBM PC—AD574A Interface

Note: Due to the large number of options that may be installed in the PC, the I/O bus loading should be limited to one Schottky TTL load. Therefore, a buffer/driver should be used when interfacing more than two AD574As to the I/O bus.

8086 Interface

The data mode select pin (12/8) of the AD574A should be connected to V_{LOGIC} to provide a 12-bit data output. To prevent possible bus contention, a demultiplexed and buffered address/data bus is recommended. In the cases where the 8-bit short conversion cycle is not used, A0 should be tied to digital common. Figure 18 shows a typical 8086 configuration.



Figure 18. 8086—AD574A with Buffered Bus Interface

For clock speeds greater than 4 MHz wait state insertion similar to Figure 16 is recommended to ensure sufficient CE and R/C pulse duration.

The AD574A can also be interfaced in a stand-alone mode (see Figure 13). A low going pulse derived from the 8086's WR signal logically ORed with a low address decode starts the conversion. At the end of the conversion, STS clocks the data into the three-state latches.

68000 Interface

The AD574, when configured in the stand-alone mode, will easily interface to the 4 MHz version of the 68000 microprocessor. The 68000 R/W signal combined with a low address decode initiates conversion. The UDS or LDS signal, with the decoded address, generates the DTACK input to the processor, latching in the AD574A's data. Figure 19 illustrates this configuration.

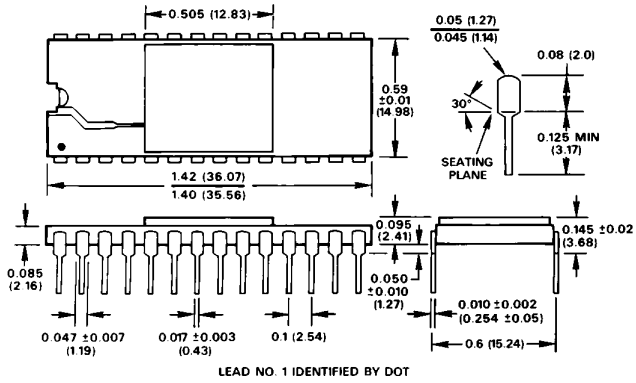


Figure 19. 68000—AD574A Interface

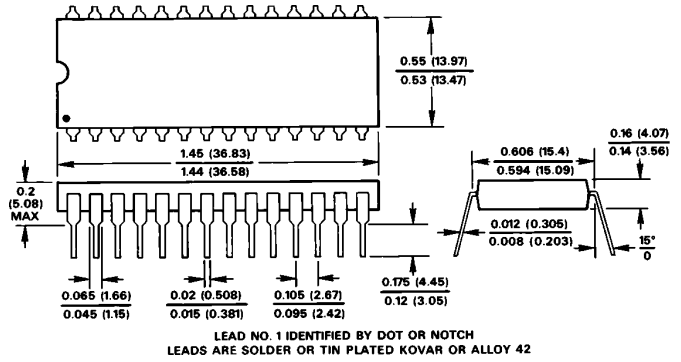
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

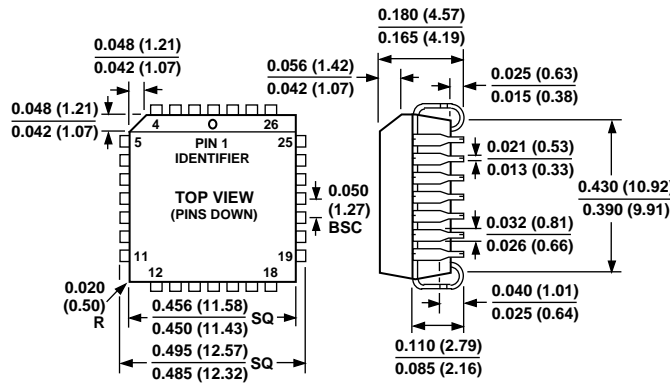
28-Pin Ceramic DIP Package (D-28)



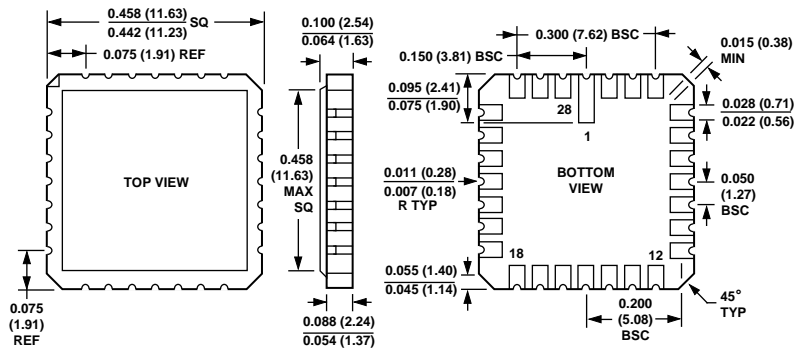
28-Lead Plastic DIP Package (N-28A)



28-Terminal PLCC Package (P-28A)



28-Terminal LCC Package (E-28A)



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