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## MM74HC273 Octal D-Type Flip-Flops with Clear

### General Description

The MM74HC273 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC273 is functionally as well as pin compatible to the 74LS273. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

### Features

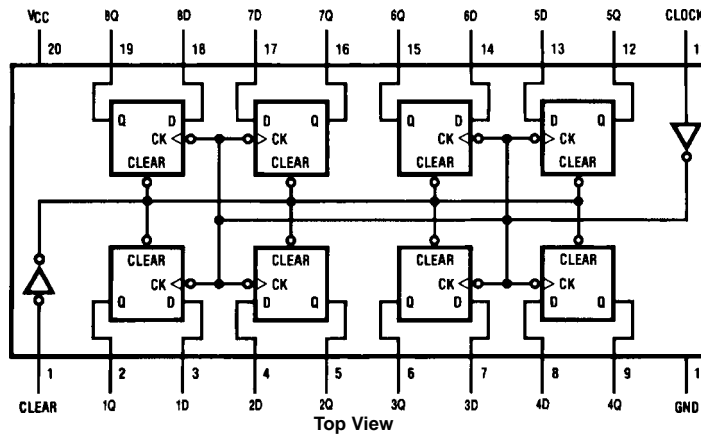
- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1  $\mu$ A maximum
- Low quiescent current: 80  $\mu$ A (74 Series)
- Output drive: 10 LS-TTL loads

### Ordering Code:

Order Number	Package Number	Package Description
MM74HC273WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC273N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



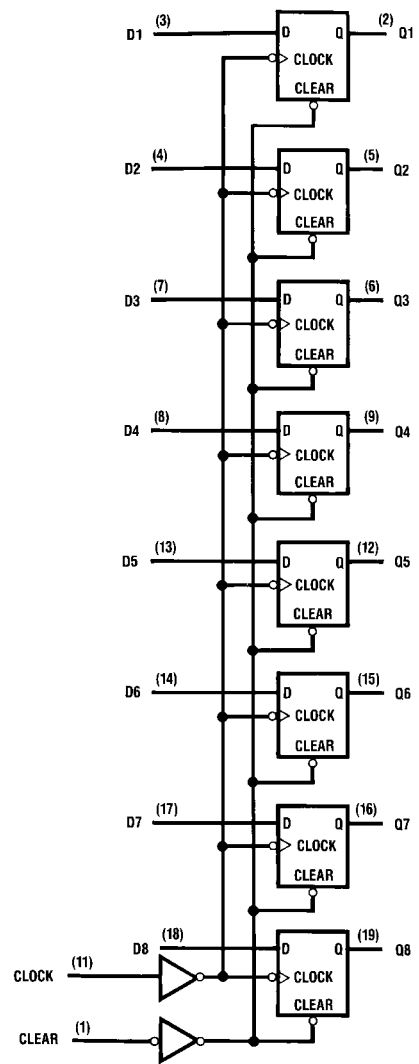
### Truth Table

(Each Flip-Flop)

Clear	Inputs		D	Outputs
	Clear	Clock		Q
L	X	X	X	L
H	↑	H	H	H
H	↑	L	L	L
H	L	X	X	Q <sub>0</sub>

H = HIGH Level (Steady State)  
 L = LOW Level (Steady State)  
 X = Don't Care  
 ↑ = Transition from LOW-to-HIGH level  
 Q<sub>0</sub> = The level of Q before the indicated steady state input conditions were established

### Logic Diagram



<b>Absolute Maximum Ratings</b> <sup>(Note 1)</sup>		<b>Recommended Operating Conditions</b>						
<sup>(Note 2)</sup>		Min	Max	Units				
Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V	2	6	V				
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$							
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$							
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA	0	$V_{CC}$	V				
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA							
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA							
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C							
Power Dissipation ( $P_D$ )	<sup>(Note 3)</sup> 600 mW	Operating Temperature Range ( $T_A$ )		°C				
S.O. Package only	500 mW							
Lead Temperature ( $T_L$ )	260°C	Input Rise or Fall Times						
<sup>(Soldering 10 seconds)</sup>								
		$(t_r, t_f) V_{CC} = 2.0V$	1000	ns				
		$V_{CC} = 4.5V$	500	ns				
		$V_{CC} = 6.0V$	400	ns				
<b>Note 1:</b> Absolute Maximum Ratings are those values beyond which damage to the device may occur.								
<b>Note 2:</b> Unless otherwise specified all voltages are referenced to ground.								
<b>Note 3:</b> Power Dissipation temperature derating — plastic "N" package: - 12 mW/°C from 65°C to 85°C.								
<b>DC Electrical Characteristics</b> <sup>(Note 4)</sup>								
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8	80	160	$\mu A$
<b>Note 4:</b> For a power supply of 5V $\pm 10\%$ the worst case output voltages ( $V_{OH}$ , and $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ , $I_{CC}$ , and $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.								

AC Electrical Characteristics					
$V_{CC} = 5V, T_A = 25^\circ C, C_L = 15\text{ pF}, t_r = t_f = 6\text{ ns}$					
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		50	30	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock to Output		18	27	ns
$t_{PHL}$	Maximum Propagation Delay, Clear to Output		18	27	ns
$t_{REM}$	Minimum Removal Time, Clear to Clock		10	20	ns
$t_s$	Minimum Setup Time Data to Clock		10	20	ns
$t_H$	Minimum Hold Time Clock to Data		-2	0	ns
$t_W$	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics								
$C_L = 50\text{ pF}, t_r = t_f = 6\text{ ns}$ (unless otherwise specified)								
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$	$T_A = -40\text{ to }85^\circ C$	$T_A = -55\text{ to }125^\circ C$	Units	
				Typ	Guaranteed Limits			
$f_{MAX}$	Maximum Operating Frequency		2.0V	16	5	4	3	MHz
			4.5V	74	27	21	18	MHz
			6.0V	78	31	24	20	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock to Output		2.0V	38	135	170	205	ns
			4.5V	14	27	34	41	ns
			6.0V	12	23	29	35	ns
$t_{PHL}$	Maximum Propagation Delay, Clear to Output		2.0V	42	135	170	205	ns
			4.5V	19	27	34	41	ns
			6.0V	18	23	29	35	ns
$t_{REM}$	Minimum Removal Time Clear to Clock		2.0V	0	25	32	37	ns
			4.5V	0	5	6	7	ns
			6.0V	0	4	5	6	ns
$t_s$	Minimum Setup Time Data to Clock		2.0V	26	100	125	150	ns
			4.5V	7	20	25	30	ns
			6.0V	5	17	21	25	ns
$t_H$	Minimum Hold Time Clock to Data		2.0V	-15	0	0	0	ns
			4.5V	-6	0	0	0	ns
			6.0V	-4	0	0	0	ns
$t_W$	Minimum Pulse Width Clock or Clear		2.0V	34	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	20	ns
$t_r, t_f$	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	11	15	19	22	ns
			6.0V	9	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per flip-flop)		45				pF
$C_{IN}$	Maximum Input Capacitance			7	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



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DETAIL A

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D**

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  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A**

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А