Dual, 12-/14-/16-Bit,1 GSPS Digital-to-Analog Converters

Data Sheet

AD9776A/AD9778A/AD9779A

FEATURES

- Low power: 1.0 W @ 1 GSPS, 600 mW @ 500 MSPS, full operating conditions
- Single carrier W-CDMA ACLR = 80 dBc @ 80 MHz IF
- Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
- Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth
- Auxiliary DACs allow control of external VGA and offset control
- Multiple chip synchronization interface
- High performance, low noise PLL clock multiplier
- Digital inverse sinc filter
- 100-lead, exposed paddle TQFP

APPLICATIONS

- Wireless infrastructure
  - W-CDMA, CDMA2000, TD-SCDMA, WiMax, GSM, LTE
- Digital high or low IF synthesis
- Internal digital upconversion capability
- Transmit diversity
- Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9776A/AD9778A/AD9779A are dual, 12-/14-/16-bit, high dynamic range digital-to-analog converters (DACs) that provide a sample rate of 1 GSPS, permitting a multicarrier generation up to the Nyquist frequency. They include features optimized for direct conversion transmission applications, including complex digital modulation and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the ADL537x FMOD series from Analog Devices, Inc. A 3-wire interface provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The devices are manufactured on an advanced 0.18 µm CMOS process and operate on 1.8 V and 3.3 V supplies for a total power consumption of 1.0 W. They are enclosed in a 100-lead thin quad flat package (TQFP).

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. A proprietary DAC output switching technique enhances dynamic performance.
3. The current outputs are easily configured for various single-ended or differential circuit topologies.
4. CMOS data input interface with adjustable setup and hold.
5. Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth.

TYPICAL SIGNAL CHAIN

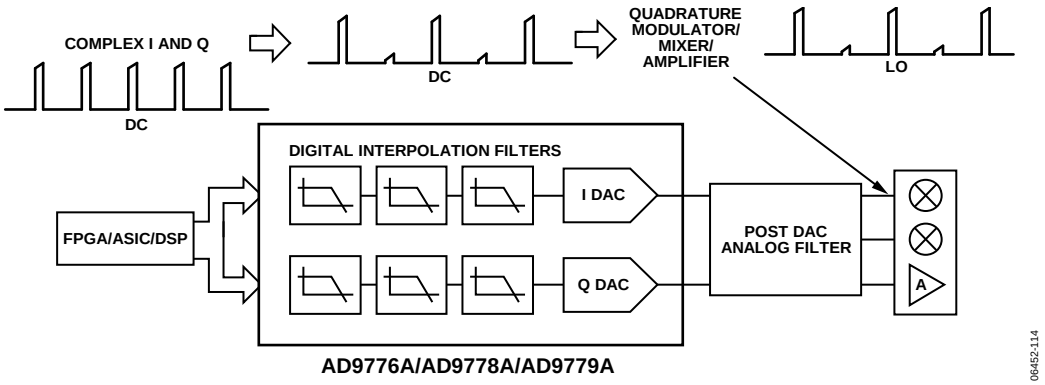

Figure 1.

Rev. C

Document Feedback

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REVISION HISTORY

9/2017—Rev. B to Rev. C

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9/2008—Rev. A to Rev. B

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3/2008—Rev. 0 to Rev. A

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Replaced Transmit Path Gain and Offset Correction Section 40
Replaced Input Data Ports Section 42
Replaced Device Synchronization Section 45
Deleted Figure 112 to Figure 117 58

8/2007—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

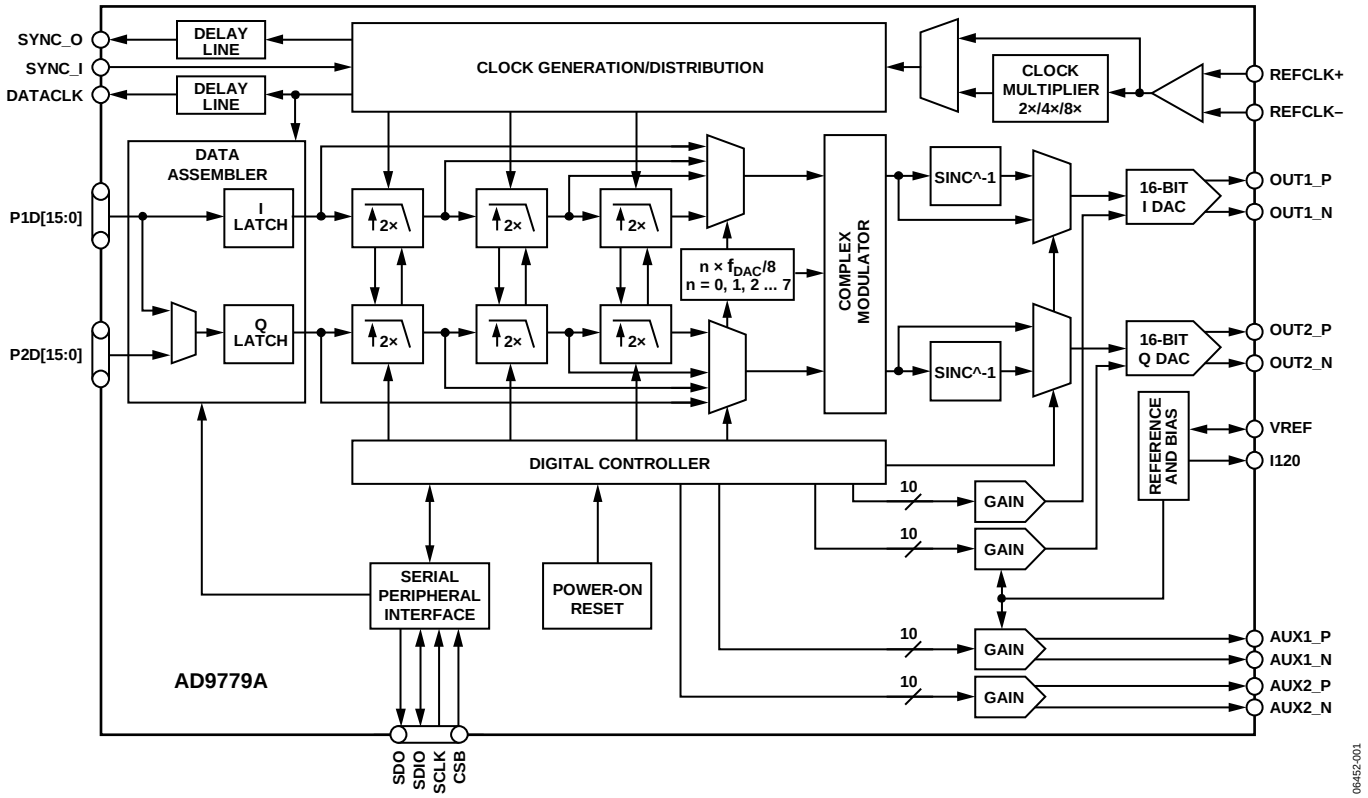

Figure 2. AD9779A Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

	AD9776A			AD9778A			AD9779A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.1			±0.65			±2.1		LSB
Integral Nonlinearity (INL)		±0.86			±1.5			±6.0		LSB
MAIN DAC OUTPUTS										
Offset Error	−0.001	0	+0.001	−0.001	0	+0.001	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		±2			±2			±2		% FSR
Full-Scale Output Current[1]	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
Gain DAC Monotonicity		Guaranteed			Guaranteed			Guaranteed		
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/°C
Gain		100			100			100		ppm/°C
Reference Voltage		30			30			30		ppm/°C
AUXILIARY DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current[1]	−1.998		+1.998	−1.998		+1.998	−1.998		+1.998	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		MΩ
Auxiliary DAC Monotonicity		Guaranteed			Guaranteed			Guaranteed		
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		kΩ
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	2.05	1.70	1.8	2.05	1.70	1.8	2.05	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	2.05	1.70	1.8	2.05	1.70	1.8	2.05	V
POWER CONSUMPTION[2]										
1× Mode, f_{DAC} = 100 MSPS, IF = 1 MHz		250	300		250	300		250	300	mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL Off		498			498			498		mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL On		588			588			588		mW
4× Mode, f_{DAC}/4 Modulation, f_{DAC} = 500 MSPS, IF = 137.5 MHz, Q DAC Off		572			572			572		mW
8× Mode, f_{DAC}/4 Modulation, f_{DAC} = 1 GSPS, IF = 262.5 MHz		980			980			980		mW
Power-Down Mode		2.5	9.8		2.5	9.8		2.5	9.8	mW
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.
[2] See the Power Dissipation section for more details.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High		2.0			V
Input V_{IN} Logic Low				0.8	V
Maximum Input Data Rate at Interpolation					
1×		300			MSPS
2×		250			MSPS
4×		200			MSPS
8×	DVDD18, CVDD18 = 1.8 V ± 5%	112.5			MSPS
	DVDD18, CVDD18 = 1.9 V ± 5%	125			MSPS
	DVDD18, CVDD18 = 2.0 V ± 2%	137.5			MSPS
CMOS OUTPUT LOGIC LEVEL (DATACLK, PIN 37)[1]					
Output V_{OUT} Logic High		2.4			V
Output V_{OUT} Logic Low				0.4	V
DATACLK Output Duty Cycle	At 250 MHz, into 5 pF load	40	50	60	%
LVDS RECEIVER INPUTS (SYNC_I+, SYNC_I–)	SYNC_I+ = V_{IA}, SYNC_I– = V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}		825		1575	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate	Additional limits on f_{SYNC_I} apply; see description of Register 0x05, Bits[3:1], in Table 14			250	MSPS
Setup Time, SYNC_I to REFCLK		0.4			ns
Hold Time, SYNC_I to REFCLK		0.55			ns
LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O–)	SYNC_O+ = V_{OA}, SYNC_O– = V_{OB}, 100 Ω termination				
Output Voltage High, V_{OA} or V_{OB}				1375	mV
Output Voltage Low, V_{OA} or V_{OB}		1025			mV
Output Differential Voltage, $\|V_{OD}\|$		150	200	250	mV
Output Offset Voltage, V_{OS}		1150		1250	mV
Output Impedance, R_O	Single-ended	80	100	120	Ω
DAC CLOCK INPUT (REFCLK+, REFCLK–)					
Differential Peak-to-Peak Voltage		400	800	2000	mV
Common-Mode Voltage		300	400	500	mV
Maximum Clock Rate	DVDD18, CVDD18 = 1.8 V ± 5%, PLL off	900			MHz
	DVDD18, CVDD18 = 1.9 V ± 5%, PLL off	1000			MHz
	DVDD18, CVDD18 = 2.0 V ± 2%, PLL off	1100			MHz
	DVDD18, CVDD18 = 2.0 V ± 2%, PLL on	250			MHz

[1] Specification is at a DATACLK frequency of 100 MHz into a 1 kΩ load, with maximum drive capability of 8 mA. At higher speeds or greater loads, best practice suggests using an external buffer for this signal.

DIGITAL INPUT DATA TIMING SPECIFICATIONS

All modes, −40°C to +85°C.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT DATA[1]					
Setup Time	Input data to DATACLK	3.0			ns
Hold Time	Input data to DATACLK	−0.05			ns
Setup Time	Input data to REFCLK	−0.80			ns
Hold Time	Input data to REFCLK	3.80			ns
LATENCY					
1× Interpolation	With or without modulation		25		DACCLK cycles
2× Interpolation	With or without modulation		70		DACCLK cycles
4× Interpolation	With or without modulation		146		DACCLK cycles
8× Interpolation	With or without modulation		297		DACCLK cycles
Inverse Sync			18		DACCLK cycles
3-WIRE INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High, t_{PWH}				12.5	ns
Minimum Pulse Width Low, t_{PWL}				12.5	ns
Setup Time, t_{DS}	SDIO to SCLK	2.8			ns
Hold Time, t_{DH}	SDIO to SCLK	0.0			ns
Setup Time, t_{DS}	CSB to SCLK	2.8			ns
Data Valid, t_{DV}	SDO to SCLK	2.0			ns
POWER-UP TIME[2]			260		ms
RESET					
Minimum Pulse Width, High				2	DACCLK cycles

[1] Specified values are with PLL disabled. Timing vs. temperature and data valid keep out windows (that is, the minimum amount of time valid data must be presented to the device to ensure proper sampling) are delineated in Table 28.
[2] Measured from CSB rising edge when Register 0x00, Bit 4, is written from 1 to 0 with the VREF decoupling capacitor equal to 0.1 µF.

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 4.

	AD9776A			AD9778A			AD9779A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (SFDR)										
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		82			82			82		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		81			81			82		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		85			85			87		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		87			87			91		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		80			85			85		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		75			81			81		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		75			80			81		dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT-TONE, 500 kHz TONE SPACING										
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		−152			−155			−158		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		−155			−159			−160		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		−157.5			−160			−161		dBm/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		76			78			79		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		69			73			74		dBc
W-CDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		77.5			80			81		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		76			78			78		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
AVDD33, DVDD33	AGND, DGND, CGND	−0.3 V to +3.6 V
DVDD18, CVDD18	AGND, DGND, CGND	−0.3 V to +2.1 V
AGND	DGND, CGND	−0.3 V to +0.3 V
DGND	AGND, CGND	−0.3 V to +0.3 V
CGND	AGND, DGND	−0.3 V to +0.3 V
I120, VREF, IPTAT	AGND	−0.3 V to AVDD33 + 0.3 V
OUT1_P, OUT1_N, OUT2_P, OUT2_N, AUX1_P, AUX1_N, AUX2_P, AUX2_N	AGND	−1.0 V to AVDD33 + 0.3 V
P1D[15:0], P2D[15:0]	DGND	−0.3 V to DVDD33 + 0.3 V
DATACLK, TXENABLE	DGND	−0.3 V to DVDD33 + 0.3 V
REFCLK+, REFCLK−	CGND	−0.3 V to CVDD18 + 0.3 V
RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I−, CSB, SCLK, SDIO, SDO	DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

For optimal thermal performance, the exposed paddle (EPAD) should be soldered to the ground plane for the 100-lead, thermally enhanced TQFP package.

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
100-Lead TQFP				
EPAD Soldered	19.1	12.4	7.1	°C/W
EPAD Not Soldered	27.4			°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

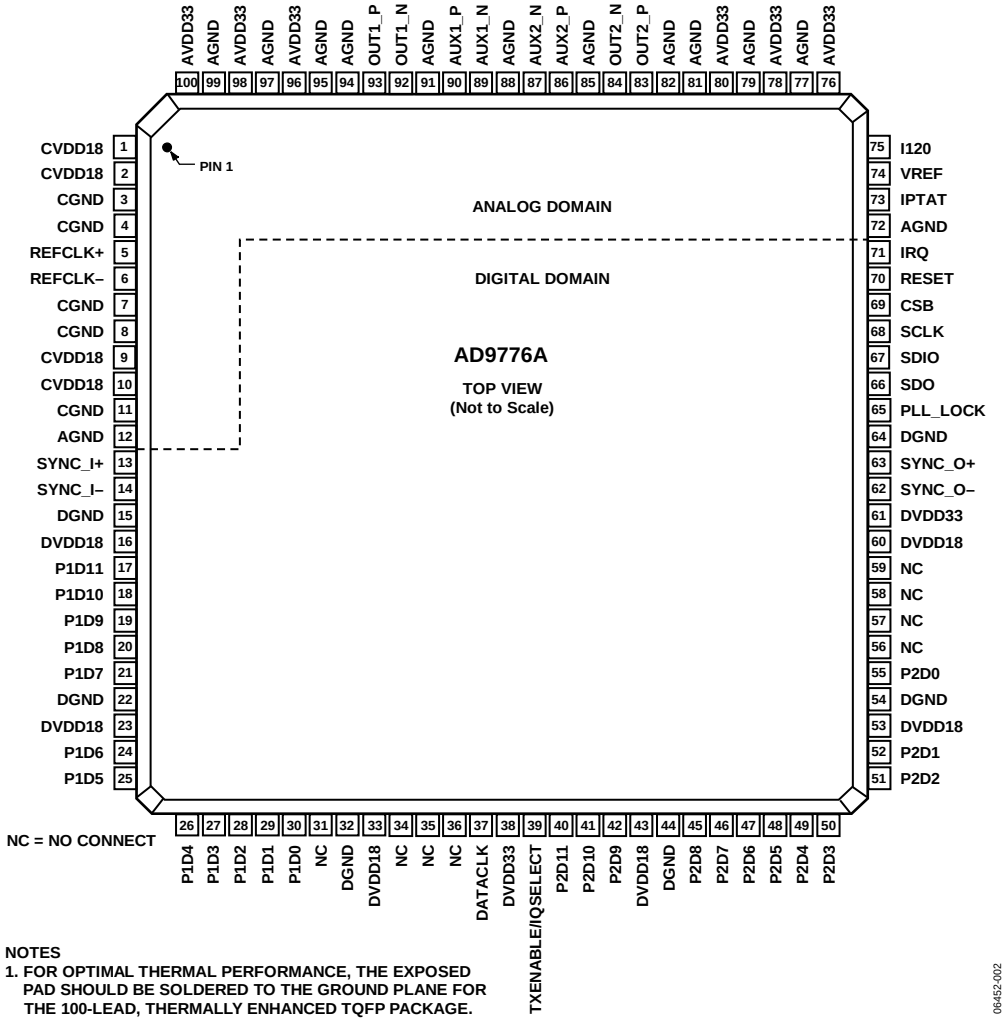

Figure 3. AD9776A Pin Configuration

Table 7. AD9776A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Ground.
4	CGND	Clock Ground.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Ground.
8	CGND	Clock Ground.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Ground.
12	AGND	Analog Ground.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Ground.
16	DVDD18	1.8 V Digital Supply.
17	P1D11	Port 1, Data Input D11 (MSB).
18	P1D10	Port 1, Data Input D10.
19	P1D9	Port 1, Data Input D9.
20	P1D8	Port 1, Data Input D8.
21	P1D7	Port 1, Data Input D7.
22	DGND	Digital Ground.
23	DVDD18	1.8 V Digital Supply.
24	P1D6	Port 1, Data Input D6.
25	P1D5	Port 1, Data Input D5.
26	P1D4	Port 1, Data Input D4.
27	P1D3	Port 1, Data Input D3.
28	P1D2	Port 1, Data Input D2.
29	P1D1	Port 1, Data Input D1.
30	P1D0	Port 1, Data Input D0 (LSB).
31	NC	No Connect.
32	DGND	Digital Ground.
33	DVDD18	1.8 V Digital Supply.
34	NC	No Connect.

Pin No.	Mnemonic	Description
35	NC	No Connect.
36	NC	No Connect.
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE/ IQSELECT	Transmit Enable. In single port mode, this pin also functions as IQSELECT.
40	P2D11	Port 2, Data Input D11 (MSB).
41	P2D10	Port 2, Data Input D10.
42	P2D9	Port 2, Data Input D9.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Ground.
45	P2D8	Port 2, Data Input D8.
46	P2D7	Port 2, Data Input D7.
47	P2D6	Port 2, Data Input D6.
48	P2D5	Port 2, Data Input D5.
49	P2D4	Port 2, Data Input D4.
50	P2D3	Port 2, Data Input D3.
51	P2D2	Port 2, Data Input D2.
52	P2D1	Port 2, Data Input D1.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Ground.
55	P2D0	Port 2, Data Input D0 (LSB).
56	NC	No Connect.
57	NC	No Connect.
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O−	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Ground.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	3-Wire Interface Port Data Output.
67	SDIO	3-Wire Interface Port Data Input/Output.
68	SCLK	3-Wire Interface Port Clock.
69	CSB	3-Wire Interface Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Ground.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Ground.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Ground.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Ground.
82	AGND	Analog Ground.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Ground.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Ground.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Ground.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Ground.
95	AGND	Analog Ground.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Ground.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Ground.
100	AVDD33	3.3 V Analog Supply.

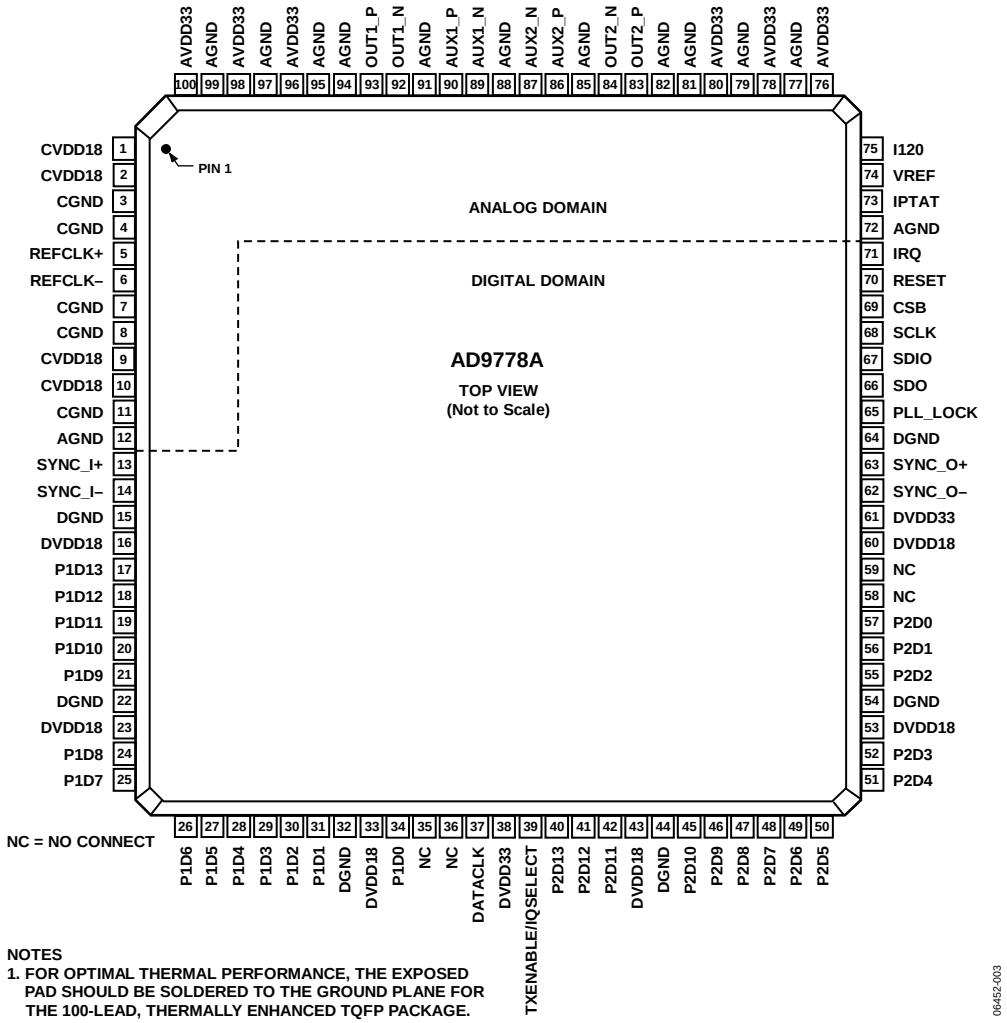

Figure 4. AD9778A Pin Configuration

Table 8. AD9778A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Ground.
4	CGND	Clock Common.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Ground.
8	CGND	Clock Ground.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Ground.
12	AGND	Analog Ground.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Ground.
16	DVDD18	1.8 V Digital Supply.
17	P1D13	Port 1, Data Input D13 (MSB).
18	P1D12	Port 1, Data Input D12.
19	P1D11	Port 1, Data Input D11.
20	P1D10	Port 1, Data Input D10.
21	P1D9	Port 1, Data Input D9.
22	DGND	Digital Ground.
23	DVDD18	1.8 V Digital Supply.
24	P1D8	Port 1, Data Input D8.
25	P1D7	Port 1, Data Input D7.
26	P1D6	Port 1, Data Input D6.
27	P1D5	Port 1, Data Input D5.
28	P1D4	Port 1, Data Input D4.
29	P1D3	Port 1, Data Input D3.
30	P1D2	Port 1, Data Input D2.
31	P1D1	Port 1, Data Input D1.
32	DGND	Digital Ground.
33	DVDD18	1.8 V Digital Supply.
34	P1D0	Port 1, Data Input D0 (LSB).
35	NC	No Connect.
36	NC	No Connect.

Pin No.	Mnemonic	Description
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE/ IQSELECT	Transmit Enable. In single port mode, this pin also functions as IQSELECT.
40	P2D13	Port 2, Data Input D13 (MSB).
41	P2D12	Port 2, Data Input D12.
42	P2D11	Port 2, Data Input D11.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Ground.
45	P2D10	Port 2, Data Input D10.
46	P2D9	Port 2, Data Input D9.
47	P2D8	Port 2, Data Input D8.
48	P2D7	Port 2, Data Input D7.
49	P2D6	Port 2, Data Input D6.
50	P2D5	Port 2, Data Input D5.
51	P2D4	Port 2, Data Input D4.
52	P2D3	Port 2, Data Input D3.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Ground.
55	P2D2	Port 2, Data Input D2.
56	P2D1	Port 2, Data Input D1.
57	P2D0	Port 2, Data Input D0 (LSB).
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Ground.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	3-Wire Interface Port Data Output.
67	SDIO	3-Wire Interface Port Data Input/Output.
68	SCLK	3-Wire Interface Port Clock.
69	CSB	3-Wire Interface Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.

Pin No.	Mnemonic	Description
72	AGND	Analog Ground.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Ground.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Ground.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Ground.
82	AGND	Analog Ground.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Ground.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Ground.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Ground.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Ground.
95	AGND	Analog Ground.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Ground.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Ground.
100	AVDD33	3.3 V Analog Supply.

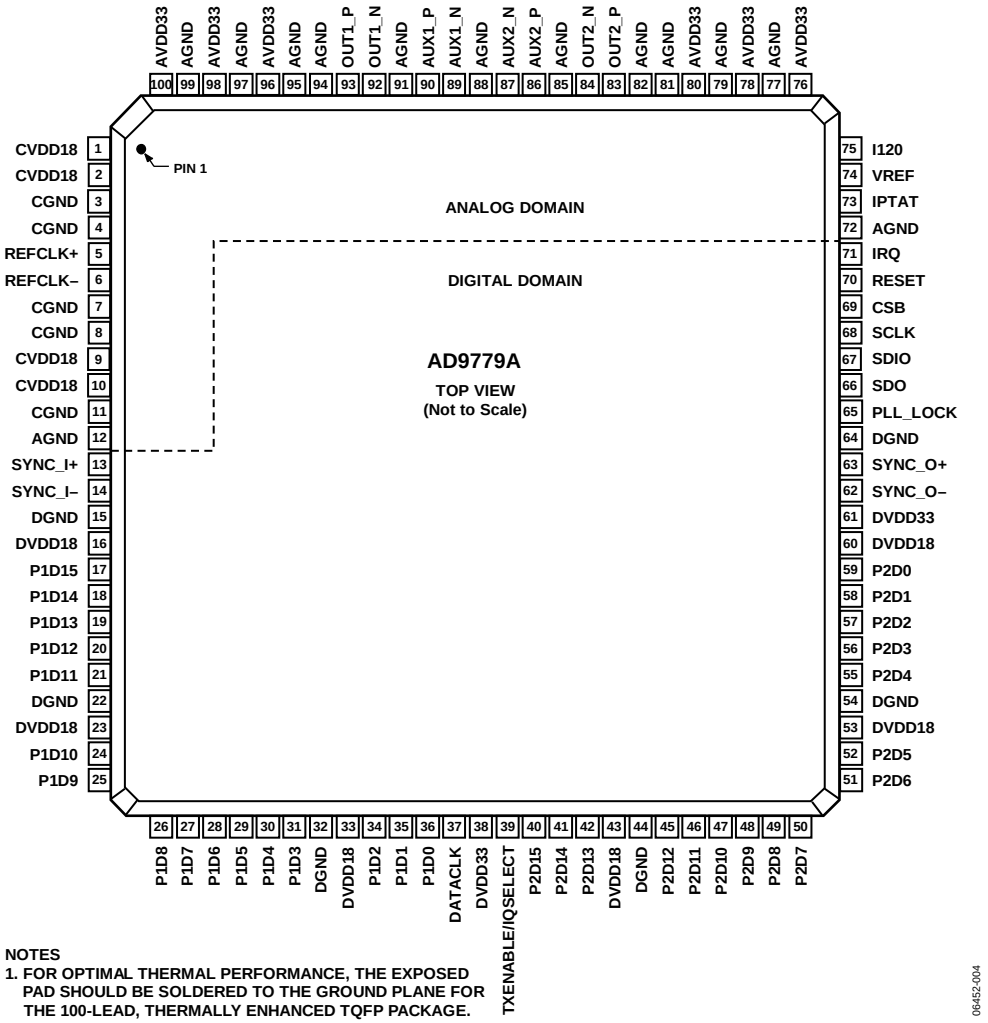

Figure 5. AD9779A Pin Configuration

Table 9. AD9779A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Ground.
4	CGND	Clock Ground.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Ground.
8	CGND	Clock Ground.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Ground.
12	AGND	Analog Ground.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Ground.
16	DVDD18	1.8 V Digital Supply.
17	P1D15	Port 1, Data Input D15 (MSB).
18	P1D14	Port 1, Data Input D14.
19	P1D13	Port 1, Data Input D13.
20	P1D12	Port 1, Data Input D12.
21	P1D11	Port 1, Data Input D11.
22	DGND	Digital Ground.
23	DVDD18	1.8 V Digital Supply.
24	P1D10	Port 1, Data Input D10.
25	P1D9	Port 1, Data Input D9.
26	P1D8	Port 1, Data Input D8.
27	P1D7	Port 1, Data Input D7.
28	P1D6	Port 1, Data Input D6.
29	P1D5	Port 1, Data Input D5.
30	P1D4	Port 1, Data Input D4.
31	P1D3	Port 1, Data Input D3.
32	DGND	Digital Ground.
33	DVDD18	1.8 V Digital Supply.
34	P1D2	Port 1, Data Input D2.
35	P1D1	Port 1, Data Input D1.
36	P1D0	Port 1, Data Input D0 (LSB).

Pin No.	Mnemonic	Description
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE/ IQSELECT	Transmit Enable. In single port mode, this pin also functions as IQSELECT.
40	P2D15	Port 2, Data Input D15 (MSB).
41	P2D14	Port 2, Data Input D14.
42	P2D13	Port 2, Data Input D13.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Ground.
45	P2D12	Port 2, Data Input D12.
46	P2D11	Port 2, Data Input D11.
47	P2D10	Port 2, Data Input D10.
48	P2D9	Port 2, Data Input D9.
49	P2D8	Port 2, Data Input D8.
50	P2D7	Port 2, Data Input D7.
51	P2D6	Port 2, Data Input D6.
52	P2D5	Port 2, Data Input D5.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Ground.
55	P2D4	Port 2, Data Input D4.
56	P2D3	Port 2, Data Input D3.
57	P2D2	Port 2, Data Input D2.
58	P2D1	Port 2, Data Input D1.
59	P2D0	Port 2, Data Input D0 (LSB).
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Ground.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	3-Wire Interface Port Data Output.
67	SDIO	3-Wire Interface Port Data Input/Output.
68	SCLK	3-Wire Interface Port Clock.
69	CSB	3-Wire Interface Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.

Pin No.	Mnemonic	Description
72	AGND	Analog Ground.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Ground.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Ground.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Ground.
82	AGND	Analog Ground.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Ground.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Ground.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Ground.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Ground.
95	AGND	Analog Ground.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Ground.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Ground.
100	AVDD33	3.3 V Analog Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

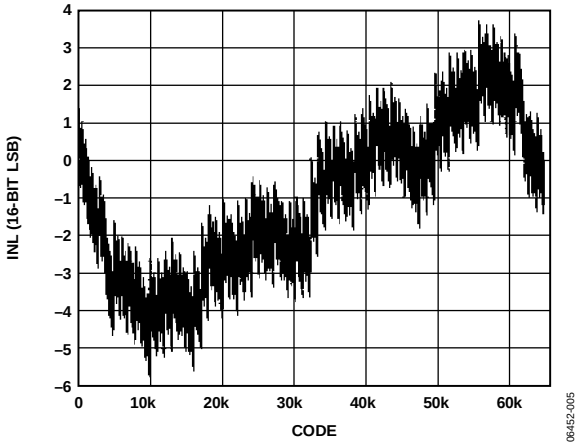

Figure 6. AD9779A Typical INL

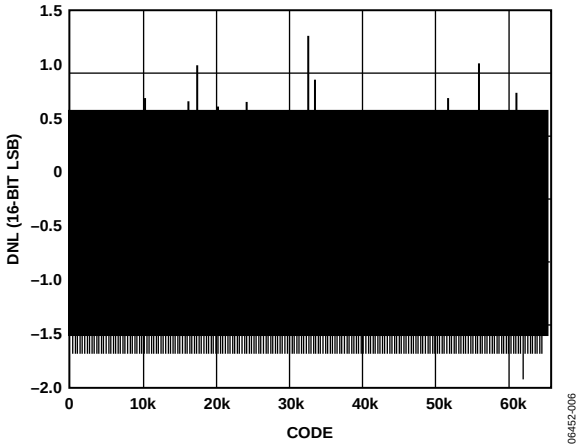

Figure 7. AD9779A Typical DNL

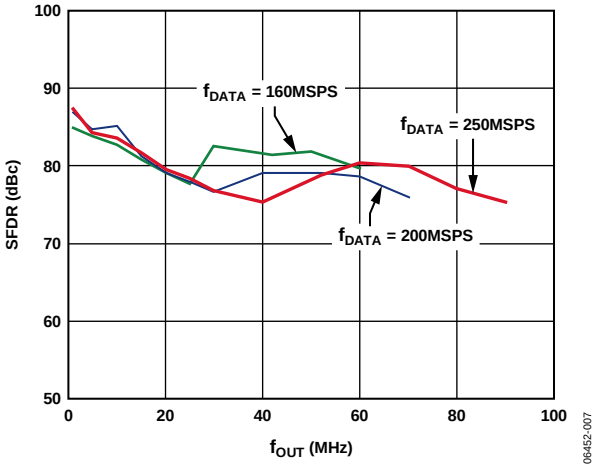

Figure 8. AD9779A In-Band SFDR vs. f_{OUT}, 1× Interpolation

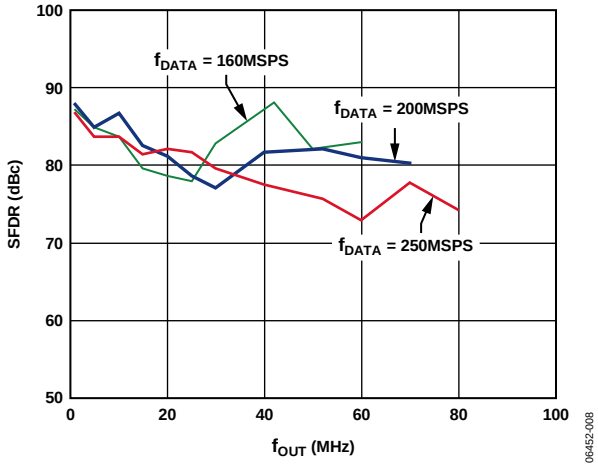

Figure 9. AD9779A In-Band SFDR vs. f_{OUT}, 2× Interpolation

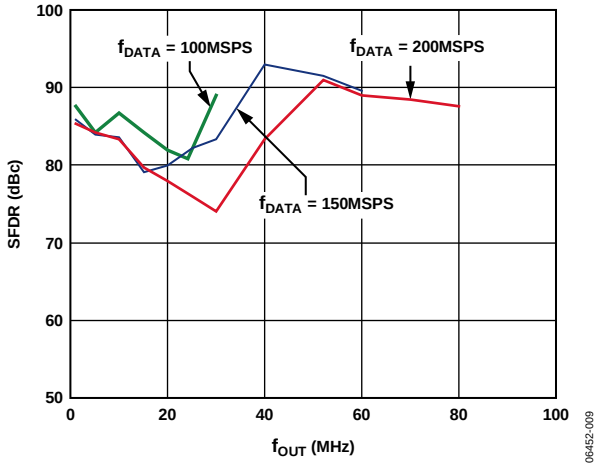

Figure 10. AD9779A In-Band SFDR vs. f_{OUT}, 4× Interpolation

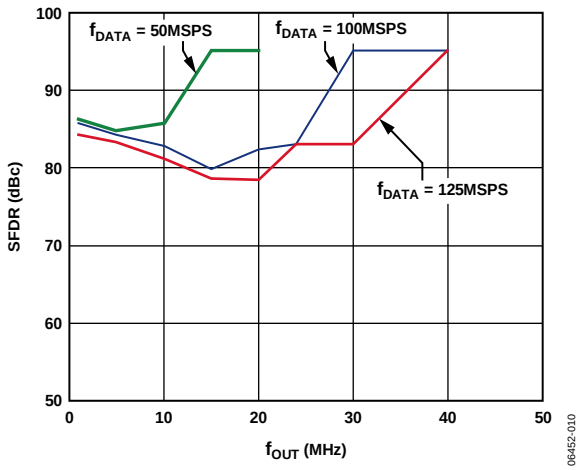

Figure 11. AD9779A In-Band SFDR vs. f_{OUT}, 8× Interpolation

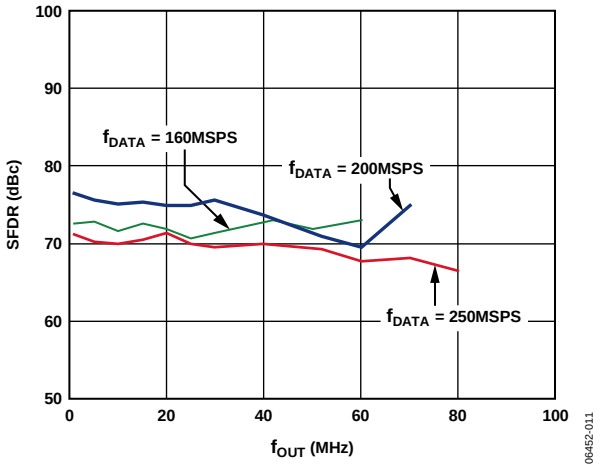

Figure 12. AD9779A Out-of-Band SFDR vs. f_{OUT}, 2× Interpolation

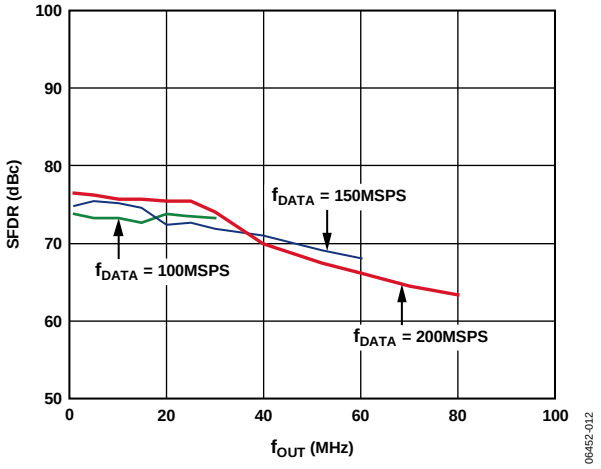

Figure 13. AD9779A Out-of-Band SFDR vs. f_{OUT}, 4× Interpolation

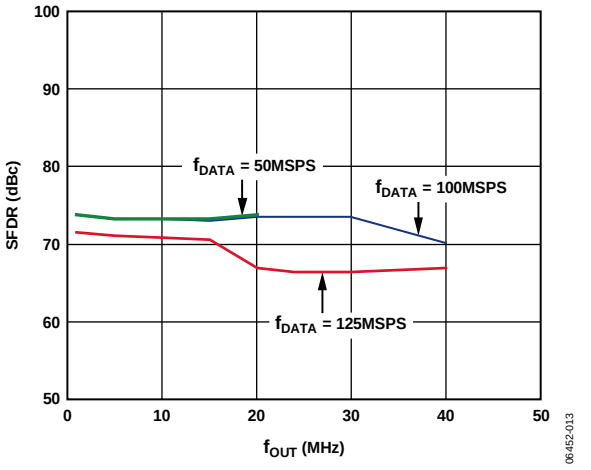

Figure 14. AD9779A Out-of-Band SFDR vs. f_{OUT}, 8× Interpolation

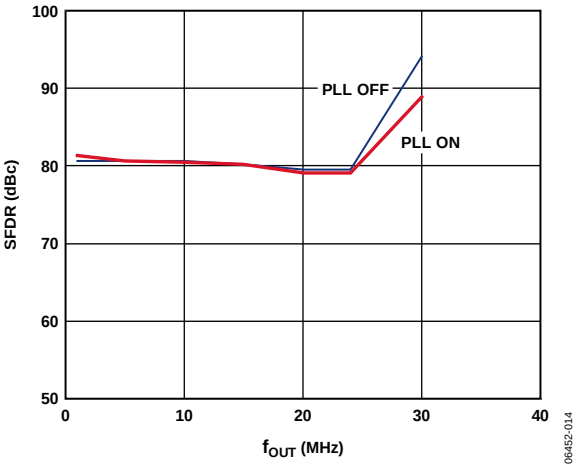

Figure 15. AD9779A In-Band SFDR vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/Off

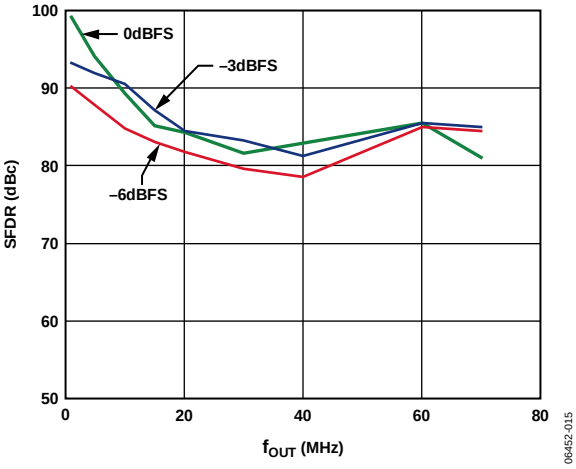

Figure 16. AD9779A In-Band SFDR vs. f_{OUT}, Digital Full Scale

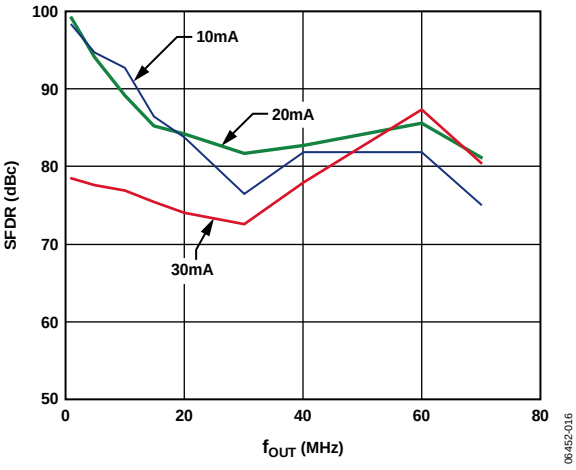

Figure 17. AD9779A In-Band SFDR vs. f_{OUT}, Output Full-Scale Current

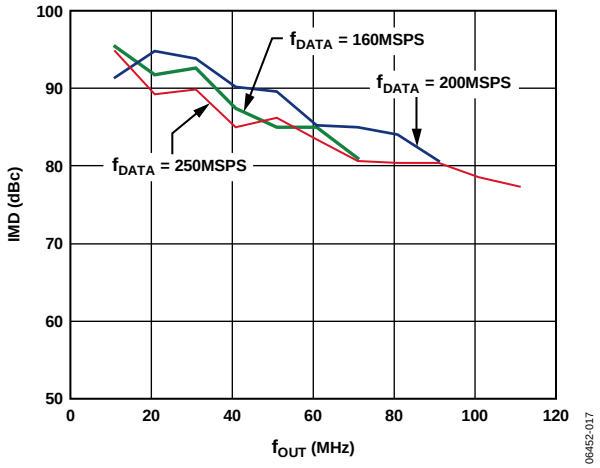

Figure 18. AD9779A Third-Order IMD vs. f_{OUT}, 1× Interpolation

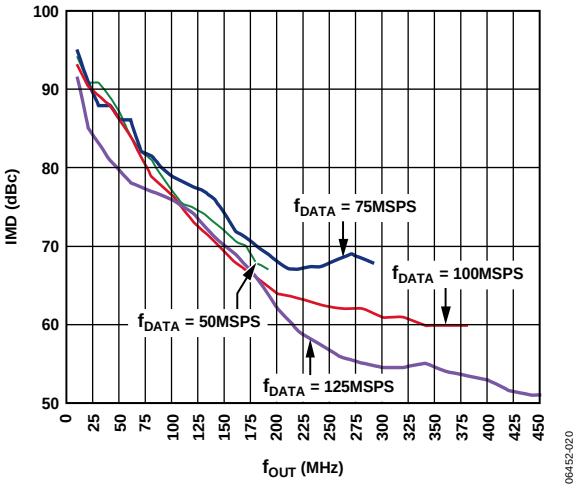

Figure 21. AD9779A Third-Order IMD vs. f_{OUT}, 8× Interpolation

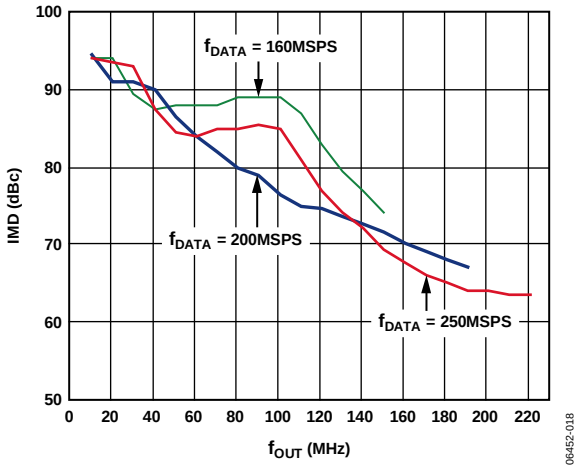

Figure 19. AD9779A Third-Order IMD vs. f_{OUT}, 2× Interpolation

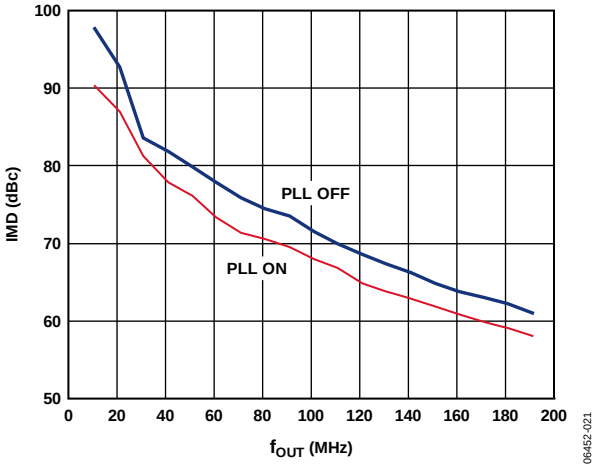

Figure 22. AD9779A Third-Order IMD vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/Off

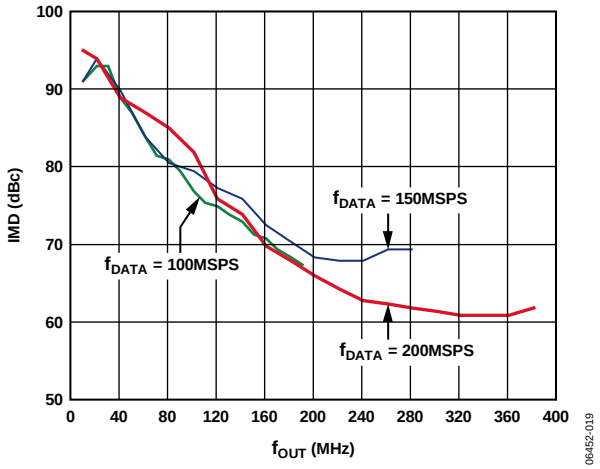

Figure 20. AD9779A Third-Order IMD vs. f_{OUT}, 4× Interpolation

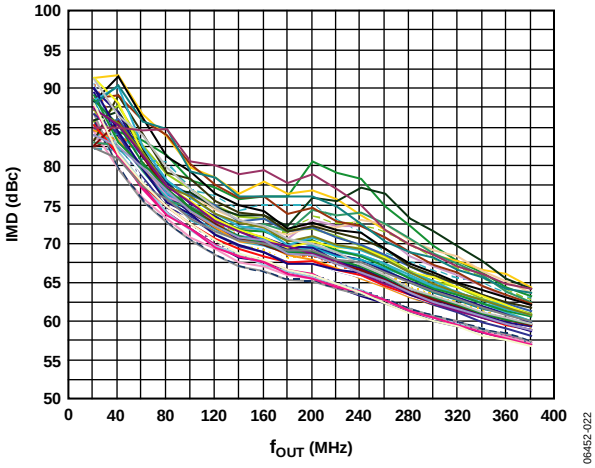

Figure 23. AD9779A Third-Order IMD vs. f_{OUT}, Over 50 Parts, 4× Interpolation, f_{DATA} = 200 MSPS

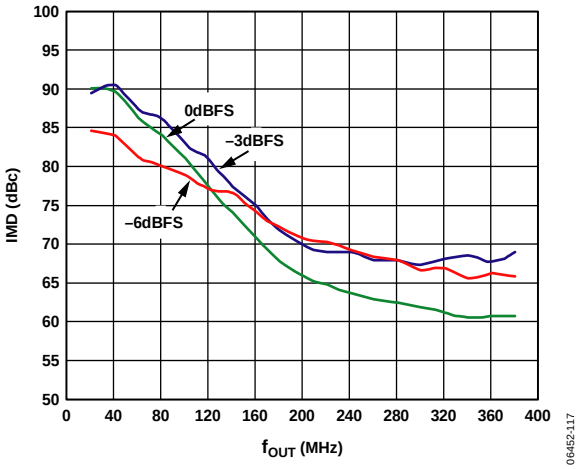

Figure 24. AD9779A IMD Performance vs. f_{OUT}, Digital Full-Scale Input Over Output Frequency, 4× Interpolation, f_{DATA} = 200 MSPS

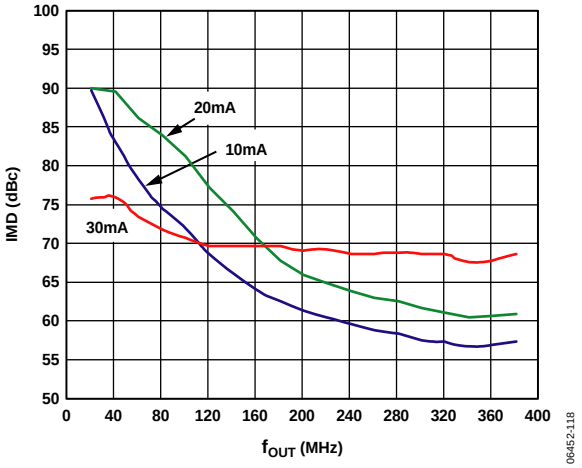

Figure 25. AD9779A IMD Performance vs. f_{OUT}, Full-Scale Output Current Over Output Frequency, 4× Interpolation, f_{DATA} = 200 MSPS

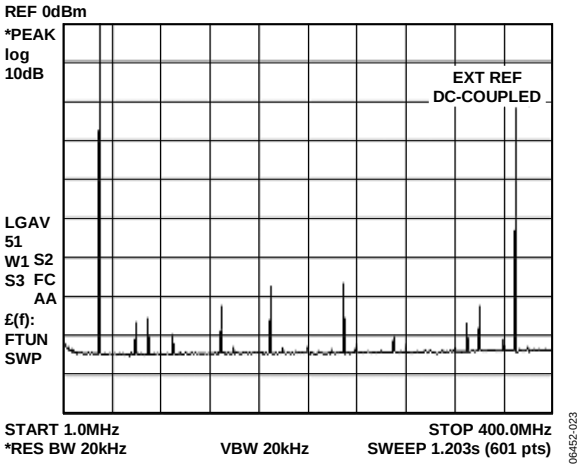

Figure 26. AD9779A Single Tone, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz

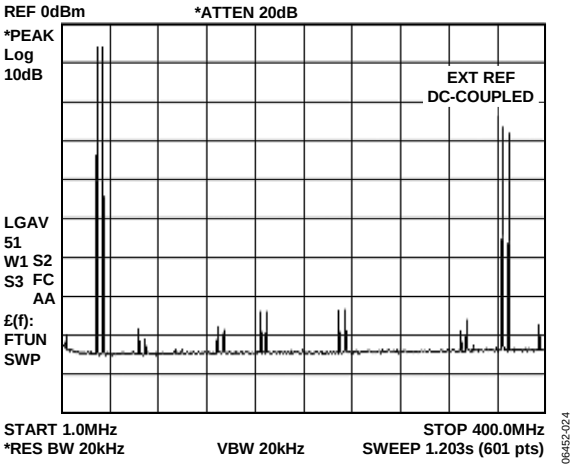

Figure 27. AD9779A Two-Tone Spectrum, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz, 35 MHz

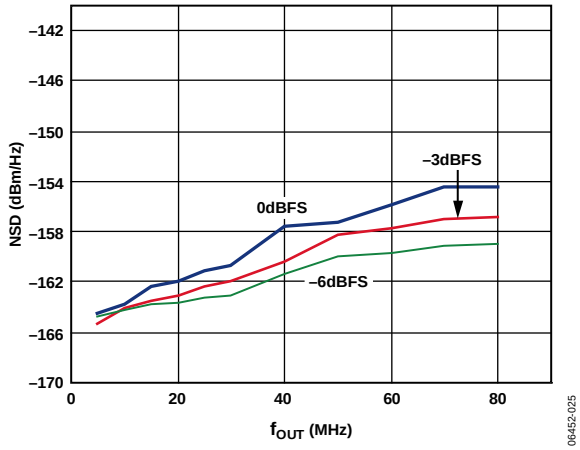

Figure 28. AD9779A Noise Spectral Density vs. f_{OUT}, Digital Full-Scale Over Output Frequency of Single-Tone Input, 2× Interpolation, f_{DATA} = 200 MSPS

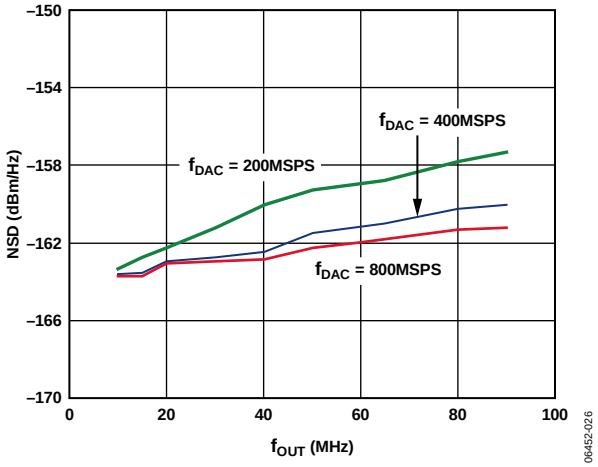

Figure 29. AD9779A Noise Spectral Density vs. f_{OUT}, f_{DAC} Over Output Frequency for Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

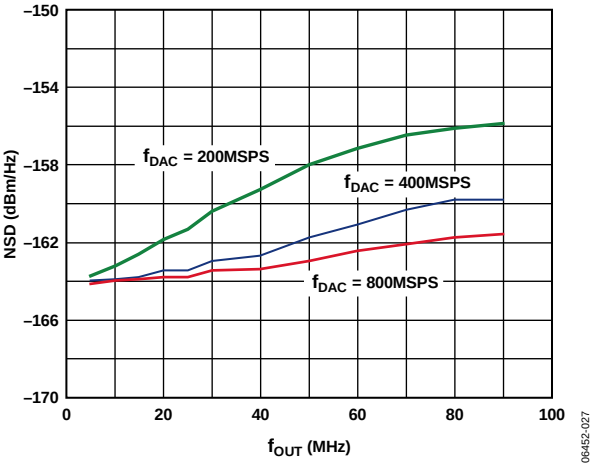

Figure 30. AD9779A Noise Spectral Density vs. f_{OUT}, f_{DAC} Over Output Frequency with a Single-Tone Input at –6 dBFS

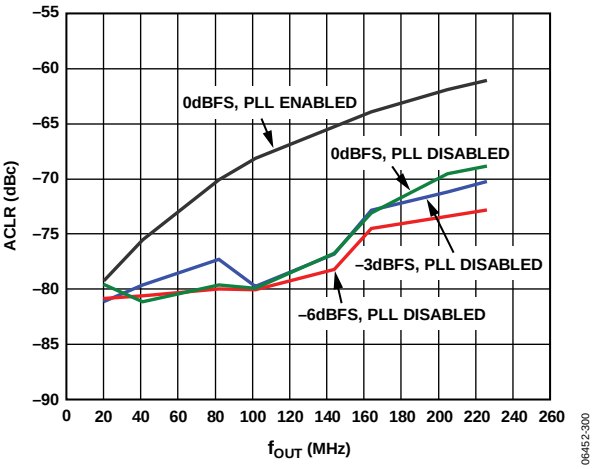

Figure 31. AD9779A ACLR for First Adjacent Band W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

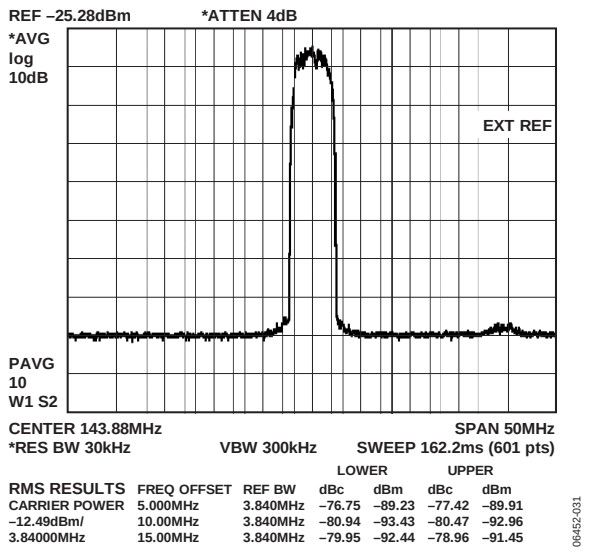

Figure 32. AD9779A W-CDMA Signal, 4× Interpolation, f_{DATA} = 122.88 MSPS, $f_{DAC}/4$ Modulation

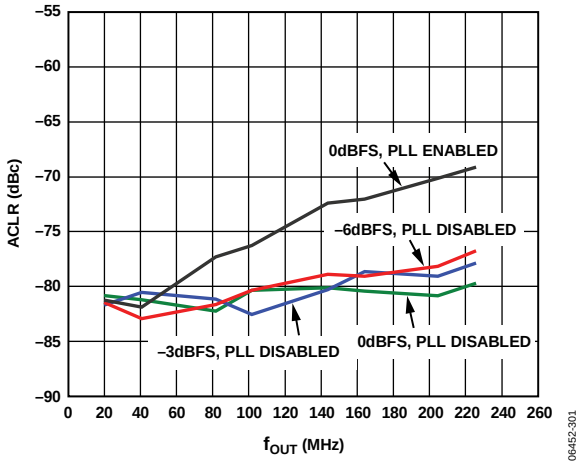

Figure 33. AD9779A ACLR for Second Adjacent Band W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

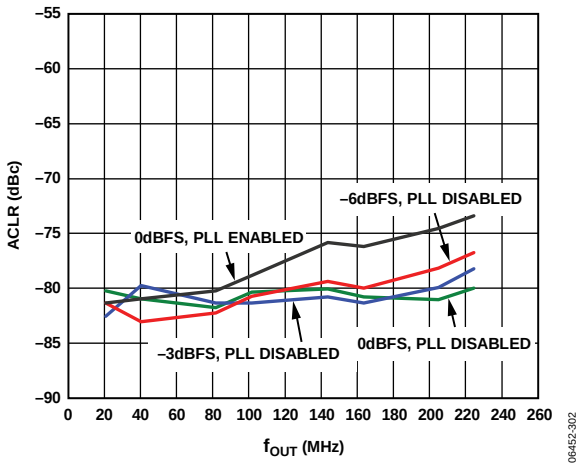

Figure 34. AD9779A ACLR for Third Adjacent Band W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

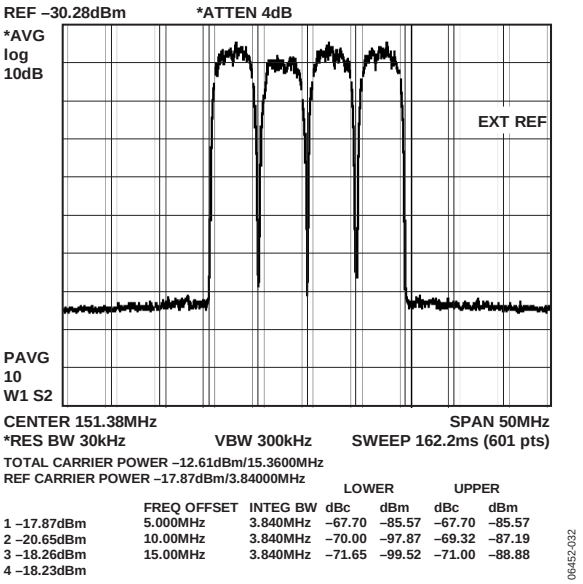

Figure 35. AD9779A Multicarrier W-CDMA Signal, 4× Interpolation, f_{DAC} = 122.88 MSPS, $f_{DAC}/4$ Modulation

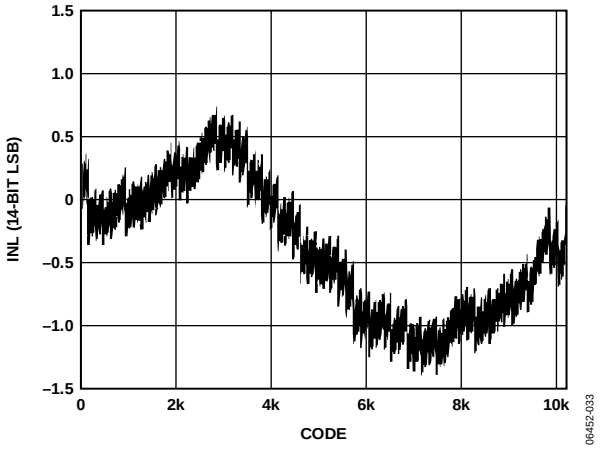

Figure 36. AD9778A Typical INL

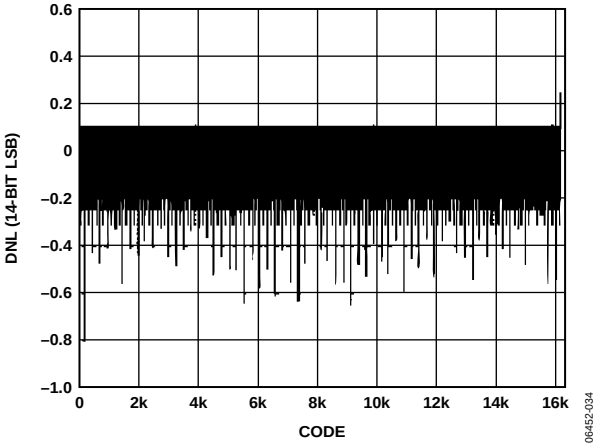

Figure 37. AD9778A Typical DNL

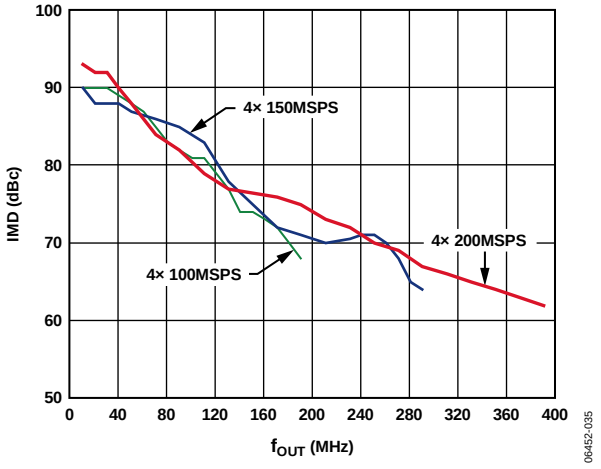

Figure 38. AD9778A IMD vs. f_{OUT}, 4× Interpolation

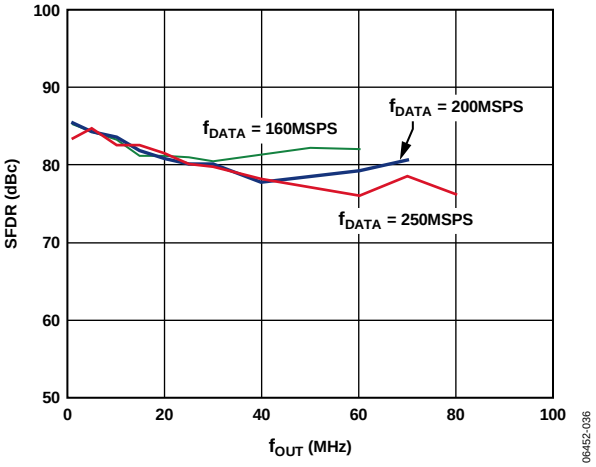

Figure 39. AD9778A In-Band SFDR vs. f_{OUT}, 2× Interpolation

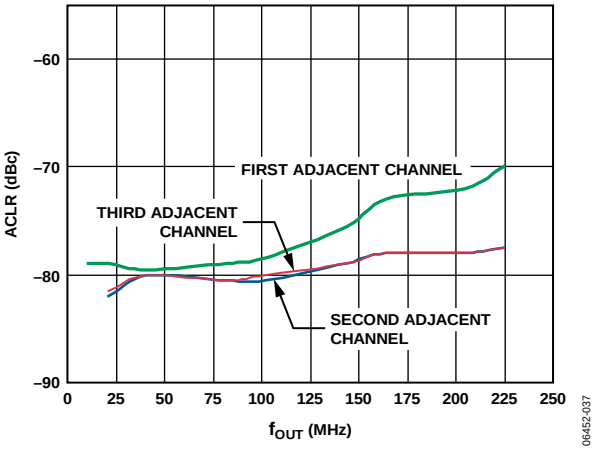

Figure 40. AD9778A ACLR, Single Carrier W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS

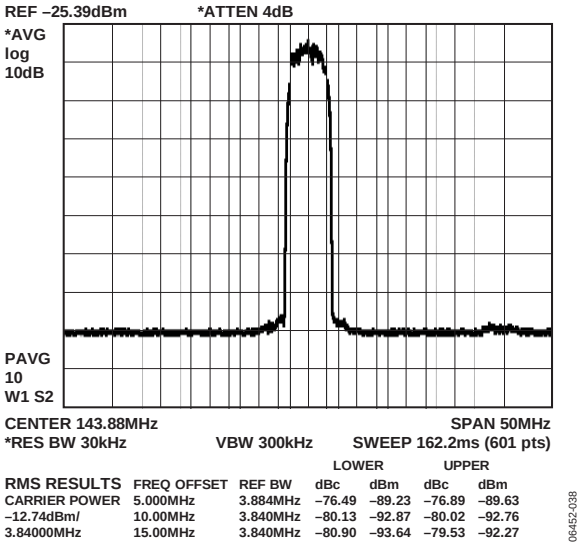

Figure 41. AD9778A ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

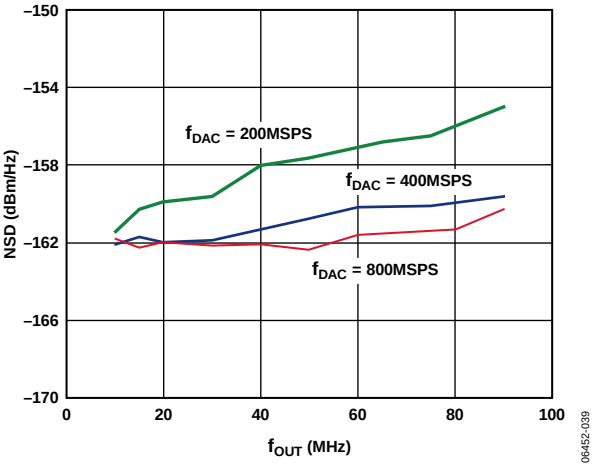

Figure 42. AD9778A Noise Spectral Density vs. f_{OUT} for Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

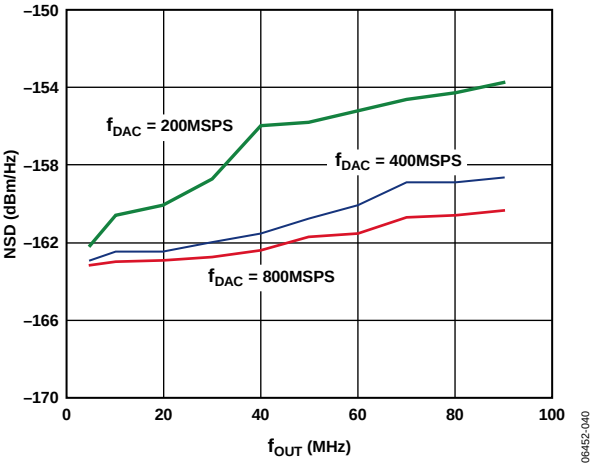

Figure 43. AD9778A Noise Spectral Density vs. f_{OUT} with Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

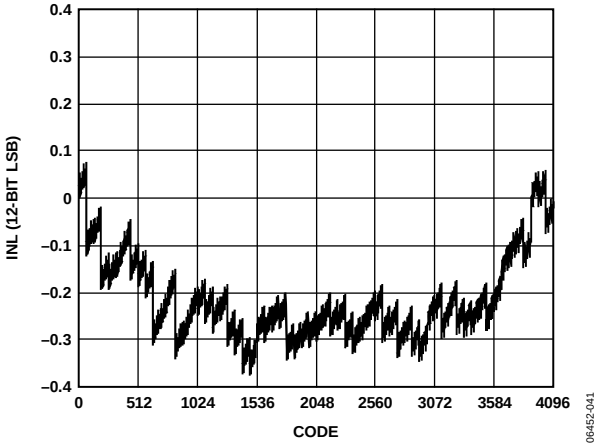

Figure 44. AD9776A Typical INL

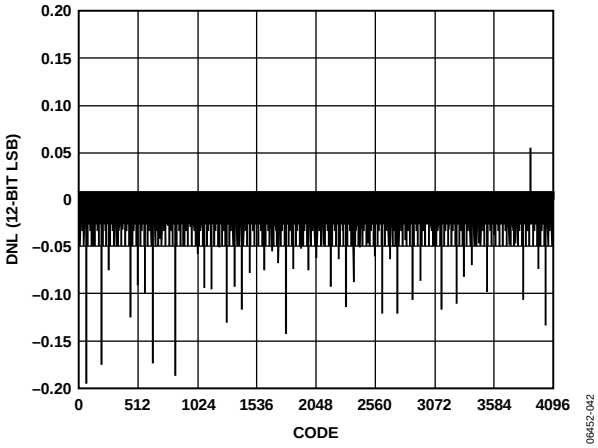

Figure 45. AD9776A Typical DNL

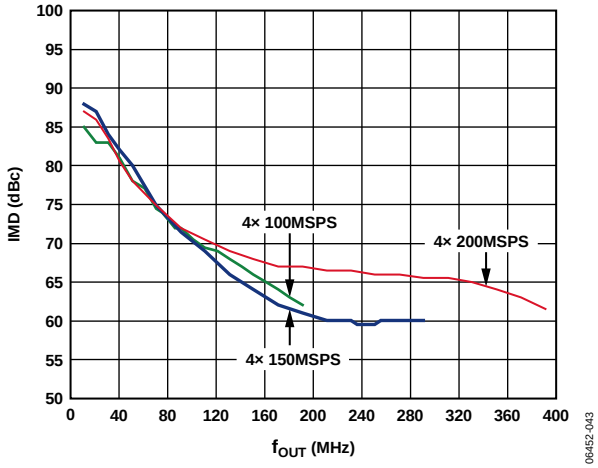

Figure 46. AD9776A IMD vs. f_{OUT}, 4× Interpolation

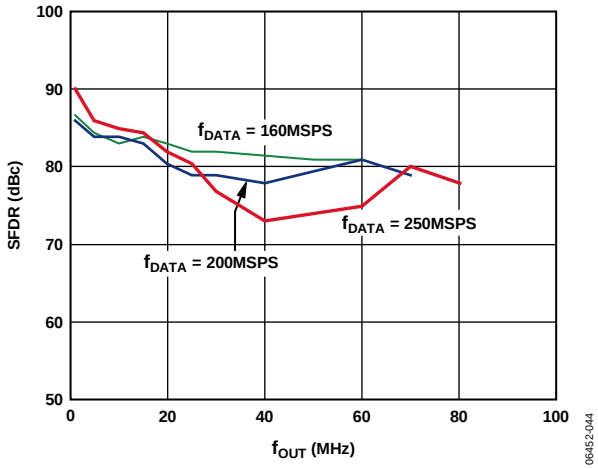

Figure 47. AD9776A In-Band SFDR vs. f_{OUT}, 2× Interpolation

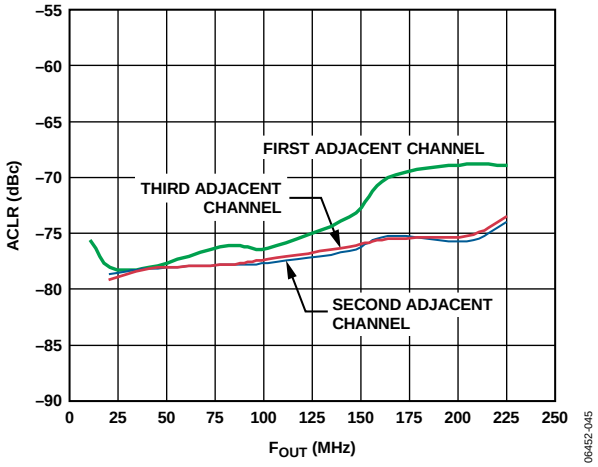

Figure 48. AD9776A ACLR vs. f_{OUT}, f_{DATA} = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

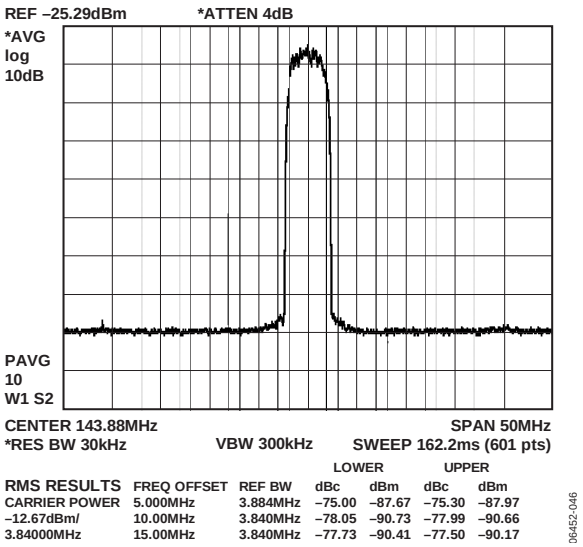

Figure 49. AD9776A Single Carrier W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS

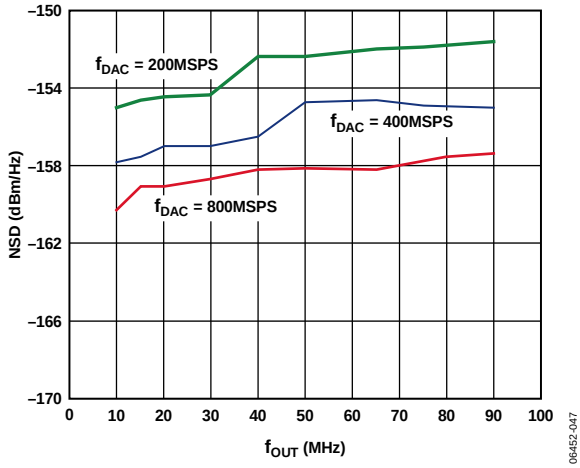

Figure 50. AD9776A Noise Spectral Density vs. f_{OUT}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

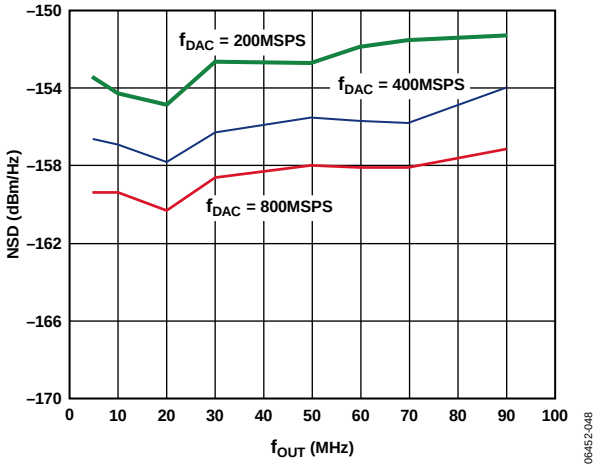

Figure 51. AD9776A Noise Spectral Density vs. f_{OUT}, Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

TERMINOLOGY

Integral Nonlinearity (INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current at Code 0 from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
Gain error is the difference between the actual and the ideal output spans. The actual span is determined by the difference between the full-scale output and the bottom-scale output.

Output Compliance Range
Output compliance range is the range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

In-Band Spurious-Free Dynamic Range (SFDR)
In-band SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Out-of-Band Spurious-Free Dynamic Range (SFDR)
Out-of-band SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the band that starts at the frequency of the input data rate and ends at the Nyquist frequency of the DAC output sample rate. Normally, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths to the DAC output.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in dBc of the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9776A/AD9778A/AD9779A have many features that make them highly suited for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface with common quadrature modulators when designing single sideband transmitters. The speed and performance of the parts allow wider bandwidths and more carriers to be synthesized than in previously available DACs. The digital engine uses an innovative filter architecture that combines the interpolation with a digital quadrature modulator. This allows the parts to perform digital quadrature frequency upconversions. The on-chip synchronization circuitry enables multiple devices to be synchronized to each other, or to a system clock.

DIFFERENCES BETWEEN AD9776/AD9778/AD9779 AND AD9776A/AD9778A/AD9779A

REFCLK Maximum Frequency vs. Supply

With some restrictions on the DVDD18 and CVDD18 power supplies, the AD9776A/AD9778A/AD9779A support a maximum sample rate of 1100 MHz. Table 2 lists the valid operating frequencies vs. power supply voltage.

REFCLK Amplitude

With a differential sinusoidal clock applied to REFCLK, the PLL on the AD9776/AD9778/AD9779 does not achieve optimal noise performance unless the REFCLK differential amplitude is increased to 2 V p-p. Note that if an LVPECL driver is used on the AD9776/AD9778/AD9779, the PLL exhibits optimal performance if the REFCLK amplitude is well within LVPECL specifications (<1.6 V p-p differential). The design of the PLL on the AD9779A has been improved so that even with a sinusoidal clock, the PLL still achieves optimal amplitude if the swing is 1.6 V p-p.

PLL Lock Ranges

The individual lock ranges for the AD9776A/AD9778A/AD9779A PLL are wider than those for the AD9776/AD9778/AD9779. This means that the AD9776A/AD9778A/AD9779A PLL remains in lock in a given range over a wider temperature range than the AD9776/AD9778/AD9779. See Table 23 for PLL lock ranges for the AD9776A/AD9778A/AD9779A.

PLL Optimal Settings

The optimal settings for the AD9776/AD9778/AD9779 differ from the AD9776A/AD9778A/AD9779A. Refer to the PLL Bias Settings section for complete details.

Input Data Timing

See Table 28 for timing specifications vs. temperature. The input data timing specifications (setup and hold) are different for the AD9776A/AD9778A/AD9779A than they are for the AD9776/AD9778/AD9779.

DATACLK Delay Range

In the AD9776/AD9778/AD9779, the input data delay was controlled by Register 0x04, Bits[7:4]. At 25°C, the delay was stepped by approximately 180 ps/increment. In the AD9776A/AD9778A/AD9779A, an extra bit has been added, which effectively doubles the delay range. This bit is now located at Register 0x01, Bit 1. The increment/step on the AD9776A/AD9778A/AD9779A remains at ~180 ps.

Version Register

The version register (Register 0x1F) of the AD9776A/AD9778A/AD9779A reads a value of 0x07. The version register of the AD9776/AD9778/AD9779 reads a value of 0x03.

Table 10. Register Value Differences Between AD9776/AD9778/AD9779 and AD9776A/AD9778A/AD9779A

Part No.	PLL Loop Bandwidth, Register 0x0A, Bits[4:0]	PLL Bias, Register 0x09, Bits[2:0]	VCO Control Voltage, Register 0x0A, Bits[7:5]	PLL VCO Drive, Register 0x08, Bits[1:0]
AD9776/AD9778/AD9779	11111	111	010	00
AD9776A/AD9778A/AD9779A	01111	011	011	11

3-WIRE INTERFACE

The 3-wire port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The port is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols.

The interface allows read and write access to all registers that configure the AD9776A/AD9778A/AD9779A. Single- or multiple-byte transfers are supported, as well as MSB-first or LSB-first transfer formats. Serial data input/output can be accomplished through a single bidirectional pin (SDIO) or through two unidirectional pins (SDIO/SDO).

The serial port configuration is controlled by Register 0x00, Bits[7:6]. It is important to note that any change made to the serial port configuration occurs immediately upon writing to the last bit of this byte. Therefore, it is possible with a multibyte transfer to write to this register and change the configuration in the middle of a communication cycle. Care must be taken to compensate for the new configuration within the remaining bytes of the current communication cycle.

Use of a single-byte transfer when changing the serial port configuration is recommended to prevent unexpected device behavior.

As described in this section, all serial port data is transferred to/from the device in synchronization with the SCLK pin. If synchronization is lost, the device has the ability to asynchronously terminate an I/O operation, putting the serial port controller into a known state and, thereby, regaining synchronization.

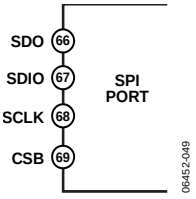

Figure 52. 3-Wire Interface Port

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases of a communication cycle with the AD9776A/AD9778A/AD9779A. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coinciding with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the CSB pin followed by a logic low resets the 3-wire interface port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation, regardless of the state of the internal registers or the other signal levels at the inputs to the 3-wire interface port. If the 3-wire interface port is in an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes, as determined by the instruction byte. Using one multibyte transfer is preferred. Single-byte data transfers are useful in reducing CPU overhead when register access requires only one byte. Registers change immediately upon writing to the last bit of each transfer byte.

INSTRUCTION BYTE

See Table 11 for information contained in the instruction byte.

Table 11. 3-Wire Interface Instruction Byte

MSB							LSB
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation.

N1 and N0, Bit 6 and Bit 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The translation for the number of bytes to be transferred is listed in Table 12.

A4, A3, A2, A1, and A0—Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0, respectively, of the instruction byte—determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the device, based on the LSB-first bit (Register 0x00, Bit 6).

Table 12. Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer two bytes
1	0	Transfer three bytes
1	1	Transfer four bytes

SERIAL INTERFACE PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and controls the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select (CSB)

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communication lines. The SDO and SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, configuring the SDIO pin as unidirectional.

Serial Data Out (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by the LSB-/MSB-first register bit (Register 0x00, Bit 6). The default is MSB-first format (LSB/MSB first = 0).

When MSB-first format is selected (LSB/MSB first = 0), the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from high address to low address. In MSB-first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB/MSB first = 1 (LSB first) the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte, followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB-first format is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB-first format is active.

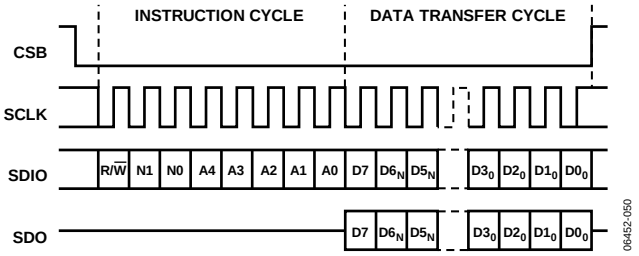

Figure 53. Serial Register Interface Timing, MSB First

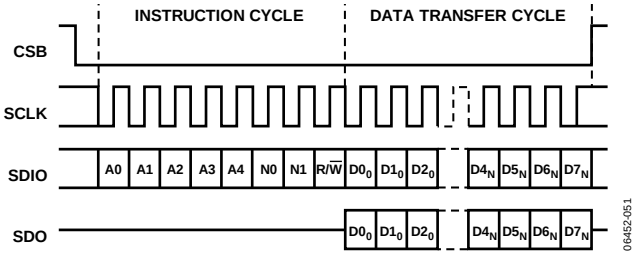

Figure 54. Serial Register Interface Timing, LSB First

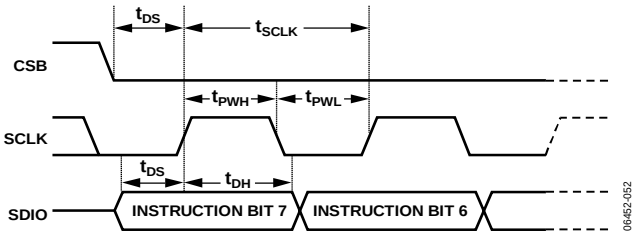

Figure 55. Timing Diagram for 3-Wire Interface Register Write

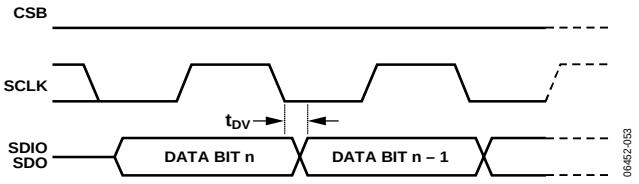

Figure 56. Timing Diagram for 3-Wire Interface Register Read

3-WIRE INTERFACE REGISTER MAP

Note that all unused register bits should be kept at the device default values.

Table 13.

Register Name	Address										
	Hex	Decimal	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Comm	0x00	00	SDIO bidirectional	LSB/MSB first	Software reset	Power-down mode	Auto power-down enable		PLL lock indicator (read only)		0x00
Digital Control	0x01	01	Interpolation Factor[1:0]		Filter Modulation Mode[3:0]				DATACLK Delay[4]	Zero stuffing enable	0x00
	0x02	02	Data format	Single port	Real mode	DATACLK delay enable	Inverse sinc enable	DATACLK invert	TxEnable invert	Q first	0x00
Sync Control	0x03	03	DATACLK delay mode	Reserved (set to 0)	DATACLK Divide[1:0]		Data Timing Margin[3:0]				0x00
	0x04	04	DATACLK Delay[3:0]				SYNC_O Divide[2:0]			SYNC_O Delay[4]	0x00
	0x05	05	SYNC_O Delay[3:0]				SYNC_I Ratio[2:0]			SYNC_I Delay[4]	0x00
	0x06	06	SYNC_I Delay[3:0]				SYNC_I Timing Margin[3:0]				0x00
	0x07	07	SYNC_I enable	SYNC_O enable	SYNC_O triggering edge	Clock State[4:0]					0x00
PLL Control	0x08	08	PLL Band Select[5:0]						PLL VCO Drive[1:0]		0xE7
	0x09	09	PLL enable	PLL VCO Divide Ratio[1:0]		PLL Loop Divide Ratio[1:0]		PLL Bias[2:0]			0x52
Misc. Control	0x0A	10	VCO Control Voltage[2:0] (read only)			PLL Loop Bandwidth[4:0]					0x1F
I DAC Control	0x0B	11	I DAC Gain Adjustment[7:0]								0xF9
	0x0C	12	I DAC sleep	I DAC power-down					I DAC Gain Adjustment[9:8]		0x01
Aux DAC1 Control	0x0D	13	Auxiliary DAC1 Data[7:0]								0x00
	0x0E	14	Auxiliary DAC1 sign	Auxiliary DAC1 current direction	Auxiliary DAC1 power-down				Auxiliary DAC1 Data[9:8]		0x00
Q DAC Control	0x0F	15	Q DAC Gain Adjustment[7:0]								0xF9
	0x10	16	Q DAC sleep	Q DAC power-down					Q DAC Gain Adjustment[9:8]		0x01
Aux DAC2 Control	0x11	17	Auxiliary DAC2 Data[7:0]								0x00
	0x12	18	Auxiliary DAC2 sign	Auxiliary DAC2 current direction	Auxiliary DAC2 power-down				Auxiliary DAC2 Data[9:8]		0x00
	0x13 to 0x18	19 to 24	Reserved								
Interrupt	0x19	25	Data timing error IRQ	Sync timing error IRQ		Data timing error type	Data timing error IRQ enable	Sync timing error IRQ enable		Internal sync loopback	0x00
Version	0x1F	31	Version[7:0]								0x07

Table 14. 3-Wire Interface Register Description

Register Name	Register Address	Bits	Parameter	Function	Default
Comm	0x00	7	SDIO bidirectional	0: use SDIO pin as input data only. 1: use SDIO as both input and output data.	0
	0x00	6	LSB/MSB first	0: first bit of serial data is MSB of data byte. 1: first bit of serial data is LSB of data byte.	0
	0x00	5	Software reset	Bit must be written with a 1 and then 0 to soft reset the 3-wire interface register map.	0
	0x00	4	Power-down mode	0: all circuitry is active. 1: disable all digital and analog circuitry, only 3-wire interface port is active.	
	0x00	3	Auto power-down enable	Controls auto power-down mode. See the Power-Down and Sleep Modes section.	0
	0x00	1	PLL lock indicator (read only)	0: PLL is not locked. 1: PLL is locked.	
Digital Control	0x01	7:6	Interpolation Factor[1:0]	00: 1× interpolation. 01: 2× interpolation 10: 4× interpolation. 11: 8× interpolation.	00
	0x01	5:2	Filter Modulation Mode[3:0]	See Table 19 for filter modes.	0000
	0x01	1	DATACLK Delay[4]	Sets MSB of delay of REFCLK input to DATACLK output.	0
	0x01	0	Zero stuffing enable	0: zero stuffing off. 1: zero stuffing on.	0
	0x02	7	Data format	0: twos compliment. 1: unsigned binary.	0
	0x02	6	Single port	0: both P1D and P2D data ports enabled. 1: data for both DACs received on P1D data port.	0
	0x02	5	Real mode	0: enable Q path for signal processing. 1: disable Q path data (internal Q channel clocks disabled, I and Q modulators disabled).	0
	0x02	4	DATACLK delay enable	Enables the DATACLK delay feature. More details on this feature are shown in the Optimizing the Data Input Timing section.	
	0x02	3	Inverse sinc enable	0: inverse sinc filter disabled. 1: inverse sinc filter enabled.	0
	0x02	2	DATACLK invert	0: output DATACLK same phase as internal data sampling clock, DCLK_SMP signal. 1: output DATACLK opposite phase as internal data sampling clock, DCLK_SMP signal.	0
	0x02	1	TxEnable invert	Inverts the polarity of Pin 39, the TXENABLE input pin (also functions as IQSELECT).	0
	0x02	0	Q first	0: in interleaved mode, the I data precedes the Q data on the input port. 1: in interleaved mode, the Q data precedes the I data on the input port.	

Register Name	Register Address	Bits	Parameter	Function	Default
Sync Control	0x03	7	Reserved	Should always be set to 0.	0
	0x03	6	Reserved	Should always be set to 1.	0
	0x03	5:4	DATACLK Divide[1:0]	DATACLK output divider value. 00: divide by 1. 01: divide by 2. 10: divide by 4. 11: divide by 1.	00
	0x03	3:0	Data Timing Margin[3:0]	Sets the timing margin required to prevent the data timing error IRQ bit from being asserted.	0000
	0x04	7:4	DATACLK Delay[3:0]	Sets delay of REFCLK input to DATACLK output (see Table 29 for details).	0000
	0x04	3:1	SYNC_O Divide[2:0]	The frequency of the SYNC_O signal is equal to f_{DAC}/N, where N is set as follows: 000: N = 32. 001: N = 16. 010: N = 8. 011: N = 4. 100: N = 2. 101: N = 1. 110: N = undefined. 111: N = undefined.	000
	0x04	0	SYNC_O Delay[4]	The SYNC_O Delay[4:0] value programs the value of the delay line of the SYNC_O signal. The delay of SYNC_O is relative to REFCLK. The delay line resolution is 80 ps per step. 00000: nominal delay. 00001: adds 80 ps delay to SYNC_O. 00010: adds 160 ps delay to SYNC_O. … 11111: Adds 2480 ps delay to SYNC_O.	0
	0x05	7:4	SYNC_O Delay[3:0]		0000
	0x05	3:1	SYNC_I Ratio[2:0]	This value controls the number of SYNC_I input pulses required to generate a synchronization pulse (see Table 30 for details).	000
	0x05	0	SYNC_I Delay[4]	The SYNC_I Delay[4:0] value programs the value of the delay line of the SYNC_I signal. The delay line resolution is 80 ps per step. 00000: nominal delay. 00001: adds 80 ps delay to SYNC_I. 00010: adds 160 ps delay to SYNC_I. … 11111: adds 2480 ps delay to SYNC_I.	0
	0x06	7:4	SYNC_I Delay[3:0]		0000
	0x06	3:0	SYNC_I Timing Margin[3:0]		0000
	0x07	7	SYNC_I enable	1: enables the SYNC_I input.	0
	0x07	6	SYNC_O enable	1: enables the SYNC_O output.	0
	0x07	5	SYNC_O triggering edge	0: SYNC_O changes on REFCLK falling edge. 1: SYNC_O changes on REFCLK rising edge.	0
	0x07	4:0	Clock State[4:0]	This value determines the state of the internal clock generation state machine upon synchronization.	0

Register Name	Register Address	Bits	Parameter	Function	Default
PLL Control	0x08	7:2	PLL Band Select[5:0]	This sets the operating frequency range of the VCO. For details (see Table 23).	111001
	0x08	1:0	PLL VCO Drive[1:0]	Controls the signal strength of the VCO output. Set to 11 for optimal performance.	11
	0x09	7	PLL enable	0: PLL off, DAC sample clock is sourced directly by the REFCLK input. 1: PLL on, DAC clock synthesized internally from REFCLK input via PLL clock multiplier.	0
	0x09	6:5	PLL VCO Divide Ratio[1:0]	Sets the value of the VCO output divider, which determines the ratio of the VCO output frequency to the DAC sample clock frequency, f_{VCO}/f_{DACCLK}. 00: $f_{VCO}/f_{DACCLK} = 1$. 01: $f_{VCO}/f_{DACCLK} = 2$. 10: $f_{VCO}/f_{DACCLK} = 4$. 11: $f_{VCO}/f_{DACCLK} = 8$.	10
	0x09	4:3	PLL Loop Divide Ratio[1:0]	Sets the value of the DACCLK divider, which determines the ratio of the DAC sample clock frequency to the REFCLK frequency, f_{DACCLK}/f_{REFCLK}. 00: $f_{DACCLK}/f_{REFCLK} = 2$. 01: $f_{DACCLK}/f_{REFCLK} = 4$. 10: $f_{DACCLK}/f_{REFCLK} = 8$. 11: $f_{DACCLK}/f_{REFCLK} = 16$.	10
	0x09	2:0	PLL Bias[2:0]	Controls VCO bias current. Set to 011 for optimal performance.	010
Misc. Control	0x0A	7:5	VCO Control Voltage[2:0] (read only)	000 to 111, proportional to voltage at VCO control voltage input, readback only. A value of 011 indicates the VCO centered in its frequency range.	000
	0x0A	4:0	PLL Loop Bandwidth[4:0]	Controls the bandwidth of the PLL filter. Increasing the value lowers the loop bandwidth. Set to 01111 for optimal performance.	11111
I DAC Control	0x0C	1:0	I DAC Gain Adjustment[9:8]	The I DAC Gain Adjustment[9:0] value is the I DAC 10-bit gain setting word. Bit 9 is the MSB and Bit 0 is the LSB.	01
	0x0B	7:0	I DAC Gain Adjustment[7:0]		11111001
	0x0C	7	I DAC sleep	0: I DAC on. 1: I DAC off, but reference remains powered.	0
	0x0C	6	I DAC power-down	0: I DAC on. 1: I DAC off.	0
Aux DAC1 Control	0x0E	1:0	Auxiliary DAC1 Data[9:8]	The auxiliary DAC 1 Data [9:0] value is the Aux DAC1 10-bit output current control word. Magnitude of the auxiliary DAC current increases with increasing value. Bit 9 is the MSB and Bit 0 is the LSB.	00
	0x0D	7:0	Auxiliary DAC1 Data[7:0]		00000000
	0x0E	7	Auxiliary DAC1 sign	0: AUX1_P active. 1: AUX1_N active.	0
	0x0E	6	Auxiliary DAC1 current direction	0: source. 1: sink.	0
	0x0E	5	Auxiliary DAC1 power-down	0: auxiliary DAC1 on. 1: auxiliary DAC1 off.	0
Q DAC Control	0x10	1:0	Q DAC Gain Adjustment[9:8]	The Q DAC Gain Adjustment[9:0] value is the Q DAC 10-bit gain setting word. Bit 9 is the MSB and Bit 0 is the LSB.	01
	0x0F	7:0	Q DAC Gain Adjustment[7:0]		11111001
	0x10	7	Q DAC sleep	0: Q DAC on. 1: Q DAC off.	0
	0x10	6	Q DAC power-down	0: Q DAC on. 1: Q DAC off.	0

Register Name	Register Address	Bits	Parameter	Function	Default
AUX DAC2 Control	0x12	1:0	Auxiliary DAC2 Data[9:8]	Auxiliary DAC2 Data[9:0] is the 10-bit output current control word. Magnitude of the auxiliary DAC current increases with increasing value. Bit 9 is the MSB and Bit 0 is the LSB.	00
	0x11	7:0	Auxiliary DAC2 Data[7:0]		00000000
	0x12	7	Auxiliary DAC2 sign	0: AUX2_P active. 1: AUX2_N active.	0
	0x12	6	Auxiliary DAC2 current direction	0: source. 1: sink.	0
	0x12	5	Auxiliary DAC2 power-down	0: auxiliary DAC2 on. 1: auxiliary DAC2 off.	0
	0x13 to 0x18		Reserved		
Interrupt	0x19	7	Data timing error IRQ	Read only. Active high indicates a timing violation occurred on the input data port. The IRQ is latched. This bit is cleared when the Interrupt register is read.	0
	0x19	6	Sync timing error IRQ	Read only. Active high indicates a timing violation occurred on the SYNC_I input. The IRQ is latched. This bit is cleared when the Interrupt register is read.	0
	0x19	4	Data timing error type	Read only. Indicates the timing error type. 0: hold time violation. 1: setup time violation. Meaningful when data timing error IRQ is active.	0
	0x19	3	Data timing error IRQ enable	0: data timing error IRQ is masked. 1: data timing error IRQ is enabled.	0
	0x19	2	Sync timing error IRQ enable	0: sync timing error IRQ is masked. 1: sync timing error IRQ is enabled.	0
	0x19	0	Internal sync loopback	The received SYNC_O signal is looped back to the SYNC_I signal.	0
Version	0x1F	7:0	Version[7:0]	Indicates device hardware revision number.	00000111

INTERPOLATION FILTER ARCHITECTURE

The AD9776A/AD9778A/AD9779A can provide up to 8× interpolation, or the interpolation filters can be entirely disabled. It is important to note that the input signal should be backed off by approximately 0.01 dB from full scale to avoid overflowing the interpolation filters. The coefficients of the low-pass filters and the inverse sinc filter are given in Table 15, Table 16, Table 17, and Table 18. Spectral plots for the filter responses are shown in Figure 57, Figure 58, and Figure 59.

Table 15. Low-Pass Filter 1

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(55)	−4
H(2)	H(54)	0
H(3)	H(53)	+13
H(4)	H(52)	0
H(5)	H(51)	−34
H(6)	H(50)	0
H(7)	H(49)	+72
H(8)	H(48)	0
H(9)	H(47)	−138
H(10)	H(46)	0
H(11)	H(45)	+245
H(12)	H(44)	0
H(13)	H(43)	−408
H(14)	H(42)	0
H(15)	H(41)	+650
H(16)	H(40)	0
H(17)	H(39)	−1003
H(18)	H(38)	0
H(19)	H(37)	+1521
H(20)	H(36)	0
H(21)	H(35)	−2315
H(22)	H(34)	0
H(23)	H(33)	+3671
H(24)	H(32)	0
H(25)	H(31)	−6642
H(26)	H(30)	0
H(27)	H(29)	+20,755
H(28)		+32,768

Table 16. Low-Pass Filter 2

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	−2
H(2)	H(22)	0
H(3)	H(21)	+17
H(4)	H(20)	0
H(5)	H(19)	−75
H(6)	H(18)	0
H(7)	H(17)	+238
H(8)	H(16)	0
H(9)	H(15)	−660
H(10)	H(14)	0
H(11)	H(13)	+2530
H(12)		+4096

Table 17. Low-Pass Filter 3

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(15)	−39
H(2)	H(14)	0
H(3)	H(13)	+273
H(4)	H(12)	0
H(5)	H(11)	−1102
H(6)	H(10)	0
H(7)	H(9)	+4964
H(8)		+8192

Table 18. Inverse Sinc Filter

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(9)	+2
H(2)	H(8)	−4
H(3)	H(7)	+10
H(4)	H(6)	−35
H(5)		+401

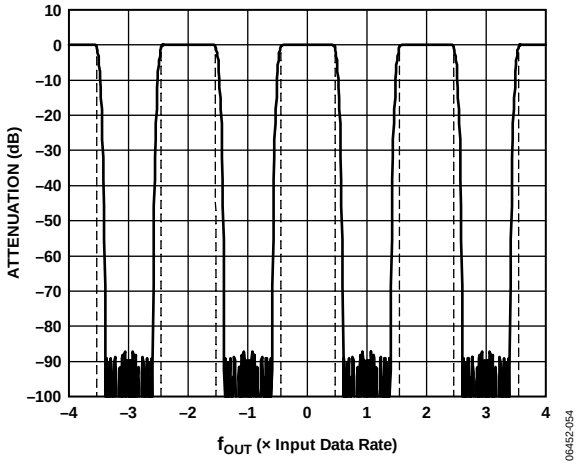

Figure 57. 2× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

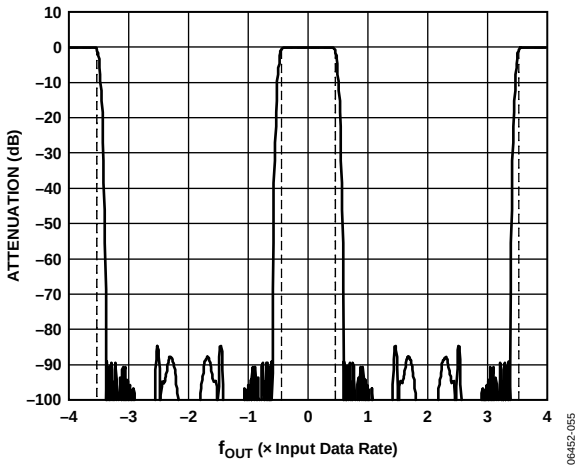

Figure 58. 4× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

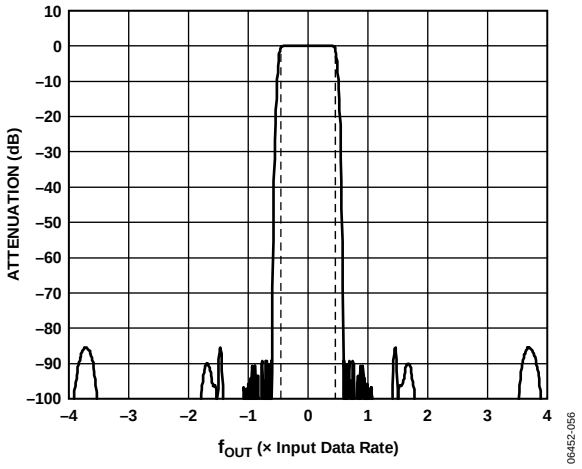

Figure 59. 8× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

With the interpolation filter and modulator combined, the incoming signal can be placed anywhere within the Nyquist region of the DAC output sample rate. When the input signal is complex, this architecture allows modulation of the input signal to positive or negative Nyquist regions (see Table 19).

The Nyquist regions of up to 4× the input data rate can be seen in Figure 60.

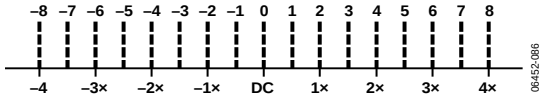

Figure 60. Nyquist Zones

Figure 57, Figure 58, and Figure 59 show the low-pass response of the digital filters with no modulation. By turning on the modulation feature, the response of the digital filters can be tuned to anywhere within the DAC bandwidth. As an example, Figure 61 to Figure 67 show the nonshifted mode filter responses for 8× interpolation (refer to Table 19 for shifted/nonshifted mode filter responses).

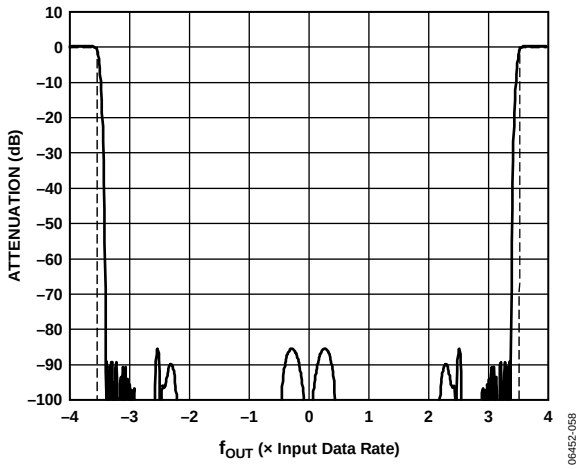

Figure 61. Interpolation/Modulation Combination of $4f_{DAC}/8$ Filter

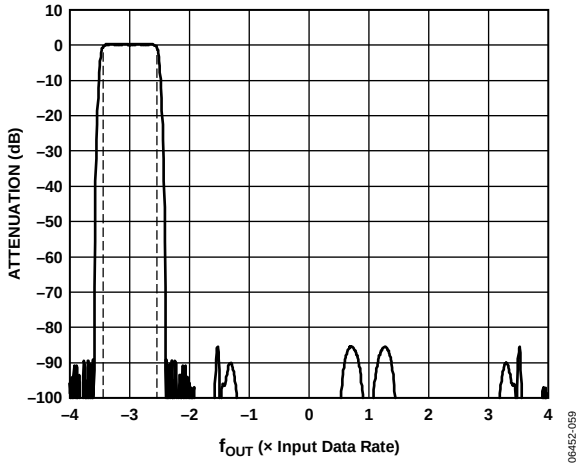

Figure 62. Interpolation/Modulation Combination of $-3f_{DAC}/8$ Filter

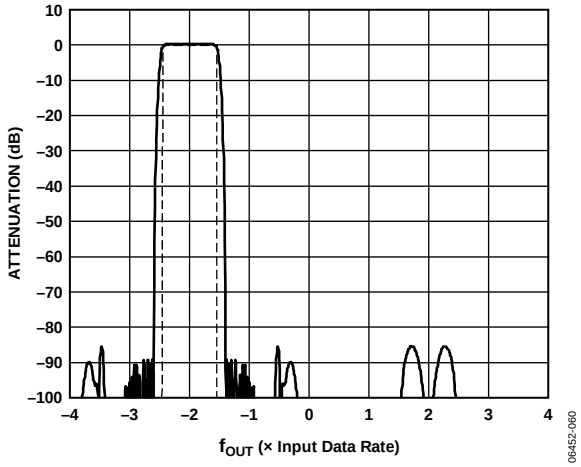

Figure 63. Interpolation/Modulation Combination of $-2f_{DAC}/8$ Filter

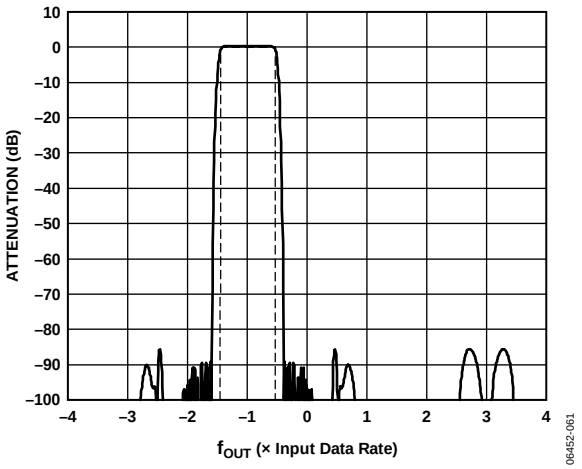

Figure 64. Interpolation/Modulation Combination of $-f_{DAC}/8$ Filter

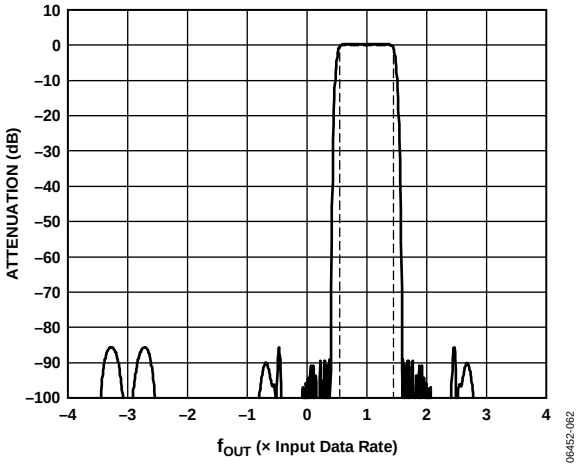

Figure 65. Interpolation/Modulation Combination of $f_{DAC}/8$ Filter

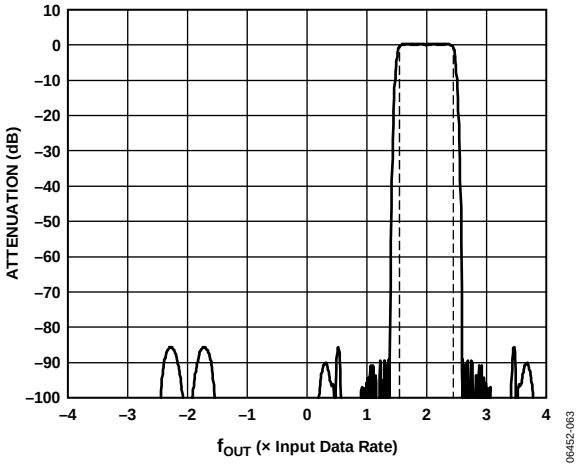

Figure 66. Interpolation/Modulation Combination of $2f_{DAC}/8$ Filter

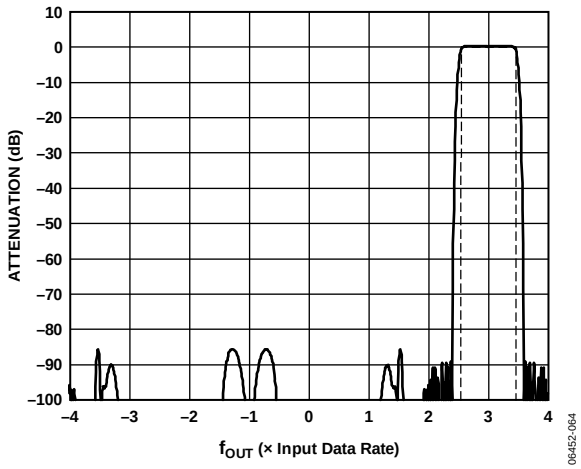

Figure 67. Interpolation/Modulation Combination of $3f_{DAC}/8$ Filter

Shifted mode filter responses allow the pass band to be centered around ±0.5 f_{DATA}, ±1.5 f_{DATA}, ±2.5 f_{DATA}, and ±3.5 f_{DATA}. Switching to the shifted mode response does not affect the center frequency of the signal. Instead, the pass band of the filter is simply shifted. For example, use the response shown in Figure 67 and assume the signal in-band is a complex signal over the bandwidth 3.2 f_{DATA} to 3.3 f_{DATA}. If the shifted mode filter response is then selected, the pass band becomes centered at 3.5 f_{DATA}. However, the signal remains at the same place in the spectrum. The shifted mode capability allows the filter pass band to be placed anywhere in the DAC Nyquist bandwidth.

The AD9776A/AD9778A/AD9779A are dual DACs with internal complex modulators built into the interpolating filter response. In dual channel mode, the devices expect the real and imaginary components of a complex signal at Digital Input Port 1 and Digital Input Port 2 (I and Q, respectively). The DAC outputs then represent the real and imaginary components of the input signal, modulated by the complex carrier ($f_{DAC}/2$, $f_{DAC}/4$, or $f_{DAC}/8$).

With Register 0x02, Bit 6, set, the device accepts interleaved data on Port 1 in the I, Q, I, Q … sequence. Note that in interleaved mode, the channel data rate at the beginning of the I and Q data paths is now half the input data rate because of the interleaving. The maximum input data rate is still subject to the maximum specification of the device. This limits the synthesis bandwidth available at the input in interleaved mode.

With Register 0x02, Bit 5 (the real mode bit), set, the Q channel and the internal I and Q digital modulation are turned off. The output spectrum at the I DAC then represents the signal at Digital Input Port 1, interpolated by 1×, 2×, 4×, or 8×.

The general recommendation is that if the desired signal is within ±0.4 × f_{DATA}, use the nonshifted filter mode. Outside of this, the shifted filter mode should be used. In any situation, the total bandwidth of the signal is less than 0.8 × f_{DATA}.

Table 19. Interpolation Filter Modes, (Register 0x01, Bits[5:2])

Interpolation Factor[7:6]	Filter Modulation Mode[5:2]	Modulation	Nyquist Zone Pass Band	Frequency Normalized to f_{DAC}			Comments
				Low	Center	High	
8	0x00	DC	0	−0.05	0	+0.05	In 8× interpolation; BW (min) = 0.0375 × f_{DAC} BW (max) = 0.1 × f_{DAC}
8	0x01	DC shifted	+1	+0.0125	+0.0625	+0.1125	
8	0x02	$f_{DAC}/8$	+2	+0.075	+0.125	+0.175	
8	0x03	$f_{DAC}/8$ shifted	+3	+0.1375	+0.1875	+0.2375	
8	0x04	$f_{DAC}/4$	+4	+0.2	+0.25	+0.3	
8	0x05	$f_{DAC}/4$ shifted	+5	+0.2625	+0.3125	+0.3625	
8	0x06	$3f_{DAC}/8$	+6	+0.325	+0.375	+0.425	
8	0x07	$3f_{DAC}/8$ shifted	+7	+0.3875	+0.4375	+0.4875	
8	0x08	$f_{DAC}/2$	±8	−0.55	−0.5	−0.45	
8	0x09	$f_{DAC}/2$ shifted	−7	−0.4875	−0.4375	−0.3875	
8	0x0A	$-3f_{DAC}/8$	−6	−0.425	−0.375	−0.343	
8	0x0B	$-3f_{DAC}/8$ shifted	−5	−0.3625	−0.3125	−0.2625	
8	0x0C	$-f_{DAC}/4$	−4	−0.3	−0.25	−0.2	
8	0x0D	$-f_{DAC}/4$ shifted	−3	−0.2375	−0.1875	−0.1375	
8	0x0E	$-f_{DAC}/8$	−2	−0.175	−0.125	−0.075	
8	0x0F	$-f_{DAC}/8$ shifted	−1	−0.1125	−0.0625	−0.0125	
4	0x00	DC	0	−0.1	0	+0.1	In 4× interpolation; BW (min) = 0.075 × f_{DAC} BW (max) = 0.2 × f_{DAC}
4	0x01	DC shifted	+1	+0.025	+0.125	+0.225	
4	0x02	$f_{DAC}/4$	+2	+0.15	+0.25	+0.35	
4	0x03	$f_{DAC}/4$ shifted	+3	+0.275	+0.375	+0.475	
4	0x04	$f_{DAC}/2$	±4	−0.6	−0.5	−0.4	
4	0x05	$f_{DAC}/2$ shifted	−3	−0.475	−0.375	−0.275	
4	0x06	$-f_{DAC}/4$	−2	−0.35	−0.25	−0.15	
4	0x07	$-f_{DAC}/4$ shifted	−1	−0.225	−0.125	−0.025	
2	0x00	DC	0	−0.2	0	+0.2	In 2× interpolation; BW (min) = 0.15 × f_{DAC} BW (max) = 0.4 × f_{DAC}
2	0x01	DC shifted	+1	+0.05	+0.25	+0.45	
2	0x02	$f_{DAC}/2$	±2	−0.7	−0.5	−0.3	
2	0x03	$f_{DAC}/2$ shifted	−1	−0.45	−0.25	−0.05	

INTERPOLATION FILTER BANDWIDTH LIMITS

The AD9776A/AD9778A/AD9779A use a novel interpolation filter architecture that allows DAC IF frequencies to be generated anywhere in the spectrum. Figure 68 shows the traditional choice of DAC IF output bandwidth placement. Note that there are no possible filter modes in which the carrier can be placed near 0.5 × f_{DATA}, 1.5 × f_{DATA}, 2.5 × f_{DATA}, and so on.

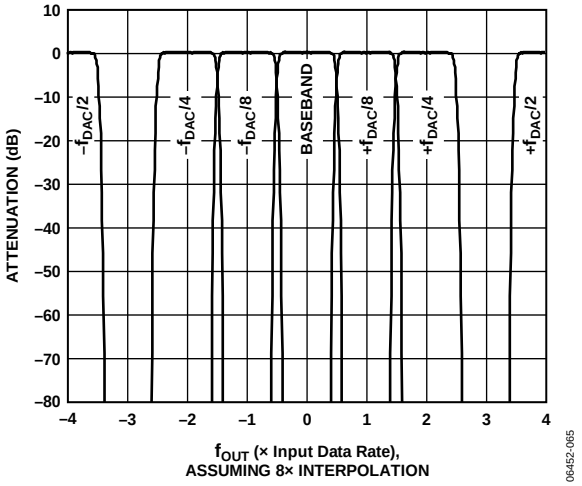

Figure 68. Traditional Bandwidth Options for TxDAC Output IF

The filter architecture not only allows the interpolation filter pass bands to be centered in the middle of the input Nyquist zones (as explained in this section), but also allows the possibility of a 3 × f_{DAC}/8 modulation mode when interpolating by 8. With all of these filter combinations, a carrier of given bandwidth can be placed anywhere in the spectrum and fall into a possible pass band of the interpolation filters. The possible bandwidths accessible with the filter architecture are shown in Figure 69 and Figure 70. Note that the shifted and nonshifted filter modes are all accessible by programming the filter mode for a particular interpolation rate.

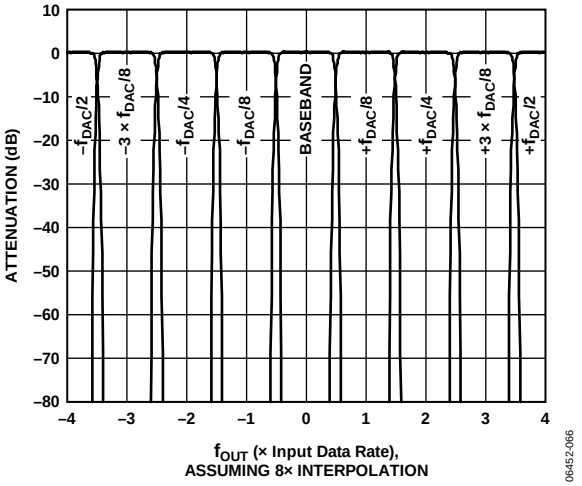

Figure 69. Nonshifted Bandwidths Accessible with the Filter Architecture

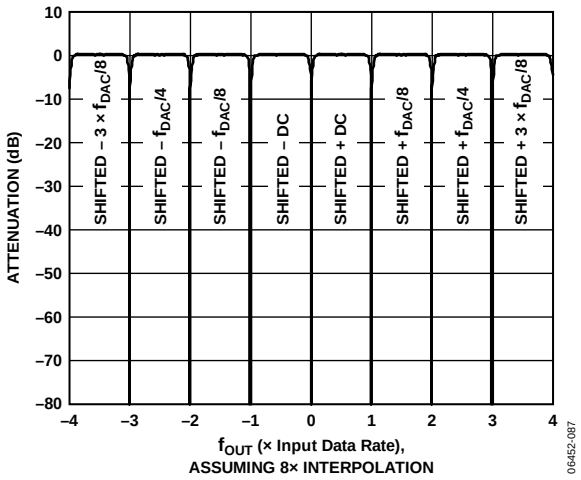

Figure 70. Shifted Bandwidths Accessible with the Filter Architecture

With this filter architecture, a signal placed anywhere in the spectrum is possible. However, the signal bandwidth is limited by the input sample rate of the DAC and the specific placement of the carrier in the spectrum. The bandwidth restriction resulting from the combination of filter response and input sample rate is often referred to as the synthesis bandwidth, because this is the largest bandwidth that the DAC can synthesize.

The maximum bandwidth condition exists if the carrier is placed directly in the center of one of the filter pass bands. In this case, the total 0.1 dB bandwidth of the interpolation filters is equal to 0.8 × f_{DATA}. As Table 19 shows, the synthesis bandwidth as a fraction of the DAC output sample rate drops by a factor of 2 for every doubling of interpolation rate. The minimum bandwidth condition exists, for example, if a carrier is placed at 0.25 × f_{DATA}. In this situation, if the nonshifted filter response is enabled, the high end of the filter response cuts off at 0.4 × f_{DATA}, thus limiting the high end of the signal bandwidth. If the shifted filter response is instead enabled, then the low end of the filter response cuts off at 0.1 × f_{DATA}, thus limiting the low end of the signal bandwidth. The minimum bandwidth specification that applies for a carrier at 0.25 × f_{DATA} is therefore 0.3 × f_{DATA}. The minimum bandwidth behavior is repeated over the spectrum for carriers placed at (±n ± 0.25) × f_{DATA}, where n is any integer.

Digital Modulation

The digital quadrature modulation occurs within the interpolation filter. The modulation shifts the frequency spectrum of the incoming data by the frequency offset selected. The frequency offsets available are multiples of the input data rate. The modulation is equivalent to multiplying the quadrature input signal by a complex carrier signal, C(t), of the following form:

$$C(t) = \cos(\omega_c t) + j \sin(\omega_c t)$$

As shown in Table 20, the mixing functions of most of the modes result in cross-coupling of samples between the I and Q channels. The I and Q channels only operate independently with the $f_S/2$ mode. This means that real modulation using both the I and Q DAC outputs can only be done in the $f_S/2$ mode. All other modulation modes require complex input data and produce complex output signals.

Table 20. Modulation Mixing Sequences

Modulation	Mixing Sequence
$f_{DAC}/2$	I = I, −I, I, −I, …
	Q = Q, −Q, Q, −Q, …
$f_{DAC}/4$	I = I, Q, −I, −Q, …
	Q = Q, −I, −Q, I, …
$-f_{DAC}/4$	I = I, −Q, −I, Q, …
	Q = Q, I, −Q, −I, …
$f_{DAC}/8$	I = I, r(I + Q), Q, r(−I + Q), −I, −r(I + Q), −Q, r(I − Q), …
	Q = Q, r(Q − I), −I, −r(Q + I), −Q, r(−Q + I), I, r(Q + I), …
	where r = √2/2

INVERSE SINC FILTER

The inverse sinc filter is implemented as a nine-tap FIR filter. It is designed to provide less than ±0.05 dB pass-band ripple up to a frequency of 0.4 × f_{DATA}. To provide the necessary gain at the upper end of the pass band, the inverse sinc filter has an intrinsic insertion loss of 3.4 dB. The transfer function is shown in Figure 71 and the tap coefficients are given in Table 21.

Table 21. Inverse Sinc Filter

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(9)	+2
H(2)	H(8)	−4
H(3)	H(7)	+10
H(4)	H(6)	−35
H(5)	N/A	+401

The inverse sinc filter is disabled by default. It can be enabled by setting the inverse sinc enable bit (Bit 3) in Register 0x02.

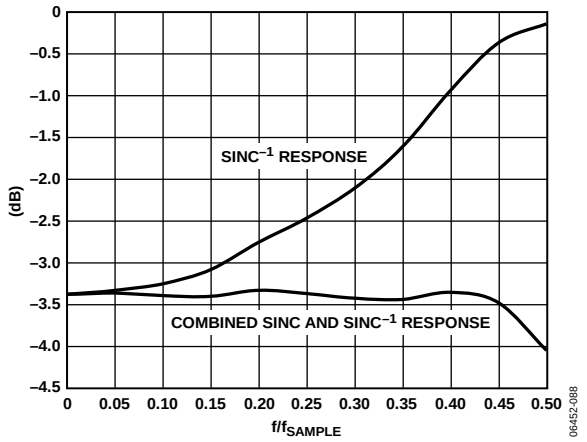

Figure 71. Transfer Function of Inverse Sinc Filter with the DAC sin(x)/x Output

SOURCING THE DAC SAMPLE CLOCK

The AD9776A/AD9778A/AD9779A offer two modes of sourcing the DAC sample clock (DACCLK). The first mode employs an on-chip clock multiplier that accepts a reference clock operating at the lower input frequency, most commonly the data input frequency. The on-chip PLL then multiplies the reference clock up to a higher frequency, which can then be used to generate all of the internal clocks required by the DAC. The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier removes the burden of generating and distributing the high speed DACCLK at the board level. The second mode bypasses the clock multiplier circuitry and allows DACCLK to be directly sourced through the REFCLK pins. This mode enables the user to source a very high quality input clock directly to the DAC core. Sourcing the DACCLK directly through the REFCLK pins may be necessary in demanding applications that require the lowest possible DAC output noise at higher output frequencies.

In either case (that is, using the on-chip clock multiplier or sourcing the DACCLK directly though the REFCLK pins), it is necessary that the REFCLK signal have low jitter to maximize the DAC noise performance.

DIRECT CLOCKING

When the PLL is disabled (Register 0x09, Bit 7 = 0), the REFCLK input is used directly as the DAC sample clock (DACCLK). The frequency of REFCLK needs to be the input data rate multiplied by the interpolation factor (and by an additional factor of 2 if zero stuffing is enabled).

CLOCK MULTIPLICATION

When the PLL is enabled (Register 0x09, Bit 7 = 1), the clock multiplication circuit generates the DAC sample clock from the lower rate REFCLK input. The functional diagram of the clock multiplier is shown in Figure 72.

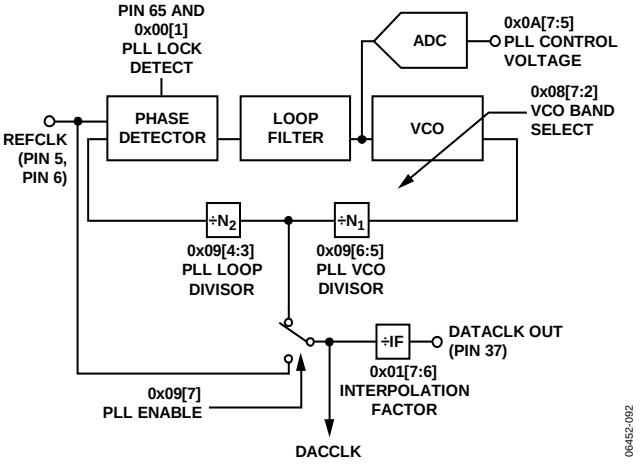

Figure 72. Clock Multiplier Circuit

The clock multiplier circuit operates such that the VCO outputs a frequency, f_{VCO}, equal to the REFCLK input signal frequency multiplied by N1 × N2.

$$f_{VCO} = f_{REFCLK} \times (N1 \times N2)$$

The DAC sample clock frequency, f_{DACCLK}, is equal to

$$f_{DACCLK} = f_{REFCLK} \times N2$$

When the PLL is enabled, the maximum input clock frequency f_{REFCLK} is 250 MHz. The values of N1 and N2 must be chosen to keep f_{VCO} in the optimal operating range of 1.0 GHz to 2.0 GHz. Once the VCO output frequency is known, the correct PLL band select (Register 0x08, Bits[7:2]) value can be chosen.

PLL Bias Settings

There are three bias settings for the PLL circuitry that should be programmed to their nominal values. The PLL values shown in Table 22 are the recommended settings for these parameters.

Table 22. PLL Settings

PLL 3-Wire Interface Control	Address		Optimal Setting
	Register	Bits	
PLL Loop Bandwidth	0x0A	[4:0]	01111
PLL VCO Drive	0x08	[1:0]	11
PLL Bias	0x09	[2:0]	011

The PLL loop bandwidth variable configures the bandwidth of the PLL loop filter. A setting of 00000 configures the bandwidth to be approximately 1 MHz. A setting of 11111 configures the bandwidth to be approximately 10 MHz. The optimal value of 01111 sets the loop bandwidth to be approximately 3 MHz.

Configuring the PLL Band Select Value

The PLL VCO has a valid operating range from approximately 1.0 GHz to 2.0 GHz. This range is covered in 63 overlapping frequency bands, as shown in Table 23. For any desired VCO output frequency, there are multiple valid PLL band select values. It is important to note that the data shown in Table 23 is for a typical device. Device-to-device variations can shift the actual VCO output frequency range by 30 MHz to 40 MHz. In addition, the VCO output frequency varies as a function of temperature. Therefore, it is required that the optimal PLL band select value be determined for each individual device at a particular operating temperature.

The device has an automatic PLL band select feature on chip. When this feature is enabled, the device determines the optimal PLL band setting for the device at the given temperature. This setting holds for a ±60°C temperature swing in ambient temperature. If the device is operated in an environment that experiences a larger temperature swing, an offset should be applied to the automatically selected PLL band.

Table 23. Typical VCO Frequency Range vs. PLL Band Select Value

PLL Lock Ranges Over Temperature, −40°C to +85°C		
	VCO Frequency Range (MHz)	
PLL Band Select	f_{LOW}	f_{HIGH}
111111 (63)	Auto mode	
111110 (62)	1975	2026
111101 (61)	1956	2008
111100 (60)	1938	1992
111011 (59)	1923	1977
111010 (58)	1902	1961
111001 (57)	1883	1942
111000 (56)	1870	1931
110111 (55)	1848	1915
110110 (54)	1830	1897
110101 (53)	1822	1885
110100 (52)	1794	1869
110011 (51)	1779	1853
110010 (50)	1774	1840
110001 (49)	1748	1825
110000 (48)	1729	1810
101111 (47)	1730	1794
101110 (46)	1699	1780
101101 (45)	1685	1766
101100 (44)	1684	1748
101011 (43)	1651	1729
101010 (42)	1640	1702
101001 (41)	1604	1681
101000 (40)	1596	1658
100111 (39)	1564	1639
100110 (38)	1555	1606
100101 (37)	1521	1600
100100 (36)	1514	1575
100011 (35)	1480	1553
100010 (34)	1475	1529
100001 (33)	1439	1505
100000 (32)	1435	1489

PLL Lock Ranges Over Temperature, −40°C to +85°C		
	VCO Frequency Range (MHz)	
PLL Band Select	f_{LOW}	f_{HIGH}
011111 (31)	1402	1468
011110 (30)	1397	1451
011101 (29)	1361	1427
011100 (28)	1356	1412
011011 (27)	1324	1389
011010 (26)	1317	1375
011001 (25)	1287	1352
011000 (24)	1282	1336
010111 (23)	1250	1313
010110 (22)	1245	1299
010101 (21)	1215	1277
010100 (20)	1210	1264
010011 (19)	1182	1242
010010 (18)	1174	1231
010001 (17)	1149	1210
010000 (16)	1141	1198
001111 (15)	1115	1178
001110 (14)	1109	1166
001101 (13)	1086	1145
001100 (12)	1078	1135
001011 (11)	1055	1106
001010 (10)	1047	1103
001001 (9)	1026	1067
001000 (8)	1019	1072
000111 (7)	998	1049
000110 (6)	991	1041
000101 (5)	976	1026
000100 (4)	963	1011
000011 (3)	950	996
000010 (2)	935	981
000001 (1)	922	966
000000 (0)	911	951

Configuring PLL Band Select with Temperature Sensing

The following procedure outlines a method for setting the PLL band select value for a device operating at a particular temperature that holds for a change in ambient temperature over the total −40°C to +85°C operating range of the device without further user intervention. Note that REFCLK must be applied to the device during this procedure.

1. Program the values of N1 (Register 0x09, Bits[6:5]) and N2 (Register 0x09, Bits[4:3]), along with the PLL settings shown in Table 22.
2. Set the PLL band (Register 0x08, Bits[7:2]) to 63 to enable PLL auto mode.
3. Wait for the PLL_LOCK pin or the PLL lock indicator (Register 0x00, Bit 1) to go high. This should occur within 5 ms.
4. Read back the 6-bit PLL band (Register 0x08, Bits[7:2]).
5. Based on the temperature when the PLL auto band select is performed, set the PLL band indicated in either Table 24 or Table 25 by rewriting the readback values into the PLL Band Select parameter (Register 0x08, Bits[7:2]).

This procedure requires temperature sensing upon start-up or reset of the device to optimally choose the PLL band select value that holds over the entire operating temperature range. If the optimal band is in the range of 0 to 31 (lower VCO frequency), refer to Table 24.

Table 24. Setting Optimal PLL Band, When Band Is in the Lower Range (0 to 31)

If System Startup Temperature Is	Set PLL Band as Follows
−40°C to −10°C	Set PLL band = readback band + 2
−10°C to +15°C	Set PLL band = readback band + 1
15°C to 55°C	Set PLL band = readback band
55°C to 85°C	Set PLL band = readback band − 1

If the optimal band is in the range of 32 to 62 (higher VCO frequency), refer to Table 25.

Table 25. Setting Optimal PLL Band, When Band Is in the Higher Range (32 to 62)

If System Startup Temperature Is	Set PLL Band as Follows
−40°C to −30°C	Set PLL band = readback band + 3
−30°C to −10°C	Set PLL band = readback band + 2
−10°C to +15°C	Set PLL band = readback band + 1
15°C to 55°C	Set PLL band = readback band
55°C to 85°C	Set PLL band = readback band − 1

Known Temperature Calibration with Memory

If temperature sensing is not available in the system, a factory calibration at a known temperature is another method for guaranteeing lock over temperature. Factory calibration can be performed as follows:

1. Program the values of N1 (Register 0x09, Bits[6:5]) and N2 (Register 0x09, Bits[4:3]), along with the PLL settings shown in Table 22.
2. Set the PLL band (Register 0x08, Bits[7:2]) to 63 to enable PLL auto mode.
3. Wait for the PLL_LOCK pin or the PLL lock indicator (Register 0x00, Bit 1) to go high. This should occur within 5 ms.
4. Read back the 6-bit PLL band (Register 0x08, Bits[7:2]).
5. Based on the temperature when the PLL auto band select is performed, store into nonvolatile memory the PLL band indicated in either Table 24 or Table 25. On system power-up or restart, load the stored PLL band value into the PLL band select parameter (Register 0x08, Bits[7:2]).

Set-and-Forget Device Option

If the PLL band select configuration methods described in the previous sections cannot be implemented in a particular system, there may be a screened device option that can satisfy the system requirements. This allows the user to preload a specific PLL band select value for all devices that holds over temperature. Example REFCLK and VCO frequencies are shown in Table 26.

Table 26. Typical VCO Frequency Range vs. PLL Band Select Value

f_{REFCLK} (MHz)	f_{VCO} (MHz)	Guaranteed PLL Band	Total PLL Divide Ratio
59.73335	955.7336	2	16
61.44	1966.08	61	32
67.2	1075.2	11	16
76.8	1228.8	20	16
80.01	1280	23	16
81.92	1310.72	25	16
92.16	1474.56	34	16
112.0	1792.0	50	16
119.4667	955.7336	2	8
122.88	1966.08	61	16

DRIVING THE REFCLK INPUT

The REFCLK input requires a low jitter differential drive signal. The signal level can range from 400 mV p-p differential to 1.6 V p-p differential centered about a 400 mV input common-mode voltage. Looking at the single-ended inputs, REFCLK+ or REFCLK–, each input pin can safely swing from 200 mV p-p to 800 mV p-p about the 400 mV common-mode voltage. Although these input levels are not directly LVDS compatible, REFCLK can be driven by an offset ac-coupled LVDS signal, as shown in Figure 73.

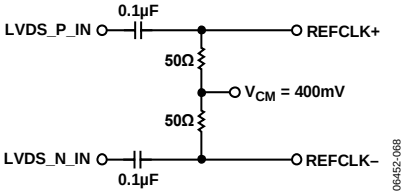

Figure 73. LVDS REFCLK Drive Circuit

If a clean sine clock is available, it can be transformer-coupled to REFCLK, as shown in Figure 73. Use of a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through a CMOS to LVDS translator, and then ac-coupled as described in this section. Alternatively, it can be transformer-coupled and clamped, as shown in Figure 74.

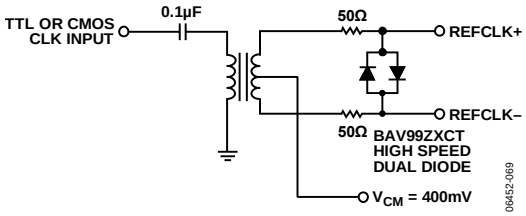

Figure 74. TTL or CMOS REFCLK Drive Circuit

A simple bias network for generating V_{CM} is shown in Figure 75. It is important to use CVDD18 and CGND for the clock bias circuit. Any noise or other signal that is coupled onto the clock is multiplied by the DAC digital input signal and can degrade DAC performance.

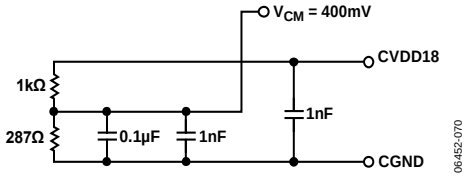

Figure 75. REFCLK V_{CM} Generator Circuit

FULL-SCALE CURRENT GENERATION

INTERNAL REFERENCE

Full-scale current on the I DAC and Q DAC can be set from 8.66 mA to 31.66 mA. Initially, the 1.2 V band gap reference is used to set up a current in an external resistor connected to I120 (Pin 75). A simplified block diagram of the reference circuitry is shown in Figure 76. The recommended value for the external resistor is 10 kΩ, which sets up an $I_{REFERENCE}$ in the resistor of 120 μA, which in turn provides a DAC output full-scale current of 20 mA. Because the gain error is a linear function of this resistor, a high precision resistor improves gain matching to the internal matching specification of the devices. Gain drift over temperature is also affected by this resistor. A resistor with a low temperature coefficient is recommended in applications requiring good gain stability.

Internal current mirrors provide a current-gain scaling, where the I DAC or Q DAC gain is a 10-bit word in the 3-wire interface port register (Register 0x0B, Register 0x0C, Register 0x0F, and Register 0x10). The default value for the DAC gain registers gives an I_{FS} of approximately 20 mA. I_{FS} is equal to

$$I_{FS} = \frac{1.2\,\text{V}}{R} \times \left(\frac{27}{12} + \left(\frac{6}{1024} \times DAC\ Gain \right) \right) \times 32$$

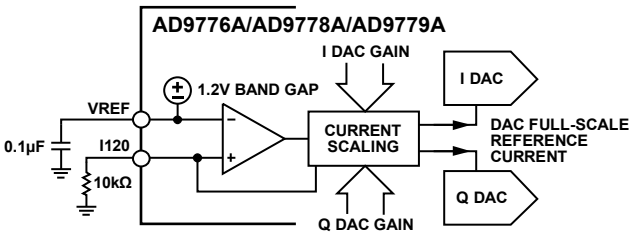

Figure 76. Reference Circuitry

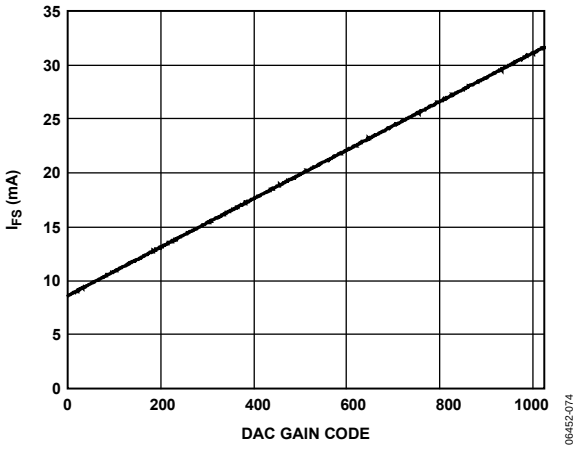

Figure 77. I_{FS} vs. DAC Gain Code

GAIN AND OFFSET CORRECTION

Analog quadrature modulators make it very easy to realize single sideband radios. However, there are several nonideal aspects of quadrature modulator performance. Among these analog degradations are

- Gain mismatch: The gain in the real and imaginary signal paths of the quadrature modulator may not be matched perfectly. This leads to less than optimal image rejection because the cancellation of the negative frequency image is less than perfect.
- Local oscillator (LO) feedthrough: The quadrature modulator has a finite dc-referred offset, as well as coupling from its LO port to the signal inputs. These can lead to significant spectral spurs at the frequency of the quadrature modulator LO.

The AD9776A/AD9778A/AD9779A have the capability to correct for both of these analog degradations. Note that these degradations drift over temperature; therefore, if close to optimal single sideband performance is desired, a scheme for sensing these degradations over temperature and correcting for them may be necessary.

I/Q CHANNEL GAIN MATCHING

Gain matching is achieved by adjusting the values in the DAC gain registers. For the I DAC, these values are in the 0x0B and 0x0C I DAC control registers. For the Q DAC, these values are in the 0x0F and 0x10 Q DAC control registers. These are 10-bit values. To perform gain compensation, raise or lower the value of one of these registers by a fixed step size and measure the amplitude of the unwanted image. If the unwanted image is increasing in amplitude, stop the procedure and try the same adjustment on the other DAC control register. Do this until the image rejection cannot be improved through further adjustment of these registers.

It should be noted that LO feedthrough compensation is independent of gain. However, gain compensation can affect the LO compensation because the gain compensation may change the common-mode level of the signal. The dc offset of some modulators is common-mode level dependent. Therefore, it is recommended that the gain adjustment be performed prior to LO compensation.

AUXILIARY DAC OPERATION

Two auxiliary DACs are provided on the AD9776A/AD9778A/AD9779A. The full-scale output current on these DACs is derived from the 1.2 V band gap reference and external resistor between the I120 pin and ground. The gain scale from the reference amplifier current ($I_{REFERENCE}$) to the auxiliary DAC reference current is 16.67 mA with the auxiliary DAC gain set to full scale (10-bit values, 3-wire interface Register 0x0D and 3-wire interface Register 0x11). This results in a full-scale current of approximately 2 mA for auxiliary DAC1 and auxiliary DAC2.

The auxiliary DAC structure is shown in Figure 78. Only one of the two output pins of the auxiliary DAC is active at a time. The inactive side goes to a high impedance state (>100 kΩ). The active output pin is chosen by writing to Bit 7 of Register 0x0E and Register 0x12.

The active output can act as either a current source or a current sink. When sourcing current, the output compliance voltage is 0 V to 1.6 V. When sinking current, the output compliance voltage is 0.8 V to 1.6 V. The output pin is chosen to be a current source or current sink by writing to Bit 6 of Register 0x0E and Register 0x12.

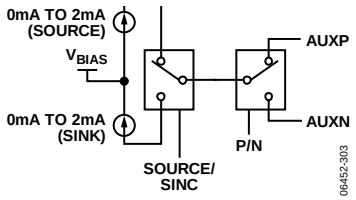

Figure 78. Auxiliary DAC Source/Sink for AD9776A/AD9778A/AD97779A

The magnitude of the auxiliary DAC1 current is controlled by the 0x0D and 0x0E auxiliary DAC1 control registers; the magnitude of the auxiliary DAC2 current is controlled by the 0x11 and 0x12 auxiliary DAC2 control registers. These auxiliary DACs have the ability to source or sink current. This is programmable via Bit 6 in either auxiliary DAC control register. The choice of sinking or sourcing should be made at circuit design time. There is no advantage to switching between current source or current sink once the circuit is in place.

The auxiliary DACs can be used for LO cancellation when the DAC output is followed by a quadrature modulator. This LO feedthrough is caused by the input-referred dc offset voltage of the quadrature modulator (and the DAC output offset voltage mismatch) and may degrade system performance.

Typical DAC-to-quadrature modulator interfaces are shown in Figure 79. Often, the input common-mode voltage for the modulator is much higher than the output compliance range of the DAC, making ac coupling or a dc level shift necessary. If the required common-mode input voltage on the quadrature modulator matches that of the DAC, then the dc shown in Figure 79 can be used. A low-pass or band-pass passive filter is recommended when spurious signals from the DAC (distortion and DAC images) at the quadrature modulator inputs may affect the system performance. Placing the filter at the location shown in Figure 79 allows easy design of the filter because the source and load impedances can easily be designed close to 50 Ω.

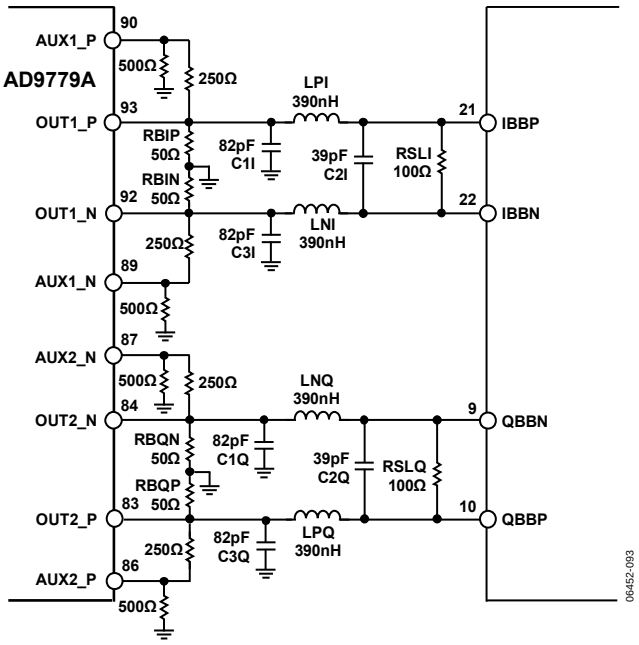

Figure 79. Typical Use of Auxiliary DACs AC Coupling to Quadrature Modulator

LO FEEDTHROUGH COMPENSATION

The LO feedthrough compensation is the most complex of all three operations. This is due to the structure of the offset auxiliary DACs, as shown in Figure 78. To achieve LO feedthrough compensation in a circuit, each of four outputs of these auxiliary DACs can be connected through a 500 Ω resistor to ground and through a 250 Ω resistor to one of the four quadrature modulator signal inputs. The purpose of these connections is to drive a very small amount of current into the nodes at the quadrature modulator inputs, therefore adding a slight dc bias to one of the quadrature modulator signal inputs.

To achieve LO feedthrough compensation, the user should start with the default conditions of the auxiliary DAC sign registers, and then increment the magnitude of one or the other auxiliary DAC output currents. While this is being done, the amplitude of the LO feedthrough at the quadrature modulator output should be sensed. If the LO feedthrough amplitude increases, try either changing the sign of the auxiliary DAC being adjusted or adjusting the output current of the other auxiliary DAC. It may take practice before an effective algorithm is achieved.

Using the AD9776A/AD9778A/AD9779A evaluation board, the LO feedthrough can typically be adjusted down to the noise floor, although this is not stable over temperature.

RESULTS OF GAIN AND OFFSET CORRECTION

The results of gain and offset correction can be seen in Figure 80 and Figure 81. Figure 80 shows the output spectrum of the quadrature demodulator before gain and offset correction. Figure 81 shows the output spectrum after correction. The LO feedthrough spur at 2.1 GHz has been suppressed to the noise level. This result can be achieved by applying the correction, but the correction needs to be repeated after a large change in temperature.

Note that the gain matching improved the negative frequency image rejection, but there is still a significant image present. The remaining image is now due to phase mismatch in the quadrature modulator. Phase mismatch can be distinguished from gain mismatch by the shape of the image. Note that the image in Figure 80 is relatively flat and the image in Figure 81 slopes down with frequency. Phase mismatch is frequency dependent, so an image dominated by phase mismatch has this sloping characteristic.

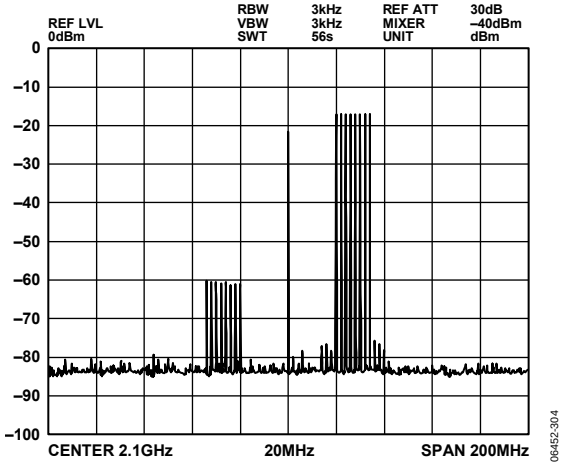

Figure 80. AD9779A and ADL5372 with a Multitone Signal at 2.1 GHz, No Gain or LO Compensation

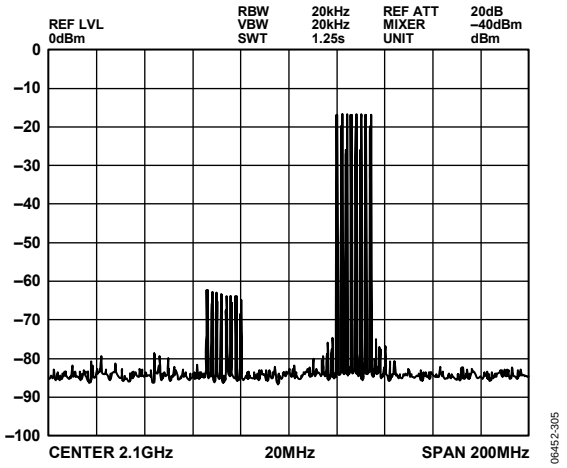

Figure 81. AD9779A and ADL5372 with a Multitone Signal at 2.1 GHz, Gain and LO Compensation Optimized

INPUT DATA PORTS

The AD9776A/AD9778A/AD9779A can operate in two data input modes: dual port mode and single port mode. For the default dual port mode (single port bit = 0), each DAC receives data from a dedicated input port. In single port mode (single port bit = 1), both DACs receive data from Port 1. In single port mode, DAC1 and DAC2 data is interleaved, and the TXENABLE input is used to steer data to the intended DAC. In dual port mode, the TXENABLE input is used to power down the digital data path.

In dual port mode, the data must be delivered at the input data rate. In single port mode, data must be delivered at twice the input data rate of each DAC. Because the data inputs function up to a maximum of 300 MSPS, it is practical to operate with input data rates up to 150 MHz per DAC in single port mode.

In dual port and single port modes, a data clock output (DATACLK) signal is available as a fixed time base with which to drive data from an FPGA or other data source. This output signal operates at the input data rate.

SINGLE PORT MODE

In single port mode, data for both DACs is received on the Port 1 input bus (P1D[15:0]). I and Q data samples are interleaved and are sampled on the rising edges of DATACLK. Along with the data, a framing signal must be supplied on the TXENABLE input (Pin 39), which steers incoming data to its respective DAC. When TXENABLE is high, the corresponding data-word is sent to the I DAC. When TXENABLE is low, the corresponding data is sent to the Q DAC. The timing of the digital interface in interleaved mode is shown in Figure 83.

The Q first bit (Register 0x02, Bit 0) controls the pairing order of the input data. With the Q first bit set to the default of 0, the I-Q pairing sent to the DACs is the two input data-words corresponding to TXENABLE low followed by TXENABLE high. With the Q first bit set to 1, the I-Q pairing sent to the DACs is the two input data-words corresponding to TXENABLE high, followed by TXENABLE low. Note that with either order pairing, the data sent with TXENABLE high is directed to the I DAC, and the data sent with TXENABLE low is directed to the Q DAC.

DUAL PORT MODE

In dual port mode, data for each DAC is received on the respective input bus (P1D[15:0] or P2D[15:0]). I and Q data arrive simultaneously and are sampled on the rising edge of the DATACLK signal. The TXENABLE signal must be high to enable the transmit path.

INPUT DATA REFERENCED TO DATACLK

The simplest method of interfacing to the AD9776A/AD9778A/AD9779A is when the input data is referenced to the DATACLK output. The DATACLK output is a buffered version (with some fixed delay) of the internal clock that is used to latch the input data. Therefore, if setup and hold times of the input data with respect to DATACLK are met, the input data is latched correctly. Detailed timing diagrams for the single and dual port cases using DATACLK as the timing reference are shown in Figure 82.

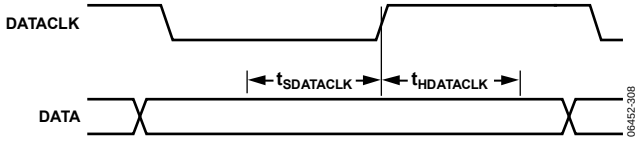

Figure 82. Input Data Port Timing, Data Referenced to DATACLK

Table 28 shows the setup and hold time requirements for the input data over the operating temperature range of the device. Also shown is the keep out window (KOW). The keep out window is the sum of the setup and hold times of the interface. This is the minimum amount of time valid data must be presented to the device to ensure proper sampling.

DATACLK Frequency Settings

The DATACLK signal is derived from the internal DAC sample clock, DACCLK. The frequency of the DATACLK output depends on several programmable settings. Normally, the frequency of DATACLK is equal to the input data rate. The relationship between the frequency of DACCLK and DATACLK is

$$f_{DATACLK} = \frac{f_{DACCLK}}{IF \times ZS \times SP \times DATACLKDIV}$$

where the variables *IF*, *ZS*, *SP*, and *DATACLKDIV* have the values shown in Table 27.

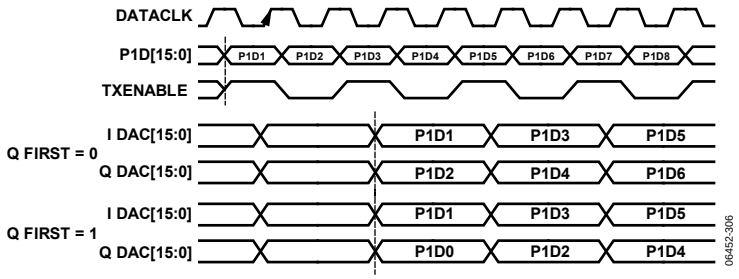

Figure 83. Single Port Mode Digital Interface Timing

The DATACLKDIV only affects the DATACLK output frequency, not the frequency of the data sampling clock. To maintain an $f_{DATACLK}$ frequency that samples the input data that remains consistent with the expected data rate, DATACLKDIV should be set to 00.

Table 27. DACCLK to DATACLK Divisor Values

		Address	
Variable	**Value**	**Register**	**Bit**
IF	Interpolation factor (1, 2, 4, or 8)	0x01	[7:6]
ZS	1, if zero stuffing is disabled 2, if zero stuffing is enabled	0x01	[0]
SP	0.5, if single port is enabled 1, if dual port is selected	0x02	[6]
DATACLKDIV	1, 2, or 4	0x03	[5:4]

INPUT DATA REFERENCED TO REFCLK

In some systems, it may be more convenient to use the REFCLK input than the DATACLK output as the input data timing reference. If the frequency of DACCLK is equal to the frequency of the data input (without interpolation), then the data with respect to REFCLK± timing specifications in Table 28 apply directly without further considerations. If the frequency of DACCLK is greater than the frequency of the input data, a divider is used to generate the DATACLK output (and the internal data sampling clock). This divider creates a phase ambiguity between REFCLK and DATACLK, which results in uncertainty in the sampling time. To establish fixed setup and hold times of the data interface, this phase ambiguity must be eliminated.

To eliminate the phase ambiguity, the SYNC_I input pins (Pin 13 and Pin 14) must be used to force the data to be sampled on a specific REFCLK edge. The relationship among REFCLK, SYNC_I, and input data is shown in Figure 84 and Figure 85. Therefore, both SYNC_I and data must meet the timing in Table 28 for reliable data transfer into the device.

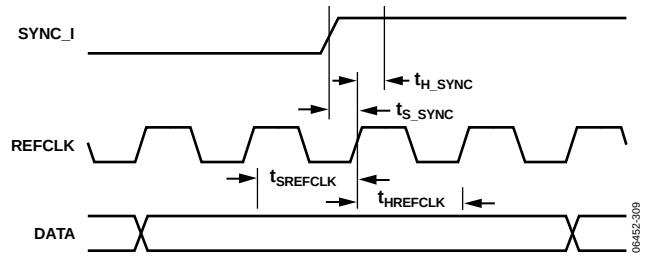

Figure 84. Input Data Port Timing, Data Referenced to REFCLK, $f_{DACCLK} = f_{REFCLK}$

Note that even though the setup and hold times of SYNC_I are relative to REFCLK, the SYNC_I input is sampled at the internal DACCLK rate. In the case where the PLL is employed, SYNC_I must be asserted to meet the setup time with respect to REFCLK (t_{S_SYNC}), but cannot be asserted prior to the previous rising edge of the internal SYNC_I sample clock. In other words, the SYNC_I assert edge has to be placed between its successive keep out windows that replicate at the DACCLK rate, not the REFCLK rate. The valid window for asserting SYNC_I is shaded gray in Figure 85 for the case where the PLL provides a DACCLK frequency of four times the REFCLK frequency. Thus, the minimum setup time is t_{S_SYNC}, and the maximum setup time is $t_{DACCLK} - t_{H_SYNC}$.

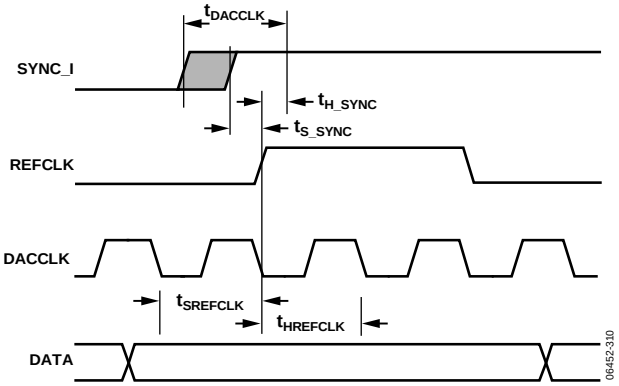

Figure 85. Input Data Port Timing, Data Referenced to REFCLK, $f_{DACCLK} = f_{REFCLK} \times 4$

More details of the synchronization circuitry are found in the Device Synchronization section of this data sheet.

Table 28. Data Timing Specifications vs. Temperature

		PLL Disabled			PLL Enabled		
Timing Parameter	**Temperature**	**Min t_S (ns)**	**Min t_H (ns)**	**Min KOW (ns)**	**Min t_S (ns)**	**Min t_H (ns)**	**Min KOW (ns)**
Data with Respect to REFCLK±	−40°C	−0.80	3.35	2.55	−0.83	3.87	2.99
	+25°C	−1.00	3.50	2.50	−1.06	4.04	2.98
	+85°C	−1.10	3.80	2.70	−1.19	4.37	3.16
	−40°C to +85°C	−0.80	3.80	3.00	−0.83	4.37	3.54
Data with Respect to DATACLK	−40°C	2.50	−0.05	2.45	2.50	−0.05	2.45
	+25°C	2.70	−0.20	2.50	2.70	−0.20	2.50
	+85°C	3.00	−0.40	2.60	3.00	−0.40	2.60
	−40°C to +85°C	3.00	−0.05	2.95	3.00	−0.05	2.95
SYNC_I± to REFCLK±	−40°C	0.30	0.65	0.95	0.27	1.17	1.39
	+25°C	0.25	0.75	1.00	0.19	1.29	1.48
	+85°C	0.15	0.90	1.05	0.06	1.47	1.51
	−40°C to +85°C	0.30	0.90	1.20	0.27	1.47	1.74

OPTIMIZING THE DATA INPUT TIMING

The AD9776A/AD9778A/AD9779A have on-chip circuitry that enables the user to optimize the input data timing by adjusting the relationship between the DATACLK output and DCLK_SMP (the internal clock that samples the input data). This optimization is made by a sequence of 3-wire interface register read and write operations. The timing optimization can be done under strict control of the user. This function is only available when the input data is referenced to the DATACLK output.

Figure 86 shows the circuitry that detects sample timing errors and adjusts the data interface timing. The DCLK_SMP signal is the internal clock used to latch the input data. Ultimately, it is the rising edge of this signal that needs to be centered in the valid sampling period of the input data. This is accomplished by adjusting the time delay, t_D, which changes the DATACLK timing and, as a result, the arrival time of the input data with respect to DCLK_SMP.

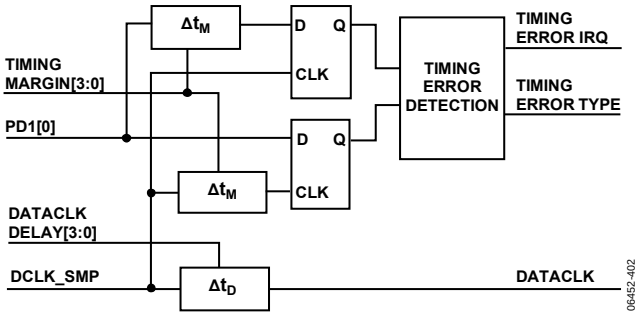

Figure 86. Timing Error Detection and Optimization Circuitry

The error detect circuitry works by creating two sets of sampled data (referred to as the margin test data) in addition to the actual sampled data used in the device data path. One set of sampled data is latched before the actual data sampling point. The other set of sampled data is latched after the actual data sampling point. If the margin test data match the actual data, the sampling is considered valid and no error is declared. If there is a mismatch between the actual data and the margin test data, an error is declared.

The Data Timing Margin[3:0] variable determines how much before and after the actual data sampling point the margin test data are latched. Therefore, the data timing margin variable determines how much setup and hold margin the interface needs for the data timing error IRQ to remain inactive (show error free operation). Therefore, the timing error IRQ is set whenever the setup and hold margins drop below the Data Timing Margin[3:0] value and does not necessarily indicate that the data latched into the device is incorrect.

In addition to setting the data timing error IRQ, the data timing error type bit is indicated when an error occurs. The data timing error type bit is set low to indicate a hold error and high to indicate a setup error. Figure 87 shows a timing diagram of the data interface and the status of the data timing error type bit.

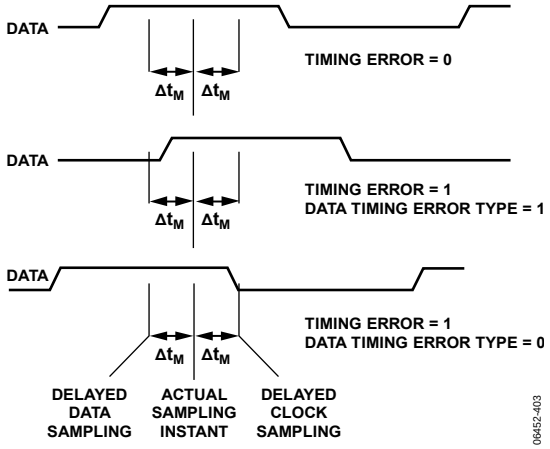

Figure 87. Timing Diagram of Margin Test Data

Manual Timing Optimization

When the device is operating in manual timing optimization mode (Register 0x03, Bit 7 = 0), the device does not alter the DATACLK Delay[3:0] value from what is programmed by the user. By default, the DATACLK delay enable bit is inactive. This bit must be set high for the DATACLK Delay[3:0] value to be realized. The delay (in absolute time) when programming DATACLK delay between 00000 and 11111 varies from about 700 ps to about 6.5 ns. The typical delays per increment over temperature are shown in Table 29.

Table 29. Data Delay Line Typical Delays Over Temperature

Delay	−40°C	+25°C	+85°C	Unit
Zero Code Delay (Delay Upon Enabling Delay Line)	630	700	740	ps
Average Unit Delay	175	190	210	ps

When the device is placed into manual mode, the error checking logic is activated. If the IRQs are enabled, an interrupt is generated if a setup/hold violation is detected. One error check operation is performed per device configuration. Any change to the Data Timing Margin[3:0] or DATACLK Delay[3:0] values triggers a new error check operation.

DEVICE SYNCHRONIZATION

System demands can impose two different requirements for synchronization. Some systems require multiple DACs to be synchronized to each other. This is the case when supporting transmit diversity or beam forming, where multiple antennas are used to transmit a correlated signal. In this case, the DAC outputs need to be phase aligned with each other, but there may not be a requirement for the DAC outputs to be aligned with a system level reference clock. In systems with a time division multiplexing transmit chain, one or more DACs may need to be synchronized with a system level reference clock. The options for synchronizing devices under these two conditions are described in the Synchronization Logic Overview section and the Synchronizing Devices to a System Clock section.

SYNCHRONIZATION LOGIC OVERVIEW

Figure 88 shows the block diagram of the on-chip synchronization logic. The basic operation of the synchronization logic is to generate a single DACCLK-cycle-wide initialization pulse that sets the clock generation state machine logic to a known state. This initialization pulse loads the clock generation state machine with the Clock State[4:0] value as its next state. If the initialization pulse from the synchronization logic is generated properly, it is active for one DACCLK cycle, every 32 DACCLK cycles. Because the clock generation state machine has 32 states operating at the DACCLK rate, every initialization pulse received after the first pulse loads the state in which the state machine is already in, maintaining proper clocking operation of the device.

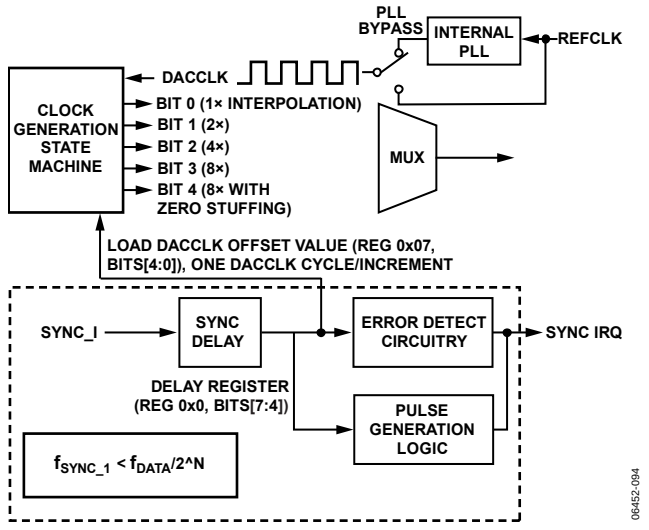

Figure 88. Synchronization Circuitry Block Diagram

Nominally, the SYNC_I input should have one rising edge every 32 clock cycles (or multiple of 32 clock cycles) to maintain proper synchronization. The pulse generation logic can be programmed to suppress outgoing pulses if the incoming SYNC_I frequency is greater than DACCLK/32. Extra pulses can be suppressed by the ratios listed in Table 30. The SYNC_I frequency can be lower than DACCLK/32 as long as output pulses are generated from the pulse generation circuit on a multiple of 32 DACCLK periods. In any case, the maximum frequency of SYNC_I must be less than $f_{DATACLK}$.

Table 30. Settings Required to Support Various SYNC_I Frequencies

SYNC_I Ratio[2:0]	SYNC_I Rising Edges Required for Synchronization Pulse
000	1 (default)
001	2
010	4
011	8
100	16
101	Invalid setting
110	Invalid setting
111	Invalid setting

As an example, if a SYNC_I signal with a frequency of $f_{DACCLK}/4$ is used, then both 011 and 100 are valid settings for the SYNC_I Ratio[2:0] value. A setting of 011 results in one initialization pulse being generated every 32 DACCLK cycles, and a setting of 100 results in one initialization pulse being generated every 64 DACCLK cycles. Both cases result in proper device synchronization.

The Clock State[4:0] value is the state to which the clock generation state machine resets upon initialization. By varying this value, the timing of the internal clocks with respect to the SYNC_I signal can be adjusted. Every increment of the Clock State[4:0] value advances the internal clocks by one DACCLK period.

Synchronization Timing Error Detection

The synchronization logic has error detection circuitry similar to the input data timing. The SYNC_I Timing Margin[3:0] variable determines how much setup and hold margin the synchronization interface needs for the sync timing error IRQ bit to remain inactive (that is, to indicate error free operation). Therefore, the sync timing error IRQ bit is set whenever the setup and hold margins drop below the SYNC_I Timing Margin[3:0] value and, therefore, does not necessarily indicate that the SYNC_I input was latched incorrectly.

When the sync timing error IRQ bit is set, corrective action can be taken to restore timing margin. One course of action is to temporarily reduce the timing margin until the sync timing error IRQ is cleared. Then, increase the SYNC_I delay by two increments and check whether the timing margin has increased or decreased. If it has increased, continue incrementing the value of SYNC_I delay until the margin is maximized. However, if incrementing the SYNC_I delay reduced the timing margin, then the delay should be reduced until the timing margin is optimized.

SYNCHRONIZING DEVICES TO A SYSTEM CLOCK

The AD9776A/AD9778A/AD9779A offer a pulse mode synchronization scheme (see Figure 89) to align the DAC outputs of multiple devices within a system to the same DACCLK edge. The internal clocks are synchronized by providing either a one-time pulse or a periodic signal to the SYNC_I inputs (SYNC_I+, SYNC_I–). The SYNC_I signal is sampled by the internal DACCLK sample rate clock.

The SYNC_I input frequency has the following constraint:

$$f_{SYNC_I} \leq f_{DATA}$$

When the internal clocks are synchronized, the data-sampling clocks between all devices are phase aligned. The data input timing relationships can be referenced to either REFCLK or DATACLK.

For this synchronization scheme, all devices are slave devices, and the system clock generation/distribution chip serves as the master. It is vital that the SYNC_I signal be distributed between the DACs with low skew. Likewise, the REFCLK signals must be distributed with low skew. Any skew on these signals between the DACs must be accounted for in the timing budget. Figure 89 shows an example clock and synchronization input scheme.

Figure 90 shows the timing of the SYNC_I input with respect to the REFCLK input. Note that although the timing is relative to the REFCLK signal, SYNC_I is sampled at the DACCLK rate. This means that the rising edge of the SYNC_I signal must occur after the hold time of the preceding DACCLK rising edge, not the preceding REFCLK rising edge.

INTERRUPT REQUEST OPERATION

The IRQ pin (Pin 71) acts as an alert in the event that the device has a timing error and should be queried (by reading Register 0x19) to determine the exact fault condition. The IRQ pin is an open-drain, active low output. The IRQ pin should be pulled high external to the device. This pin can be tied to the IRQ pins of other devices with open-drain outputs to wire-OR these pins together.

There are two different error flags that can trigger an interrupt request: a data timing error flag or a sync timing error flag. By default, when either or both of these error flags are set, the IRQ pin is active low. Either or both of these error flags can be masked to prevent them from activating an interrupt on the IRQ pin.

The error flags are latched and remain active until the interrupt register, Register 0x19, is either read from or the error flag bits are overwritten.

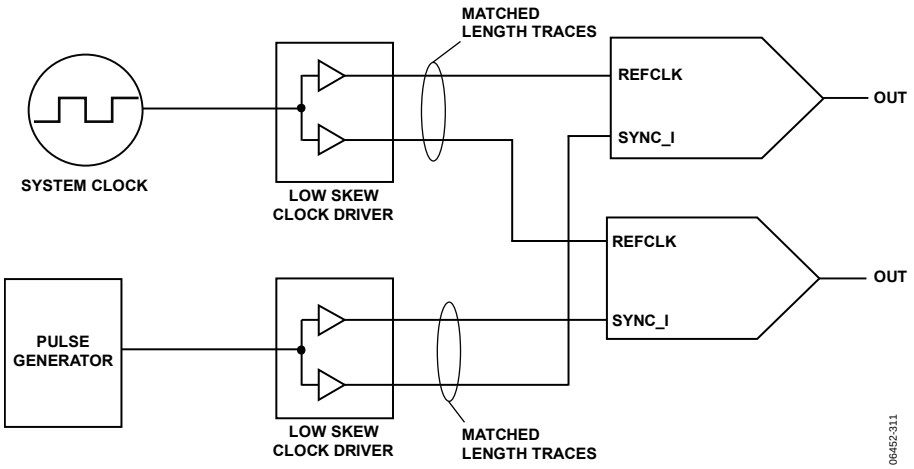

Figure 89. Multichip Synchronization in Pulse Mode

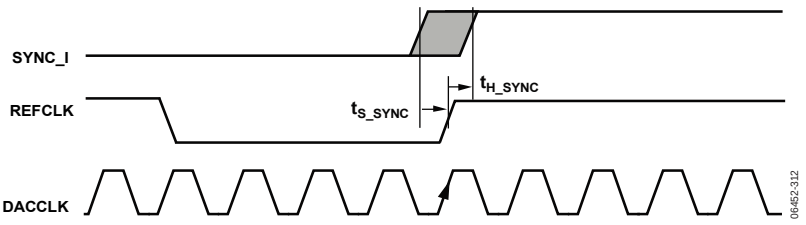

Figure 90. Timing Diagram of SYNC_I with Respect to REFCLK When Synchronizing Multiple Devices to Each Other

POWER DISSIPATION

Figure 91 to Figure 99 show the power dissipation of the 1.8 V and 3.3 V digital and clock supplies in single DAC mode and dual DAC mode. In addition to this, the power dissipation/current of the 3.3 V analog supply (mode and speed independent) in single DAC mode is 102 mW/31 mA. In dual DAC mode, this is 182 mW/55 mA. When the PLL is enabled, it adds 50 mA/90 mW to the 1.8 V clock supply.

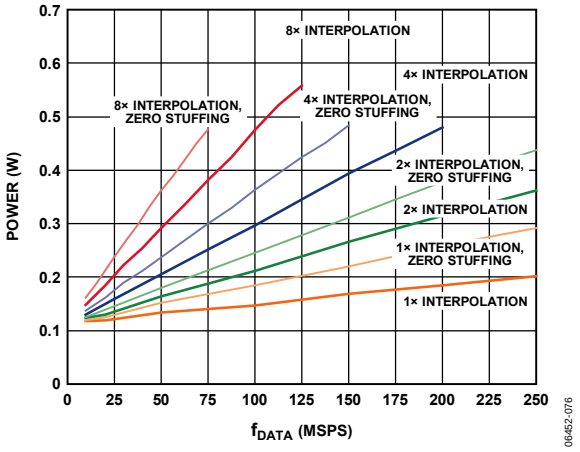

Figure 91. Total Power Dissipation, I Data Only, Real Mode

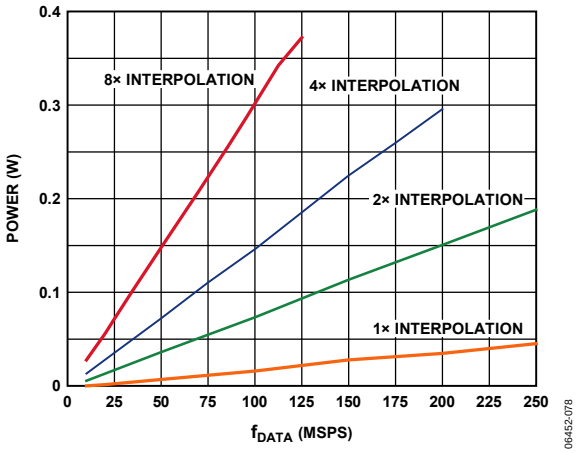

Figure 92. Power Dissipation, Digital 1.8 V Supply, I Data Only, Real Mode, Does Not Include Zero Stuffing

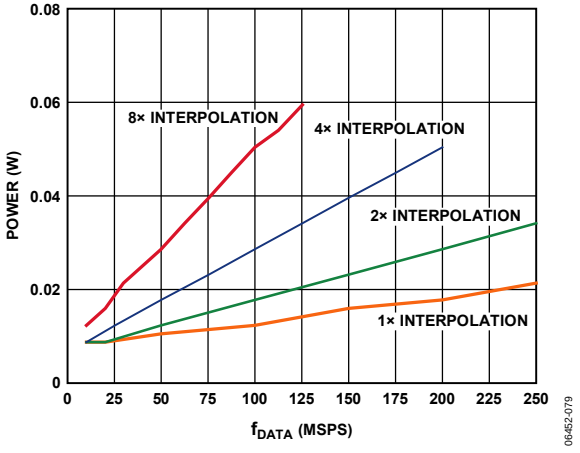

Figure 93. Power Dissipation, Clock 1.8 V Supply, I Data Only, Real Mode, Includes Modulation Modes, Does Not Include Zero Stuffing

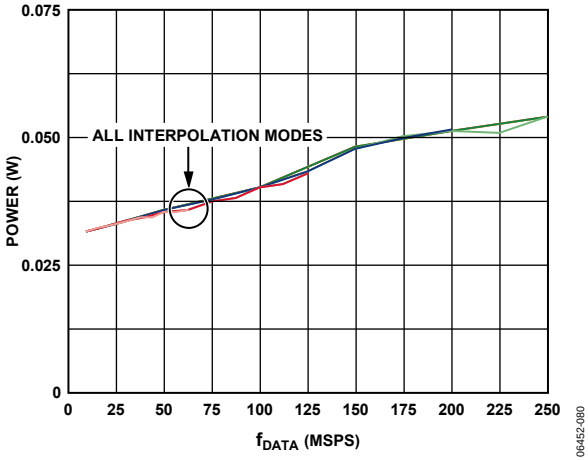

Figure 94. Power Dissipation, Digital 3.3 V Supply, I Data Only, Real Mode, Includes Modulation Modes and Zero Stuffing

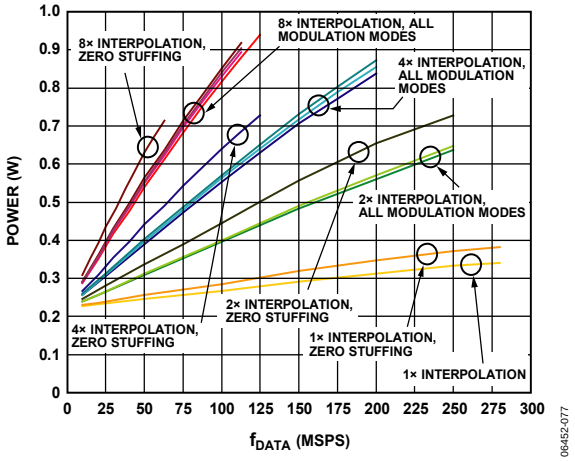

Figure 95. Total Power Dissipation, Dual DAC Mode

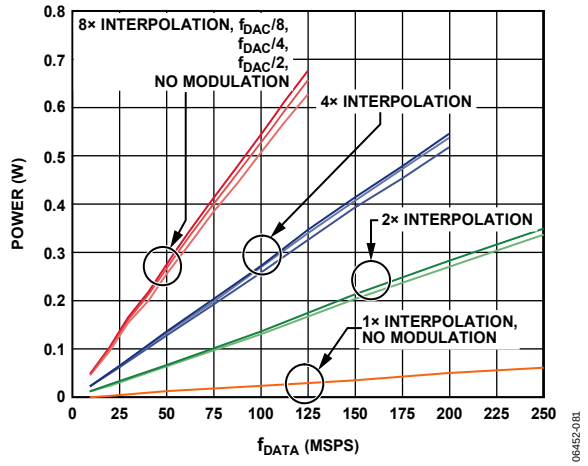

Figure 96. Power Dissipation, Digital 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

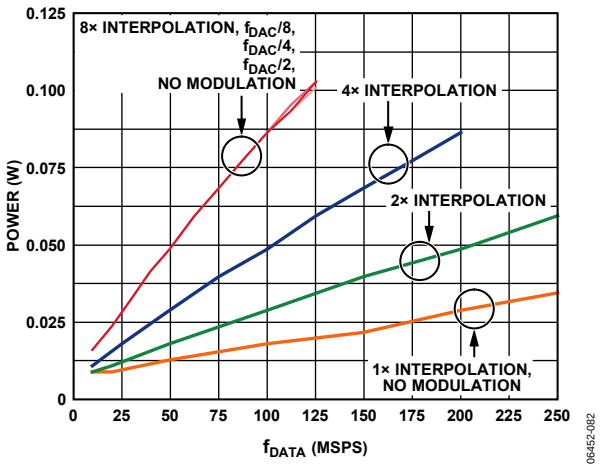

Figure 97. Power Dissipation, Clock 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

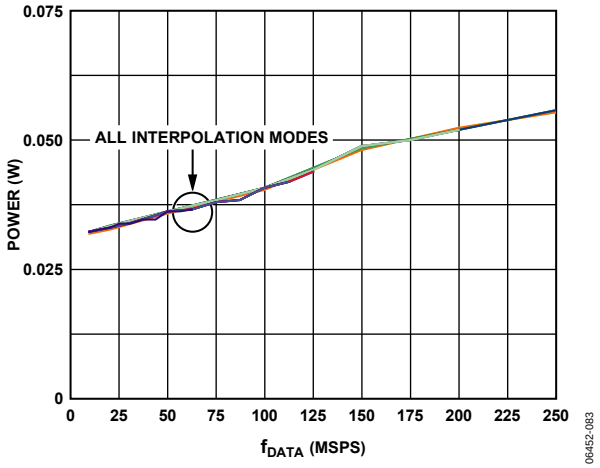

Figure 98. Power Dissipation, Digital 3.3 V Supply, I and Q Data, Dual DAC Mode

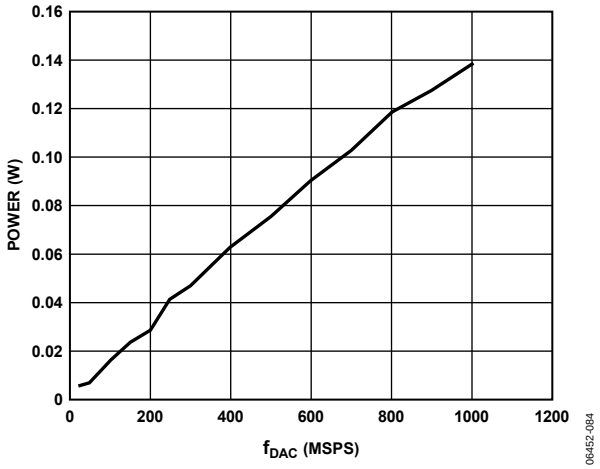

Figure 99. DVDD18 Power Dissipation of Inverse Sinc Filter

POWER-DOWN AND SLEEP MODES

The AD9776A/AD9778A/AD9779A have a variety of power-down modes; thus, the digital engine, main TxDACs, or auxiliary DACs can be powered down individually or together. Via the 3-wire interface port, the main TxDACs can be placed in sleep or power-down mode. In sleep mode, the TxDAC output is turned off, thus reducing power dissipation. The reference remains powered on, however, so that recovery from sleep mode is very fast. With the power-down mode bit set (Register 0x00, Bit 4), all analog and digital circuitry, including the reference, is powered down. The 3-wire interface port remains active in this mode. This mode offers more substantial power savings than sleep mode, but the turn-on time is much longer. The auxiliary DACs also have the capability to be programmed into sleep mode via the 3-wire interface port. The auto power-down enable bit (Register 0x00, Bit 3) controls the power-down function for the digital section of the devices. The auto power-down function works in conjunction with the TXENABLE pin (Pin 39); see Table 31 for details.

Table 31.

TXENABLE (Pin 39)	Description
0	If auto power-down enable bit = 0, flush data path with 0s. If auto power-down enable bit = 1, flush data for multiple REFCLK cycles; then, automatically place the digital engine in power-down state. DACs, reference, and 3-wire interface port are not affected.
1	Normal operation.

EVALUATION BOARD OVERVIEW

EVALUATION BOARD OPERATION

The AD9776A/AD9778A/AD9779A evaluation board is provided to help users quickly become familiar with the operation of the device and to evaluate the device performance. To operate the evaluation board, the user needs a PC, a 5 V power supply, a clock source, and a digital data source. The user also needs a spectrum analyzer or an oscilloscope to observe the DAC output.

The typical evaluation setup is shown in Figure 100. A sine or square wave clock can be used to source the DAC sample clock. The spectral purity of the clock directly affects the device performance. A low noise, low jitter clock source is required.

All necessary connections to the evaluation board are shown in more detail in Figure 101.

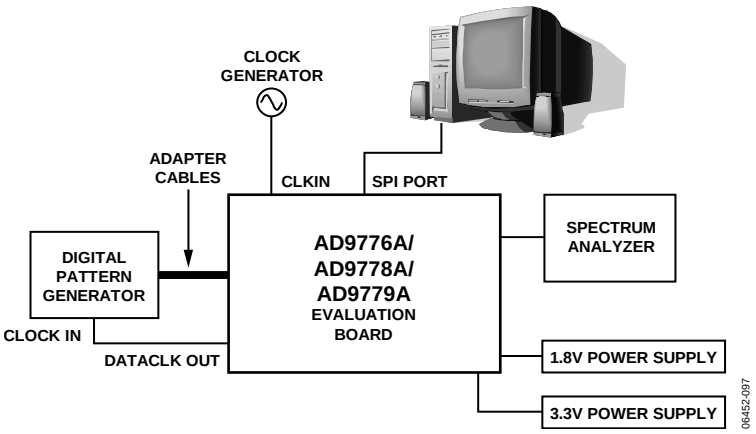

Figure 100. Typical Test Setup

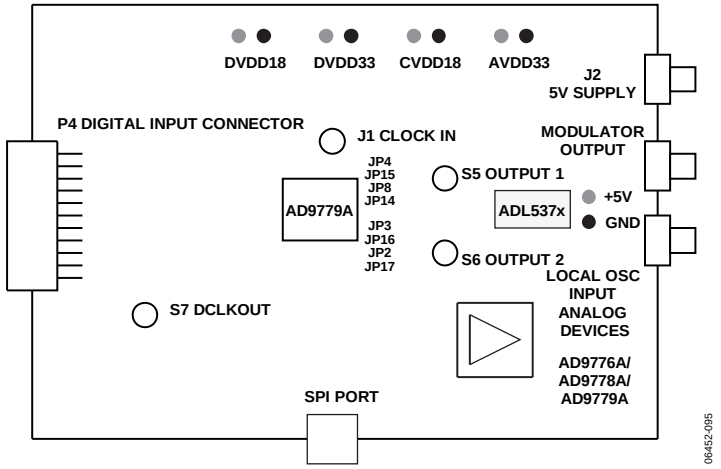

Figure 101. AD9776A/AD9778A/AD9779A Evaluation Board Showing All Connections

The evaluation board comes with software that allows the user to program the on-chip configuration registers. Via the 3-wire interface port, the devices can be programmed into any of its various operating modes. The default software window is shown in Figure 102.

The evaluation board also comes populated with the ADL537x modulator to allow for the evaluation of an RF subsystem. Complete details on the evaluation board and the 3-wire interface software can be downloaded from the Analog Devices website.

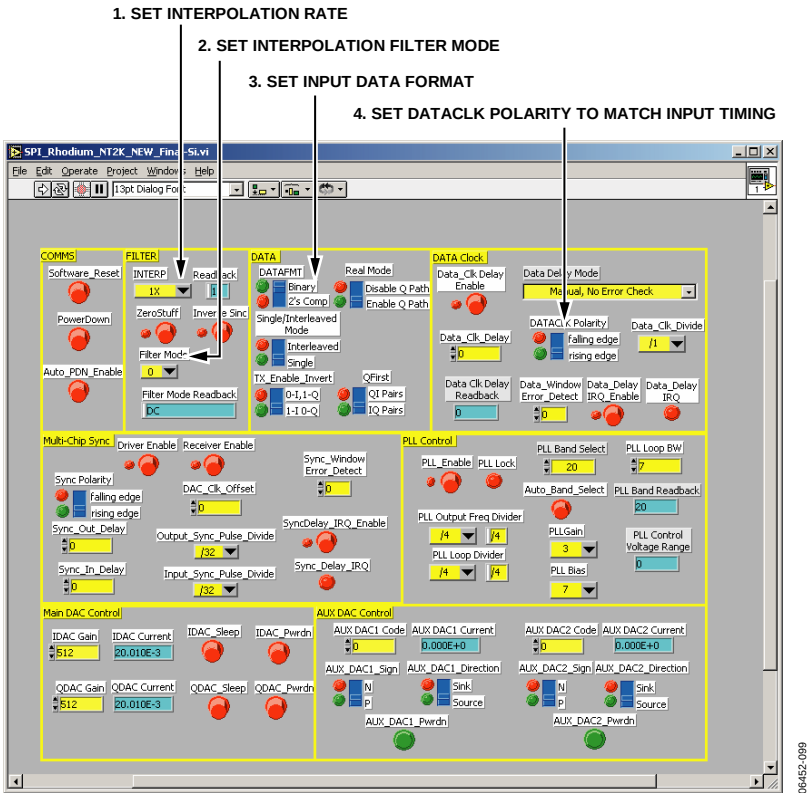

Figure 102. 3-Wire Interface Port Software Window

OUTLINE DIMENSIONS

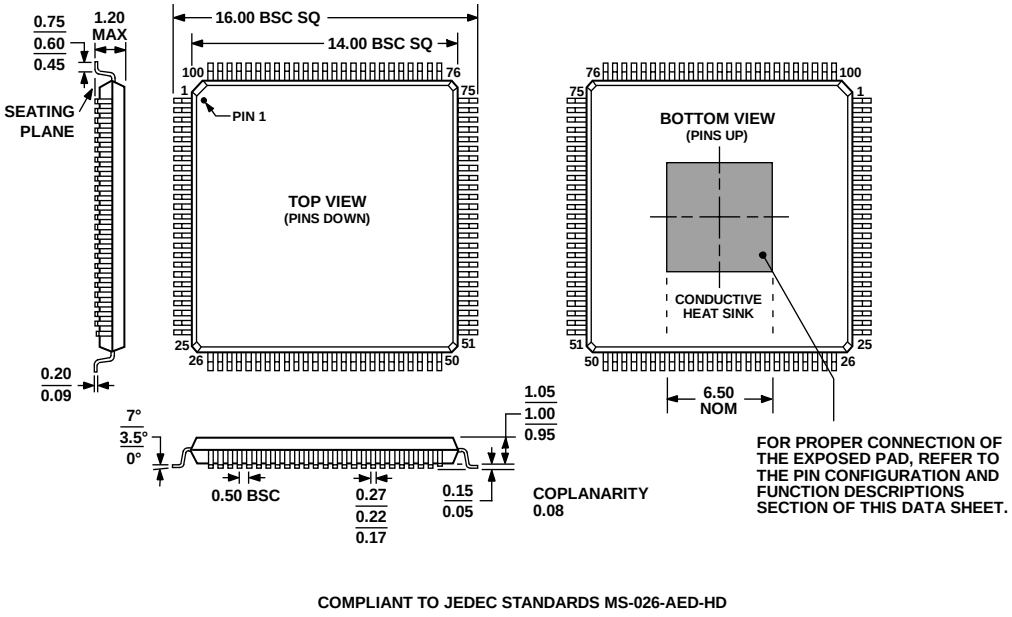

Figure 103. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9776ABSVZ	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-1
AD9776ABSVZRL	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-1
AD9778ABSVZ	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-1
AD9778ABSVZRL	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-1
AD9779ABSVZ	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-1
AD9779ABSVZRL	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-1

[1] Z = RoHS Compliant Part.

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