High Voltage, Quad-Channel 12-Bit Voltage Output DAC

Data Sheet

AD5504

FEATURES

Quad-channel high voltage DAC
12-bit resolution
Pin selectable 30 V or 60 V output range
Integrated precision reference
Low power serial interface with readback capability
Integrated temperature sensor alarm function
Power-on reset
Simultaneous updating via $\overline{\text{LDAC}}$
Wide operating temperature: −40°C to +105°C

APPLICATIONS

Programmable voltage sources
High voltage LED drivers
Receiver bias in optical communications

GENERAL DESCRIPTION

The AD5504 is a quad-channel, 12-bit, serial input, digital-to-analog converter with on-chip high voltage output amplifiers and an integrated precision reference. The DAC output voltage ranges are programmable via the range select pin ($\overline{\text{R_SEL}}$). If $\overline{\text{R_SEL}}$ is held high, the DAC output ranges are 0 V to 30 V. If $\overline{\text{R_SEL}}$ is held low, the DAC output ranges are 0 V to 60 V. The on-chip output amplifiers allow an output swing within the range of AGND + 0.5 V to V_{DD} − 0.5 V.

The AD5504 has a high speed serial interface, which is compatible with SPI®-, QSPI™-, MICROWIRE™-, and DSP-interface standards and can handle clock speeds of up to 16.667 MHz.

FUNCTIONAL BLOCK DIAGRAM

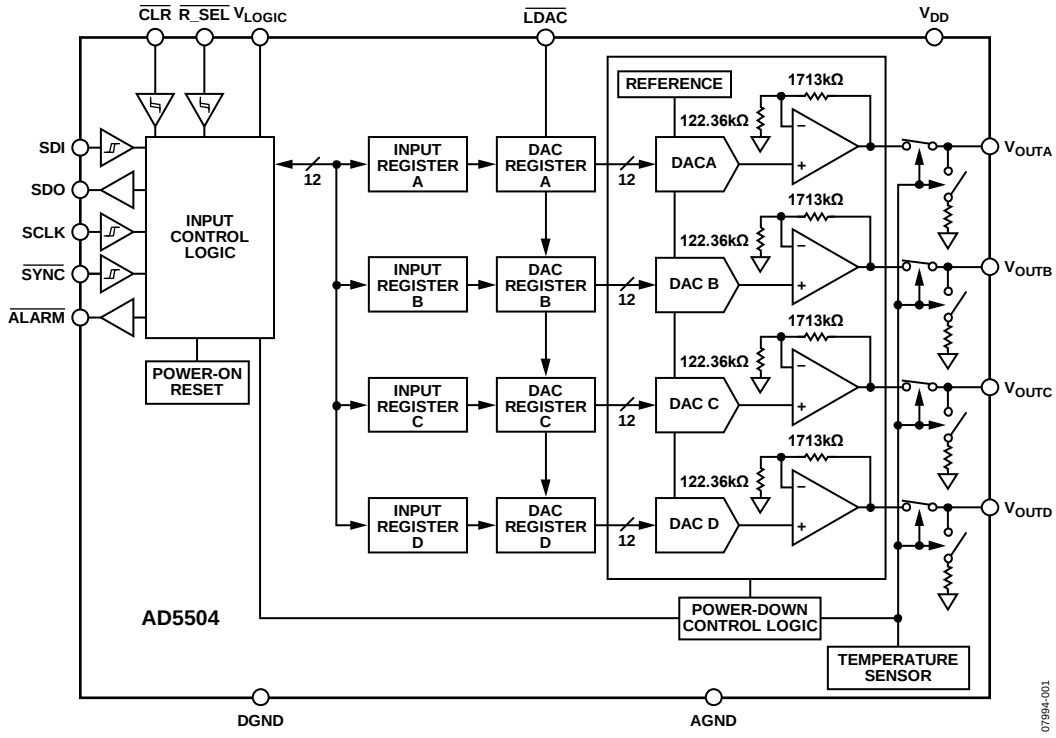

Figure 1.

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REVISION HISTORY

12/12—Rev. A to Rev. B

Changes to t_4 Parameter, Table 4 ... 6
Changes to Figure 3 and Figure 4 ... 7
Changes to Pin 3 Description, Table 7 and Pin 4 Description, Table 7 ... 9
Changes to Write Mode Section ... 16
Changes to Table 10 ... 17

10/10—Rev. 0 to Rev. A

Changes to Figure 3 and Figure 4 ... 7

7/09—Revision 0: Initial Version

The serial interface offers the user the capability of both writing to, and reading from, most of the internal registers. To reduce power consumption at power up, only the digital section of the AD5504 is powered up initially. This gives the user the ability to program the DAC registers to the required value while typically only consuming 30 μA of supply current. The AD5504 incorporates power-on reset circuitry that ensures the DAC registers power up in a known condition and remain there until a valid write to the device has taken place. The analog section is powered up by issuing a power-up command via the SPI interface. The AD5504 provides software-selectable output loads while in the power-down mode.

The AD5504 has an on-chip temperature sensor. When the temperature on the die exceeds 110°C, the $\overline{\text{ALARM}}$ pin (an active low CMOS output pin) flags an alarm and the AD5504 enters a temperature power-down mode disconnecting the output amplifier thus removing the short-circuit condition. The AD5504 remains in power-down mode until a software power-up command is executed.

The AD5504 is available in a compact 16-lead TSSOP. The AD5504 is guaranteed to operate over the extended temperature range of −40°C to +105°C.

Table 1. Related Device

Part No.	Description
AD5501	High Voltage, 12-Bit Voltage Output DAC

SPECIFICATIONS

V_{DD} = 10 V to 62 V; V_{LOGIC} = 2.3 V to 5.5 V; R_L = 60 kΩ; C_L = 200 pF; −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments
ACCURACY[2]						
Resolution			12		Bits	
Differential Nonlinearity	DNL	−1		1	LSB	
Integral Nonlinearity	INL					
60 V Mode		−2		+2	LSB	V_{DD} = 62 V
30 V Mode		−3		+3	LSB	V_{DD} = 62 V
V_{OUTX} Temperature Coefficient[3, 4, 5]			50		ppm/°C	DAC code = half scale
Zero-Scale Error	V_{ZSE}			100	mV	DAC code = 0
Zero-Scale Error Drift[4]			60		µV/°C	60 V mode
Offset Error[6]	V_{OE}	−80		+120	mV	
Offset Error Drift[4]			60		µV/°C	60 V mode
Full-Scale Error	V_{FSE}	−325		+275	mV	
Full-Scale Error Drift[4]			1		mV/°C	−40°C to +25°C; 60 V mode
			350		µV/°C	+25°C to +105°C; 60 V mode
Gain Error		−0.6		+0.6	% of FSR	
Gain Temperature Coefficient[4]			10		ppm of FSR/°C	60 V mode
DC Crosstalk[4]						R_L = 60 kΩ to AGND or V_{DD}
Due to Single Channel Full-Scale Output Change			3		mV	60 V mode
Due to Powering Down (Per Channel)			4		mV	60 V mode
OUTPUT CHARACTERISTICS						
Output Voltage Range[7]		AGND + 0.5		V_{DD} − 0.5	V	
Short-Circuit Current[4, 8]			2		mA	On any single channel
Capacitive Load Stability[4]						1 V to 4 V step
R_L = 60 kΩ to ∞				1	nF	
Load Current[4]		−1		+1	mA	On any single channel
DC Output Impedance[4]			3		Ω	
DC Output Leakage[4]			10		µA	
DIGITAL INPUTS						
Input Logic High	V_{IH}	2.0			V	V_{LOGIC} = 4.5 V to 5.5 V
		1.8			V	V_{LOGIC} = 2.3 V to 3.6 V
Input Logic Low	V_{IL}			0.8	V	V_{LOGIC} = 2.3 V to 5.5 V
Input Current	I_{IL}			±1	µA	
Input Capacitance[4]	I_{IC}		5		pF	
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	V_{LOGIC} − 0.4 V			V	I_{SOURCE} = 200 µA
Output Low Voltage	V_{OL}			DGND + 0.4 V	V	I_{SINK} = 200 µA
Three-State Leakage Current						
SDI, SDO, SCLK, $\overline{\text{LDAC}}$, $\overline{\text{CLR}}$, R_$\overline{\text{SEL}}$		−1		+1	µA	
$\overline{\text{ALARM}}$		−10		+10	µA	
Output Capacitance[4]			5		pF	

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments
POWER SUPPLIES						
V_{DD}		10		62	V	
V_{LOGIC}		2.3		5.5	V	
Quiescent Supply Current ($I_{QUIESCENT}$)			2	3	mA	Static conditions; DAC outputs = midscale
Logic Supply Current (I_{LOGIC})			0.4	2	µA	$V_{IH} = V_{LOGIC}$; V_{IL} = DGND
DC PSRR[4]						DAC output = full-scale
60 V Mode		68			dB	
30 V Mode		76			dB	
POWER-DOWN MODE						
Supply Current	I_{DD_PWD}					
Software Power-Down Mode			30	50	µA	
Junction Temperature[8]	T_J			130	°C	$T_J = T_A + P_{TOTAL} \times \theta_{JA}$

[1] Typical specifications represent average readings at 25°C, V_{DD} = 62 V and V_{LOGIC} = 5 V.
[2] Valid in output voltage range of (V_{DD} − 0.5 V) to (AGND + 0.5 V). Outputs are unloaded.
[3] Includes linearity, offset, and gain drift.
[4] Guaranteed by design and characterization. Not production tested.
[5] V_{OUTX} refers to V_{OUTA}, V_{OUTB}, V_{OUTC}, or V_{OUTD}.
[6] DAC code = 32 for 60 V mode; DAC code = 64 for 30 V mode.
[7] The DAC architecture gives a fixed linear voltage output range of 0 V to 30 V if $\overline{R_SEL}$ is held high and 0 V to 60 V if $\overline{R_SEL}$ is held low. As the output voltage range is limited by output amplifier compliance, V_{DD} should be set to at least 0.5 V higher than the maximum output voltage to ensure compliance.
[8] If the die temperature exceeds 110°C, the AD5504 enters a temperature power-down mode putting the DAC outputs into a high impedance state thereby removing the short-circuit condition. Overheating caused by long term short-circuit condition(s) is detected by an integrated thermal sensor. After power-down, the AD5504 stays powered down until a software power-up command is executed.

AC CHARACTERISTICS

V_{DD} = 10 V to 62 V; V_{LOGIC} = 2.3 V to 5.5 V; R_L = 60 kΩ; C_L = 200 pF; −40°C < T_A < +105°C, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments[3]
AC CHARACTERISTICS					
Output Voltage Settling Time					¼ to ¾ scale settling to ±1 LSB, R_L = 60 kΩ
60 V Mode		45	55	µs	
30 V Mode		25	35	µs	
Slew Rate		0.65		V/µs	
Digital-to-Analog Glitch Energy		300		nV-s	1 LSB change around major carry in 60 V mode
Glitch Impulse Peak Amplitude		170		mV	60 V mode
Digital Feedthrough		40		nV-s	
Digital Crosstalk		5		nV-s	
Analog Crosstalk		600		nV-s	
DAC-to-DAC Crosstalk		600		nV-s	
Peak-to-Peak Noise		140		µV p-p	0.1 Hz to 10 Hz; DAC code = 0x800
		4		mV p-p	0.1 Hz to 10 kHz; DAC code = 0x800

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to + 105°C, typical at 25°C.

TIMING CHARACTERISTICS

V_{DD} = 30 V, V_{LOGIC} = 2.3 V to 5.5 V and −40°C < T_A < +105°C; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	60	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	25	ns min	$\overline{SYNC}$ falling edge to SCLK rising edge setup time
t_5	15	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	20	ns min	Minimum $\overline{SYNC}$ high time
t_9	20	ns min	$\overline{LDAC}$ pulse width low
t_{10}	50	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{11}	15	ns min	$\overline{CLR}$ pulse width low
t_{12}	100	ns typ	$\overline{CLR}$ pulse activation time
t_{13}	20	µs typ	$\overline{ALARM}$ clear time
t_{14}	110	ns min	SCLK cycle time in read mode
t_{15}[3]	55	ns max	SCLK rising edge to SDO valid
t_{16}[3]	25	ns min	SCLK to SDO data hold time
t_{17}[4]	50	µs max	Power-on reset time (this is not shown in the timing diagrams)
t_{18}[5]	50	µs max	Power-on time (this is not shown in the timing diagrams)
t_{19}	5	µs typ	$\overline{ALARM}$ clear to output amplifier turn on (this is not shown in the timing diagrams)

[1] All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Maximum SCLK frequency is 16.667 MHz.
[3] Under load conditions shown in Figure 2.
[4] Time from when the V_{DD}/V_{LOGIC} supplies are powered-up to when a digital interface command can be executed.
[5] Time required from execution of power-on software command to when the DAC outputs have settled to 1 V.

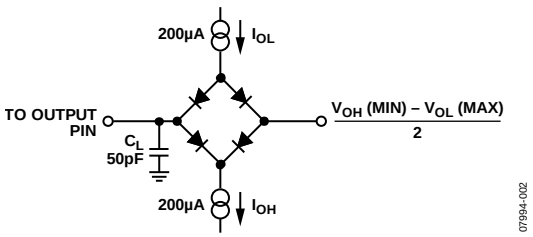
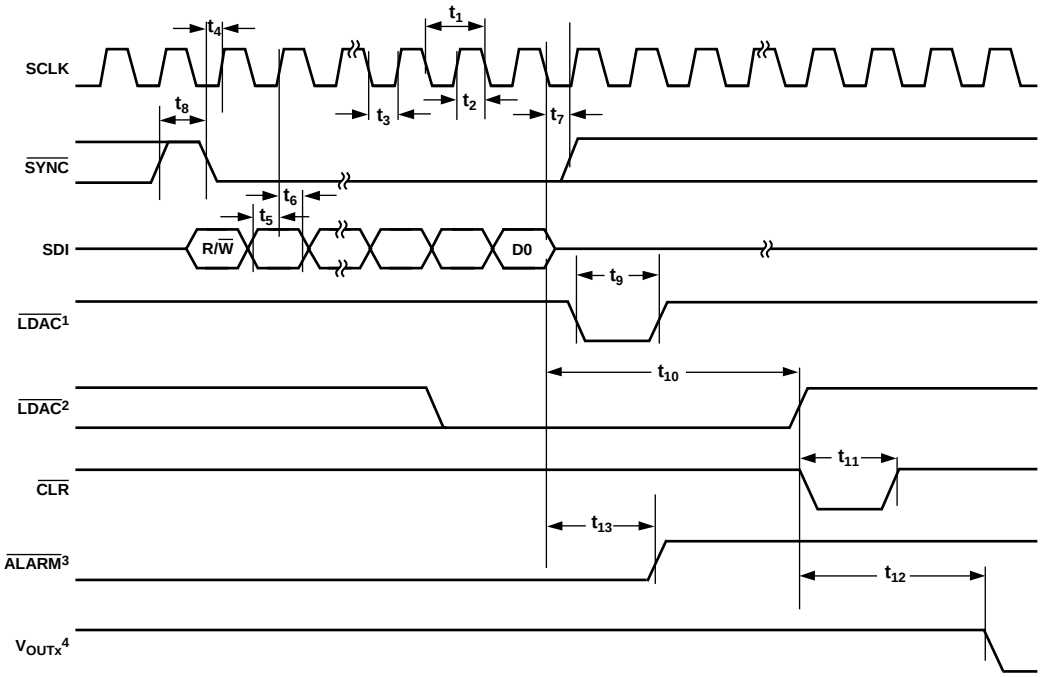


Figure 2. Load Circuit for SDO Timing Diagram



[1]ASYNCHRONOUS LDAC UPDATE MODE.
[2]SYNCHRONOUS LDAC UPDATE MODE.
[3]IN THE EVENT OF OVERTEMPERATURE CONDITION.
[4]V_{OUTx} REFERS TO ANY OF V_{OUTA}, V_{OUTB}, V_{OUTC} OR V_{OUTD}.

Figure 3. Write Timing Diagram

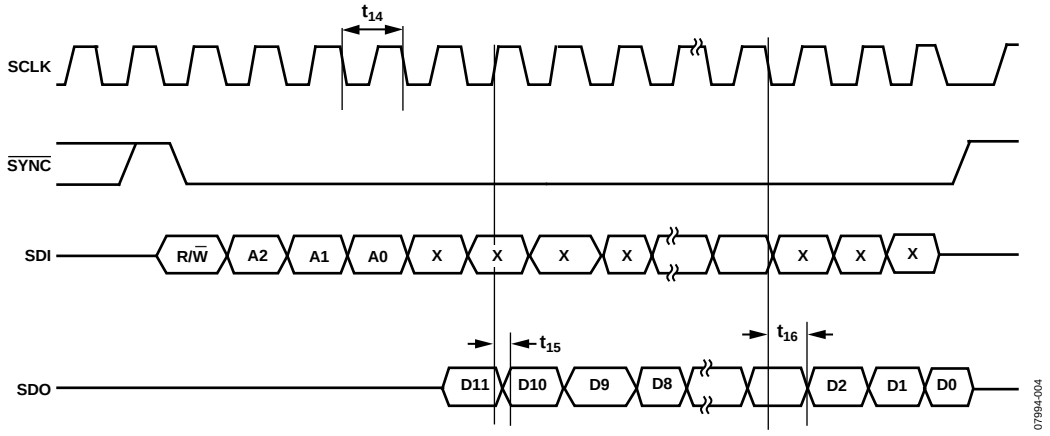


Figure 4. Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
V_{DD} to AGND	−0.3 V, + 64 V
V_{LOGIC} to DGND	−0.3 V to +7 V
V_{OUTX} to AGND[1]	−0.3 V to V_{DD} + 0.3 V
Digital Input to DGND	−0.3 V to V_{LOGIC} + 0.3 V
SDO Output to DGND	−0.3 V to V_{LOGIC} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Maximum Junction Temperature (T_J Maximum)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature Range	20 sec to 40 sec

[1] V_{OUTX} refers to V_{OUTA}, V_{OUTB}, V_{OUTC}, or V_{OUTD}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance is for a JEDEC 4-layer(2S2P) board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead TSSOP	112.60	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

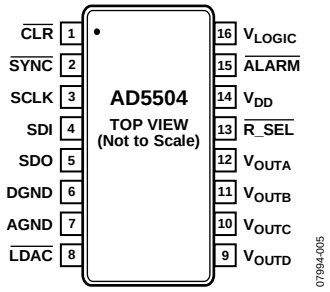


Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are set to 0x000 and the outputs to zero scale.
2	$\overline{\text{SYNC}}$	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register and data is transferred in on the rising edges of the following clocks. The selected DAC register is updated on the 16th falling SCLK, unless $\overline{\text{SYNC}}$ is taken high before this edge, in which case, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
3	SCLK	Serial Clock Input. Data is clocked into the input shift register on the rising edge of the serial clock input. Data can be transferred at rates up to 16 MHz.
4	SDI	Serial Data Input. This part has a 16-bit shift register. Data is clocked into the register on the rising edge of the serial clock input.
5	SDO	Serial Data Output. CMOS output. This pin serves as the readback function for all DAC and control registers. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
6	DGND	Digital Ground Pin.
7	AGND	Analog Ground Pin.
8	$\overline{\text{LDAC}}$	Load DAC Input. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to update simultaneously. Alternatively, this pin can be tied permanently low.
9	V_{OUTD}	Buffered Analog Output Voltage from DAC D.
10	V_{OUTC}	Buffered Analog Output Voltage from DAC C.
11	V_{OUTB}	Buffered Analog Output Voltage from DAC B.
12	V_{OUTA}	Buffered Analog Output Voltage from DAC A.
13	$\overline{\text{R_SEL}}$	Range Select Pin. Tying this pin to DGND selects a DAC output range of 0 V to 60 V, alternatively tying $\overline{\text{R_SEL}}$ to V_{LOGIC} selects a DAC output range of 0 V to 30 V.
14	V_{DD}	Positive Analog Power Supply. 10 V to 62 V for the specified performance. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
15	$\overline{\text{ALARM}}$	Active Low CMOS Output Pin. This pin flags an alarm if the temperature on the die exceeds 110°C.
16	V_{LOGIC}	Logic Power Supply; 2.3 V to 5.5 V. Decouple this pin with 0.1µF ceramic capacitors and 10 µF capacitors.

TYPICAL PERFORMANCE CHARACTERISTICS

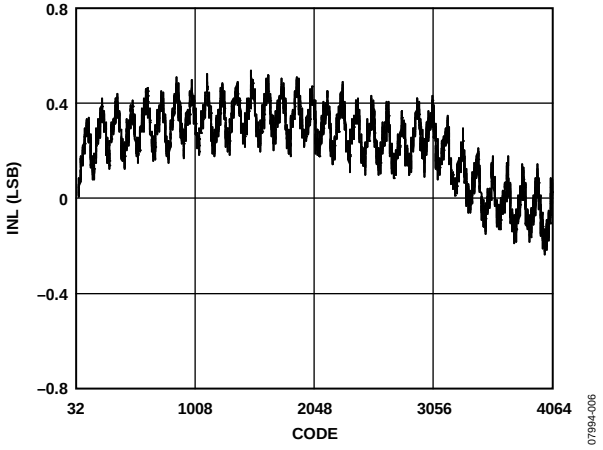


Figure 6. Typical INL

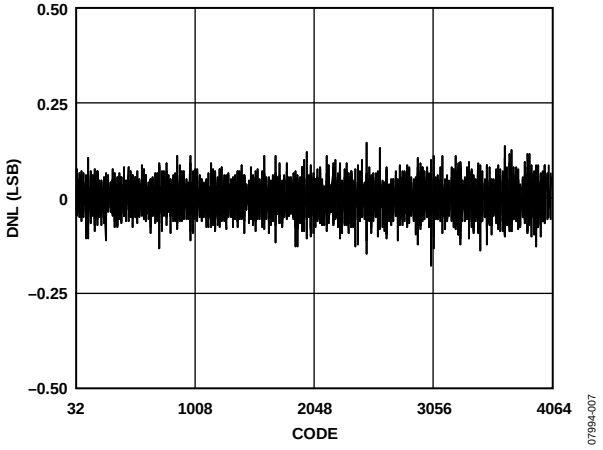


Figure 7. Typical DNL

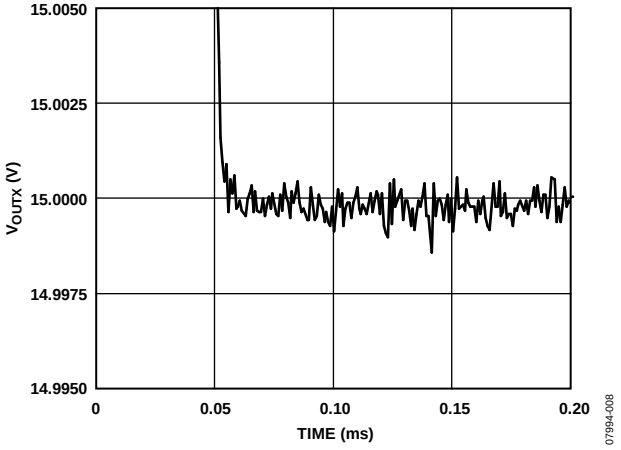


Figure 8. Output Settling Time (High to Low)

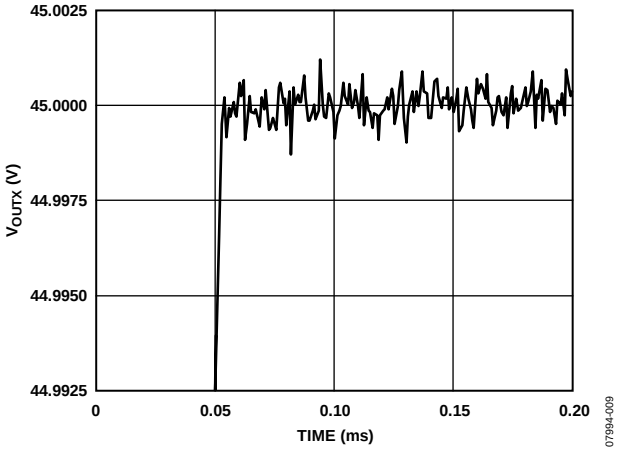


Figure 9. Output Settling Time (Low to High)

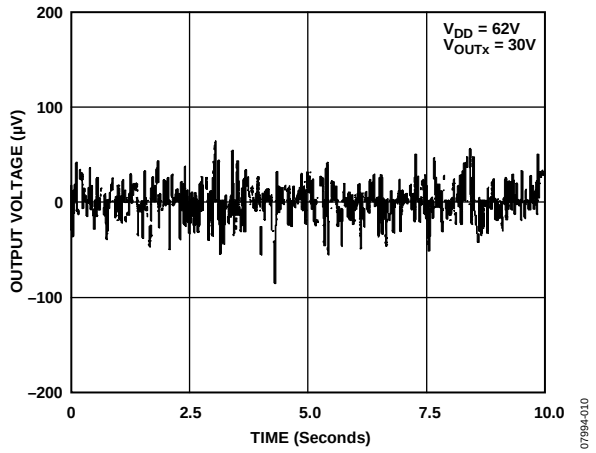


Figure 10. Output Noise

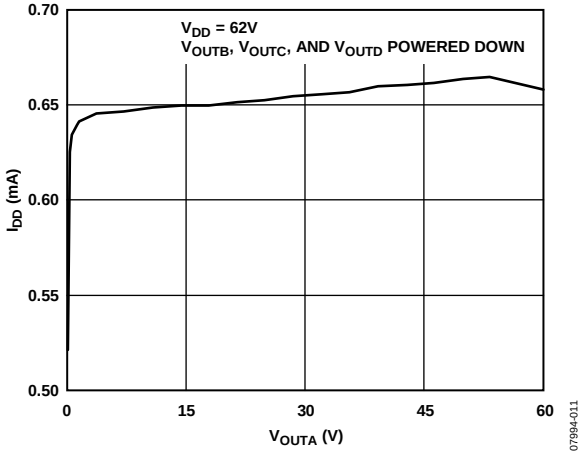


Figure 11. I_{DD} vs. V_{OUTA}

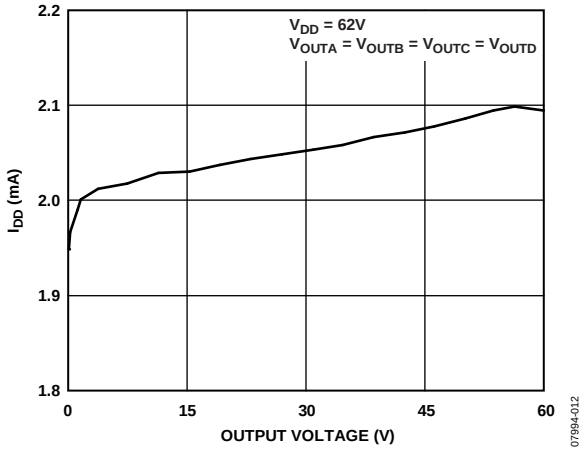


Figure 12. I_{DD} vs. V_{OUTA} to V_{OUTD}

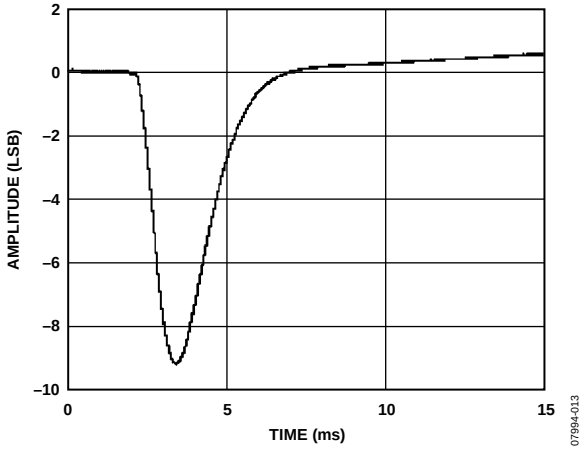


Figure 13. Digital-to-Analog Negative Glitch Impulse

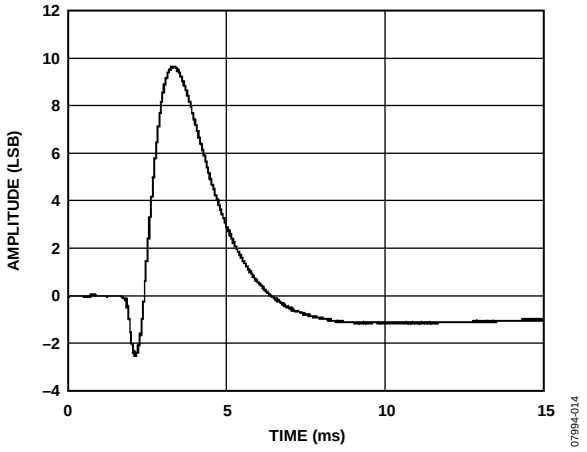


Figure 14. Digital-to-Analog Positive Glitch Impulse

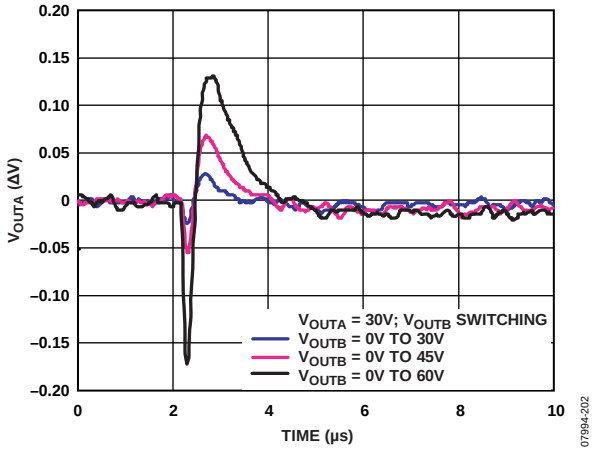


Figure 15. DAC-to-DAC Crosstalk

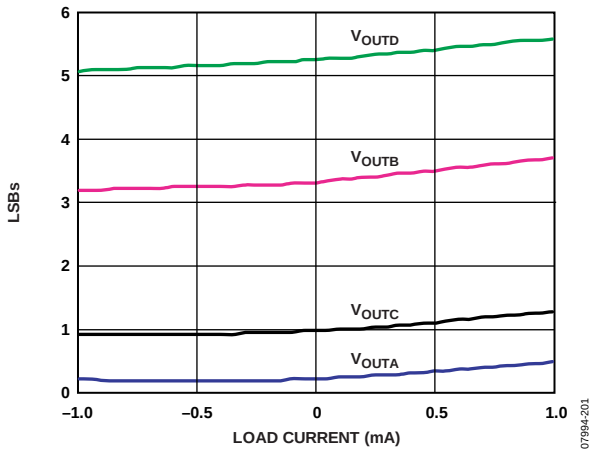


Figure 16. DAC-to-DAC Mismatch

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5504 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts.

Zero-Code Error Drift

Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Offset Error

A measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in millivolts in the linear region of the transfer function. Offset error is measured on the AD5504 with Code 32 loaded in the DAC registers for 60 V mode and with Code 64 loaded in the DAC registers for 30 V mode. Offset error is expressed in millivolts.

Offset Error Drift

Offset error drift is a measure of the change in offset error with a change in temperature. It is expressed in μV/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFF) is loaded into the DAC register. Full-scale error is expressed in millivolts.

Full-Scale Error Drift
Full-scale error drift is a measure of the change in full-scale error with a change in temperature. It is expressed in μV/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Gain Temperature Coefficient
The gain temperature coefficient is a measure of the change in gain with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

DC and AC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUTA}, V_{OUTB}, V_{OUTC}, or V_{OUTD} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. For dc PSRR, V_{DD} is dc varied ±10%. For ac PSRR, V_{DD} is ac varied ±10%.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in millivolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in μV/mA.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to ($\overline{SYNC}$ held high). It is specified in nV-s and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{LDAC}$ high, and then pulsing $\overline{LDAC}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Capacitive Load Stability

Capacitive load stability refers to the ability of the amplifier to drive a capacitive load. An amplifier output is considered stable if any overshoot or ringing has stopped before approximately 1.5 times the settling time of the DAC has elapsed.

THEORY OF OPERATION

The AD5504 contains four DACs, four output amplifiers, and a precision reference in a single package. The architecture of a single DAC channel consists of a 12-bit resistor string DAC followed by an output buffer amplifier. The part operates from a single-supply voltage of 10 V to 62 V. The DAC output voltage range is selected via the range select, $\overline{\text{R_SEL}}$, pin. The DAC output range is 0 V to 30 V if $\overline{\text{R_SEL}}$ is held high and 0 V to 60 V if $\overline{\text{R_SEL}}$ is held low. Data is written to the AD5504 in a 16-bit word format (see Table 8), via a serial interface.

POWER-UP STATE

On power-up, the power-on reset circuitry clears the bits of the control register to 0x40 (see Table 10). This ensures that the analog section is initially powered down, which helps reduce power consumption. The user can program the DAC registers to the required values while typically consuming only 30 µA of supply current. The power-on reset circuitry also ensures that all the input and DAC registers power up in a known condition, 0x000, and remain there until a valid write to the device has taken place. The analog section can be powered up by setting any or all of Bit C2 to Bit C5 of the control register to 1.

POWER-DOWN MODE

Each DAC channel can be individually powered up or powered down by programming the control register (see Table 10). When the DAC channel is powered down, the associated analog circuitry turns off to reduce power consumption. The digital section of the AD5504 remains powered up. The output of the DAC amplifier can be three-stated or connected to AGND via an internal 20 kΩ resistor, depending on the state of Bit C6 in the control register. The power-down mode does not change the contents of the DAC register to ensure that the DAC channel returns to its previous voltage when the power-down bit is set to 1. The AD5504 also offers the user the flexibility of updating the DAC registers during power-down. The control register can be read back at any time to check the status of the bits.

DAC CHANNEL ARCHITECTURE

The architecture of a single DAC channel consists of a 12-bit resistor string DAC followed by an output buffer amplifier (see Figure 17). The resistor string section is simply a string of resistors, each of Value R from V_{REF} generated by the precision reference to AGND. This type of architecture guarantees DAC monotonicity. The 12-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier multiplies the DAC output voltage to give a fixed linear voltage output range of 0 V to 60 V if $\overline{\text{R_SEL}}$ = 0 or 0 V to 30 V if $\overline{\text{R_SEL}}$ = 1. Each output amplifier is capable of driving a 60 kΩ load while allowing an output swing within the range of AGND + 0.5 V and V_{DD} − 0.5 V.

Because the DAC architecture gives a fixed voltage output range of 0 V to 30 V or 0 V to 60 V, the user should set V_{DD} to at least 30.5 V or 60.5 V to use the maximum DAC resolution. The data format for the AD5501 is straight binary and the output voltage follows the formula

$$V_{OUT} = \frac{D}{4096} \times Range$$

where:

D is the code loaded to the DAC.

Range = 30, if $\overline{\text{R_SEL}}$ is high, and 60 if $\overline{\text{R_SEL}}$ is low.

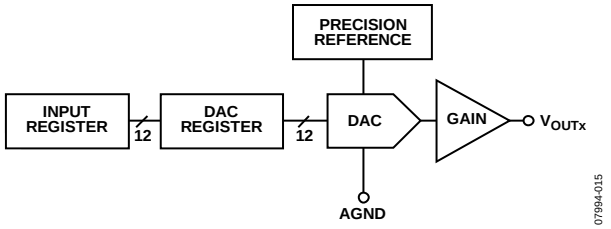


Figure 17. DAC Channel Architecture (Single-Channel Shown)

SELECTING THE OUTPUT RANGE

The output range of the DACs is selected by the $\overline{\text{R_SEL}}$ pin. When the $\overline{\text{R_SEL}}$ pin is connected to Logic 1, the DAC output voltages can be set between 0 V and 30 V. When the $\overline{\text{R_SEL}}$ pin is connected to Logic 0, the DAC output voltages can be set between 0 V and 60 V. The state of $\overline{\text{R_SEL}}$ can be changed any time when the serial interface is not being used, that is, not during a read or write operation. When the $\overline{\text{R_SEL}}$ pin is changed, the voltage on the output pin remains the same until the next write to the DAC register (and $\overline{\text{LDAC}}$ is brought low). For example, if the user writes 0x800 to the DAC register when in 30 V mode ($\overline{\text{R_SEL}}$ = 1), the output voltage is 15 V (assuming $\overline{\text{LDAC}}$ is low or has been pulsed low). When the user switches to 60 V mode ($\overline{\text{R_SEL}}$ = 0), the output stays at 15 V until the user writes a new value to the DAC register. $\overline{\text{LDAC}}$ must be low or be pulsed low for the output to change.

$\overline{\text{CLR}}$ FUNCTION

The AD5504 has a hardware $\overline{\text{CLR}}$ pin that is an asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge sensitive. Bringing the $\overline{\text{CLR}}$ line low clears the contents of the input register and the DAC registers to 0x000. The $\overline{\text{CLR}}$ pulse activation time, that is, the falling edge of $\overline{\text{CLR}}$ to when the output starts to change, is typically 100 ns.

$\overline{\text{LDAC}}$ FUNCTION

The DAC outputs can be updated using the hardware $\overline{\text{LDAC}}$ pin. $\overline{\text{LDAC}}$ is normally high. On the falling edge of $\overline{\text{LDAC}}$, data is copied from the input registers to the DAC registers, and the DAC outputs are updated simultaneously (asynchronous update mode, see Figure 3). If the $\overline{\text{LDAC}}$ is kept low, or is low on the falling edge of the 16th SCLK, the appropriate DAC register and DAC output are updated automatically (synchronous update mode, see Figure 3).

TEMPERATURE SENSOR

The AD5504 has an integrated temperature sensor that causes the part to enter thermal shutdown mode when the temperature on the die exceeds 110°C. In thermal shutdown mode, the analog section of the device powers down and the DAC outputs are disconnected, but the digital section remains operational, which is equivalent to setting the power-down bit in the control register. To indicate that the AD5504 has entered temperature shutdown mode, Bit 0 of the control register is set to 1 and the $\overline{\text{ALARM}}$ pin goes low. The AD5504 remains in temperature shutdown mode with Bit 0 set to 1 and the $\overline{\text{ALARM}}$ pin low, even if the die temperature falls, until Bit 0 in the control register is cleared to 0.

POWER DISSIPATION

Drawing current from any of the voltage output pins causes a temperature rise in the die and package of the AD5504. The package junction temperature (T_J) should not exceed 130°C for normal operation. If the die temperature exceeds 110°C, the AD5504 enters thermal shutdown mode as described in the Temperature Sensor section.

The amount of heat generated can be calculated using the formula

$$T_J = T_A + (P_{TOTAL} \times \theta_{JA})$$

where:
T_J is the package junction temperature.
T_A is the ambient temperature.
P_{TOTAL} is the total power being consumed by the AD5504.
θ_{JA} is the thermal impedance of the AD5504 package (see the Absolute Maximum Ratings section for this value).

POWER SUPPLY SEQUENCING

The power supplies for the AD5504 can be applied in any order without affecting the device. However, the AGND and DGND pins should be connected to the relevant ground plane before the power supplies are applied. None of the digital input pins (SCLK, SDI, $\overline{\text{SYNC}}$, R_SEL and $\overline{\text{CLR}}$) should be allowed to float during power up. The digital input pins can be connected to pull-up (to V_{LOGIC}) or pull-down (to DGND) resistors as required.

SERIAL INTERFACE

The AD5504 has a serial interface ($\overline{SYNC}$, SCLK, SDI, and SDO), which is compatible with SPI interface standards, as well with as most DSPs. The AD5504 allows writing of data, via the serial interface, to the input and control registers. The DAC registers are not directly writeable or readable.

The input shift register is 16 bits wide (see Table 8). The 16-bit word consists of one read/write (R/$\overline{W}$) control bit, followed by three address bits and 12 DAC data bits. Data is loaded MSB first.

WRITE MODE

To write to a register, the R/$\overline{W}$ bit should be 0. The three address bits in the input register (see Table 9) then determine the register to update. The address bits (A2 to A0) are used for either DAC register selection or for writing to the control register. Data is clocked into the selected register during the remaining 12 clocks of the same frame. Figure 3 shows a timing diagram of a typical AD5504 write sequence. The write sequence begins by bringing the $\overline{SYNC}$ line low. Data on the SDI line is clocked into the 16-bit shift register on the rising edge of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in the selected DAC/DACs input register/registers or a change in the mode of operation). The AD5504 does not require a continuous SCLK and dynamic power can be saved by transmitting clock pulses during a serial write only. At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence for a falling edge of $\overline{SYNC}$ to initiate the next write sequence. Operate all interface pins close to the supply rails to minimize power consumption in the digital input buffers.

READ MODE

The AD5504 allows data readback via the serial interface from every register directly accessible to the serial interface, which is all registers except the DAC registers. To read back a register, it is first necessary to tell the AD5504 that a readback is required. This is achieved by setting the R/$\overline{W}$ bit to 1. The three address bits then determine the register from which data is to be read back. Data from the selected register is then clocked out of the SDO pin on the next twelve clocks of the same frame.

The SDO pin is normally three-stated but becomes driven on the rising edge of the fifth clock pulse. The pin remains driven until the data from the register has been clocked out or the $\overline{SYNC}$ pin is returned high. Figure 4 shows the timing requirements during a read operation. Note that due to timing requirements of t_{14} (110 ns), the maximum speed of the SPI interface during a read operation should not exceed 9 MHz.

WRITING TO THE CONTROL REGISTER

The control register is written when Bits[DB14:DB12] are 1. The control register sets the power-up state of the DAC outputs. A write to the control register must be followed by another write operation. The second write operation can be a write to a DAC input register or a NOP write. Figure 18 shows some typical combinations.

Table 8. Input Register Bit Map

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/$\overline{W}$	A2	A1	A0	Data											

Table 9. Input Register Bit Functions

Bit	Description			
R/$\overline{W}$	Indicates a read from or a write to the addressed register.			
A2, A1, A0	These bits determine if the input registers or the control register are to be accessed.			
	A2	**A1**	**A0**	**Function/Address**
	0	0	0	No operation
	0	0	1	DAC A input register
	0	1	0	DAC B input register
	0	1	1	DAC C input register
	1	0	0	DAC D input register
	1	0	1	Write data contents to all four DAC input registers
	1	1	0	Reserved
	1	1	1	Control register
D11:D0	Data bits			

Table 10. Control Register Functions

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0[1]
R/$\overline{W}$	1	1	1	0	0	0	0	0	C6	C5	C4	C3	C2	C1	C0

[1] Read-only bit. This bit should be 0 when writing to the control register.

Table 11. Control Register Function Bit Descriptions

Bit No.	Bit Name	Description
DB0	C0	C0 = 0: the device is not in thermal shutdown mode. C0 = 1: the device is in thermal shutdown mode.
DB1	C1	C1 = 0: reserved. This bit should be 0 when writing to the control register.
DB2	C2[1]	C2 = 0: DAC Channel A power-down (default). C2 = 1: DAC Channel A power-up.
DB3	C3[1]	C3 = 0: DAC Channel B power-down (default). C3 = 1: DAC Channel B power-up.
DB4	C4[1]	C4 = 0: DAC Channel C power-down (default). C4 = 1: DAC Channel C power-up.
DB5	C5[1]	C5 = 0: DAC Channel D power-down (default). C5 = 1: DAC Channel D power-up.
DB6	C6	C6 = 0: outputs connected to AGND through a 20 kΩ resistor (default). C6 = 1: outputs are three-stated.

[1] If Bit C2 to Bit C5 are set to 0, the part is placed in power-down mode.

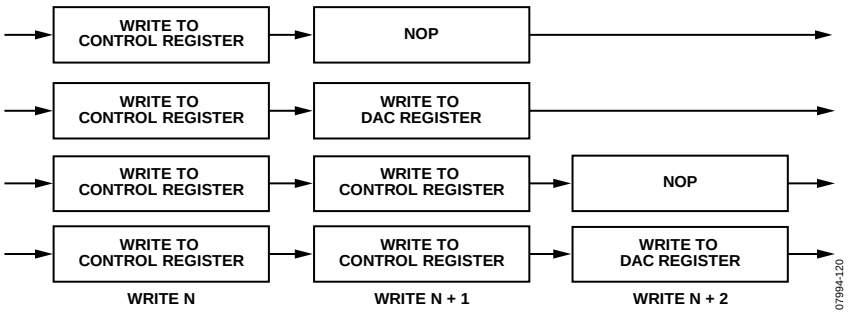


Figure 18. Control Register Write Sequences

INTERFACING EXAMPLES

The SPI interface of the AD5504 is designed to allow it to be easily connected to industry-standard DSPs and microcontrollers. Figure 19 shows how the AD5504 can be connected to the Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5504. Programmable input/output pins are also available and can be used to read or set the state of the digital input or output pins associated with the interface.

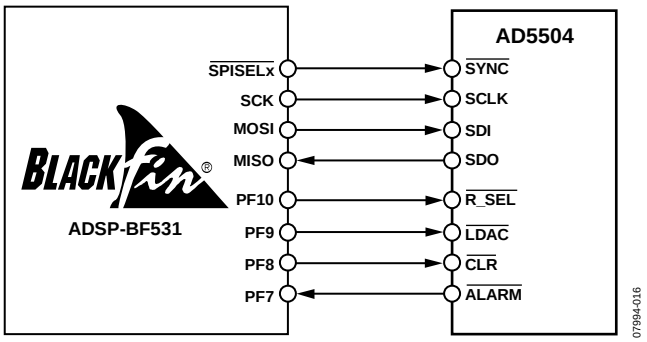


Figure 19. Interfacing to a Blackfin DSP

The Analog Devices ADSP-21065L is a floating point DSP with two serial ports (SPORTs). Figure 20 shows how one SPORT can be used to control the AD5504. In this example, the transmit frame synchronization (TFS) pin is connected to the receive frame synchronization (RFS) pin. The transmit and receive clocks (TCLK and RCLK) are also connected together. The user can write to the AD5504 by writing to the transmit register. When a read operation is performed, the data is clocked out of the AD5504 on the last 12 SCLKs. The DSP receive interrupt can be used to indicate when the read operation is complete.

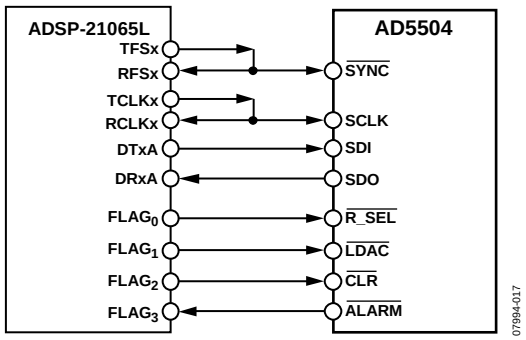


Figure 20. Interfacing to an ADSP-21065L DSP

OUTLINE DIMENSIONS

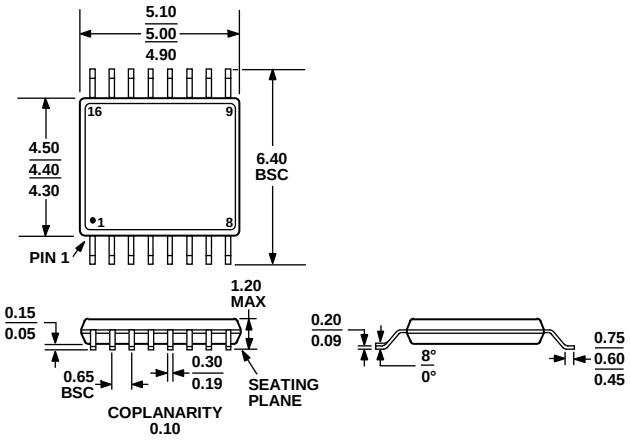


Figure 21. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5504BRUZ	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD5504BRUZ-REEL	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-AD5504EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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