

# DIO5632

## Single Inductor-Dual Output Power Supply

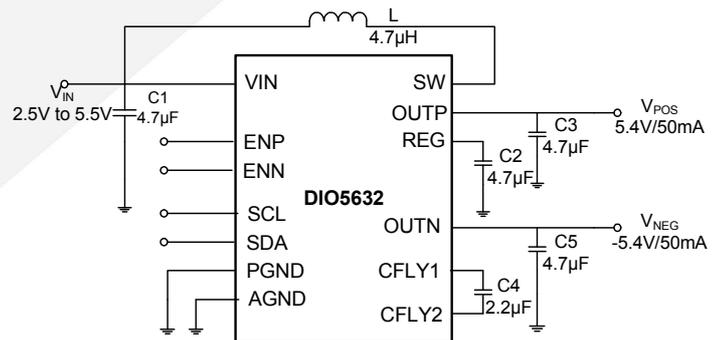
### Features

- SIMO(Single-Inductor Multiple-Output) Regulator Technology
- >85% Efficiency at  $I_{OUT}>10mA$
- 2.5-V to 5.5-V Input Voltage Range
- Under voltage Lockout Rising/Falling
- Programmable Output Voltage
- Positive Output Voltage Range: 4V to 6V (0.1-V step)
- Negative Output Voltage Range: -4V to -6V (0.1-V step)
- 1% Output Voltage Accuracy
- Programmable Active Discharge
- Internal EEPROM Type Memory (1000x Re-programmable)
- Excellent Line Regulation
- Advanced Power-Save Mode for Light-Load Efficiency
- Thermal Shutdown
- 15-Ball CSP Package
- QFN3\*4-20 Package
- QFN4\*4-20 Package

### Descriptions

The DIO5632 is designed to support general positive/negative driven applications. The device uses a single inductor scheme in order to provide the user the smallest solution size possible as well as high efficiency. With its input voltage range of 2.5V to 5.5V, it is optimized for products powered by single-cell batteries (Li-Ion, Ni-Li, Li-Polymer) and output currents up to 100 mA. The device is delivered in a WCSP package of 15 balls or in two QFN packages of 20 pins.

### Typical Application



### Applications

- TFT LCD Smart phones
- TFT LCD Tablets
- OLED Displays
- General Dual Power Supply Applications

### Ordering Information

Order Part Number	Top Marking		T <sub>A</sub>	Package	
DIO5632WL15	5632	Green	-40 to +85°C	CSP-15 Ball	Tape & Reel,3000
DIO5632QL20	DIO5632	Green	-40 to +85°C	QFN3*4-20	Tape & Reel,5000
DIO5632CL20	DIO5632	Green	-40 to +85°C	QFN4*4-20	Tape & Reel,5000

### Pin Assignments

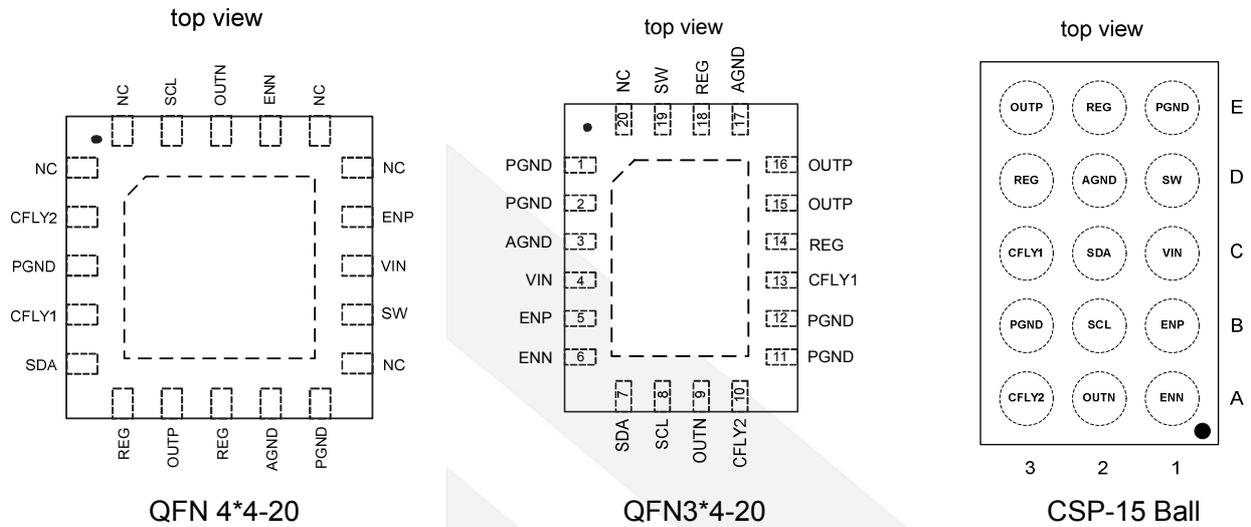


Figure 1 Pin Assignment

### Pin Definitions

PIN	I/O	Description
AND	–	Analog ground
CFLY1	I/O	Negative charge pump flying capacitor pin
CFLY2	I/O	Negative charge pump flying capacitor pin
ENN	I	Enable pin for $V_{NEG}$ rail
ENP	I	Enable pin for $V_{POS}$ rail
OUTP	O	Output pin of the LDO ( $V_{POS}$ )
OUTN	O	Output pin of the negative charge pump ( $V_{NEG}$ )
PGND	–	Power ground
REG	I/O	Boost converter output pin
SCL	I/O	I <sup>2</sup> C interface clock signal pin
SDA	I/O	I <sup>2</sup> C interface data signal pin
SW	I/O	Switch pin of the boost converter
VIN	I	Input voltage supply pin
NC	–	No Connected



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## Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Voltage Range on CFLY1, ENN, ENP, OUTP, REG, SCL,SDA, SW, VIN		-0.3 to 7	V
Voltage Range on CFLY2, OUTN		-7 to 0.3	V
Operating Temperature Range.		-40 to +85	°C
Junction Temperature Range		-40 to 150	°C
Package Thermal Resistance 15balls CSP, $\theta_{JA}$		76.5	°C/W
Storage Temperature		-65 to +150	°C
Lead Temperature (soldering, 10s)		260	°C
ESD Susceptibility	HBM	2000	V
	CDM	500	

## Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
Input Voltage Range	2.5 to 5.5	V
Inductor	2.2 to 4.7	$\mu$ H
Input capacitor	4.7	$\mu$ F
Fly capacitor	2.2	$\mu$ F
Output capacitors	4.7	$\mu$ F
Junction Temperature Range	-40 to 125	°C
Ambient Temperature Range	-40 to 85	°C



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## Electrical Characteristics

$T_A=25^{\circ}\text{C}$ ,  $V_{IN}=3.7\text{V}$ ,  $ENN=ENP=V_{IN}$ ,  $V_{POS}=5.4\text{V}$ ,  $V_{NEG}=-5.4\text{V}$ , unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>SUPPLY CURRENT</b>						
$V_{IN}$	Input voltage range		2.5		5.5	V
$V_{UVLO}$	Under voltage lockout threshold	$V_{IN}$ rising			2.5	V
	UVLO delay	$V_{IN}$ falling			2.3	V
$I_Q$	Quiescent current			0.54		mA
	Thermal shutdown			140		$^{\circ}\text{C}$
	Thermal shutdown hysteresis			20		$^{\circ}\text{C}$
<b>LOGIC ENN, ENP, SCL, SDA</b>						
$V_{IH}$	High level input voltage	$V_{IN}=2.5\text{V to }5.5\text{V}$	1.1			V
$V_{IL}$	Low level input voltage				0.54	V
$R_{EN}$	ENN, ENP pulldown resistors			200		k $\Omega$
<b>BOOST CONVERTER</b>						
$I_{LIM}$	Boost converter valley current limit		0.9	1.2	1.5	A
$f_{SW}$	Boost converter switching frequency		1.35	1.8	2.25	MHz
<b>LDO OUTPUT <math>V_{POS}</math></b>						
$V_{POS}$	Positive output voltage range		4		6	V
$V_{POS\_acc}$	Positive output voltage accuracy		-1%		0.01	
$I_{POS}$	Positive output current capability		200			mA
$V_{DO}$	Dropout voltage	$V_{REG}=V_{POS(NOM)}=5.4\text{V}$ , $I_{OUT}=150\text{ mA}$		160		mV
	Line regulation	$V_{IN}=2.5\text{V to }5.5\text{V}$ , $I_{OUT}=50\text{ mA}$		2.7		mV
	Load regulation	$\Delta I_{OUT}=100\text{ mA}$		3.4		%/A
$R_D$	Discharge resistor	Programmable; 20, 40, 60, 80, four steps	20		80	$\Omega$
	Soft-Start delay Time	Programmable		0.25		ms
					0.82	



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### NEGATIVE CHARGE PUMP OUTPUT $V_{NEG}$

$V_{NEG}$	Negative output voltage range		-4.0		-6.0	V
$V_{NEG\_acc}$	Negative output voltage accuracy		-1%		0.01	
$I_{NEG}$	Negative output current capability	Smartphone MODE	50			mA
		Tablet MODE	100			mA
$f_{OSC}$	Negative charge pump switching frequency		0.8	1.0	1.2	MHz
	Line regulation	$V_{IN}=2.5V$ to $5.5V$ , $I_{OUT}=50mA$		3.3		mV
	Load regulation	$\Delta I_{OUT}=100mA$		6.1		%/A
$R_D$	Discharge resistor	Programmable; 20, 40, 60, 80, four steps	20		80	$\Omega$
	Soft-Start delay Time	Programmable		0.4		ms
				1.6		

### I<sup>2</sup>C Interface Timing Requirements/Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$f_{SCL}$	SCL clock frequency	Standard MODE			100	kHz
		Fast MODE			400	kHz
$t_{LOW}$	LOW period of the SCL clock	Standard MODE	4.7			$\mu s$
		Fast MODE	1.3			$\mu s$
$t_{HIGH}$	HIGH period of the SCL clock	Standard MODE	4			$\mu s$
		Fast MODE	600			ns
$t_{BUF}$	Bus free time between a STOP and START condition	Standard MODE	4.7			$\mu s$
		Fast MODE	1.3			$\mu s$
$t_{hd,STA}$	Hold time for a repeated START condition	Standard MODE	4			$\mu s$
		Fast MODE	600			ns
$t_{su,STA}$	Setup time for a repeated START condition	Standard MODE	4.7			$\mu s$
		Fast MODE	600			ns

$t_{su;DAT}$	Data setup time	Standard MODE	250		ns
		Fast MODE	100		ns
$t_{hd;DAT}$	Data hold time	Standard MODE	0.05	3.45	$\mu$ s
		Fast MODE	0.05	0.9	$\mu$ s
$t_{RCL1}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard MODE	20 +0.1CB	1000	ns
		Fast MODE	20 +0.1CB	1000	ns
$t_{RCL}$	Rise time of SCL signal	Standard MODE	20 +0.1CB	1000	ns
		Fast MODE	20 +0.1CB	300	ns
$t_{FCL}$	Fall time	Standard MODE	20 +0.1CB	300	ns
		Fast MODE	20 +0.1CB	300	ns
$t_{RDA}$	Rise time of SDA signal	Standard MODE	20 +0.1CB	1000	ns
		Fast MODE	20 +0.1CB	300	ns
$t_{FDA}$	Fall time of SDA signal	Standard MODE	20 +0.1CB	300	ns
		Fast MODE	20 +0.1CB	300	ns
$t_{su;STO}$	Setup time for STOP condition	Standard MODE	4		$\mu$ s
		Fast MODE	600		ns
$C_B$	Capacitive load for SDA and SCL			0.4	nF

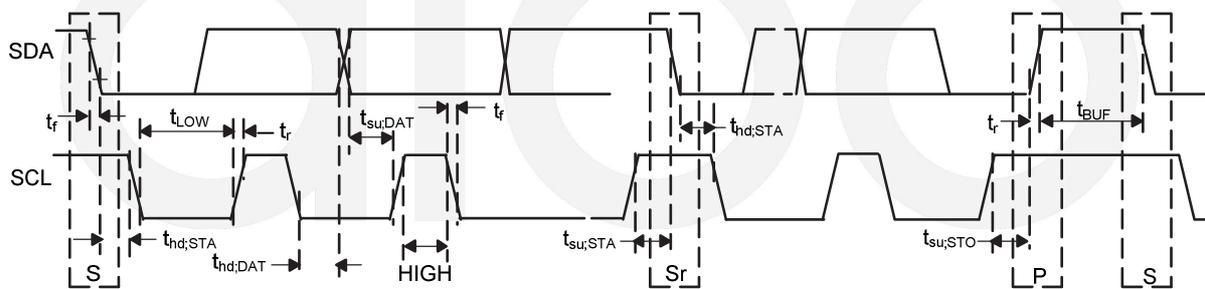


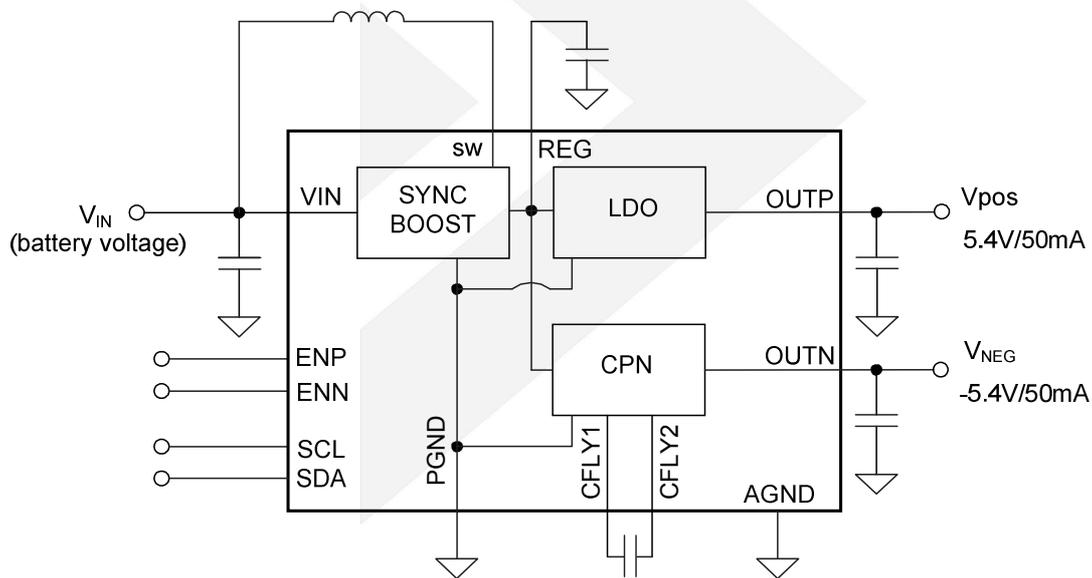
Figure 2 Serial Interface Timing For F/S-Mode

## Detailed Description

### 1. Overview

The DIO5632, supporting input voltage from 2.5V to 5.5V, operates with a single inductor scheme to provide a high efficiency with a small solution size. The synchronous boost converter generates a positive voltage that is regulated down by an integrated LDO, providing the positive supply rail ( $V_{POS}$ ). The negative supply rail ( $V_{NEG}$ ) is generated by an integrative charge pump (or CPN) driven from the boost converter output pin REG. The operating mode can be selected between Smartphone and Tablet in order to select the necessary output current capability and to get the best efficiency possible based on the application. The device topology allows a 100% asymmetry of the output currents.

### 2. Functional Block Diagram



**Figure 3. Function Block Diagram**

### 3. Feature Description

#### 3.1 Under Voltage Lockout (UVLO)

The DIO5632 integrates an under voltage lockout block (UVLO) that enables the device once the voltage on the VIN pin exceeds the UVLO threshold (2.5V maximum). No output voltage will however be generated as long as the enable signals are not pulled HIGH. The device, as well as all converters (boost converter, LDO, CPN), will be disabled as soon as the  $V_{IN}$  voltage falls below the UVLO threshold. The UVLO threshold is designed in a way that the DIO5632 will continue operating as long as  $V_{IN}$  stays above 2.3V. This guarantees a proper operation even in the event of extensive line transients when the battery gets suddenly heavily loaded.

For DIO5632, a 40ms delay is starting as soon as the UVLO threshold is reached. This delay prevents the device to be disabled and enabled by an unwanted VIN voltage spike. Once this delay has passed, the output rails can



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be enabled as desired with the enable signals without any delay. And the UVLO 40ms delay time can be enable/disable by factory programming.

### 3.2 Active Discharge

An active discharge of the positive rail and/or the negative rail can be programmed (DISP and CISN bits respectively – refer to DAC Registers). If programmed to be active, the discharge will occur at power down, when the enable signals go LOW. See Power-Down And Discharge (LDO) and Power-Down And Discharge (CPN) for a detailed description of how each device variant implements the active discharge function.

### 3.3 Boost Converter

#### 3.3.1 Boost Converter Operation

The synchronous boost converter uses a current mode topology and operates at a quasi-fixed frequency of typically 1.8MHz, allowing chip inductors such as 2.2 $\mu$ H or 4.7 $\mu$ H to be used. The converter is internally compensated and provides a regulated output voltage automatically adjusted depending on the programmed  $V_{POS}$  and  $V_{NEG}$  voltage. The boost converter operates either in continuous conduction mode (CCM) or Pulse Frequency Modulation mode (PFM), depending on the load current in order to provide the highest efficiency possible.

#### 3.3.2 Power-Up And Soft-Start (Boost Converter)

The boost converter starts switching as soon as the enable signal is pulled HIGH and the voltage on VIN pin is above the UVLO threshold. For DIO5632, in the case where the enable signal is already HIGH when  $V_{IN}$  reaches the UVLO threshold, the boost converter will only start switching after a 40ms delay has passed.

The boost converter starts up with an integrated soft-start to avoid drawing excessive inrush current from the supply. The output voltage  $V_{REG}$  is slowly ramped up to its target value.

#### 3.3.3 Power-Down (Boost Converter)

The boost converter stops switching when  $V_{IN}$  is below the UVLO threshold or when both output rails are disabled. For example, due to a special sequencing, the LDO might still be operating while the CPN is already disabled, in which case, the boost will continue operating until the LDO has been disabled.

#### 3.3.4 Isolation (Boost Converter)

The boost converter output (REG) is isolated from the input supply  $V_{IN}$ , providing a true shutdown.

#### 3.3.5 Output Voltage (Boost Converter)

The output voltage of the boost converter is automatically adjusted depending on the programmed  $V_{POS}$  and  $V_{NEG}$  voltage.

#### 3.3.6 Advanced Power-Save Mode For Light-Load Efficiency And PFM

The DIO5632 device integrates a power save mode to improve efficiency at light load. In power save mode the converter stops switching when the inductor current reaches 0 A. The device resumes its switching activity with one or more pulses once the  $V_{REG}$  voltage falls below its regulation level, and goes again into power save mode once the inductor current reaches 0 A. The pulse duration remains constant, but the frequency of these pulses varies according to the output load. This operating mode is also known as Pulse Frequency Modulation or PFM.

### **3.4 LDO Regulator**

#### **3.4.1 LDO Operation**

The Low Dropout regulator (or LDO) generates the positive voltage rail  $V_{POS}$  by regulating down the output voltage of the boost converter ( $V_{REG}$ ). Its inherent power supply rejection helps filtering the output ripple of the boost converter in order to provide on OUTP pin a clean voltage, e.g. to supply the source driver IC of the display.

#### **3.4.2 Power-Up And Soft-Start (LDO)**

The LDO starts operating as soon as the ENP signal is pulled HIGH,  $V_{IN}$  voltage is above the UVLO threshold and the boost converter has reached its Power Good threshold.

In the case where the enable signal is already HIGH when  $V_{IN}$  exceeds the UVLO threshold, the boost converter will start first and the LDO will only start after the boost converter has reached its target voltage.

The LDO integrates a soft-start that slowly ramps up its output voltage  $V_{POS}$  regardless of the output capacitor, as long as the LDO current limit is not reached. For DIO5632, the typical ramp-up time can be programmed to be 0.25ms/0.82ms by factory programming.

#### **3.4.3 Power-Down And Discharge (LDO)**

The LDO stops operating when  $V_{IN}$  is below the UVLO threshold or when ENP is pulled LOW.

The positive rail can be actively discharged to GND during power-down if required. A discharge selection bit is available to enable or disable this function.

#### **3.4.4 Isolation (LDO)**

The LDO is isolating the  $V_{POS}$  rail from  $V_{REG}$  (boost converter output) as long as the rail is not enabled in order to ensure flexible startup like  $V_{NEG}$  before  $V_{POS}$ .

#### **3.4.5 Setting The Output Voltage (LDO)**

The output voltage of the LDO is programmable via a I<sup>2</sup>C compatible interface, from 4.0V to 6.0V with 100mV steps. For more details, please refer to the DAC Settings section.

### **3.5 Negative Charge Pump**

#### **3.5.1 Operation**

The negative charge pump (CPN) generates the negative voltage rail  $V_{NEG}$  by inverting and regulating the output voltage of the boost converter ( $V_{REG}$ ). The charge pump uses 4 switches and an external flying capacitor to generate the negative rail. Two of the switches are turned on in the first phase to charge the flying capacitor up to  $V_{REG}$ , and in the second phase they are turned-off and the two others turn on to pump the energy negatively out of the OUTN capacitor.

#### **3.5.2 Power-Up And Soft-Start (CPN)**

The CPN starts operating as soon as the ENN signal is pulled HIGH,  $V_{IN}$  voltage is above the UVLO threshold and the boost converter has reached its Power Good threshold.

In the case where the enable signal is already HIGH when  $V_{IN}$  reaches the UVLO threshold, the boost converter will start first and the CPN will only start after the boost converter has reached its target voltage.



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The CPN integrates a soft-start that slowly ramps up its output voltage  $V_{NEG}$  within a time defined by the selected mode, the output voltage and the output capacitor value. For DIO5632, the typical ramp-up time can be programmed to be 0.4ms/1.6ms by factory programming.

### 3.5.3 Power-Down And Discharge (CPN)

The CPN stops operating when  $V_{IN}$  is below the UVLO threshold or when ENN is pulled LOW.

The negative rail can be actively discharged to GND during power-down if required. A discharge selection bit is available to enable or disable this function.

### 3.5.4 Isolation (CPN)

The CPN isolates the  $V_{NEG}$  rail from  $V_{REG}$  (boost converter output) as long as the rail is not enabled in order to ensure flexible startup like  $V_{POS}$  before  $V_{NEG}$ .

### 3.5.5 Setting The Output Voltage (CPN)

The output voltage of the CPN is programmable via a I<sup>2</sup>C compatible interface, from 4.0V to 6.0V with 100mV steps. For more details, please refer to the DAC Settings section.

## 4. Device Functional Mode

### 4.1 Enabling and Disabling the Device

The DIO5632 is enabled as long as the  $V_{IN}$  voltage is above the UVLO and one of the enable pins (ENP or ENN) is HIGH. Pulling ENP or ENN LOW disables either rail ( $V_{POS}$  or  $V_{NEG}$  respectively); and, pulling both pins LOW disables the device entirely.

## 5. Programming

### 5.1 I<sup>2</sup>C Serial Interface Description

The DIO5632 communicates through an industry standard I<sup>2</sup>C compatible interface, to receive data in slave mode. I<sup>2</sup>C is a 2-wire serial interface developed by Philips Semiconductor.

The DIO5632 integrates a non-volatile memory (EEPROM) that allows the storage of the DAC values into the registers with a capability of up to 1000 programming cycles maximum.

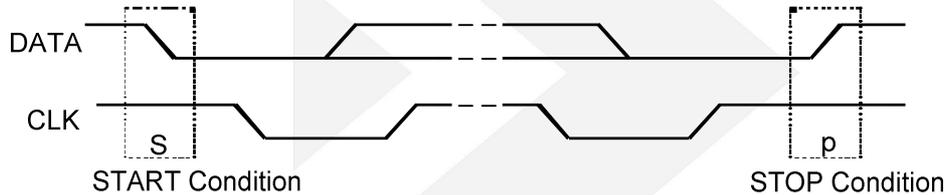
The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The DIO5632 works as a slave and supports the following data transfer modes, as defined in the I<sup>2</sup>C-Bus specification: standard mode (100 kbps) and fast mode (400 kbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The DIO5632 supports 7-bit addressing. The device 7-bit address is 3E, and the LSB enables the write or read function.

MSB		DIO5632					Address	LSB
0	1	1	1	1	1	1	0	R/W
R/W = R/(W)								

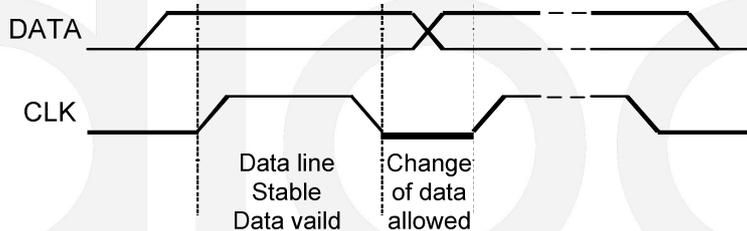
**Figure 4. DIO5632 Slave Address Bvte**

The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on SCL, controls the bus access, and generates START and STOP conditions. A START initiates a new data transfer to a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.



**Figure 5. Start And Stop Conditions**

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/(W) on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledgment, ACK, by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this Acknowledgment, the master knows that communication link with a slave has been established.



**Figure 6. Bit Transfer on The Serial Interface**

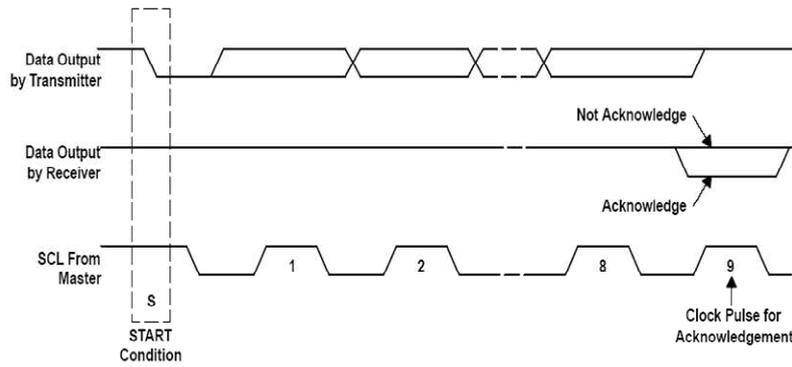


Figure 7. Acknowledge On The IC Bus<sup>2</sup>

The master generates further SCL cycles to either transmit data to the slave (R/W bit=0) or receive data from the slave (R/W bit=1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To terminate the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high. This releases the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C compatible devices must recognize the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

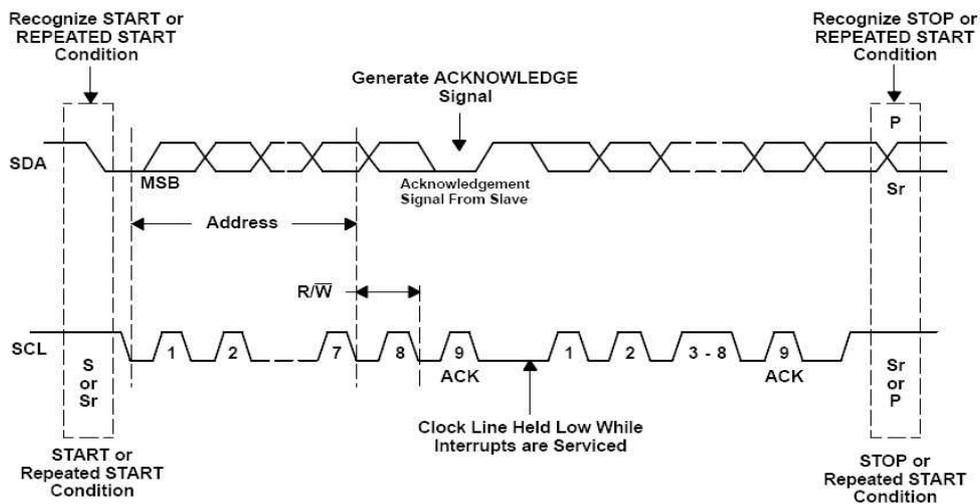
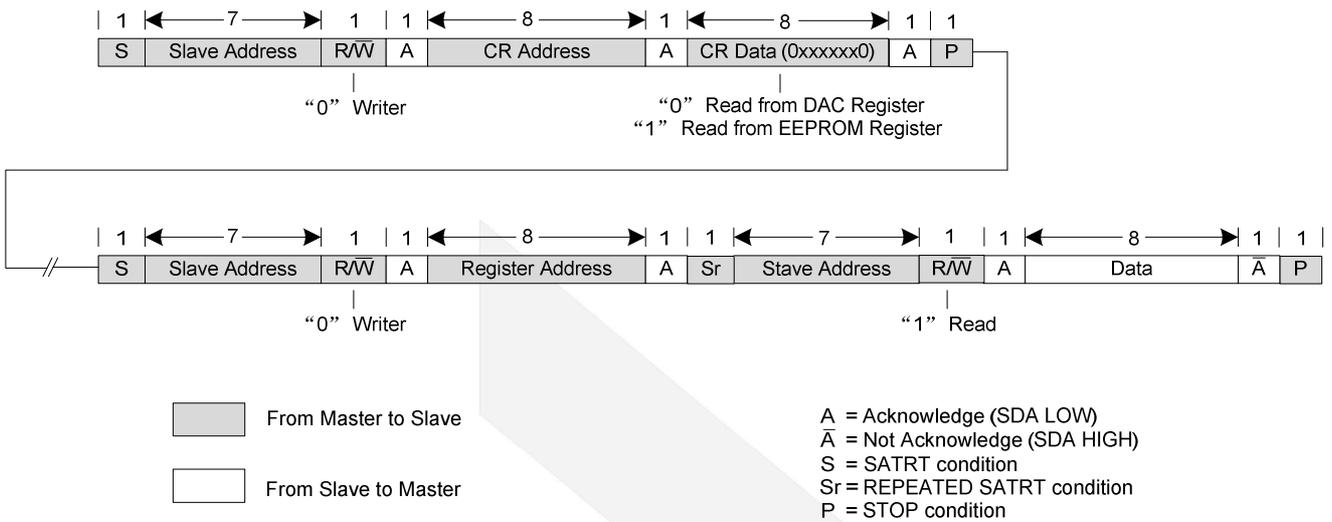
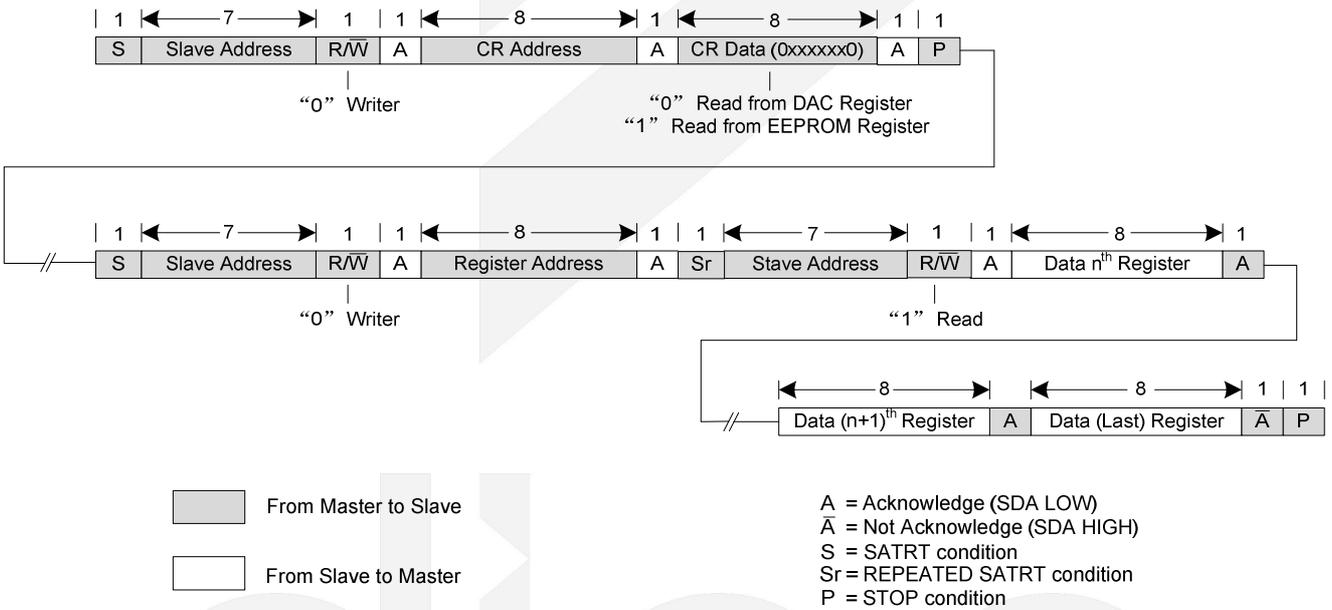


Figure 8. Bus Protocol





**Figure 12. “Read” Data From DAC/EEPROM — Transfer Format In F/S-Mode**



**Figure 13. “Read” Data From DAC/EEPROM — Transfer Format In F/S-Mode Featuring Register Address Auto-Increment**

## 6. Register Maps

The DIO5632 has one non-volatile memory which contains the initial value of the DAC and one volatile memory which contains the DAC setting. The non-volatile memory is called the Initial Value Register (IVR) and the volatile memory is called DAC Register (DR). The non-volatile IVR and the volatile memory is called DAC Register (DR). The non-volatile IVR and the volatile DR are accessed with the same address.

**Start option:** At power-up, the value contained in the IVR is loaded into the volatile DR and IVR presets the DAC to the last stored setting within less than 20µs. The programmed factory value if IVR of each address is described below and, at power-up, these data byte set the output voltage of each rail.

**Write description:** The user has to program all data registers first (0x00 ~ 0x03), Then set the WED (Write EEPROM Data) bit to 1 once all desired data are addressed. A dead time of 50ms is then initiated during which all the register data (0x00 ~0x03) are stored into the non volatile EEPROM cell. During that time, there should be no data flowing through the I<sup>2</sup>C because the I<sup>2</sup>C interface is momentarily not responding.

After the 50ms have passed, the WED bit is automatically reset to 0, and the user is able to read the values or program again.

**Slave address:** 0x3E

X=R/W            R/W=1→read mode  
                      R/W=0→write mode

## 6.1 DAC Registers

Address 0x00								
MSB								LSB
Reserved	Reserved	Reserved	VPOS	VPOS	VPOS	VPOS	VPOS	

**Figure 14. VPOS Register – 0x00**

Address 0x00								
MSB								LSB
Reserved	Reserved	Reserved	VNEG	VNEG	VNEG	VNEG	VNEG	

**Figure 15. VNEG Register – 0x01**

Address 0x00								
MSB								LSB
Reserved	APPS	Reserved	Reserved	Reserved	Reserved	DISP	DISN(1)	

**Figure 16. APPS – DISP - DISN Register – 0x03**

(1) See Power-Down And Discharge (LDO) and Power-Down And Discharge (CPN) for a detailed description of how each device variant implements the active discharge function.

Address 0x00								
MSB								LSB
WED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EE/(DR)	

**Figure 17. Control Register – 0xFF**

The Reserved bits are ignored when written and return either 0 or 1 when read.

Attempting to read data from register addresses not listed in the following section will result in 0x00 being read out.



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### 6.2 DAC Settings

The following tables show the DAC values and the corresponding voltages of each block address.

VPOS-0x00	VPOS	VNEG-0x01	VNEG	APPS-0x03	APPLICATION
00h	4.0V	00h	-4.0V	0	Smartphone
01h	4.1V	01h	-4.1V	1	Tablet
02h	4.2V	02h	-4.2V		
03h	4.3V	03h	-4.3V		
04h	4.4V	04h	-4.4V		
05h	4.5V	05h	-4.5V	DISP—0x03	ACTIVE DISCHARGE
06h	4.6V	06h	-4.6V	0	No discharge
07h	4.7V	07h	-4.7V	1	V <sub>POS</sub> actively
08h	4.8V	08h	-4.8V		discharged
09h	4.9V	09h	-4.9V		
0Ah	5.0V	0Ah	-5.0V	DISN—0x03	ACTIVE DISCHARGE
0Bh	5.1V	0Bh	-5.1V	0	No discharge
0Ch	5.2V	0Ch	-5.2V	1	V <sub>NEG</sub> actively
0Dh	5.3V	0Dh	-5.3V		discharged
0Eh	5.4V	0Eh	-5.4V		
0Fh	5.5V	0Fh	-5.5V		
10h	5.6V	10h	-5.6V		
11h	5.7V	11h	-5.7V		
12h	5.8V	12h	-5.8V		
13h	5.9V	13h	-5.9V		
14h	6.0V	14h	-6.0V		

## Application and Implementation

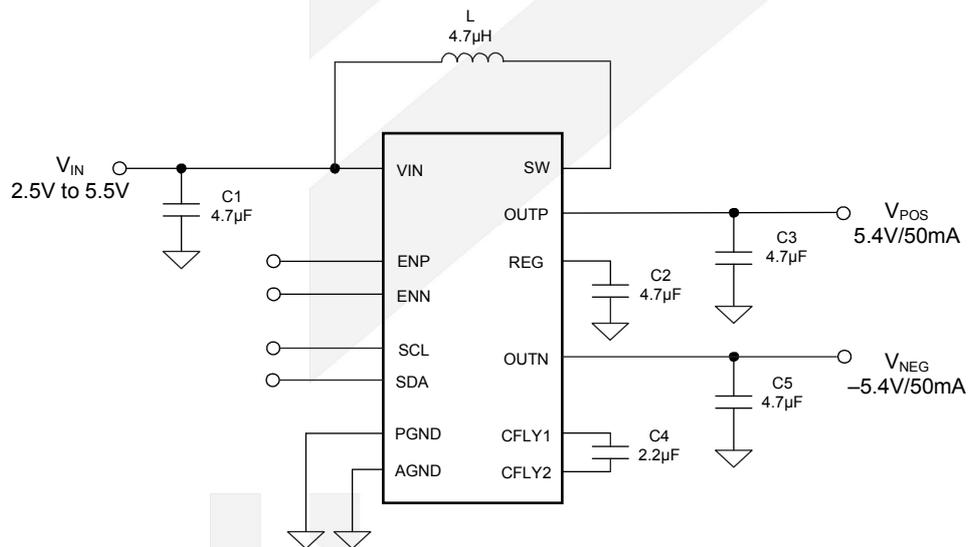
### 1. Application Information

The DIO5632 devices, primarily intended to supplying TFT LCD displays, can be used for any application that requires positive and negative supplies, ranging from  $\pm 4V$  to  $\pm 6V$  and current up to 100mA. Both output voltages can be set independently and their sequencing is also independent. The following section presents the different operating modes that the device can support as well as the different features that user can select.

### 2. Typical Applications

#### 2.1 Low-current Applications( $\leq 50mA$ )

The DIO5632 can be programmed to Smartphone mode with the APPS bit to support applications that require output currents up to 50mA (refer to DAC Settings). The Smartphone mode limits the negative charge pump output current to 50mA DC in order to provide the highest efficiency possible. The  $V_{POS}$  rail can deliver up to 200mA DC regardless of the mode. Output peak currents are supported by the output capacitors.



**Figure 18. Typical Application Circuit For Smart phones**

#### 2.1.1 Design Requirements

PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5V to 5.5V
Output Voltage	4.0V to 6.0V
Output Current Rating	50 mA
Boost Converter Switching Frequency	1.8 MHz
Negative Charge Pump Switching Frequency	1.0 MHz

## 2.1.2 Detailed Design Procedure

### 2.1.2.1 Sequencing

Each output rail ( $V_{POS}$  and  $V_{NEG}$ ) is enabled and disabled using an external enable signal. If not explicitly specified, the enable signal in the rest of the document refers to ENN or ENP: ENP for positive rail  $V_{POS}$  and ENN for the negative rail  $V_{NEG}$ .

### 2.1.2.2 Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency number from the provided efficiency curves at the application's maximum load or to use a worst case assumption for the expected efficiency, e.g., 85%.

1. Duty Cycle:  $D = 1 - \frac{V_{IN\_min} \times \eta}{V_{REG}}$
2. Inductor ripple current:  $\Delta I_L = \frac{V_{IN\_min} \times D}{f_{SW} \times L}$
3. Maximum output current:  $I_{OUT\_max} = \left( I_{LIM\_min} - \frac{\Delta I_L}{2} \right) \times (1 - D)$
4. Peak switch current of the application:  $I_{SWPEAK} = \frac{I_{OUT}}{1 - V_{REG}} + \frac{\Delta I_L}{2}$

$\eta$  = Estimated boost converter efficiency (use the number from the efficiency plots or 85% as an estimation)

$f_{SW}$  = Boost converter switching frequency (1.8 MHz)

$L$  = Selected inductor value for the boost converter (see the Inductor Selection section)

$I_{SWPEAK}$  = Boost converter switch current at the desired output current (must be  $< [I_{LIM\_min} + \Delta I_L]$ )

$\Delta I_L$  = Inductor peak-to-peak ripple current

$V_{REG} = \max(V_{POS}, |V_{NEG}|) + 200 \text{ mV}$  (in Smartphone mode — + 300 mV in Tablet mode)

$I_{OUT} = I_{OUT\_VPOS} + |I_{OUT\_VNEG}|$  ( $I_{OUT\_max}$  being the maximum current delivered on each rail)

The peak switch current is the current that the integrated switch and the inductor have to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

#### 2.1.2.2.1 Inductor Selection (Boost Converter)

Saturation current: the inductor must handle the maximum peak current ( $I_{L\_SAT} > I_{SWPEAK}$ , or  $I_{L\_SAT} > [I_{LIM\_min} + \Delta I_L]$  as conservation approach).

DC Resistance: the lower the DCR, the lower the losses.

Inductor value: in order to keep the ratio  $I_{OUT}/\Delta I_L$  low enough for proper sensing operation purpose, it is recommended to use a 4.7 $\mu$ H inductor for Smartphone mode (a 2.2 $\mu$ H might however be used, but the efficiency might be lower than with 4.7 $\mu$ H at light output loads depending on the inductor characteristics).

#### 2.1.2.2.2 Input Capacitor Selection (Boost Converter)

For best input voltage filtering low ESR ceramic capacitors are recommended. DIO5632 has an analog input pin VIN. A 4.7 $\mu$ F minimum bypass capacitor is required as close as possible from VIN to GND. This capacitor is also

used as the boost converter input capacitor.

For better input voltage filtering, this value can be increase or two capacitors can be used: one 4.7 $\mu$ F input capacitor for the boost converter as well as a 1 $\mu$ F bypass capacitor close to the VIN pin.

#### **2.1.2.2.3 Output Capacitor Selection (Boost Converter)**

For the best output voltage filtering, low-ESR ceramic capacitors are recommended. A minimum of 4.7 $\mu$ F ceramic output capacitor is required. Higher capacitor values can be used to improve the load transient response.

#### **2.1.2.3 Input Capacitor Selection (LDO)**

The LDO input capacitor is also the boost converter output capacitor.

#### **2.1.2.4 Output Capacitor Selection (LDO)**

The LDO is designed to operate with a 4.7 $\mu$ F minimum ceramic output capacitor.

#### **2.1.2.5 Input Capacitor Selection (CPN)**

The CPN input capacitor is also the boost converter output capacitor.

#### **2.1.2.6 Output Capacitor Selection (CPN)**

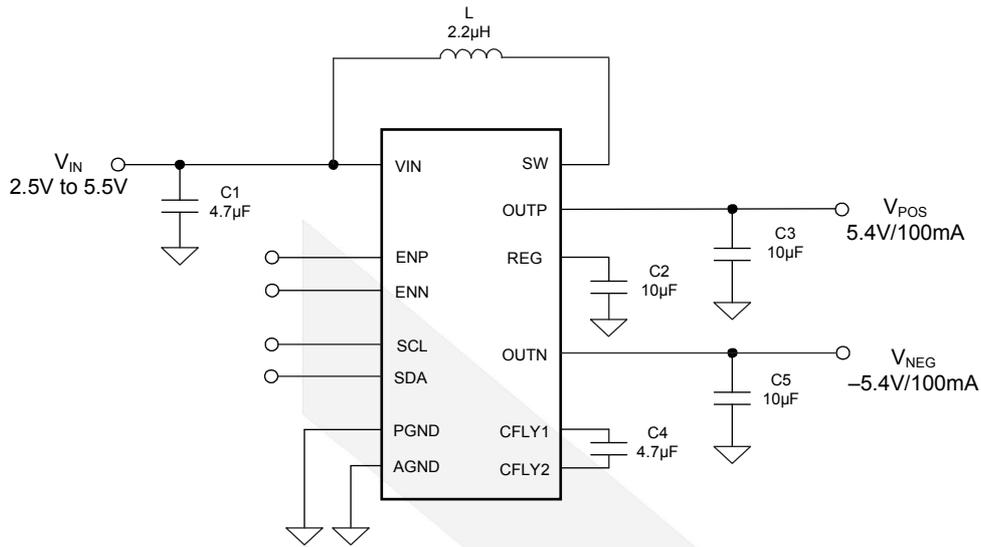
The CPN is designed to operate with a 4.7 $\mu$ F minimum ceramic output capacitor.

#### **2.1.2.7 Flying Capacitor Selection (CPN)**

The CPN needs an external flying capacitor. The minimum value is 2.2 $\mu$ F. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance. Therefore, a minimum capacitance of 1 $\mu$ F must be achieved by the capacitor at a DC bias voltage of  $|V_{NEG}|+300\text{mV}$ . For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on REG pin.

### **2.2 Mid-current Applications( $\leq 100\text{mA}$ )**

The DIO5632 can be programmed to Tablet mode with the APPS bit to support applications that require output currents up to 100mA. The Tablet mode is limiting the negative charge pump (CPN) output current to 100mA DC in order to provide the highest efficiency possible where the  $V_{(POS)}$  rail can deliver up to 200mA DC regardless of the mode. Output peak currents are supported are supported by the output capacitors.



**Figure 19. Typical Application Circuit For Tables**

## 2.2.1 Design Requirements

PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5V to 5.5V
Output Voltage	4.0V to 6.0V
Output Current Rating	100 mA
Boost Converter Switching Frequency	1.8 MHz
Negative Charge Pump Switching Frequency	1.0 MHz

## 2.2.2 Detailed Design Procedure

The design procedure for the Tablet mode is identical to the Smartphone mode, except for the BOM (bill of materials). Refer to the Sequencing for details about the sequencing. And the general component selection.

### 2.2.2.1 Boost Converter Design Procedure

#### 2.2.2.1.1 Inductor Selection (Boost Converter)

In order to keep the ratio  $I_{OUT}/\Delta I_L$  low enough for proper sensing operation purpose, it is recommended to use a 2.2µH inductor for Tablet mode. Refer to the Inductor Selection (Boost Converter) for details about the boost inductor selection.

#### 2.2.2.1.2 Inductor Capacitor Selection (Boost Converter)

A 4.7µF minimum bypass capacitor is required as close as possible from VIN to GND. This capacitor is also used as the boost converter input capacitor.

For better input voltage filtering, this value can be increased or two capacitors can be used: one 4.7 $\mu$ F input capacitor for the boost converter as well as 1 $\mu$ F bypass capacitor close to the VIN pin.

#### **2.2.2.1.3 Output Capacitor Selection (Boost Converter)**

For best output voltage filtering low ESR ceramic capacitors are recommended. A minimum of 10 $\mu$ F ceramic output capacitor is required. Higher capacitor values can be used to improve the load transient response.

#### **2.2.2.2 Input Capacitor Selection (LDO)**

The LDO input capacitor is also the boost converter output capacitor.

#### **2.2.2.3 Output Capacitor Selection (LDO)**

The LDO is designed to operate with a 4.7 $\mu$ F minimum ceramic output capacitor.

#### **2.2.2.4 Input Capacitor Selection (CPN)**

The CPN input capacitor is also the boost converter output capacitor.

#### **2.2.2.5 Output Capacitor Selection (CPN)**

The CPN is designed to operate with a 10 $\mu$ F minimum ceramic output capacitor.

#### **2.2.2.6 Flying Capacitor Selection (CPN)**

The CPN needs an external flying capacitor. The minimum value is 4.7 $\mu$ F. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance. Therefore, a minimum capacitance of 2.2 $\mu$ F must be achieved by the capacitor at a DC bias voltage of  $|V_{NEG}|+300\text{mV}$ . For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on REG pin.

## **Power Supply Recommendations**

The devices are designed to operate from an input voltage supply range between 2.5V and 5.5V. This input supply must be well regulated. A ceramic input capacitor with a value of 4.7 $\mu$ F is a typical choice.

## **Layout**

### **Layout Guidelines**

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the DIO5632 the following PCB layout guidelines are recommended.

- Keep the power ground plane on the top layer (all capacitor grounds and PGND pins must be connected together with one uninterrupted ground plane).
- AGND and PGND must be connected together on the same ground plane.
- Place the flying capacitor as close as possible to the IC.
- Always avoid vias when possible. They have high inductance and resistance. If vias are necessary, always use more than one in parallel to decrease parasitic especially for power lines.

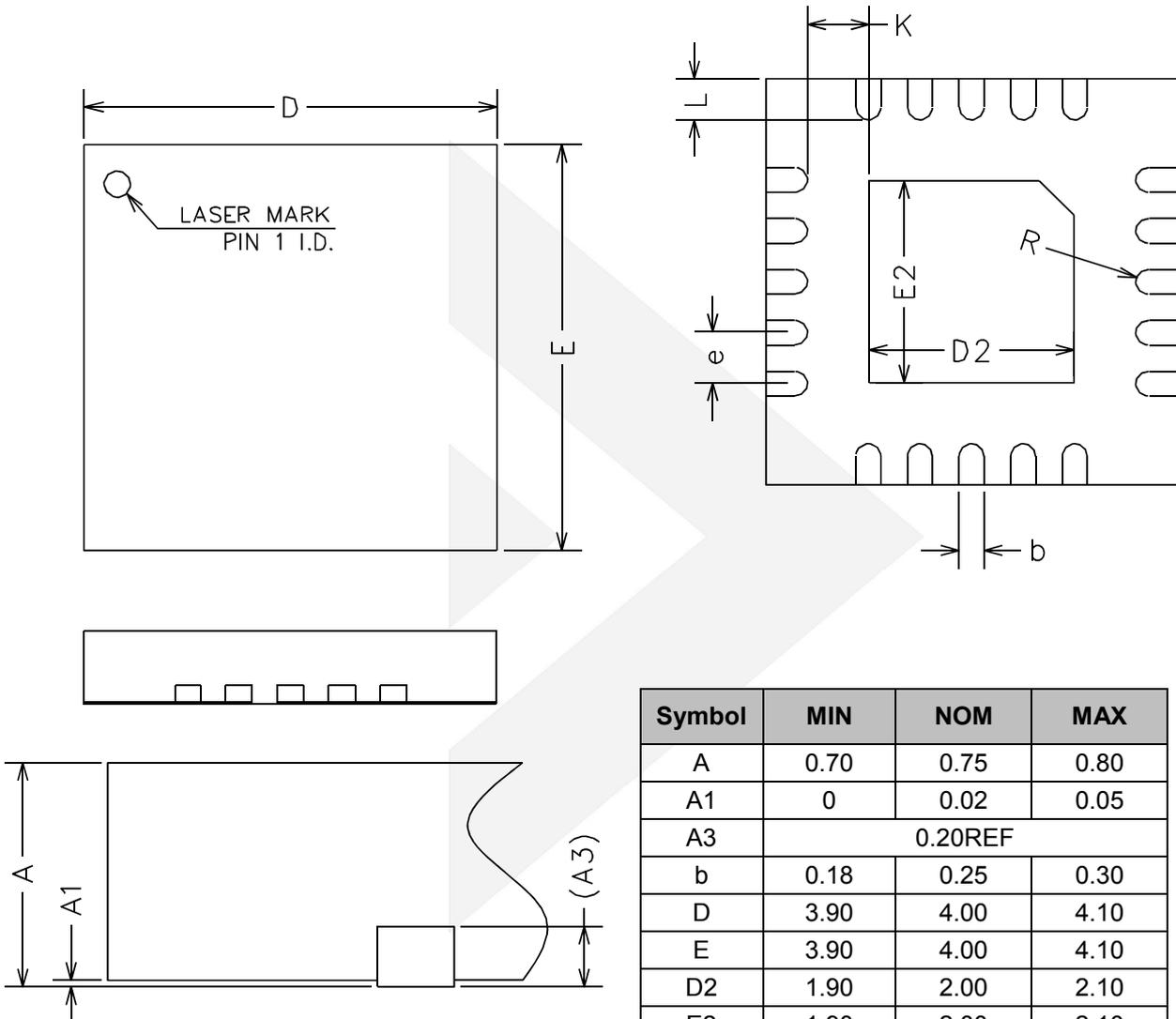


## DIO5632

- Connect REG pins together.
- For high  $dv/dt$  signals (switch pin trances): keep copper area to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For high  $di/dt$  signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Keep input capacitor close to the IC with low inductance traces.
- Keep trace from switching node pin to inductor short if possible: it reduces EMI emission and noise that may couple into other portions of the converter.
- Isolate analog signal paths from power paths.

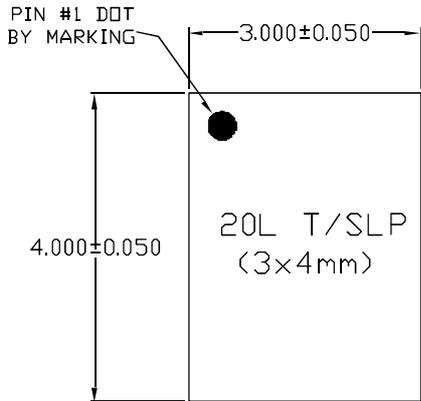


Physical Dimensions: QFN4\*4-20

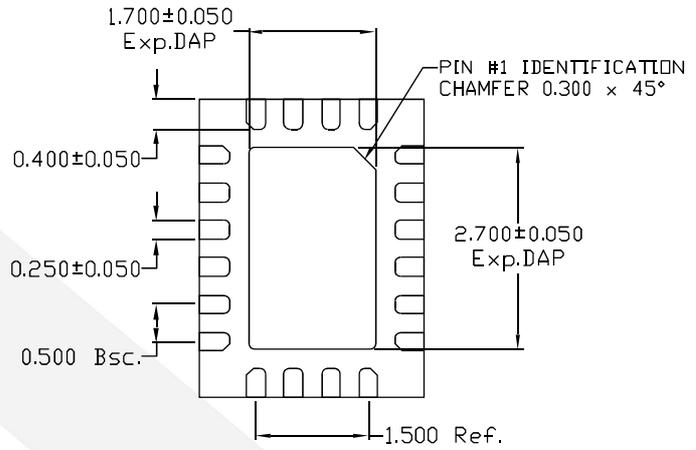


Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20REF		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	1.90	2.00	2.10
E2	1.90	2.00	2.10
e	0.40	0.50	0.60
K	0.20	-	-
L	0.35	0.40	0.45
R	0.09	-	-

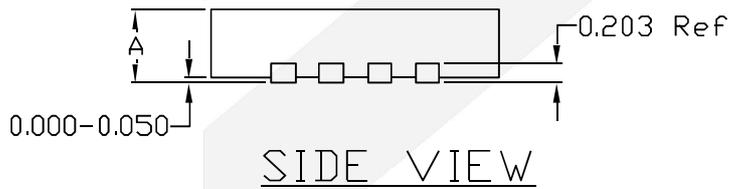
Physical Dimensions: QFN3\*4-20



TOP VIEW



BOTTOM VIEW



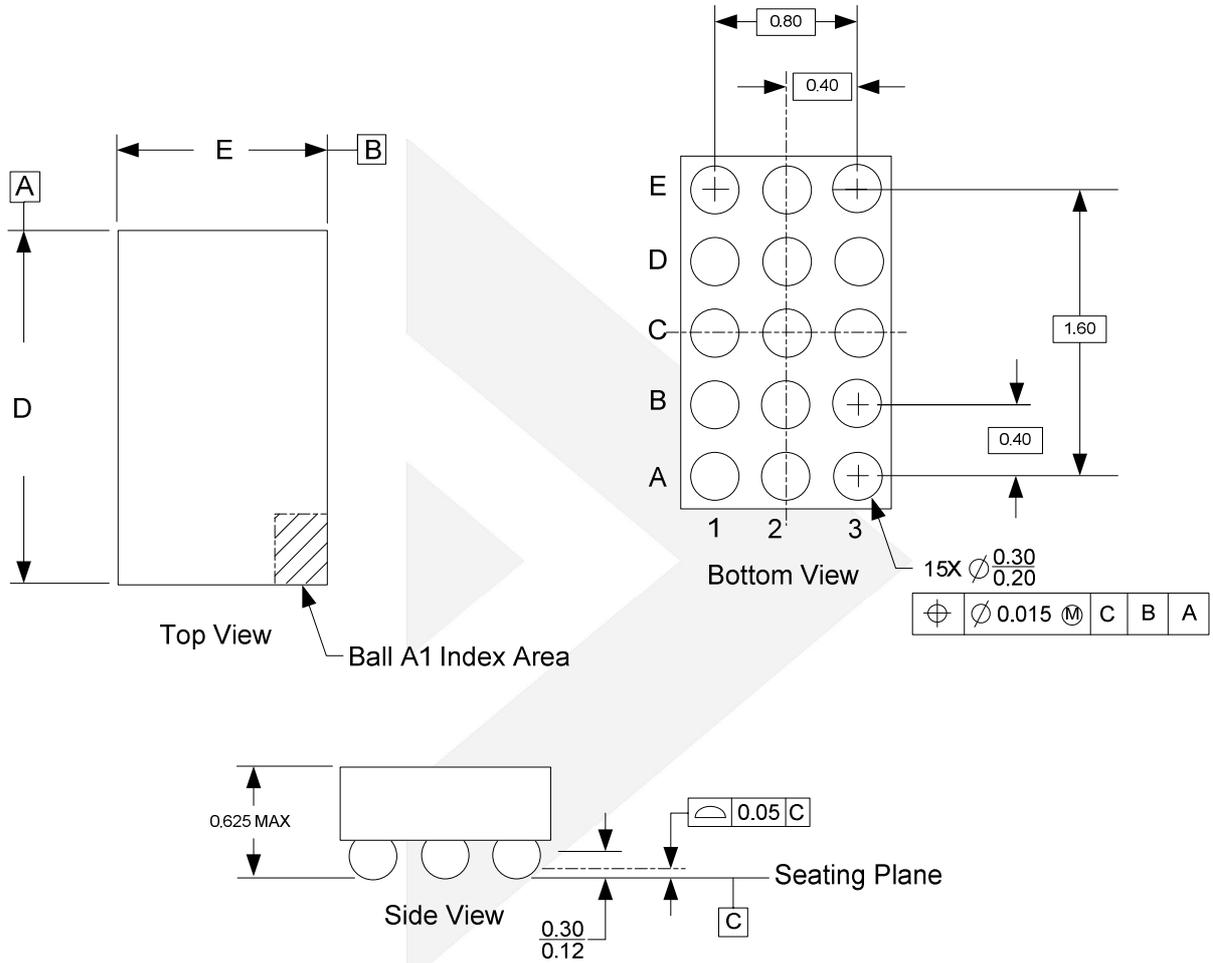
SIDE VIEW

Note:

A:Min=0.800mm , Typ=0.850mm, Max=0.900mm



Physical Dimensions: CSP-15 Ball



D:Min=2.078mm , Typ=2.11mm, Max=2.138mm  
 E:Min=1.484mm, Typ=1.51mm, Max=1.544mm





DIO5632

Single Inductor – Dual Output Power Supply

## CONTACT US

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For additional product information, or full datasheet, please contact with our Sales Department or Representatives.

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