**Product data sheet** 

## 1 General description

The 74LVT02 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

The 74LVT02 is a quad 2-input NOR gate.

### 2 Features and benefits

- Wide supply voltage range from 2.7 V to 3.6 V
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Latch-up protection
  - JESD78 Class II exceeds 500 mA
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

# 3 Ordering information

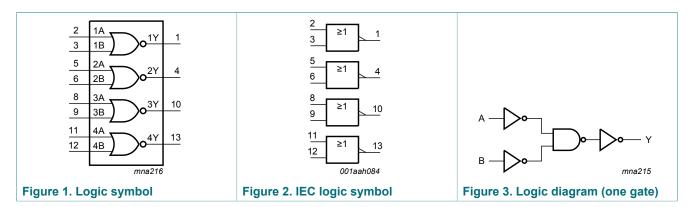
**Table 1. Ordering information** 

Type number	Package						
	Temperature range	Name	Description	Version			
74LVT02D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			
74LVT02DB	-40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1			
74LVT02PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1			



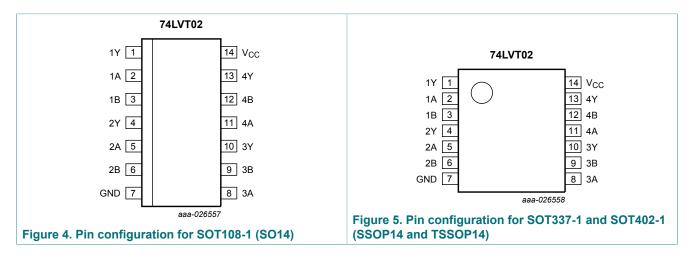
3.3 V Quad 2-input NOR gate

# 4 Functional diagram



# 5 Pinning information

## 5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y to 4Y	1, 4, 10, 13	data output
1A to 4A	2, 5, 8, 11	data input
1B to 4B	3, 6, 9,12	data input
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

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# **Functional description**

Table 3. Function table [1]

Input		Output
nA	nB	nY
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level

# **Limiting values**

### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
VI	input voltage	[1	-0.5	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state	-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
Io	output current	output in LOW-state	-	64	mA
		output in HIGH-state	-32	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	[2	_	150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 to +85 °C	_	500	mW

#### **Recommended operating conditions** 8

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		2.7	-	3.6	V
VI	input voltage		0	-	5.5	V
I <sub>OH</sub>	HIGH-level output current		-20	-	-	mA
I <sub>OL</sub>	LOW-level output current		-	-	32	mA
T <sub>amb</sub>	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

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The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

For SO14 packages: above 70 °C derate linearly with 8 mW/K.

<sup>[3]</sup> For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

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## **Static characteristics**

### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
T <sub>amb</sub> = -40	°C to +85 °C					'
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = -18 mA	-1.2		-	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
V <sub>OH</sub>	HIGH-level output	$V_{CC}$ = 2.7 V to 3.6 V; $I_{OH}$ = -100 $\mu$ A	V <sub>CC</sub> - 0.2		-	V
	voltage	V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -6 mA	2.4	-	-	V
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -20 mA	2.0	-	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC}$ = 2.7 V; $I_{OL}$ = 100 $\mu$ A	-		0.2	V
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 24 mA	-		0.5	V
		$V_{CC}$ = 3.0 V; $I_{OL}$ = 32 mA	-		0.5	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V	-	-	10	μA
		$V_{CC}$ = 3.6 V; $V_{I}$ = $V_{CC}$ or GND		-	±1	μA
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; V_1 \text{ or } V_0 = 0 \text{ V to } 4.5 \text{ V}$			±100	μΑ
I <sub>CC</sub>	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = \text{GND or } V_{CC}; I_{O} = 0 \text{ A}$				
		output HIGH	-	-	0.02	mA
		output LOW	-	1	2	mA
Δl <sub>CC</sub>	additional supply current	per input pin; $V_{CC}$ = 3.0 V to 3.6 V; one input at $V_{CC}$ - 0.6 V and other inputs at $V_{CC}$ or GND	[2] _		0.2	μΑ
Cı	input capacitance	V <sub>I</sub> = 0 V or 3.0 V	-	3	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 3.3 V. [2] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

3.3 V Quad 2-input NOR gate

# 10 Dynamic characteristics

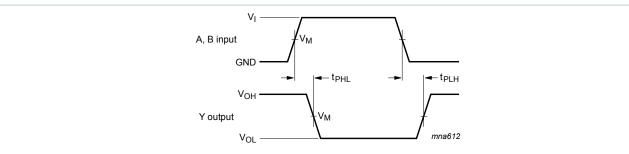
## **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$T_{amb} = -40$	0 °C to +85 °C					
t <sub>PLH</sub>	LOW to HIGH	nA or nB to nY; see Figure 6				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	5.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1	2.8	4.4	ns
t <sub>PHL</sub>	HIGH to LOW	nA or nB to nY; see Figure 6				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	3.4	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1	2.6	3.6	ns

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 3.3 V.

## 10.1 Waveforms and test circuit



Measurement points are given in <u>Table 8</u>.

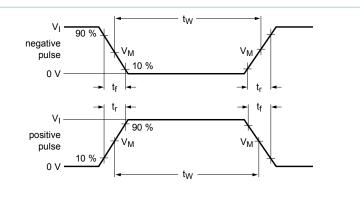
 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

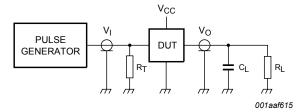
Figure 6. Input to output propagation delays

**Table 8. Measurement points** 

Input		Output
$V_{M}$	V <sub>I</sub>	V <sub>M</sub>
1.5 V	2.7 V	1.5 V

## 3.3 V Quad 2-input NOR gate





Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = load capacitance including jig and probe capacitance.

R<sub>L</sub> = load resistance.

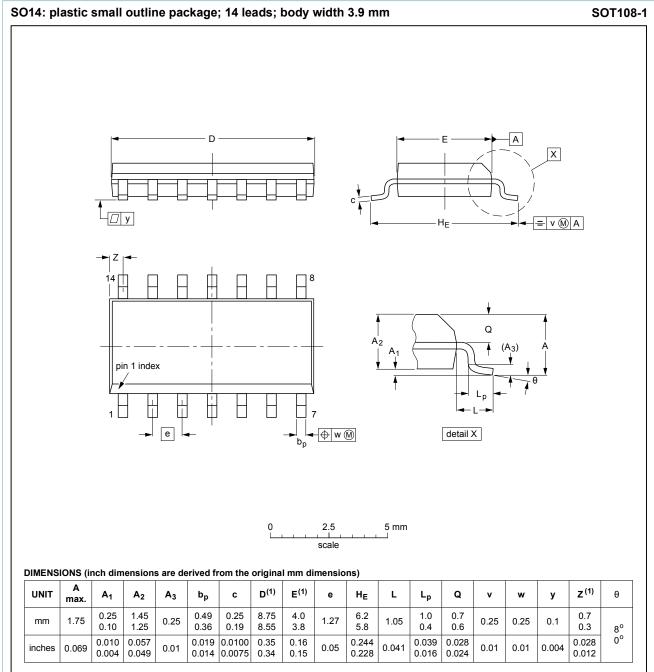
Figure 7. Test circuit for measuring switching times

Table 9. Test data

Input			Load		Test	
VI	fi	t <sub>W</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	t <sub>PLH</sub> , t <sub>PHL</sub>

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# 11 Package outline



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	1920E DATE	
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19	

Figure 8. Package outline SOT108-1 (SO14)

74LVT02

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## 3.3 V Quad 2-input NOR gate

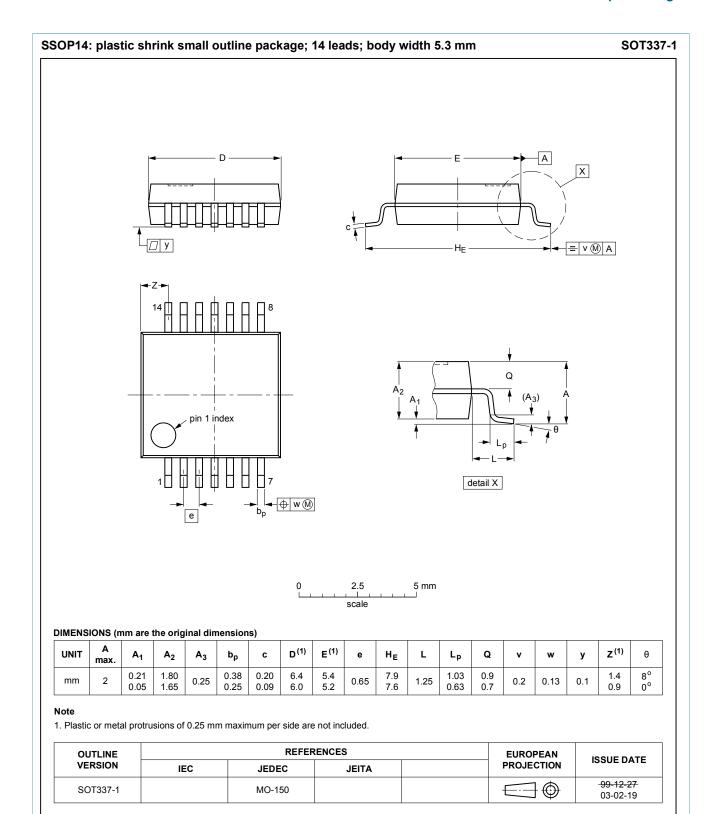
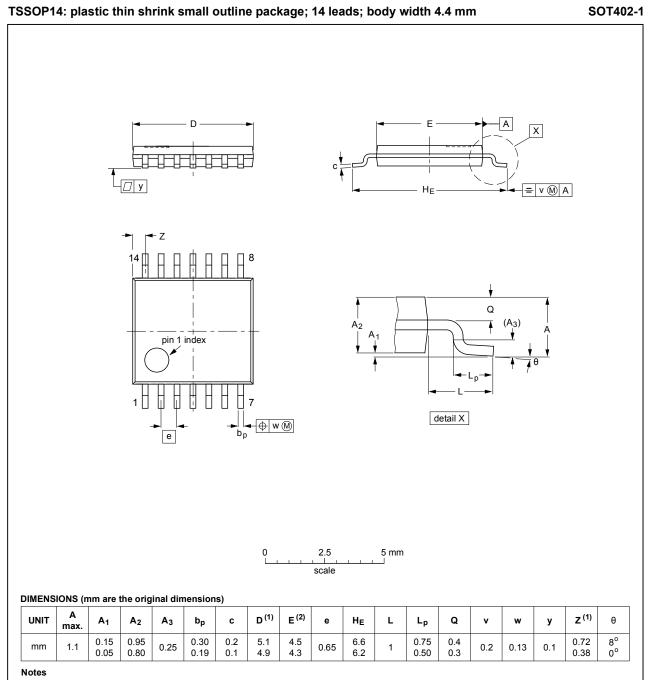


Figure 9. Package outline SOT337-1 (SSOP14)

## 3.3 V Quad 2-input NOR gate



- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				<del>99-12-27</del> 03-02-18

Figure 10. Package outline SOT402-1 (TSSOP14)

3.3 V Quad 2-input NOR gate

# 12 Abbreviations

### Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 13 Revision history

### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74LVT02 v.3	20170324	Product data sheet	-	74LVT02 v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
74LVT02 v.2	19960815	Product specification	-	74LVT02 v.1	

3.3 V Quad 2-input NOR gate

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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### 3.3 V Quad 2-input NOR gate

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# 3.3 V Quad 2-input NOR gate

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