60V Dual Output Step-Down Controller with Digital Power System Management

FEATURES

- **PMBus/I²C Compliant Serial Interface**
- **Telemetry Read-Back Includes V_{IN}, I_{IN}, V_{OUT}, I_{OUT}, Temperature and Faults**
- **Programmable Voltage, Current Limit, Digital Soft-Start/Stop, Sequencing, Margining, OV/UV/OC, Frequency, and Control Loop Compensation**
- **Output Error Less Than ±0.5% Over Temperature**
- **Integrated 16-Bit ADC and 12-Bit DAC**
- **Integrated High Side Current Sense Amplifier**
- **Internal EEPROM with ECC and Fault Logging**
- **Integrated N-Channel MOSFET Gate Drivers**

Power Conversion

- Wide V_{IN} Range: 4.5V to 60V
- V_{OUT0}, V_{OUT1} Range: 0.5V to 13.8V
- Analog Current Mode Control
- Accurate PolyPhase® Current Sharing for Up to 6 Phases (100kHz to 750kHz)
- Available in a 52-Lead (7mm × 8mm) QFN Package

APPLICATIONS

- Telecom, Datacom, and Storage Systems
- Industrial and Point of Load Applications

DESCRIPTION

The LTC®3886/LTC3886-1 is a dual PolyPhase DC/DC synchronous step-down switching regulator controller with I²C-based PMBus compliant serial interface. This controller employs a constant-frequency, current-mode architecture, with high voltage input and output capability along with programmable loop compensation. The LTC3886 is supported by the LTpowerPlay® software development tool with graphical user interface (GUI).

The $EXTV_{CC}$ pin supports voltages up to 14V allowing for optimized circuit efficiency and die temperature, and for the controller output to supply the chip power. Switching frequency, output voltage, and device address can be programmed both by digital interface as well as external configuration resistors. Parameters can be set via the digital interface or stored in EEPROM. Both outputs have an independent power good indicator and $\overline{FAULT}$ function.

The LTC3886 can be configured for discontinuous (pulse-skipping) mode or continuous inductor current mode. The LTC3886-1 also includes a sequencing off feature to discharge very large output capacitors.

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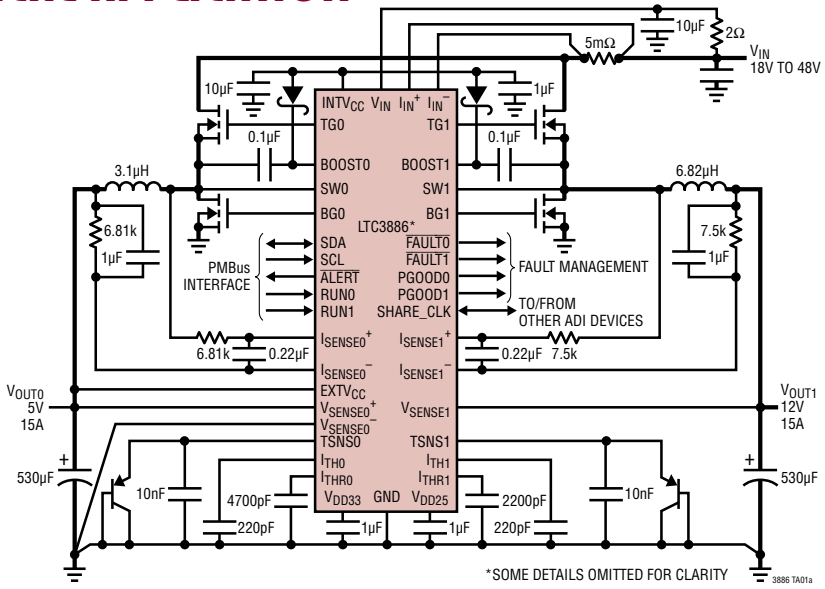
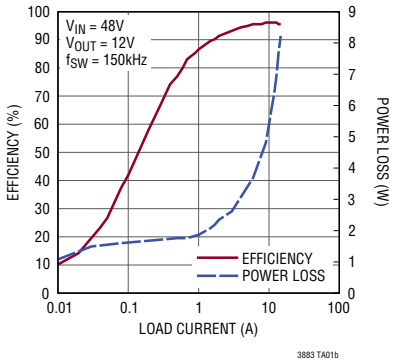
TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current



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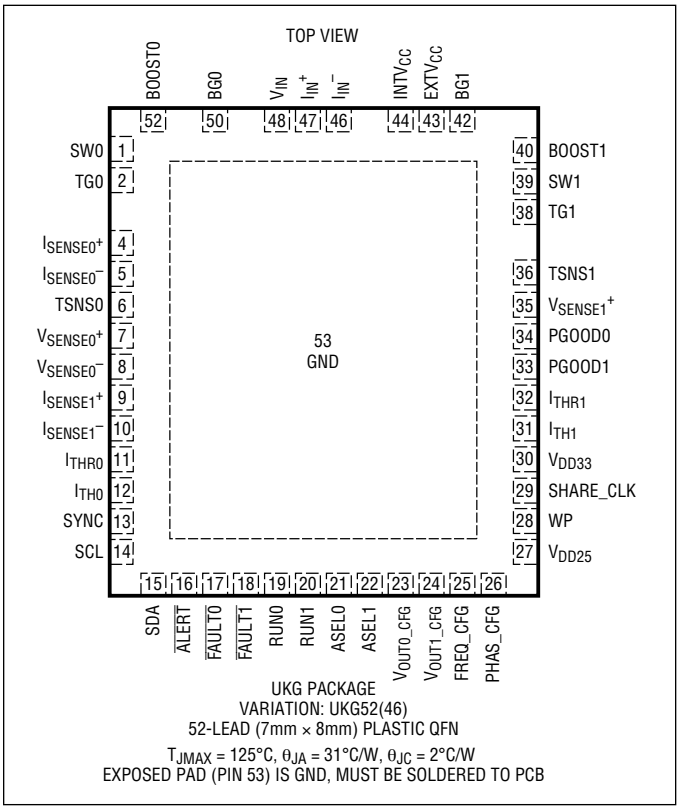
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, I_{IN}^+, I_{IN}^- ..... –0.3V to 65V
Top Gate Transient Voltage (TG0, TG1) .....–0.3V to 71V
BOOST0, BOOST1 .....–0.3V to 71V
Switch Transient Voltage (SW0, SW1) ..... –5V to 65V
$INTV_{CC}$, BG0, BG1, (BOOST0– SW0),
(BOOST1– SW1) ..... –0.3V to 6V
V_{SENSE0}^+, V_{SENSE1}^+, I_{SENSE0}^+, I_{SENSE1}^+,
I_{SENSE0}^-, I_{SENSE1}^-, $EXTV_{CC}$ ..... –0.3V to 15V
V_{SENSE0}^- ..... –0.3V to 0.3V
RUN, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
ASEL*n*, V_{OUTn_CFG}, FREQ_CFG,
PHAS_CFG, V_{DD25} ..... –0.3V to 2.75V
(V_{IN} – I_{INP}), (V_{IN} – I_{INM}) ..... –0.3V to 0.3V
PGOOD0, PGOOD1, $\overline{FAULT}$, SHARE_CLK,
I_{TH0}, I_{TH1}, I_{THR0}, I_{THR1}, V_{DD33}, WP,
TSNS0, TSNS1, SYNC ..... –0.3V to 3.6V
($EXTV_{CC}$ – V_{IN}) 13.2V
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
(Notes 2, 15, 16) ..... –40°C to 125°C*
Storage Temperature Range ..... –65°C to 150°C*

* See Derating EEPROM Retention at Temperature in the Applications Information section for junction temperatures in excess of 125°C.

PIN CONFIGURATION



Note: Pins omitted to achieve high input voltage rating.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3886EUKG#PBF	LTC3886EUKG#TRPBF	LTC3886UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C
LTC3886IUKG#PBF	LTC3886IUKG#TRPBF	LTC3886UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C
LTC3886EUKG-1#PBF	LTC3886EUKG-1#TRPBF	LTC38861UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C
LTC3886IUKG-1#PBF	LTC3886IUKG-1#TRPBF	LTC38861UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = 16V, $EXTV_{CC}$ = 0V, V_{RUN0} = 3.3V, V_{RUN1} = 3.3V f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage							
V_{IN}	Input Voltage Range	(Note 12)	●	4.5		60	V
I_Q	Input Voltage Supply Current Normal Operation	(Note 14) V_{RUN} = 3.3V, No Caps on TG and BG V_{RUN} = 0V			 26 22		 mA mA
V_{UVLO}	Undervoltage Lockout Threshold When V_{IN} > 4.2V	V_{INTVCC} Falling V_{INTVCC} Rising			3.7 3.95		V V
T_{INIT}	Initialization Time	Delay from RESTORE_USER_ALL, MFR_REST, or V_{INTVCC} > V_{UVLO} Until TON_DELAY Can Begin			35		ms
Control Loop							
V_{OUTR0}	Range 0 Maximum V_{OUT} Range 0 Set Point Accuracy Range 0 Resolution Range 0 LSB Step Size, FSR = 16.38	 2.0V ≤ V_{OUT} ≤ 13.8V (Notes 9, 10)	 ● 	 –0.5 	14.0 12 4	 0.5 	V % Bits mV
V_{OUTR1}	Range 1 Maximum V_{OUT} Range 1 Set Point Accuracy Range 1 Resolution Range 1 LSB Step Size, FSR = 8.19V	 1.0V ≤ V_{OUT} ≤ 6.6V (Notes 9, 10)	 ● 	 –0.5 	7.0 12 2	 0.5 	V % Bits mV
$V_{LINEREG}$	Line Regulation	16V < V_{IN} < 60V	●			±0.02	%/V
$V_{LOADREG}$	Load Regulation	ΔV_{ITH} = 1.35V – 0.7V ΔV_{ITH} = 1.35V – 2.0V	● ●		0.01 –0.01	0.1 –0.1	% %
$g_{m0,1}$	Resolution				3		bits
	Error Amplifier $g_{m(MAX)}$	I_{TH} =1.35V			5.76		mmho
	Error Amplifier $g_{m(MIN)}$	I_{TH} =1.35V			1.00		mmho
	Error Amplifier g_m LSB Step Size	I_{TH} =1.35V			0.68		mmho
$R_{ITHR0,1}$	Resolution				5		bits
	Compensation Resistor $R_{ITHR(MAX)}$				62		kΩ
	Compensation Resistor $R_{ITHR(MIN)}$				0		kΩ
I_{ISENSE}	Input Current	V_{ISENSE} = 14V	●		±1	±2	µA
$V_{I(ILIMIT)}$	Resolution				3		bits
	$V_{ILIM(MAX)}$	Hi Range Lo Range	● ●	68 44	75 50	82 56	mV mV
	$V_{ILIM(MIN)}$	Hi Range Lo Range			37.5 25		mV mV
Gate Driver							
TG t_r t_f	TG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
BG t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 20 20		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF			10		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF			30		ns
$t_{ON(MIN)}$	Minimum On-Time				90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = 16V, $EXTV_{CC}$ = 0V, V_{RUN0} = 3.3V, V_{RUN1} = 3.3V f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OV/UV Output Voltage Supervisor							
N	Resolution				9		Bits
V_{RANGE0}	Range 0 Maximum Threshold				14		V
V_{RANGE1}	Range 1 Maximum Threshold				7		V
V_{OUSTP0}	Range 0 Step Size, FSR = 16.352V	(Note 10)			32		mV
V_{OUSTP1}	Range 1 Step Size, FSR = 8.176V				16		mV
V_{THACC0}	Range 0 Threshold Accuracy	2V < V_{OUT} < 14V	●			±2.5	%
V_{THACC1}	Range 1 Threshold Accuracy	1V < V_{OUT} < 7V	●			±2.5	%
$t_{PROPOV1}$	OV Comparator to FAULT Low Time	V_{OD} = 10% of Threshold				35	µs
$t_{PROPUV1}$	UV Comparator to FAULT Low Time	V_{OD} = 10% of Threshold				100	µs
V_{IN} Voltage Supervisor							
N	Resolution				9		Bits
$V_{IN(RANGE)}$	Full-Scale Voltage	(Note 11)			61.32		V
$V_{IN(STP)}$	Step Size				120		mV
$V_{IN(THACCH)}$	Threshold Accuracy 12V < V_{IN} < 60V		●			±3	%
$V_{IN(THACCL)}$	Threshold Accuracy 4.5V < V_{IN} < 15V		●			±6	%
$t_{PROP(VIN)}$	Comparator Response Time (VIN_ON and VIN_OFF)	V_{OD} = 10% of Threshold				100	µs
Output Voltage Readback							
N	Resolution LSB Step Size				16 250		Bits µV
$V_{F/S}$	Full-Scale Sense Voltage	(Note 10) V_{RUN} = 0V (Note 8)			16.384		V
V_{OUT_TUE}	Total Unadjusted Error	T_J = 25°C, V_{OUT} > 1.0V (Note 8)	 ●		0.2	 ±0.5	% %
V_{OS}	Zero-Code Offset Voltage		●			±500	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms
V_{IN} Voltage Readback							
N	Resolution	(Note 5)			10		Bits
$V_{F/S}$	Full-Scale Input Voltage	(Note 11)			66.56		V
V_{IN_TUE}	Total Unadjusted Error	T_J = 25°C, V_{VIN} > 4.5V	 ●			0.4 2	% %
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms
Output Current Readback							
N	Resolution LSB Step Size	(Note 5) 0V ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 16mV 16mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 32mV 32mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 64mV 64mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 100mV			10 15.26 30.52 61 122		Bits µV µV µV µV
$I_{F/S}$	Full-Scale Output Current	(Note 7) R_{ISENSE} = 1mΩ			±100		A
I_{OUT_TUE}	Total Unadjusted Error	(Note 8) 10mV ≤ V_{ISENSE} ≤ 100mV	●			±1.5	%
V_{OS}	Zero-Code Offset Voltage					±32	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = 16V, $EXTV_{CC}$ = 0V, V_{RUN0} = 3.3V, V_{RUN1} = 3.3V f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current Readback							
N	Resolution LSB Step Size, Full-Scale Range = 16mV LSB Step Size, Full-Scale Range = 32mV LSB Step Size, Full-Scale Range = 64mV	(Note 5) 8x Gain, 0V ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 5mV 4x Gain, 0V ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 20mV 2x Gain, 0V ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 50mV			10 15.26 30.52 61		Bits µV µV µV
I_{IN_TUE}	Total Unadjusted Error (Note 8)	8x Gain, 2.5mV ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 5mV 4x Gain, 4mV ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 20mV 2x Gain, 6mV ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 50mV	● ● ●			±1.6 ±1.3 ±1.2	% % %
I_{IIN}	Input Current, I_{IN}^+ and I_{IN}^-	V_{IN} = V_{IIN+} = V_{IIN-} = 30V	●			±2	µA
V_{OS}	Zero-Code Offset Voltage					±50	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms
Supply Current Readback							
N	Resolution LSB Step Size, Full-Scale Range = 256mV	(Note 5)			10 244		Bits µV
I_{CHIP_TUE}	Total Unadjusted Error	20mV ≤ $\|I_{IN}^+ - V_{IN}\|$ ≤ 200mV	●			±2.5	%
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms
Temperature Readback (T0, T1)							
T_{RES_T}	Resolution				0.25		°C
T0_TUE	External TSNS TUE (Note 8) MFR_PWM_MODE_LTC3886[5] = 0 MFR_PWM_MODE_LTC3886[5] = 1	 ΔV_{TSNS} = 72mV (Note 17) V_{TSNS} ≤ 1.85V (Note 17)	 ● ●			 ±3 ±7	 °C °C
TI_TUE	Internal TSNS TUE	V_{RUN} = 0.0V (Note 8)			±1		°C
$t_{CONVERT_T}$	Update Rate	(Note 6)			90		ms
$INTV_{CC}$ Regulator							
V_{INTVCC_VIN}	Internal V_{CC} Voltage No Load	6V < V_{IN} < 60V	●	4.8	5	5.2	V
V_{LDO_VIN}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	±2	%
V_{INTVCC_EXT}	Internal V_{CC} Voltage No Load	5.5V < $EXTV_{CC}$ < 14V	●	4.8	5	5.2	V
V_{LDO_EXT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, $EXTV_{CC}$ = 12V			0.5	±2	%
V_{EXT_THRES}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7	4.95	V
V_{EXT_HYS}	$EXTV_{CC}$ Hysteresis Voltage				80		mV
V_{DD33} Regulator							
V_{DD33}	Internal V_{DD33} Voltage	4.5V < V_{INTVCC}		3.2	3.3	3.4	V
I_{LIM}	V_{DD33} Current Limit	V_{DD33} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			100		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold				3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold				3.1		V
V_{DD25} Regulator							
V_{DD25}	Internal V_{DD25} Voltage				2.5		V
I_{LIM}	V_{DD25} Current Limit	V_{DD25} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			80		mA
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency Accuracy	100kHz < f_{SYNC} < 750kHz Measured Falling Edge-to-Falling Edge of SYNC with FREQUENCY_SWITCH = 100.0 and 750.0	●			±10	%
$V_{TH(SYNC)}$	SYNC Input Threshold	V_{CLKIN} Falling V_{CLKIN} Rising			1 1.5		V V
$V_{OL(SYNC)}$	SYNC Low Output Voltage	I_{LOAD} = 3mA	●		0.2	0.4	V
$I_{LEAK(SYNC}$	SYNC Leakage Current in Slave Mode	0V ≤ V_{PIN} ≤ 3.6V				±5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = 16V, $EXTV_{CC}$ = 0V, V_{RUN0} = 3.3V, V_{RUN1} = 3.3V f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
θSYNC-θ0	SYNC to Channel 0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG_LTC3886[2:0] = 0,2,3 MFR_PWM_CONFIG_LTC3886[2:0] = 5 MFR_PWM_CONFIG_LTC3886[2:0] = 1 MFR_PWM_CONFIG_LTC3886[2:0] = 4,6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Channel 1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG_LTC3886[2:0] = 3 MFR_PWM_CONFIG_LTC3886[2:0] = 0 MFR_PWM_CONFIG_LTC3886[2:0] = 2,4,5 MFR_PWM_CONFIG_LTC3886[2:0] = 1 MFR_PWM_CONFIG_LTC3886[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 13)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 13)	T_J < 125°C	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < T_J ≤ 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*							
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN, $\overline{\text{FAULT}}$	●			1.35	V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN, $\overline{\text{FAULT}}$	●	0.8			V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, $\overline{\text{FAULT}}$*n*, $\overline{\text{ALERT}}$, RUN*n*, SHARE_CLK, PGOOD*n*							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Digital Inputs SHARE_CLK, WP							
V_{IH}	Input High Threshold Voltage		●		1.5	1.8	V
V_{IL}	Input Low Threshold Voltage		●	0.6	1.0		V
Leakage Current SDA, SCL, $\overline{\text{ALERT}}$, RUN							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA
Leakage Current $\overline{\text{FAULT}}$*n*, PGOOD*n*							
I_{GL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
Digital Filtering of $\overline{\text{FAULT}}$*n*							
t_{FAULT}	Input Digital Filtering $\overline{\text{FAULT}}$*n*				3		µs
Digital Filtering of PGOOD*n*							
t_{PGOOD}	Output Digital Filtering PGOOD*n*				60		µs
Digital Filtering of RUN*n*							
t_{RUN}	Input Digital Filtering RUN*n*				10		µs
PMBus Interface Timing Characteristics							
f_{SCL}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD(STA)}$	Hold Time After Start Condition. After This Period, the First Clock Is Generated		●	0.6			µs
$t_{SU(STA)}$	Repeated Start Condition Setup Time		●	0.6		10000	µs
$t_{SU(STO)}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = 16V, $EXTV_{CC}$ = 0V, V_{RUN0} = 3.3V, V_{RUN1} = 3.3V f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{SU,DAT}$	Data Setup Time Receiving Data		●	0.1			µs
$t_{TIMEOUT_SMB}$	Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads	Measured from the Last PMBus Start Event			32 255		ms ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3886 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3886E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3886I is guaranteed over the –40°C to 125°C operating junction temperature range. T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 5: The data format in PMBus is 5 bits exponent (signed) and 11 bits mantissa (signed). This limits the output resolution to 10 bits though the internal ADC is 16 bits and the calculations use 32-bit words.

Note 6: The data conversion is done in round robin fashion. All input signals are continuously converted for a typical latency of 90ms. Unless the MFR_ADC_CONTROL command is utilized.

Note 7: The IOUT_CAL_GAIN = 1.0mΩ and MFR_IOUT_TC = 0.0. Value as read from READ_IOUT in amperes.

Note 8: Part tested with PWM disabled. Evaluation in application demonstrates capability. TUE (%) = ADC Gain Error (%) + 100 • [Zero Code Offset + ADC Linearity Error]/Actual Value.

Note 9: All V_{OUT} commands assume the ADC is used to auto-zero the output to achieve the stated accuracy. LTC3886 is tested in a feedback loop that servos V_{OUT} to a specified value.

Note 10: The maximum programmable V_{OUT} voltage is 13.8V.

Note 11: The maximum V_{IN} voltage is 60V.

Note 12: When V_{IN} < 6V, $INTV_{CC}$ must be tied to V_{IN}.

Note 13: EEPROM endurance is guaranteed by design, characterization and correlation with statistical process controls. Data retention is production tested via a high temperature bake at wafer level. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification. The RESTORE_USER_ALL command (EEPROM read) is valid over the entire operating temperature range.

Note 14: The LTC3886 quiescent current (I_Q) equals the I_Q of V_{IN} plus the I_Q of $EXTV_{CC}$.

Note 15: The LTC3886 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

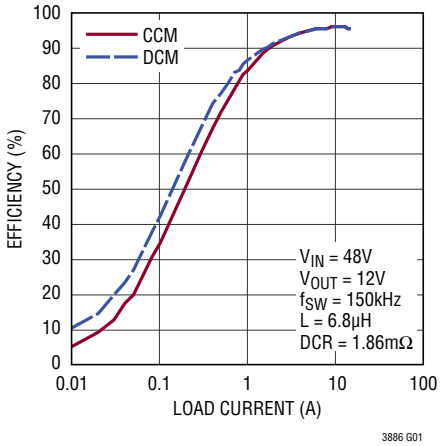
Note 16: Write operations above T_J = 85°C or below 0°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures between –40°C and 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in a degradation of retention characteristics.

Note 17: Limits guaranteed by TSNS voltage and current measurements during test, including ADC readback.

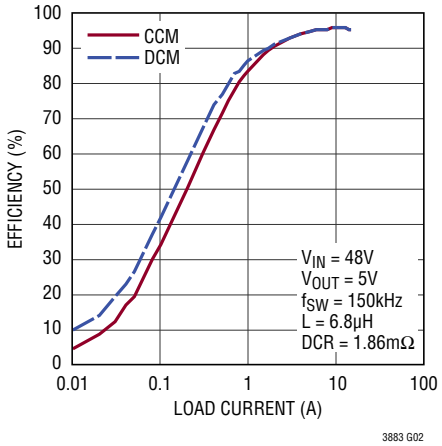
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25C, V_{IN} = 16V, $EXTV_{CC}$ = 0V, unless otherwise noted.

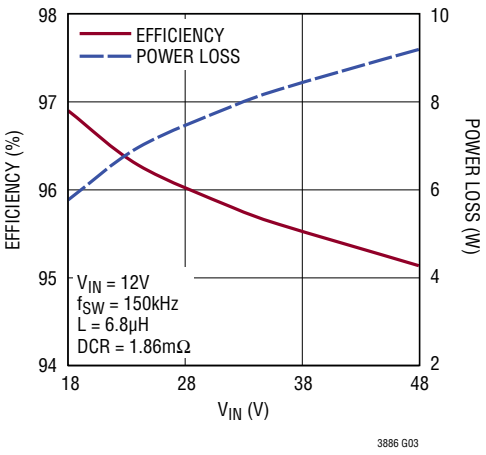
Efficiency vs Load Current, V_{OUT} = 12V



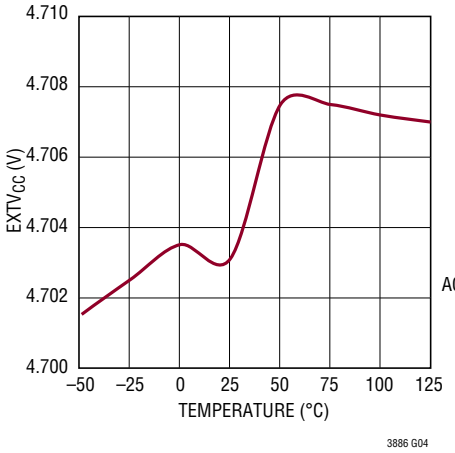
Efficiency vs Load Current, V_{OUT} = 5V



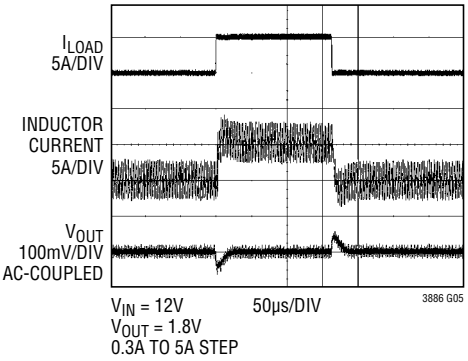
Efficiency and Power Loss vs Input Voltage



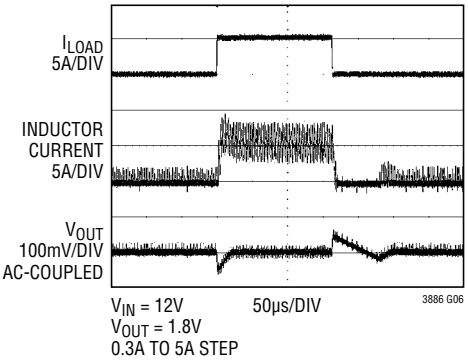
$EXTV_{CC}$ Switchover vs Temperature



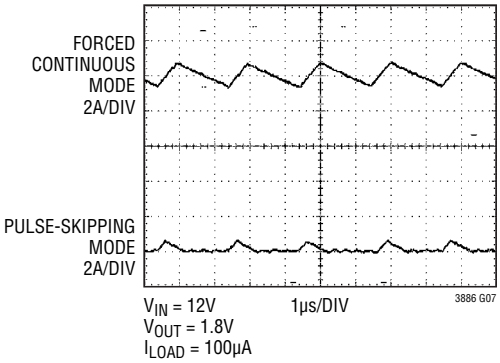
Load Step (Forced Continuous Mode)



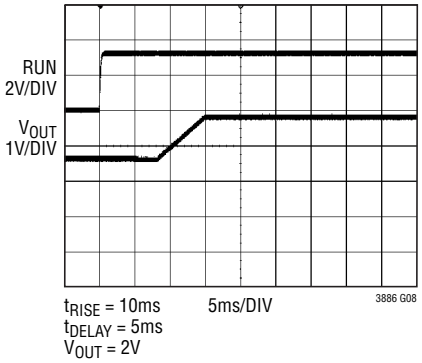
Load Step (Pulse-Skipping Mode)



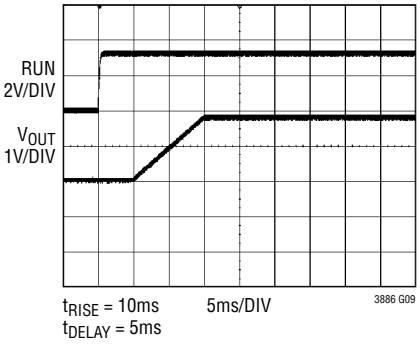
Inductor Current at Light Load



Start-Up into a Pre-Biased Load



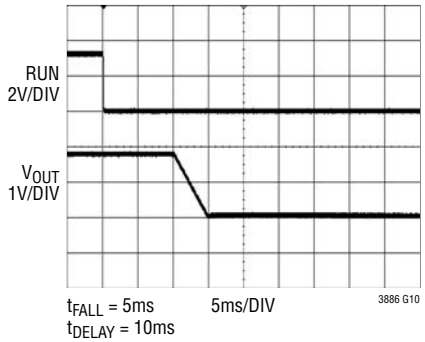
Soft-Start Ramp



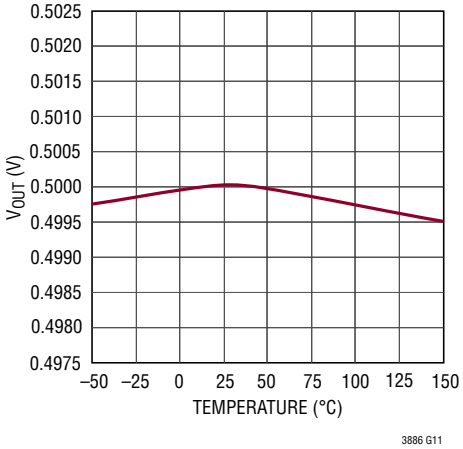
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25C, V_{IN} = 16V, $EXTV_{CC}$ = 0V, unless otherwise noted.

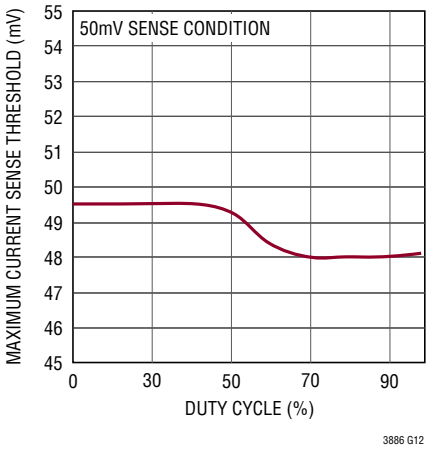
Soft-Off Ramp



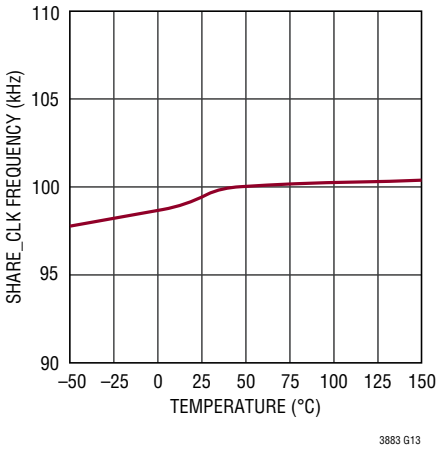
Regulated Output Voltage vs Temperature



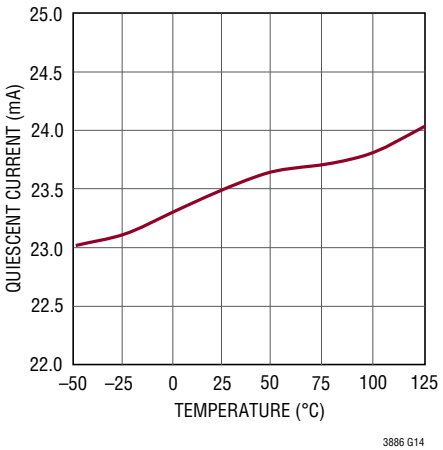
Maximum Current Sense Threshold vs Duty Cycle, V_{OUT} = 0V



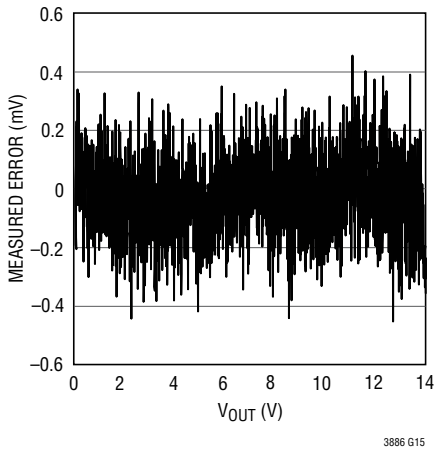
SHARE_CLK Frequency vs Temperature



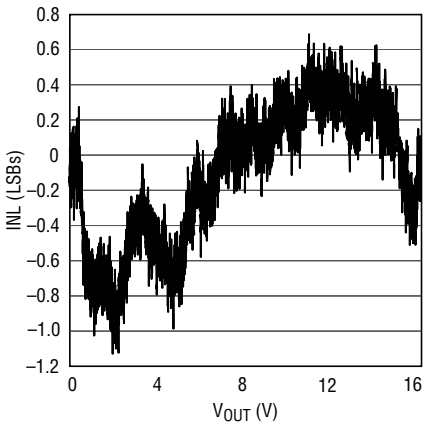
Quiescent Current vs Temperature



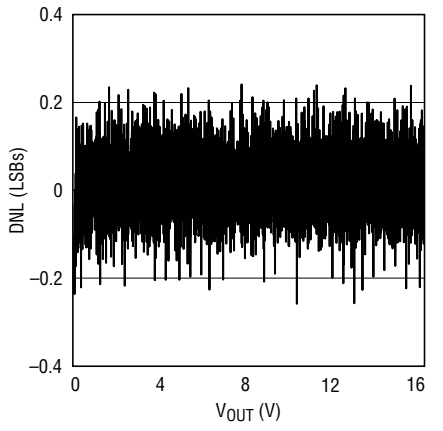
V_{OUT} Measurement Error vs V_{OUT}



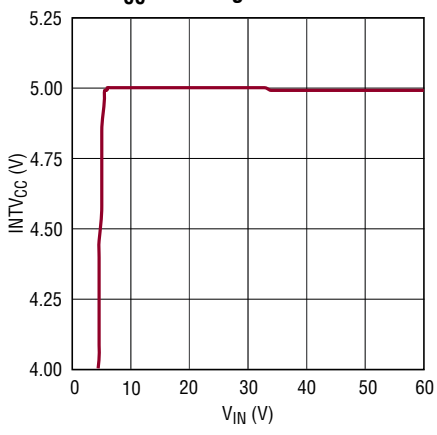
V_{OUT} Command INL



V_{OUT} Command DNL



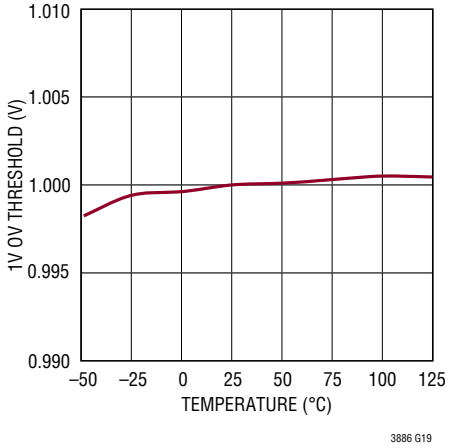
$INTV_{CC}$ Line Regulation



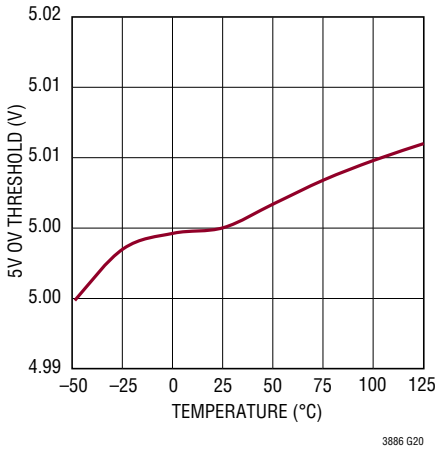
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25C, V_{IN} = 16V, $EXTV_{CC}$ = 0V, unless otherwise noted.

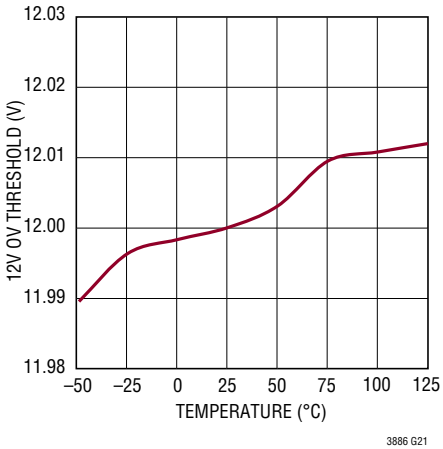
V_{OUT} OV Threshold vs Temperature (1V Target)



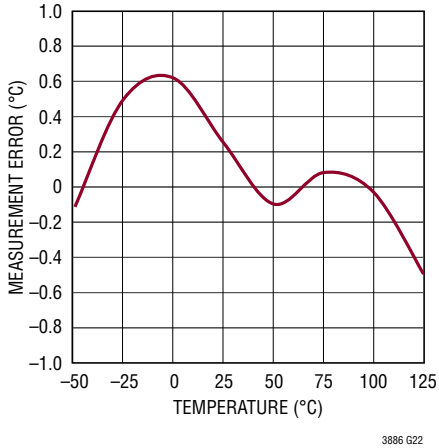
V_{OUT} OV Threshold vs Temperature (5V Target)



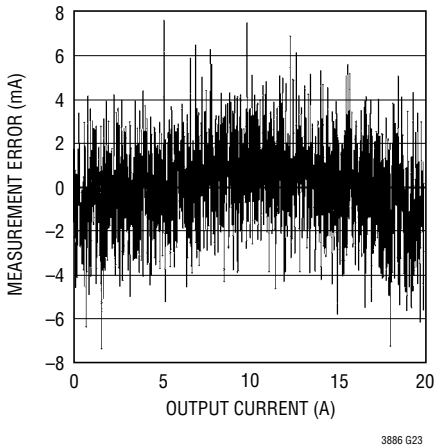
V_{OUT} OV Threshold vs Temperature (12V Target)



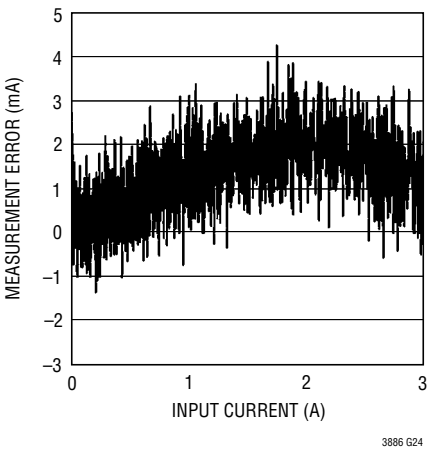
External Temperature Error vs Temperature



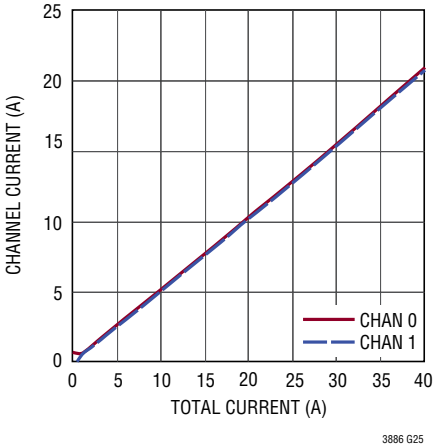
I_{OUT} Error vs I_{OUT}



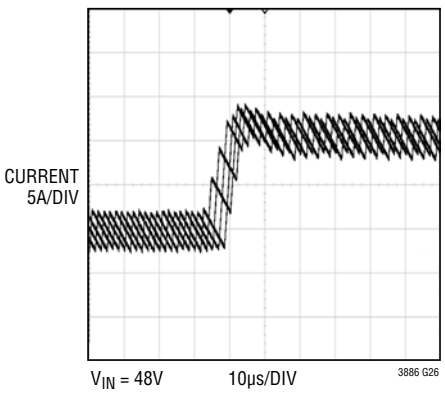
I_{IN} Error vs I_{IN}



DC Output Current Matching in a 2-Phase System (LTC3886)

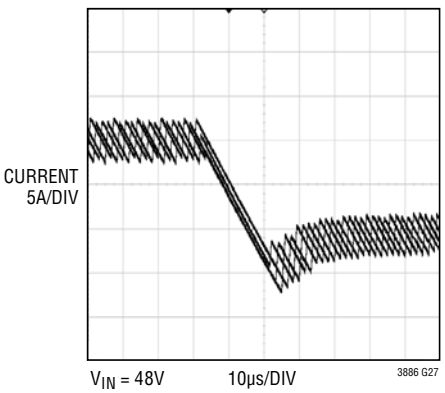


Dynamic Current Sharing During a Load Transient in a 4-Phase System



V_{IN} = 48V
V_{OUT} = 5V
f_{SW} = 150kHz
L = 6.8µH; R_{SENSE} = 3mΩ
0A TO 10A LOAD STEP

Dynamic Current Sharing During a Load Transient in a 4-Phase System



V_{IN} = 48V
V_{OUT} = 5V
f_{SW} = 150kHz
L = 6.8µH; R_{SENSE} = 3mΩ
10A TO 0A LOAD STEP

Rev F

PIN FUNCTIONS

SW0/SW1 (Pins 1, 39): Switch Node Connections to Inductors. Voltage swings at the pins are from a Schottky diode (external) voltage drop below ground to V_{IN}.

TG0/TG1 (Pins 2, 38): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltages.

I_{SENSE0}^+/I_{SENSE1}^+ (Pins 4, 9): Current Sense Comparator Inputs. The (+) input to the current comparator is normally connected to the DCR sensing network or current sensing resistor.

I_{SENSE0}^-/I_{SENSE1}^- (Pins 5, 10): Current Sense Comparator Inputs. The (–) input is connected to the output.

TSNS0/TSNS1 (Pins 6, 36): External Diode Temperature Sense. Connect to the anode of a diode-connected PNP transistor in order to sense remote temperature. Directly connect the cathode using a separate ground return path to Pin 53 of the LTC3886. A bypass capacitor between the anode and cathode must be located in close proximity to the transistor. If external temperature sense elements are not installed, short pin to ground and set the UT_FAULT_LIMIT to –275°C and the UT_FAULT_RESPONSE to ignore.

V_{SENSE0}^+/V_{SENSE1}^+ (Pins 7, 35): Positive Output Voltage Sense Inputs.

V_{SENSE0}^- (Pin 8): Channel 0 Negative Output Voltage Sense Input.

I_{THR0}/I_{THR1} (Pins 11, 32): Loop Compensation Nodes.

I_{TH0}/I_{TH1} (Pins 12, 31): Current Control Threshold and Error Amplifier Compensation Nodes. Each associated channel's current comparator tripping threshold increases with its I_{TH} voltage.

SYNC (Pin 13): External Clock Synchronization Input and Open-Drain Output Pin. If an external clock is present at this pin, the switching frequency will be synchronized to the external clock. If clock master mode is enabled, this pin will pull low at the switching frequency with a 500ns pulse width to ground. A resistor pull-up to 3.3V is required in the application.

SCL (Pin 14): Serial Bus Clock Input. Open-drain output, can hold the output low if clock stretching is enabled. A pull-up resistor to a voltage between 1.8V to 3.3V is required in the application.

SDA (Pin 15): Serial Bus Data Input and Output. A pull-up resistor to a voltage between 1.8V to 3.3V is required in the application.

$\overline{\text{ALERT}}$ (Pin 16): Open-Drain Digital Output. Connect the $\overline{\text{SMBALERT}}$ signal to this pin. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{FAULT0}}$/$\overline{\text{FAULT1}}$ (Pins 17, 18): Digital Programmable General Purpose Inputs and Outputs. Open-drain output. A pull-up resistor to a voltage between 1.8V to 3.3V is required in the application.

RUN0/RUN1 (Pins 19, 20): Enable Run Input and Output. Logic high on this pin enables the controller. Open-drain output holds the pin low until the LTC3886 is out of reset. This pin should be driven by an open-drain digital output. A pull-up resistor to a voltage between 1.8V to 3.3V is required in the application.

ASEL0/ASEL1 (Pin 21/Pin 22): Serial Bus Address Select Inputs. Connect optional 1% resistor dividers between V_{DD25} and GND to these pins to select the serial bus interface address. Refer to the Applications Information section for more detail. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{OUT_CFG0} /V_{OUT_CFG1} (Pins 23, 24): Output Voltage Select Pins. Connect a ±1% resistor divider between the chip V_{DD25}, V_{OUT_CFG} and GND in order to select output voltage. If the pin is left open, the IC will use the value programmed in the EEPROM. Refer to the Applications Information section for more detail. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

FREQ_CFG (Pin 25): Frequency Select Pin. Connect a ±1% resistor divider between the chip V_{DD25} FREQ_CFG and GND in order to select switching frequency. If the pin is left open, the IC will use the value programmed in the EEPROM. Refer to the Applications Information section for more detail. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

PIN FUNCTIONS

PHAS_CFG (Pin 26): Phase Configuration Input. Connect an optional 1% resistor divider between V_{DD25} and GND to this pin to configure the phase of each PWM channel relative to SYNC. Refer to the Applications Information section for more detail. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{DD25} (Pin 27): Internally Generated 2.5V Power Supply Output. Bypass this pin to GND with a low ESR 1µF capacitor. Do not load this pin externally except for the resistor dividers needed for the LTC3886 resistor con-figuration pins.

WP (Pin 28): Write Protect Pin Active High. An internal 10µA current source pulls the pin to V_{DD33}. If WP is high, the PMBus writes are restricted.

SHARE_CLK (Pin 29): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used to synchronize the timing between multiple ADI controllers. Tie all the SHARE_CLK pins together. All ADI controllers will synchronize to the fastest clock. A pull-up resistor to 3.3V is required in the application.

V_{DD33} (Pin 30): Internally Generated 3.3V Power Supply Output. Bypass this pin to GND with a low ESR 1µF capacitor. Do not load this pin with external current.

PGOOD0/PGOOD1 (Pins 34, 33): Power Good Indicator Outputs. Open-drain logic output that is pulled to ground when the output exceeds OV/UV thresholds. The output is deglitched by an internal 60µs filter. A pull-up resistor to 3.3V is required in the application.

BOOST1/BOOST0 (Pins 40, 52): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitor connects to this pin. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

BG0/BG1 (Pins 50, 42): Bottom Gate Driver Outputs. This pin drives the gates of the bottom N-channel MOSFET between GND and $INTV_{CC}$.

$EXTV_{CC}$ (Pin 43): External power input to an internal LDO connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ connection in the Applications Information Section. Do not float or exceed 14V on this pin. Decouple this pin to GND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. If the $EXTV_{CC}$ pin is not used, tie the pin to GND. The $EXTV_{CC}$ pin may be connected to a higher voltage than the V_{IN} pin. If the $EXTV_{CC}$ pin is tied to an output of the controller and the external load can pull the output below –0.3V, a Schottky diode from GND to $EXTV_{CC}$ must be used to protect the $EXTV_{CC}$ pin.

$INTV_{CC}$ (Pin 44): Internal Regulator 5V Output. The control circuits are powered from this voltage. Decouple this pin to GND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

I_{IN}^- (Pin 46): Negative Input of High Side Current Sense Amplifier.

I_{IN}^+ (Pin 47): Positive Input of High Side Current Sense Amplifier.

V_{IN} (Pin 48): Main Input Supply. Decouple this pin to GND with a capacitor (0.1µF to 1µF). For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together. If the input current sense amplifier is not used, this pin must be shorted to the I_{IN}^+ and I_{IN}^- pins.

GND (Exposed Pad Pin 53): Ground. All small-signal and compensation components should connect to this ground, at one point.

BLOCK DIAGRAM

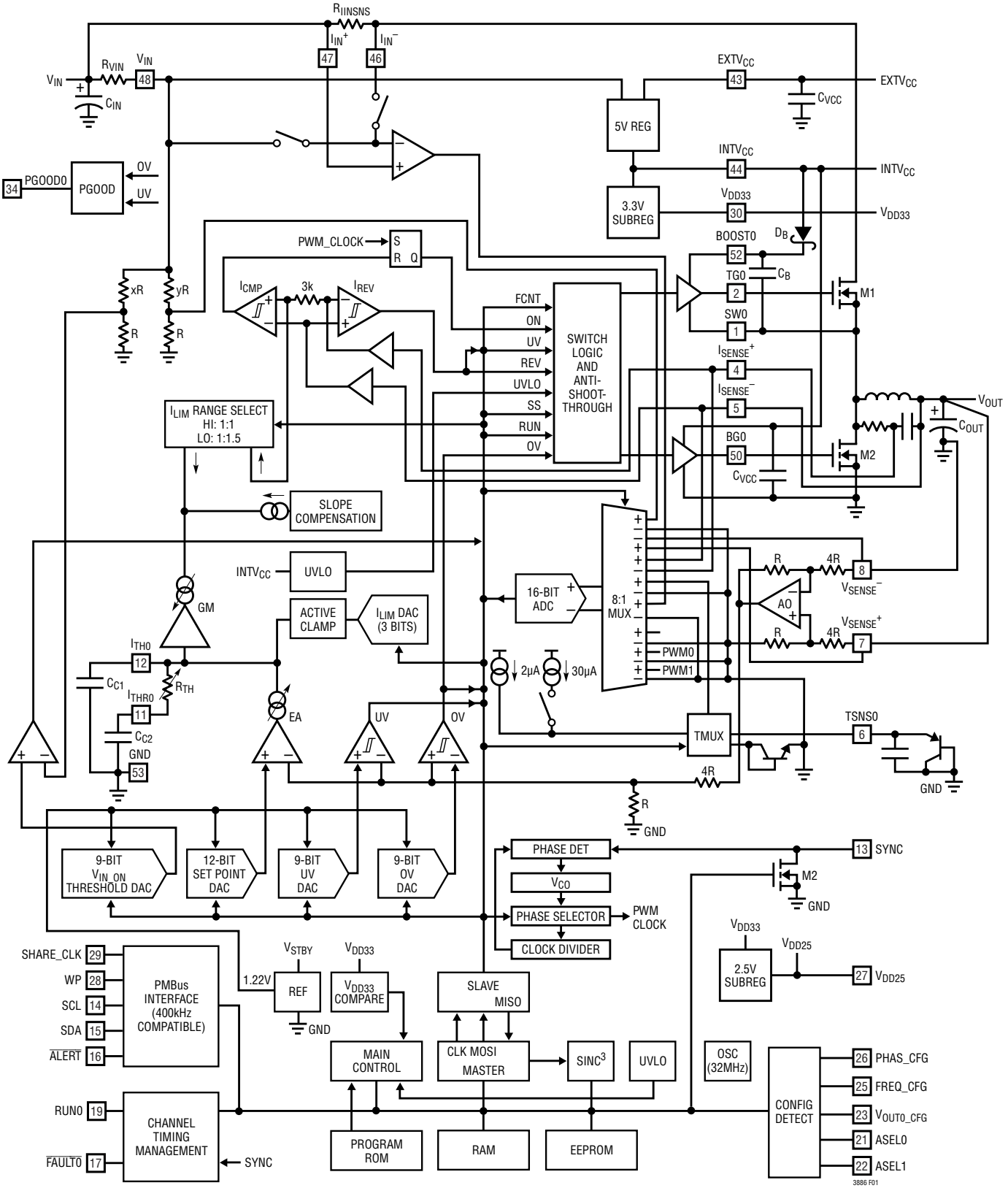


Figure 1. Block Diagram, One of Two Channels (CH0) Shown

OPERATION

OVERVIEW

The LTC3886 is a dual channel/dual phase, constant frequency, analog current mode controller for DC/DC step-down applications with a digital interface. The LTC3886 digital interface is compatible with PMBus which supports bus speeds of up to 400kHz. A typical application circuit is shown on the first page of this data sheet.

In addition all the LTC3886 features, the LTC3886-1 also includes a sequencing off feature to fully discharge very large output capacitors as fast as safely possible.

Major features include:

- Programmable Output Voltage
- Programmable Input Voltage Comparator
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable OV and UV Comparators
- Programmable On and Off Delay Times
- Programmable Output Rise/Fall Times
- Programmable Loop Compensation
- Dedicated Power Good Pin for Each Channel
- Phase-Locked Loop for Synchronous, PolyPhase Operation (2, 3, 4 or 6 Phases)
- Input and Output Voltage/Current, and Temperature Telemetry
- Fully Differential Remote Sense on Channel 0
- Integrated Gate Drivers
- Nonvolatile Configuration Memory with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Controllers
- Fault Logging
- WP Pin to Protect Internal EEPROM Configuration
- Standalone Operation After User Factory Configuration
- PMBus Version 1.2, 400kHz Compliant Interface

The PMBus interface provides access to important power management data during system operation including:

- Internal Die Temperature
- External System Temperature via Optional Diode Sense Elements
- Average Output Current
- Average Output Voltage
- Average Input Voltage
- Average Input Current
- Configurable, Latched and Unlatched Individual Fault and Warning Status

Individual channels are accessed through the PMBus using the PAGE command, i.e., PAGE 0 or 1.

Fault reporting and shutdown behavior are fully configurable using the $\overline{\text{FAULT}}n$ outputs. A dedicated pin for $\overline{\text{ALERT}}$ is provided. The shutdown operation also allows all faults to be individually masked and can be operated in either unlatched (retry) or latched modes.

Individual status commands enable fault reporting over the serial bus to identify the specific fault event. Fault or warning detection includes the following:

- Output Undervoltage/Overvoltage
- Input Undervoltage/Overvoltage
- Input and Output Overcurrent
- Internal Overtemperature
- External Overtemperature
- Communication, Memory or Logic (CML) Fault

MAIN CONTROL LOOP

The LTC3886 is a constant-frequency, current-mode step-down controller that operates at a user-defined relative phasing. During normal operation the top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin which is the

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output of the error amplifier, EA. The EA negative terminal is equal to the V_{SENSE} voltage divided by 16 (8 if range = 1). The positive terminal of the EA is connected to the output of a 12-bit DAC with values ranging from 0V to 1.024V. The output voltage, through feedback of the EA, will be regulated to 16 times the DAC output (8 times if range = 1). The DAC value is calculated by the part to synthesize the users desired output voltage. The output voltage is programmed by the user either with the resistor configuration pins detailed in Table 3 or by the V_{OUT} command (either from EEPROM, or by PMBus command). Refer to the PMBus command section of the data sheet or the PMBus specification for more details. The output voltage can be modified by the user at any time with a PMBus VOUT_COMMAND. This command will typically have a latency less than 10ms. The user is encouraged to reference the PMBus Power System Management Protocol Specification to understand how to program the LTC3886.

Continuing the basic operation description, the current mode controller will turn off the top gate when the peak current is reached. If the load current increases, V_{SENSE} will slightly droop with respect to the DAC reference. This causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on. In continuous conduction mode, the bottom MOSFET stays on until the end of the switching cycle.

EEPROM

The LTC3886 contains internal EEPROM, also referred to as NVM (nonvolatile memory), with error correction coding (ECC) to store user configuration settings and fault log information. EEPROM endurance and retention for user space and fault log pages are specified in the Absolute Maximum Ratings and Electrical Characteristics table. The LTC3886 EEPROM also contains a manufacturing section that has internal redundancy.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the EEPROM CRC Error bit in the STATUS_MFR_SPECIFIC command is set, and the $\overline{ALERT}$ and RUN pins pulled low (PWM channels off). At that point the device will respond at special address 0x7C, which is activated only after an invalid CRC has been detected. The chip will also respond at the global addresses 0x5A and 0x5B, but use of these addresses when attempting to recover from a CRC issue is not recommended. All power supply rails associated with either PWM channel of a device reporting an invalid CRC should remain disabled until the issue is resolved.

ADI recommends that the EEPROM not be written when die temperature is greater than 85°C. If internal die temperature exceeds 130°C, all EEPROM operations except RESTORE_USER_ALL and MFR_RESET are disabled. Full EEPROM operation is not re-enabled until die temperature falls below 125°C. Refer to the Applications Information section for equations to predict retention degradation due to elevated operating temperatures.

See the Applications Information section or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming, which the LTC3886 also supports.

POWER-UP AND INITIALIZATION

The LTC3886 is designed to provide standalone supply sequencing and controlled turn-on and turn-off operation. It can operate from a single V_{IN} input supply (4.5V to 60V) while three on-chip linear regulators generate internal 2.5V, 3.3V and 5V. If V_{IN} does not exceed 6V, and the $EXTV_{CC}$ pin is not driven by an external supply, the $INTV_{CC}$ and V_{IN} pins must be tied together. The LTC3886 $EXTV_{CC}$ pin can driven by an external supply to improve efficiency of the circuit and minimize power on the LTC3886. The $EXTV_{CC}$ pin must exceed approximately 4.8V before the $INTV_{CC}$ voltage LDO operates from the $EXTV_{CC}$ pin. To minimize application power, the $EXTV_{CC}$ pin can be supplied by a switching regulator, or an output of the LTC3886. The $EXTV_{CC}$ pin voltage may exceed the V_{IN} pin voltage. The controller configuration is initialized by an internal threshold based UVLO where V_{IN} must be approximately 4.2V and the 5V, 3.3V and 2.5V linear regulators must be within approximately 20% of the regulated

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values. A PMBus RESTORE_USER_ALL or MFR_RESET command forces this same initialization.

During initialization, the external configuration resistors are identified and/or contents of the EEPROM are read into the controller's commands. The BG*n*, TG*n*, PGOOD*n* and RUN*n* pins are held low. The $\overline{\text{FAULT}}$*n* pins are in high impedance mode. The LTC3886 will use the contents of Tables 3 to 6 to determine the resistor defined parameters. See the Resistor Configuration section for more detail. The resistor configuration pins only control some of the preset values of the controller. The remaining values are programmed in EEPROM either at the factory or by the user.

If the configuration resistors are not inserted or if the ignore RCONFIG bit is asserted (bit 6 of the MFR_CONFIG_ALL_LTC3886 configuration command), the LTC3886 will use only the contents of EEPROM to determine the DC/DC characteristics. The ASEL0 and ASEL1 values read at power-up or reset are always respected unless the pins are open. See the Applications Information section for more detail.

After the part has initialized, an additional comparator monitors V_{IN}. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After V_{IN} is initially applied, the part will typically require 70ms to initialize and begin the TON_DELAY timer. The read back of voltages and currents require an additional 0ms to 90ms.

SOFT-START

The part must enter the run state prior to soft-start. The RUN pin is released by the LTC3886 after the part initializes and V_{IN} is greater than the VIN_ON threshold. If multiple LTC3886s are used in an application, they all hold their respective run pins low until all devices initialize and V_{IN} exceeds the VIN_ON threshold for every device. The SHARE_CLK pin assures all the devices connected to the signal use the same time base. The SHARE_CLK pin is held low until the part has initialized after V_{IN} is applied and V_{IN} exceeds the VIN_ON threshold. The LTC3886 can be set to turn off (or remain off) if SHARE_CLK is low (set bit 2 of MFR_CHAN_CONFIG_LTC3886 to a 1). This allows the user to assure synchronization across numerous ADI ICs even if the RUN pins can not be connected together due to board constraints. In general, if the user cares about synchronization between chips it is best to connect all the respective RUN pins together and to connect all the respective SHARE_CLK pins together and pull up to V_{DD33} with a 5.49k resistor. This assures all chips begin sequencing at the same time and use the same time base.

After the RUN*n* pin releases and prior to entering a constant output voltage regulation state, the LTC3886 performs a monotonic initial ramp or "soft-start". Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set-point. Once the LTC3886 is commanded to turn on, (after power up and initialization) the controller waits for the user specified turn-on delay (TON_DELAY) prior to initiating this output voltage ramp. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting the value of TON_RISE to any value less than 0.25ms. The LTC3886 PWM always uses discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom gate is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load. When the TON_MAX_FAULT_LIMIT is reached, the part transitions to continuous mode, if so programmed. If TON_MAX_FAULT_LIMIT is set to zero, there is no time limit and the part transitions to the desired conduction mode after TON_RISE completes and V_{OUT} has exceeded the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present.

TIME-BASED SEQUENCING

The default mode for sequencing the output on and off is time based. The output is enabled after waiting TON_DELAY amount of time following either the RUN*n* pin going high, a PMBus command to turn on, or the V_{IN} pin voltage rising above a preprogrammed voltage. Off sequencing is handled in a similar way. To assure proper sequencing, make sure all ICs connect the SHARE_CLK pins together and RUN pins together. If the RUN pins can not be connected together for some reason, set bit 2 of MFR_CHAN_CONFIG_LTC3886 to a 1. This bit

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requires the SHARE_CLK pin to be clocking before the power supply output can start. When the RUN*n* pin is pulled low, the LTC3886 will hold the pin low for the MFR_RESTART_DELAY. The minimum MFR_RESTART_DELAY is TOFF_DELAY + TOFF_FALL + 136ms. This delay assures proper sequencing of all rails. The LTC3886 calculates this delay internally and will not process a shorter delay. However, a longer commanded MFR_RESTART_DELAY will be used by the part. The maximum allowed value is 65.52 seconds.

EVENT-BASED SEQUENCING

The PGOOD*n* pin is be asserted when the output UV threshold is exceeded. It is possible to feed the PGOOD*n* pin from one LTC3886 into the RUN pin of the next LTC3886 in the sequence. This can be implemented across multiple LTC3886s. If a fault in the string of rails is detected, only the faulted rail and downstream rails will fault off. The rails in the string of devices in front of the faulted rail will remain on unless commanded off.

Event-Based Sequencing by Cascading PGOODs Into RUN Pins

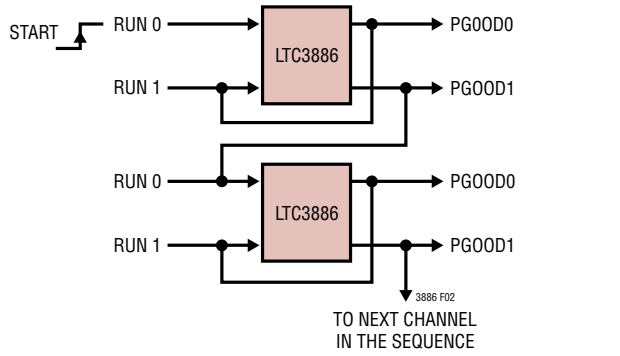

Figure 2. Event (Voltage) Based Sequencing

SHUTDOWN

The LTC3886 supports three shutdown modes. The first mode is continuous conduction mode, with user-defined turn-off delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will draw current from the load to force TOFF_FALL. The second mode is discontinuous conduction mode. In discontinuous conduction mode the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

The third shutdown mode occurs in response to a fault condition or loss of SHARE_CLK (if bit 2 of MFR_CHAN_CONFIG_LTC3886 is set to a 1) or V_{IN} falling below the VIN_OFF threshold or $\overline{FAULT}n$ pulled low externally (if the MFR_FAULT_RESPONSE is set to inhibit). Under these conditions the power stage is disabled in order to stop the transfer of energy to the load as quickly as possible. The shutdown state can be entered from the soft-start or active regulation states either through user intervention (de-asserting RUN or the PMBus OPERATION command) or in response to a detected fault or an external fault via the bidirectional $\overline{FAULT}n$ pin, or loss of SHARE_CLK (if bit 2 of MFR_CHAN_CONFIG_LTC3886 is set to a 1) or V_{IN} falling below the VIN_OFF threshold.

The LTC3886-1 shutdown mode allows very large output capacitors to be fully discharged as fast as safely possible in continuous conduction mode. The PWM channel output will remain active until the output voltage is verified by the internal ADC to be below the MFR_VOFF_THRESHOLD value. The PWM channel will shut down between 90ms and 300ms after the output voltage is below the MFR_VOFF_THRESHOLD.

In retry mode, the controller responds to a fault by shutting down and entering the inactive state for a programmable delay time (MFR_RETRY_DELAY). This delay minimizes the duty cycle associated with autonomous retries if the fault that caused the shutdown disappears once the output is disabled. The retry delay time of the LTC3886 is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. The retry delay time of the LTC3886-1 when the MFR_CHAN_CONFIG bit #0 set to 0 is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below the MFR_VOFF_THRESHOLD value. If the time from when the channel is faulted off until channel's output voltage is below MFR_VOFF_THRESHOLD exceeds TOFF_MAX_WARN_LIMIT, then a TOFF_MAX warning status will be generated. The retry delay time of the LTC3886-1 when

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the MFR_CHAN_CONFIG bit #0 set to 1 is determined by the MFR_RETRY_DELAY command. If the channel's output voltage is above MFR_VOFF_THRESHOLD, the channel will proceed to sequence on into what could be a pre-biased load. TOFF_MAX Warning status will not be generated. If multiple outputs are controlled by the same $\overline{\text{FAULT}}n$ pin, the decay time of the faulted output determines the retry delay. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG_LTC3886. Alternatively, the controller can be configured so that it remains latched-off following a fault and clearing requires user intervention such as toggling RUN or commanding the part OFF then ON.

LIGHT-LOAD CURRENT OPERATION

The LTC3886 has two PWM modes of operation, discontinuous conduction mode or forced continuous conduction mode. Mode selection is done using the MFR_PWM_MODE_LTC3886 command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

If a controller is enabled for discontinuous conduction operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom gate external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller can operate in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in discontinuous conduction operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous conduction mode may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this and turn off the offending channel. However, this fault is based on an ADC read and can take up to 90ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction.

PWM LOOP COMPENSATION

The internal PWM loop compensation resistors $R_{ITH}n$ of the LTC3886 can be adjusted using bit[4:0] of the MFR_PWM_COMP command.

The transconductance of the LTC3886 PWM error amplifier can be adjusted using bit[7:5] of the MFR_PWM_COMP command.

Refer to the Programmable Loop Compensation subsection in the Applications Information section for further details.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the master clock to other ICs through PMBus command, EEPROM setting, or external configuration resistors as outlined in Tables 4 and 5.

As clock master, the LTC3886 will drive its open-drain SYNC pin at the selected rate with a pulse width of 500ns. An external pull-up resistor between SYNC and V_{DD33} is required in this case. Only one device connected to SYNC should be designated to drive the pin. If multiple LTC3886s programmed as clock masters are wired to the same SYNC line with a pull-up resistor, just one of the devices is automatically elected to provide clocking, and the others disable their SYNC outputs.

The LTC3886 will automatically accept an external SYNC input, disabling its own SYNC drive if necessary. Whether configured to drive SYNC or not, the LTC3886 can continue PWM operation using its own internal oscillator if an external clock signal is subsequently lost. The device can also be programmed to always require an external oscillator for PWM operation by setting bit 4 of MFR_CONFIG_ALL_LTC3886. The status of the SYNC driver circuit is indicated by bit 10 of MFR_PADS.

The MFR_PWM_CONFIG_LTC3886 command can be used to configure the phase of each channel. Desired phase can also be set from EEPROM or external configuration

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resistors as outlined in Table 5. Designated phase is the relationship between the falling edge of SYNC and the internal clock edge that sets the PWM latch to turn on the top power switch. Additional small propagation delays to the PWM control pins will also apply. Both channels must be off before the FREQUENCY_SWITCH and MFR_PWM_CONFIG_LTC3886 commands can be written to the LTC3886.

The phase relationships and frequency are independent of each other, providing numerous application options. Multiple LTC3886 ICs can be synchronized to realize a PolyPhase array. In this case the phases should be separated by 360/n degrees, where n is the number of phases driving the output voltage rail.

OUTPUT VOLTAGE SENSING

The channel 0 differential amplifier allows remote, differential sensing of the load voltage with $V_{SENSE0n}$ pins. The channel 1 sense pin (V_{SENSE1}) is referenced to GND. The (telemetry) ADC is fully differential and makes measurements of channels 0 and 1 output voltages at the $V_{SENSE0n}$ and V_{SENSE1}/GND pins, respectively. The maximum allowed differential sense voltage for V_{SENSE0}^+ to V_{SENSE0}^- is 14V.

OUTPUT CURRENT SENSING

For DCR current sense applications, a resistor in series with a capacitor is placed across the inductor. In this configuration, the resistor is tied to the FET side of the inductor while the capacitor is tied to the load side of the inductor as shown in Figure 3. If the RC values are chosen such that the RC time constant matches the inductor time constant (L/DCR, where DCR is the inductor series resistance), the resultant voltage (V_{DCR}) appearing across the capacitor will equal the voltage across the inductor series resistance and thus represent the current flowing through the inductor. The RC calculations are based on the room temperature DCR of the inductor.

The RC time constant should remain constant, as a function of temperature. This assures the transient response of the circuit is the same regardless of the temperature. The DCR of the inductor has a large temperature coefficient, approximately 3900ppm/°C. The temperature coefficient of the inductor must be written to the MFR_IOUT_CAL_GAIN_TC command. The external temperature is sensed near the inductor and is used to modify the internal current limit circuit to maintain an essentially constant current limit with temperature. In this application, the I_{SENSE}^+ pin is connected to the FET side of the capacitor while the I_{SENSE}^- pin is placed on the load side of the capacitor. The current sensed from the input is then given by the expression V_{DCR}/DCR. V_{DCR} is digitized by the LTC3886's telemetry ADC with an input range of ±100mV, a noise floor of 7μV_{RMS}, and a peak-peak noise of approximately 46.5μV. The LTC3886 computes the inductor current using the DCR value stored in the IOUT_CAL_GAIN command and the temperature coefficient stored in command MFR_IOUT_CAL_GAIN_TC. The resulting current value is returned by the READ_IOUT command.

INPUT CURRENT SENSING

To sense the total input current consumed by the LTC3886 and the power stage, a resistor is placed between the supply voltage and the drain of the top N-channel MOSFET. The I_{IN}^+ and I_{IN}^- pins are connected to the sense resistor. The filtered voltage is amplified by the internal high side current sense amplifier and digitized by the LTC3886's telemetry ADC. The input current sense amplifier has three gain settings of 2x, 4x, and 8x set by the bit[6:5] of the MFR_PWM_CONFIG_3886 command. The maximum differential input sense voltage for the three gain settings is 50mV, 20mV, and 5mV respectively. The LTC3886 computes the input current using the R value stored in the IIN_CAL_GAIN command. The resulting measured power stage current is returned by the READ_IIN command.

The LTC3886 uses the RVIN resistor to measure the V_{IN} pin supply current being consumed by the LTC3886. This value is returned by the MFR_READ_ICHIP command. The chip current is calculated by using the R value stored in the MFR_RVIN command. Refer to the subsection titled Input Current Sense Amplifier in the Applications Information section for further detail.

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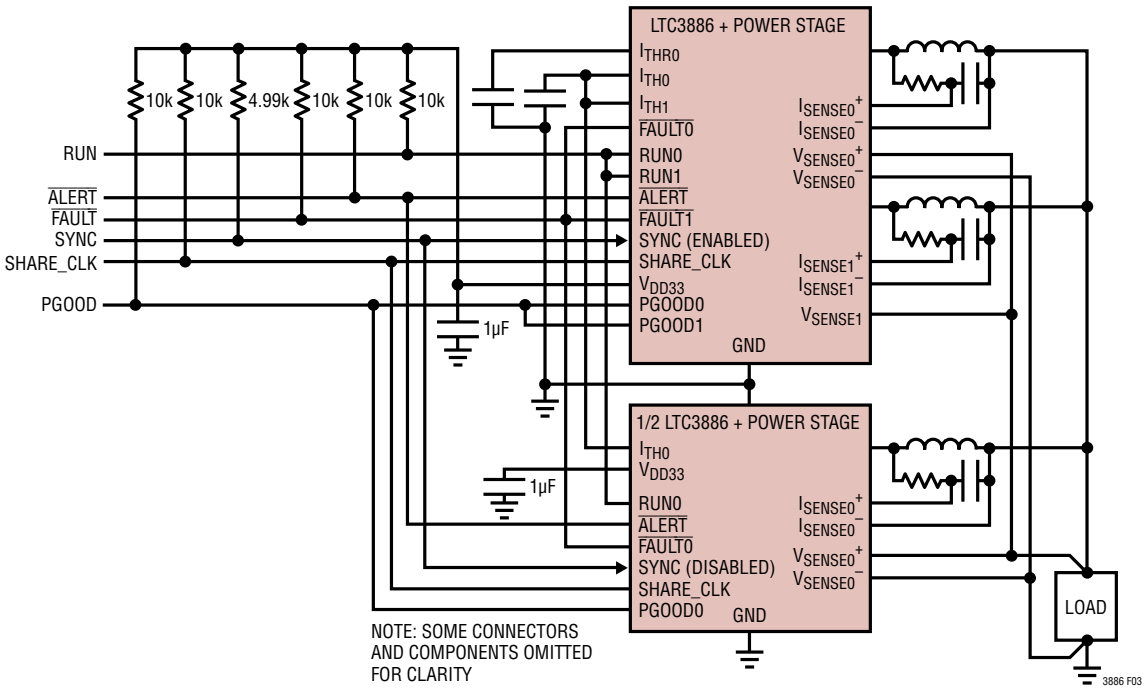

Figure 3. Load Sharing Connections for 3-Phase Operation

PolyPhase LOAD SHARING

Multiple LTC3886's can be connected in parallel in order to provide a balanced load-share solution by connecting the necessary pins. Figure 3 illustrates the shared connections required for load sharing.

The SYNC pin should only be enabled on one of the LTC3886s. The other(s) should be programmed to disable SYNC with the oscillator frequency set to the nominal value. When bit[7] of the MFR_PWM_CONFIG command is set, Channel 1 will use the feedback node of Channel 0 as its point of regulation. Do not assert bit[7] of MFR_PWM_CONFIG except in a PolyPhase application when both V_{OUT} pins are connected together and both I_{TH} pins are tied together.

EXTERNAL/INTERNAL TEMPERATURE SENSE

External temperature can best be measured using a remote, diode-connected PNP transistor such as the MMBT3906. The emitter should be connected to a TSNS pin while the base and collector terminals of the PNP transistor must be connected and returned directly to the Pin 53 of the LTC3886 GND using a Kelvin connection. The bypass capacitor between the emitter and collector must be located near the transistor. Two different currents are applied to the diode (nominally 2µA and 32µA) and the temperature is calculated from a ΔV_{BE} measurement made with the internal 16-bit monitor ADC.

The LTC3886 also supports direct V_{BE} based external temperature measurements. In this case the diode or diode network is trimmed to a specific voltage at a specific current and temperature. In general this method does not yield as accurate of a result as the single PNP transistor, but may function better in noisy applications. Refer to MFR_PWM_MODE_LTC3886 in the PMBus Command Details section for additional information on programming the LTC3886 for these two external temperature sense configurations.

The calculated temperature is returned by the PMBus READ_TEMPERATURE_1 command. Refer to the Applications Information section for details on proper layout of external temperature sense elements and PMBus commands that can be used to improve the accuracy of calculated temperatures.

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The READ_TEMPERATURE_2 command returns the internal junction temperature of the LTC3886 using an on-chip diode with a ΔV_{BE} measurement and calculation.

RCONFIG (RESISTOR CONFIGURATION) PINS

There are six input pins utilizing 1% resistor dividers between V_{DD25} and GND to select key operating parameters. The pins are ASEL0, ASEL1, FREQ_CFG, V_{OUT0_CFG}, V_{OUT1_CFG}, PHAS_CFG. If pins are floated, the value stored in the corresponding EEPROM command is used. If bit 6 of the MFR_CONFIG_ALL_LTC3886 configuration command is asserted in EEPROM, the resistor inputs are ignored upon power-up except for ASEL0 and ASEL1 which are always respected. The resistor configuration pins are only measured during power-up and an execution of a RESTORE_USER_ALL or MFR_RESET command.

The V_{OUTn_CFG} pin settings are described in Table 3. These pins select the output voltages for the LTC3886's analog PWM controllers. If the pin is open, the VOUT_COMMAND command is loaded from EEPROM to determine the output voltage. The default setting is to have the switcher off unless the voltage configuration pins are installed.

The following parameters are set as a percentage of the output voltage if the RCONFIG pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT ..... +10%
- VOUT_OV_WARN_LIMIT ..... +7.5%
- VOUT_MAX ..... +7.5%
- VOUT_MARGIN_HIGH ..... +5%
- VOUT_MARGIN_LOW ..... –5%
- VOUT_UV_WARN_LIMIT ..... –6.5%
- VOUT_UV_FAULT_LIMIT ..... –7%

The FREQ_CFG pin settings are described in Table 4. This pin selects the switching frequency. The phase relationships between the two channels and SYNC pin is determined by the PHAS_CFG pin described in Table 5. To synchronize to an external clock, the part should be put into external clock mode (SYNC output disabled but frequency set to the nominal value). If no external clock is supplied, the part will clock at the programmed frequency. If the application is multi-phase and the SYNC signal between chips is lost, the parts will not be at the same frequency increasing the ripple voltage on the output, possibly producing undesirable operation. If the external SYNC signal is being generated internally and external SYNC is not selected, bit 10 of MFR_PADS will be asserted. If no frequency is selected and the external SYNC frequency is not present, a PLL_FAULT will occur. If the user does not wish to see the $\overline{\text{ALERT}}$ from a PLL_FAULT even if there is not a valid synchronization signal at power-up, the $\overline{\text{ALERT}}$ mask for PLL_FAULT must be written. See the description on SMBALERT_MASK for more details. If the SYNC pin is connected between multiple ICs only one of the ICs should have the SYNC pin enabled, all other ICs should be configured to SYNC pin disabled.

The ASEL0 and ASEL1 pin settings are described in Table 6. ASEL1 selects the top 3 bits of the slave address for the LTC3886. ASEL0 selects the bottom 4 bits of the slave address for the LTC3886. If ASEL1 is floating, the 3 most significant bits are retrieved from the EEPROM MFR_ADDRESS command. If ASEL0 is floating, the 4 LSB bits stored in EEPROM MFR_ADDRESS command are used to determine the 4 LSB bits of the slave address. For more detail, refer to Table 6.

Note: Per the PMBus specification, pin programmed parameters can be overridden by commands from the digital interface with the exception of the ASEL*n* pins which are always honored. Do not set any part address to 0x5A or 0x5B because these are global addresses and all parts will respond to them.

FAULT HANDLING

A variety of fault and warning reporting and handling mechanisms are available. Fault and warning detection capabilities include:

- Input OV/FAULT Protection and UV Warning
- Average Input OC Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection

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- Internal and External Overtemperature Fault and Warn Protection
- External Undertemperature Fault and Warn Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection via the Bidirectional $\overline{\text{FAULT}}n$ Pins.

In addition, the LTC3886 can map any combination of fault indicators to the $\overline{\text{FAULT}}n$ pin using the propagate $\overline{\text{FAULT}}n$ response commands, MFR_FAULT_PROPAGATE_LTC3886. Typical usage of the $\overline{\text{FAULT}}n$ pin is as a driver for an external crowbar device, overtemperature alert, overvoltage alert or as an interrupt to cause a microcontroller to poll the fault commands. Alternatively, the $\overline{\text{FAULT}}n$ pin can be used as an input to detect external faults downstream of the controller that require an immediate response.

As described in the Soft-Start section, it is possible to control start-up through concatenated events. If $\overline{\text{FAULT}}n$ is used to drive the RUN pin of another controller, the unfiltered VOUT_UV fault limit should be mapped to the $\overline{\text{FAULT}}n$ pin.

Any fault or warning event will cause the $\overline{\text{ALERT}}$ pin to assert low unless the fault or warning is masked by the SMBALERT_MASK. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1, bias power is cycled or a MFR_RESET command is issued, the RUN pin is toggled OFF/ON, or the part is commanded OFF/ON via PMBus. The MFR_FAULT_PROPAGATE_LTC3886 command determines if the $\overline{\text{FAULT}}n$ pin is pulled low when a fault is detected.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Tables 7 to 11. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault condition is not present after the retry interval has elapsed, a new soft-start is attempted. If the fault persists, the controller will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling, assuming the fault condition itself is not immediately destructive. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

Status Registers and $\overline{\text{ALERT}}$ Masking

Figure 4 summarizes the internal LTC3886 status registers accessible by PMBus command. These contain indication of various faults, warnings and other important operating conditions. As shown, the STATUS_BYTE and STATUS_WORD commands also summarize contents of other status registers. Refer to PMBus Command Details for specific information.

NONE OF THE ABOVE in STATUS_BYTE indicates that one or more of the bits in the most-significant nibble of STATUS_WORD are also set.

In general, any asserted bit in a STATUS_x register also pulls the $\overline{\text{ALERT}}$ pin low. Once set, $\overline{\text{ALERT}}$ will remain low until one of the following occurs.

- A CLEAR_FAULTS, RESTORE_USER_ALL or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- The LTC3886 Successfully Transmits Its Address During a PMBus ARA
- Bias Power Is Cycled

With some exceptions, the SMBALERT_MASK command can be used to prevent the LTC3886 from asserting $\overline{\text{ALERT}}$ for bits in these registers on a bit-by-bit basis. These mask settings apply to STATUS_WORD and STATUS_BYTE in the same fashion as the status bits themselves. For example, if $\overline{\text{ALERT}}$ is masked for all bits in Channel 0 STATUS_VOUT, then $\overline{\text{ALERT}}$ is effectively masked for the V_{OUT} bit in STATUS_WORD for PAGE 0.

The BUSY bit in STATUS_BYTE also asserts $\overline{\text{ALERT}}$ low and cannot be masked. This bit can be set as a result of various internal interactions with PMBus communication. This fault occurs when a command is received that cannot be safely executed with one or both channels enabled. As discussed in Application Information, BUSY faults can be avoided by polling MFR_COMMON before executing some commands.

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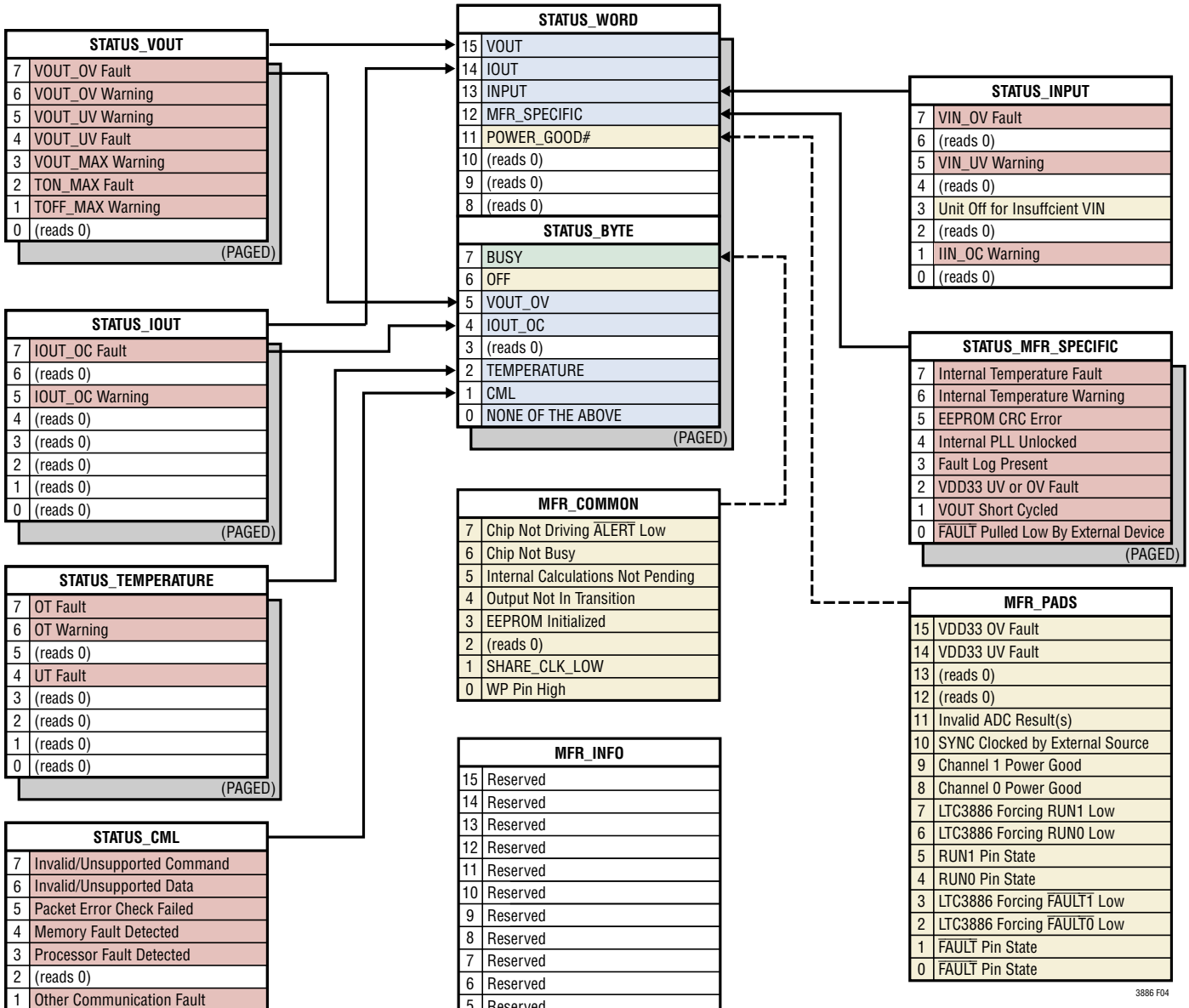

DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
General Non-Maskable Event	No	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

Figure 4. LTC3886 Status Register Summary

OPERATION

If masked faults occur immediately after power up, $\overline{\text{ALERT}}$ may still be pulled low because there has not been time to retrieve all of the programmed masking information from EEPROM.

Status information contained in MFR_COMMON and MFR_PADS can be used to further debug or clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of these registers do not affect the state of the $\overline{\text{ALERT}}$ pin and may not directly influence bits in STATUS_BYTE or STATUS_WORD.

Mapping Faults to $\overline{\text{FAULT}}$ Pins

The $\overline{\text{FAULT}}n$ pins of the LTC3886 can share faults between channels and with all ADI PMBus products including the LTC3880, LTC2974, LTC2978, LTC4676 µModule®, etc. In the event of an internal fault, one or more of the LTC3886s is configured to pull the bussed $\overline{\text{FAULT}}n$ pins low. The other LTC3886s are then configured to shut down when the $\overline{\text{FAULT}}n$ pin bus is pulled low. For autonomous group retry, the faulted LTC3886 channel is configured to release the $\overline{\text{FAULT}}n$ pin bus after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence. If the fault response is LATCH_OFF, the $\overline{\text{FAULT}}n$ pin remains asserted low until either the RUN pin is toggled OFF/ON or the part is commanded OFF/ON. The toggling of the RUN either by the pin or OFF/ON command will clear faults associated with the LTC3886. If it is desired to have all faults cleared when either RUN pin is toggled, set bit 0 of MFR_CONFIG_ALL_LTC3886 to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

Additional fault detection and handling capabilities are:

Power Good Pins

The PGOOD*n* pins of the LTC3886 are connected to the open drains of internal MOSFETs. The MOSFETs turn on and pull the PGOOD*n* pins low when the channel output voltage is not within the channels UV and OV voltage thresholds. During TON_DELAY and TON_RISE sequencing, the PG*n* pin is held low. The PGOOD*n* pin is also pulled low when the respective RUN*n* pin is low. The PGOOD*n* pin response is deglitched by an internal 60µs digital filter. The PGOOD*n* pin and PGOOD status may be different at times due to internal communication latency of up to 10µs.

CRC Protection

The integrity of the EEPROM memory is checked after a power-on reset. A CRC error will prevent the controller from leaving the reset state. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ pin will be pulled low. EEPROM repair can be attempted by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command.

The LTC3886 protects the integrity of the manufacturing data and the user data by implementing ECC and CRC checks in the EEPROM. If the ECC cannot correct the contents of a single bit fault in the EEPROM, a CRC failure will occur. This assures that all double bit faults are detected. If the CRC checks fail in either the manufacturing or user data sections of the EEPROM, the “EEPROM CRC Fault” in the STATUS_MFR_SPECIFIC command is set. If this bit remains set after being cleared by issuing a CLEAR_FAULTS or writing a 1 to this bit, an irrecoverable fault has occurred. There are no provisions for field repair of the EEPROM for these types of faults.

SERIAL INTERFACE

The LTC3886 serial interface is a PMBus compliant slave device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using either the EEPROM or an external resistor divider. In addition the LTC3886 always responds to the global broadcast address of 0x5A (7) or 0x5B (7).

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word, 7) read block, 8) write block, 9) PAGE_PLUS_READ, 10) PAGE_PLUS_WRITE, 11) SMBALERT_MASK read and 12) SMBALERT_MASK. All read operations will return a valid PEC if the PMBus master requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL_LTC3886

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command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTC3886.

Communication Protection

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the $\overline{\text{ALERT}}$ pin is pulled low.

DEVICE ADDRESSING

The LTC3886 offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

Global addressing provides a means of the PMBus master to address all LTC3886 devices on the bus. The LTC3886 global address is fixed 0x5A (7) or 0xB4 (8) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7) or 0xB6 (8) is paged and allows channel specific command of all LTC3886 devices on the bus. Other ADI device types may respond at one or both of these global addresses; therefore do not read from global addresses.

Rail addressing provides a means for the bus master to simultaneously communicate with all channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Do not read from rail addresses since multiple ADI devices may respond.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTC3886. The value of the device address is set by a combination of the ASEL0 and ASEL1 configuration pins and the MFR_ADDRESS command. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LTC3886 devices at global and rail addresses should be limited to command write operations.

RESPONSES TO V_{OUT} AND I_{OUT} FAULTS

V_{OUT} OV and UV conditions are monitored by comparators. The OV and UV limits are set in three ways.

- As a Percentage of the V_{OUT} if Using the Resistor Configuration Pins
- In EEPROM if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The I_{IN} and I_{OUT} overcurrent monitors are performed by ADC readings and calculations. Thus these values are based on average currents and can have a time latency of up to 120ms. The I_{OUT} calculation accounts for the sense resistor and the temperature coefficient of the resistor. The input current is equal to the voltage measured across the R_{IINSNS} resistor divided by the resistors value as set with the MFR_IIN_CAL_GAIN command. If this calculated input current exceeds the IN_OC_WARN_LIMIT the $\overline{\text{ALERT}}$ pin is pulled low and the IIN_OC_WARN bit is asserted in the STATUS_INPUT command.

The digital processor within the LTC3886 provides the ability to ignore the fault, shut down and latch off or shut down and retry indefinitely (retry). The retry interval is set in MFR_RETRY_DELAY and can be from 120ms to 83.88 seconds in 1ms increments. The shutdown for OV/UV and OC can be done immediately or after a user selectable deglitch time.

Output Overvoltage Fault Response

A programmable overvoltage comparator (OV) guards against transient overshoots as well as long-term overvoltages at the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared *regardless of the PMBus VOUT_OV_FAULT_RESPONSE command byte value.* This hardware level fault response delay is typically 2µs from

OPERATION

the overvoltage condition to BG asserted high. Using the VOUT_OV_FAULT_RESPONSE command, the user can select any of the following behaviors:

- OV Pull-Down Only (OV Cannot Be Ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely Using the Time Interval Specified in MFR_RETRY_DELAY

Either the Latch Off or Retry fault responses can be deglitched in increments of (0-7) • 10µs. See Table 7.

Output Undervoltage Response

The response to an undervoltage comparator output can be either:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely Using the Time Interval Specified in MFR_RETRY_DELAY

The UV responses can be deglitched. See Table 8.

Peak Output Overcurrent Fault Response

Due to the current mode control algorithm, peak output current across the inductor is always limited on a cycle by cycle basis. The value of the peak current limit is specified in sense voltage in the EC table. The current limit circuit operates by limiting the I_{TH} maximum voltage. If DCR sensing is used, the I_{TH} maximum voltage has a temperature dependency directly proportional to the TC of the DCR of the inductor. The LTC3886 automatically monitors the external temperature sensors and modifies the maximum allowed I_{TH} to compensate for this term.

The overcurrent fault processing circuitry can execute the following behaviors:

- Current Limit Indefinitely
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely Using the Time Interval Specified in MFR_RETRY_DELAY

The overcurrent responses can be deglitched in increments of (0-7) • 16ms. See Table 9.

RESPONSES TO TIMING FAULTS

TON_MAX_FAULT_LIMIT is the time allowed for V_{OUT} to rise and settle at start-up. The TON_MAX_FAULT_LIMIT condition is predicated upon detection of the VOUT_UV_FAULT_LIMIT as the output is undergoing a soft-start sequence. The TON_MAX_FAULT_LIMIT time is started after TON_DELAY has been reached and a soft-start sequence is started. The resolution of the TON_MAX_FAULT_LIMIT is 10µs. If the VOUT_UV_FAULT_LIMIT is not reached within the TON_MAX_FAULT_LIMIT time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE command value. This response may be one of the following:

- Ignore
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

This fault response is not deglitched. A value of 0 in TON_MAX_FAULT_LIMIT means the fault is ignored. The TON_MAX_FAULT_LIMIT should be set longer than the TON_RISE time.

See Table 11.

RESPONSES TO V_{IN} OV FAULTS

V_{IN} overvoltage is measured with the ADC. The response is deglitched by the 90ms typical response time of the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely Using the Time Interval Specified in MFR_RETRY_DELAY

See Table 11.

RESPONSES TO OT/UT FAULTS

Internal Overtemperature Fault/Warn Response

An internal temperature sensor protects against EEPROM damage. Above 85°C, no writes to EEPROM are recommended. Above 130°C, the internal overtemperature warn

OPERATION

threshold is exceeded and the part will NACK any EEPROM related command except RESTORE_USER_ALL or MFR_RESET and issue a CML fault for Invalid/Unsupported Command. Full EEPROM operation is re-enabled when the internal temperature has dropped below 125°C. When the die temperature exceeds 160°C the internal overtemperature fault response is enabled and the PWM is disabled until the die temperature drops below 150°C. Temperature is measured by the ADC. Internal temperature faults cannot be ignored. Internal temperature limits cannot be adjusted by the user.

See Table 10.

External Overtemperature and Undertemperature Fault Response

An external temperature sensor can be used to sense critical circuit elements like the inductor and power MOSFETs. The OT_FAULT_RESPONSE and UT_FAULT_RESPONSE commands are used to determine the appropriate response to an overtemperature and undertemperature condition, respectively. If no external sense element is used (not recommended) set the UT_FAULT_RESPONSE to ignore and set the UT_FAULT_LIMIT to –275°C. However, not using an external temperature sense element is not recommended.

The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely Using the Time Interval Specified in MFR_RETRY_DELAY

See Table 11.

RESPONSES TO EXTERNAL FAULTS

When either $\overline{\text{FAULT}}n$ pin is pulled low, the respective $\overline{\text{FAULT}}n$ bit is de-asserted in the MFR_PADS command, the $\overline{\text{FAULT}}n$ bit is set in the STATUS_MFR_SPECIFC command, the NONE_OF_THE_ABOVE bit is set in the STATUS_BYTE command, and the $\overline{\text{ALERT}}$ pin is pulled low. Responses are not deglitched. Each channel can be configured to ignore or shut down then retry in response to its $\overline{\text{FAULT}}n$ pin going low by modifying the MFR_FAULT_RESPONSE command. To avoid the $\overline{\text{ALERT}}$ pin asserting low when $\overline{\text{FAULT}}$ is pulled low, assert bit 1 of MFR_CHAN_CONFIG_LTC3886, or mask the $\overline{\text{ALERT}}$ using the SMBALERT_MASK command.

FAULT LOGGING

The LTC3886 has fault logging capability. Data is logged into memory in the order shown in Table 13. The data is stored in a continuously updated buffer in RAM. When a fault event occurs, the fault log buffer is copied from the RAM buffer into EEPROM. Fault logging is allowed at temperatures above 85°C; however, retention of 10 years is not guaranteed. When the die temperature exceeds 130°C, the fault logging is delayed until the die temperature drops below 125°C. The fault log data remains in EEPROM until a MFR_FAULT_LOG_CLEAR command is issued. Issuing this command re-enables the fault log feature. Before re-enabling fault log, be sure no faults are present and a CLEAR_FAULTS command has been issued.

When the LTC3886 powers-up or exits reset state, it checks the EEPROM for a valid fault log. If a valid fault log exists in EEPROM, the “Valid Fault Log” bit in the STATUS_MFR_SPECIFIC command will be set and an $\overline{\text{ALERT}}$ event will be generated. Also, fault logging will be blocked until the LTC3886 has received a MFR_FAULT_LOG_CLEAR command before fault logging will be re-enabled.

The information is stored in EEPROM in the event of any fault that disables the controller. The $\overline{\text{FAULT}}n$ pin being externally pulled low will not trigger a fault logging event.

BUS TIMEOUT PROTECTION

The LTC3886 implements a timeout feature to avoid persistant faults on the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 30ms or the LTC3886 will three-state the bus and ignore the given data packet. If more time is required, assert bit 3 of MFR_CONFIG_ALL_LTC3886 to allow typical bus timeouts of 255ms. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), all data bytes and the PEC byte if applicable.

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The LTC3886 allows for PMBus timeouts proportional to the length of the block read data packets. The part will add 1ms for every byte of length in excess of 32 bytes. The additional block read timeout applies primarily to the MFR_FAULT_LOG command. The timeout period defaults to 30ms.

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTC3886 supports the full PMBus frequency range from 10kHz to 400kHz.

SIMILARITY BETWEEN PMBus, SMBus AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide timeouts to prevent persistent bus errors and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, check that repeat start is supported.

The LTC3886 supports the maximum SMBus clock speed of 100kHz and is compatible with the higher speed PMBus specification (between 100kHz and 400kHz) if MFR_COMMON polling or clock stretching is enabled. For robust communication and operation refer to the Note section in the PMBus Command Summary. Clock stretching is enabled by asserting bit 1 of MFR_CONFIG_ALL_LTC3886.

PMBus SERIAL DIGITAL INTERFACE

The LTC3886 communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 5, shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC3886 is a slave device. The master can communicate with the LTC3886 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read, Block Write
- Alert Response Address

Figures 6-23 illustrate the aforementioned PMBus protocols. All transactions support PEC (parity error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended when reading the fault log.

Figure 6 is a key to the protocol diagrams in this section. PEC is optional.

A value shown below a field in the following figures is a mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/$\overline{W}$ bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

Refer to Figure 6 for a legend.

Handshaking features are included to ensure robust system communication. Please refer to the PMBus Communication and Command Processing subsection of the Applications Information section for further details.

OPERATION

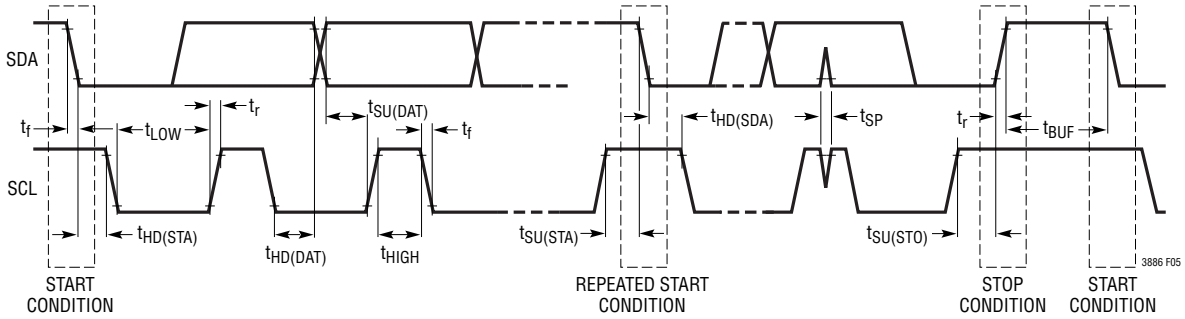

Figure 5. Timing Diagram

Table 1. Abbreviations of Supported Data Formats

	PMBus		ADI		
	TERMINOLOGY	SPECIFICATION REFERENCE	TERMINOLOGY	DEFINITION	EXAMPLE
L11	Linear	Part II ¶7.1	Linear_5s_11s	Floating point 16-bit data: value = Y • 2^N, where N = b[15:11] and Y = b[10:0], both two's compliment binary integers.	b[15:0] = 0x9807 = 10011_000_0000_0111 value = 7 • 2^{-13} = 854E-6
L16	Linear VOUT_MODE	Part II ¶8.2	Linear_16u	Floating point 16-bit data: value = Y • 2^{-12}, where Y = b[15:0], an unsigned integer.	b[15:0] = 0x4C00 = 0100_1100_0000_0000 value = 19456 • 2^{-12} = 4.75
CF	DIRECT	Part II ¶7.2	Varies	16-bit data with a custom format defined in the detailed PMBus command description.	Often an unsigned or two's compliment integer.
Reg	register bits	Part II ¶10.3	Reg	Per-bit meaning defined in detailed PMBus command description.	PMBus STATUS_BYTE command.
ASC	text characters	Part II ¶22.2.1	ASCII	ISO/IEC 8859-1 [A05]	LTC (0x4C5443)

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S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
A	ACKNOWLEDGE (THIS BIT POSITION MAY BE 0 FOR AN ACK OR 1 FOR A NACK)
P	STOP CONDITION
PEC	PACKET ERROR CODE
☐	MASTER TO SLAVE
▒	SLAVE TO MASTER
···	CONTINUATION OF PROTOCOL

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Figure 6. PMBus Packet Protocol Diagram Element Key

Figure 7. Quick Command Protocol

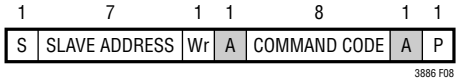


Figure 8. Send Byte Protocol

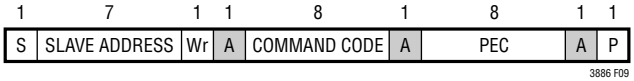


Figure 9. Send Byte Protocol with PEC

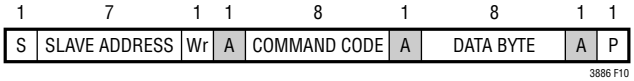


Figure 10. Write Byte Protocol

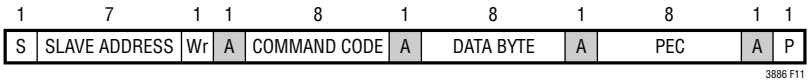


Figure 11. Write Byte Protocol with PEC

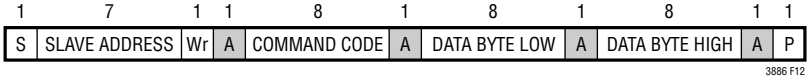


Figure 12. Write Word Protocol

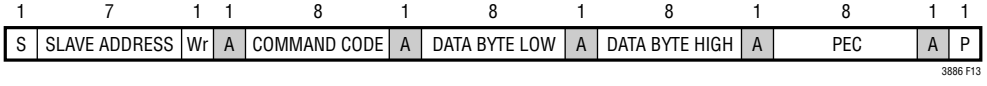


Figure 13. Write Word Protocol with PEC

OPERATION

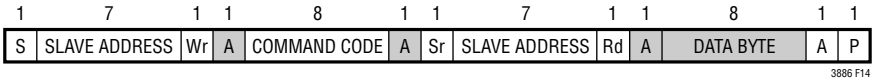


Figure 14. Read Byte Protocol

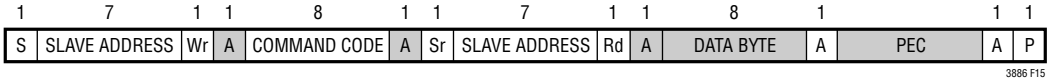


Figure 15. Read Byte Protocol with PEC

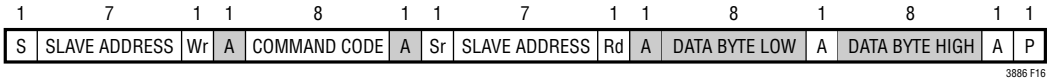


Figure 16. Read Word Protocol

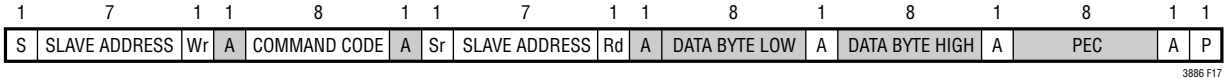


Figure 17. Read Word Protocol with PEC

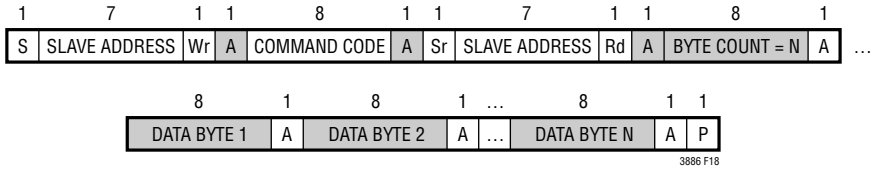


Figure 18. Block Read Protocol

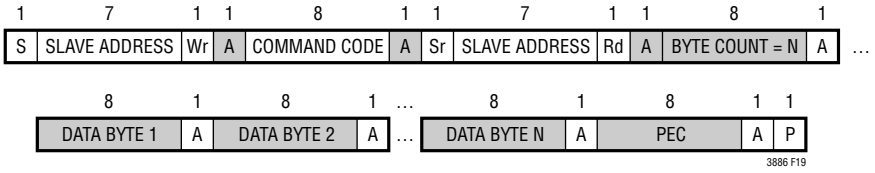


Figure 19. Block Read Protocol with PEC

OPERATION

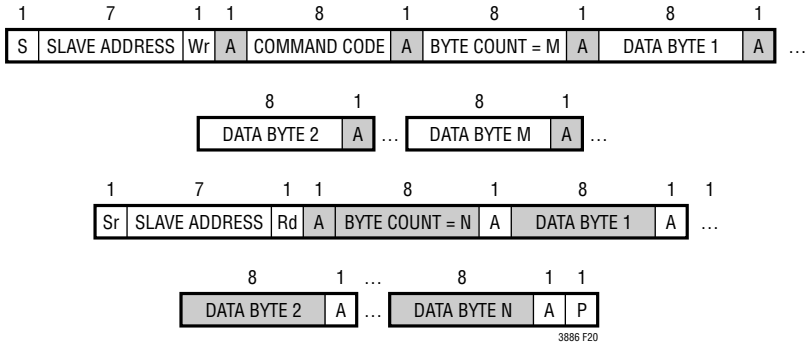


Figure 20. Block Write – Block Read Process Call

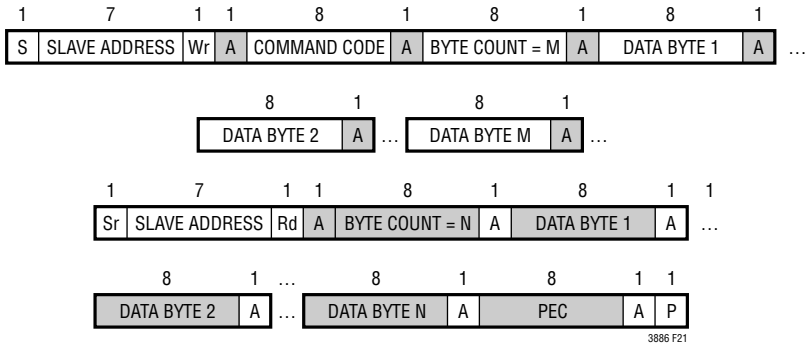


Figure 21. Block Write – Block Read Process Call with PEC

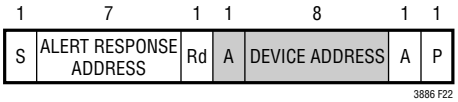


Figure 22. Alert Response Address Protocol

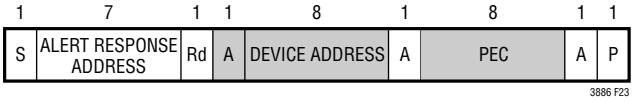


Figure 23. Alert Response Address Protocol with PEC

PMBus COMMAND SUMMARY

PMBus COMMANDS

The following tables list supported PMBus commands and manufacturer specific commands. A complete description of these commands can be found in the PMBus Power System Mgt Protocol Specification. Users are encouraged to reference this specification. Exceptions or manufacturer specific implementations are listed below in Table 2. Floating point values listed in the "DEFAULT VALUE" column are either Linear 16-bit Signed (PMBus Section 8.3.1) or Linear_5s_11s (PMBus Section 7.1) format, whichever is appropriate for the command. All commands from 0xD0 through 0xFF not listed in this table are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid undesired operation of the part. All commands from 0x00 through 0xCF not listed in this table are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event. All output voltage settings and measurements are based on the VOUT_MODE setting of 0x14. This translates to an exponent of 2^{-12}.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these circumstances the part follows the protocols defined in the PMBus Specification v1.2, Part II, Section 10.8.7, to communicate that it is busy. The part includes handshaking features to eliminate busy errors and simplify error handling software while ensuring robust communication and system behavior. Please refer to the subsection titled PMBus Communication and Command Processing in the Applications Information section for further details.

Table 2. Summary (Note: The Data Format abbreviations are detailed at the end of this table.)

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	PAGE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00	69
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x40	73
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E	73
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA	99
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N					69
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N					70
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	70
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA	110
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA	110
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	98
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ activity	Block R/W	Y	Reg		Y	see CMD	100
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14	79
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000	80
VOUT_MAX	0x24	Upper limit on the commanded output voltage including VOUT_MARGIN_HI.	R/W Word	Y	L16	V	Y	14.0 0xE000	79
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD	80

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	PAGE
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33	80
VOUT_TRANSITION_ RATE	0x27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xAA00	87
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	350 0xFABC	77
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	6.5 0xCB40	78
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	6.0 0xCB00	78
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R/W Word	Y	L11	mΩ	Y	1.8 0xBB9A	82
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A	79
VOUT_OV_FAULT_ RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	89
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133	80
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD	81
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66	81
VOUT_UV_FAULT_ RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	90
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	29.75 0xDBB8	83
IOUT_OC_FAULT_ RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	92
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	20.0 0xDA80	84
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	100.0 0xEB20	85
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8	94
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	85.0 0xEAA8	85
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–40.0 0xE580	86
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8	94
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	48.0 0xE300	78
VIN_OV_FAULT_ RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	89
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	6.3 0xCB26	78
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280	84

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	PAGE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000	86
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	8.0 0xD200	86
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10.00 0xD280	86
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	92
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000	87
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	8.00 0xD200	87
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the output to decay below 12.5% (LTC3886), MFR_VOFF_THRESHOLD (LTC3886-1).	R/W Word	Y	L11	ms	Y	150.0 0xF258	88
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA	101
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA	101
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA	102
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA	102
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA	103
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA	103
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA	104
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA	104
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA	107
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA	107
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA	107
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA	107
READ_TEMPERATURE_1	0x8D	External temperature sensor temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA	107
READ_TEMPERATURE_2	0x8E	Internal die junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA	107
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	kHz		NA	107
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		NA	108
READ_PIN	0x97	Calculated input power	R Word	N	L11	W		NA	108
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg			0x22	98
MFR_ID	0x99	The manufacturer ID of the LTC3886 in ASCII.	R String	N	ASC			LTC	98
MFR_MODEL	0x9A	LTC3886 manufacturer part number in ASCII. LTC3886-1 manufacturer part number in ASCII.	R String	N	ASC			LTC3886 LTC3886-1	98
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage including VOUT_OV_FAULT_LIMIT.	R Word	Y	L16	V		14.0 0xE000	81

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	PAGE
IC_DEVICE_ID	0xAD	Identification of the IC (LTC3886-1 only)	R Block	N	ASC		Y	LTC3886-1	98
IC_DEVICE_REV	0xAE	Revision of the IC (LTC3886-1 only)	R Block	N	ASC		Y	ACA0	99
USER_DATA_00	0xB0	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	97
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	97
USER_DATA_02	0xB2	OEM RESERVED. Typically used for part serialization	R/W Word	N	Reg		Y	NA	97
USER_DATA_03	0xB3	An EEPROM word available for the user.	R/W Word	Y	Reg		Y	0x0000	97
USER_DATA_04	0xB4	An EEPROM word available for the user.	R/W Word	N	Reg		Y	0x0000	97
MFR_INFO	0xB6	Manufacturing Specific Information	R Word		Reg			NA	104
MFR_EE_UNLOCK	0xBD	Contact factory.							116
MFR_EE_ERASE	0xBE	Contact factory.							116
MFR_EE_DATA	0xBF	Contact factory.							116
MFR_CHAN_CONFIG_ LTC3886	0xD0	LTC3886 Channel specific configuration bits. LTC3886-1 Channel specific configuration bits.	R/W Byte R/W Byte	Y Y	Reg Reg		Y Y	0x1D 0x3D	72
MFR_CONFIG_ALL_ LTC3886	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21	72
MFR_FAULT_ PROPAGATE_LTC3886	0xD2	Configuration that determines which faults are propagated to the FAULT pin.	R/W Word	Y	Reg		Y	0x6993	95
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0x70	75
MFR_PWM_MODE_ LTC3886	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC1	74
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the FAULT pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0	97
MFR_OT_FAULT_ RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0	93
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA	108
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back	R/W Byte	N	Reg			0x00	108
MFR_VOFF_THRESHOLD	0xDA	The PWM channel remains active until the ADC measures V_{OUT} below this value during sequencing OFF (LTC3886-1 only).	R/W Word	Y	L16	V	Y	0.1 0x019A	81
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350.0 0xFABC	88
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LTC3886.	R/W Word	Y	L11	ms	Y	500.0 0xFBE8	88
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA	107
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA	109
MFR_TEMPERATURE_1_ PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA	109
MFR_READ_IIN_PEAK	0xE1	Maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS	R Word	N	L11	A		NA	109

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	PAGE
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				NA	100
MFR_READ_ICHIP	0xE4	Measured supply current of the LTC3886	R Word	N	L11	A		NA	109
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA	105
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F	71
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC3886. Manufacturer code representing the LTC3886-1.	R Word	N	Reg			0x460X 0x461X	98
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	5.0 0xCA80	84
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	112
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA	116
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	Reg		Y	NA	110
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	105
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with EEPROM.	Send Byte	N				NA	111
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA	109
MFR_PWM_CONFIG_LTC3886	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10	76
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF	ppm/°C	Y	3900 0x0F3C	82
MFR_RVIN	0xF7	The resistance value of the V_{IN} pin filter element in mΩ.	R/W Word	N	L11	mΩ	Y	2000 0x0BE8	78
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	1.0 0x4000	85
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor with respect to –273.1°C	R/W Word	Y	L11	C	Y	0.0 0x8000	85
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80	71
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				NA	74

Note 1: Commands indicated with Y in the EEPROM column indicate that these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

Note 2: Commands with a default value of NA indicate “not applicable”. Commands with a default value of FS indicate “factory set on a per part basis”.

Note 3: The LTC3886 contains additional commands not listed in this table. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

Note 4: Some of the unpublished commands are read-only and will generate a CML bit 6 fault if written.

Note 5: Writing to commands not published in this table is not permitted.

Note 6: The user should not assume compatibility of commands between different parts based upon command names. Always refer to the manufacturer’s data sheet for each part for a complete definition of a command’s function.

ADI strives to keep command functionality compatible between all ADI devices. Differences may occur to address specific product requirements.

PMBus COMMAND SUMMARY

*DATA FORMAT

L11	Linear_5s_11s	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Example: For b[15:0] = 0x9807 = 'b10011_000_0000_0111 Value = $7 \cdot 2^{-13} = 854 \cdot 10^{-6}$ From "PMBus Spec Part II: Paragraph 7.1"
L16	Linear_16u	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_parameter is a 5-bit two's complement exponent that is hardwired to –12 decimal Example: For b[15:0] = 0x9800 = 'b1001_1000_0000_0000 Value = $38912 \cdot 2^{-12} = 9.50$ From "PMBus Spec Part II: Paragraph 8.2"
Reg	Register	PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Description.
I16	Integer Word	PMBus data field b[15:0] Value = Y where Y = b[15:0] is a 16 unsigned integer Example: For b[15:0] = 0x9807 = 'b1001_1000_0000_0111 Value = 38919 (decimal)
CF	Custom Format	Value is defined in detailed PMBus Command Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.
ASC	ASCII Format	A variable length string of text characters conforming to ISO/IEC 8859-1 standard.

APPLICATIONS INFORMATION

The Typical Application on the last page of this data sheet is a common LTC3886 application circuit. The LTC3886 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. The LTC3886 can nominally account for the temperature dependency of the DCR sensing element. The accuracy of the current reading and current limit are typically limited by the accuracy of the DCR of the inductor (which is programmed as the IOUT_CAL_GAIN register of the LTC3886). However, current sensing resistors provide the most accurate current sense and limiting. Other external component selections are driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Then the input and output capacitors are selected. Finally the current limit is selected. All of these components and ranges are required to be determined prior to selecting the RITH and EA_GM values in the MFR_PWM_COMP register and calculating the external compensation components. The current limit range is required because the two ranges (25mV to 50mV vs 37.5mV to 75mV) have different EA gains set with bit 7 of the MFR_PWM_MODE_LTC3886 command. The voltage RANGE bit also affects the loop gain and impacts the compensation network. The voltage RANGE is set with bit 1 of MFR_PWM_MODE_LTC3886. All other programmable parameters do not affect the loop gain, allowing parameters to be modified without impacting the transient response to load changes.

CURRENT LIMIT PROGRAMMING

The LTC3886 has two ranges of current limit programming and a total of eight levels within each range. Refer to the IOUT_OC_FAULT_LIMIT section of the PMBus commands. Within each range the error amp gain is fixed, resulting in constant loop gain. The LTC3886 will account for the temperature coefficient of the inductor DCR and automatically adjust the current limit when inductor temperature changes. The temperature coefficient of the DCR is stored in the MFR_IOUT_CAL_GAIN_TC command.

For the best current limit accuracy, use the 75mV setting. The 25mV setting will allow for the use of very low DCR inductors or sense resistors, but at the expense of current limit accuracy. Peak current limiting is on a cycle-by-cycle basis. The average inductor current is monitored by the ADC converter and can provide a warning if too much average output current is detected. An overcurrent fault is detected when the I_{TH} voltage exceeds the limit set by IOUT_OC_FAULT_LIMIT. The digital processor within the LTC3886 provides the ability to either ignore the fault, shut down and latch off or shut down and retry indefinitely (retry). Refer to the overcurrent portion of the Operation section for more detail.

I_{SENSE}^+ and I_{SENSE}^- PINS

The I_{SENSE}^+ and I_{SENSE}^- pins are the inputs to the current comparator and the A/D. The common mode input voltage range of the current comparators is 0V to 14V. Both the SENSE pins are high impedance inputs with small input currents typically less than 1µA. The high impedance inputs to the current comparators enable accurate DCR sensing. Do not float these pins during normal operation.

Filter components connected to the I_{SENSE} traces should be placed close to the IC. The positive and negative traces should be routed differentially and Kelvin connected to the current sense element, see Figure 24. A non-Kelvin connection or improper placement can add parasitic inductance and capacitance to the current sense element, degrading the signal at the sense terminals and making the programmed current limit perform poorly. In a PolyPhase system, poor placement of the sensing element will result in sub-optimal current sharing between power stages. If DCR sensing is used (Figure 25a), sense resistor R1 should be placed close to the inductor to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC

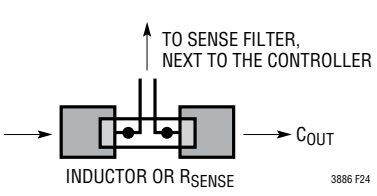
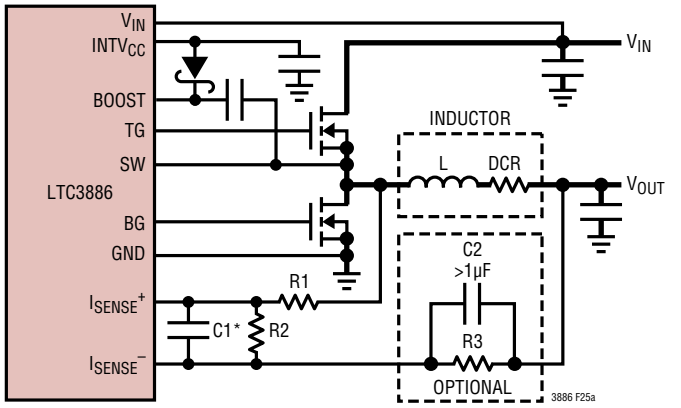


Figure 24. Optimal Sense Line Placement

APPLICATIONS INFORMATION

pins. Any impedance difference between the I_{SENSE}^+ and I_{SENSE}^- signal paths can result in loss of accuracy in the current reading of the ADC. The current reading accuracy can be improved by matching the impedance of the two signal paths. To accomplish this add a series resistor between V_{OUT} and I_{SENSE}^- equal to R1. A capacitor of 1µF or greater should be placed in parallel with this resistor. If the peak voltage is <75mV at room temperature, R2 is not required.



$((R1+R3)||R2) \times C1 = \frac{2 \times L}{DCR}$ $\quad IOUT_CAL_GAIN = DCR \times \frac{R2}{R1 + R2 + R3}$

R3 = R1

*PLACE C1 NEAR SENSE+, SENSE– PINS

Figure 25a. Inductor DCR Current Sense Circuit

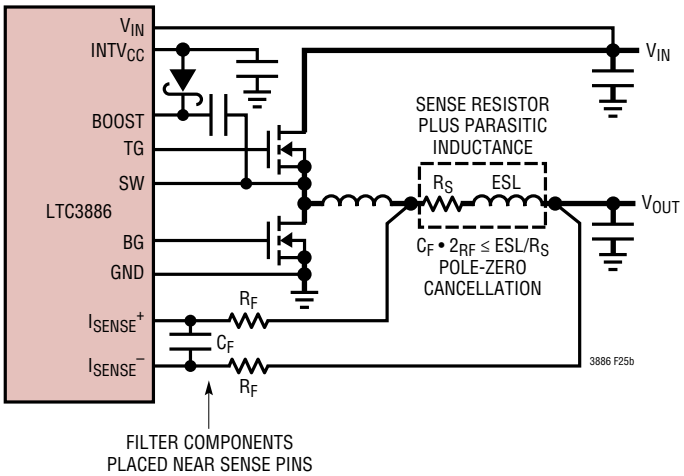


Figure 25b. Resistor Current Sense Circuit

LOW VALUE RESISTOR CURRENT SENSING

A typical sensing circuit using a discrete resistor is shown in Figure 25b. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIMIT} setting. The input common mode range of the current comparator is 0V to 14V (if V_{IN} is greater than 15V). The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Due to possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 15mV minimum ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications.

For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628/LTC3728 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. In the newer and higher current density solutions, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be less than 20mV. Also, inductor ripple currents greater than 50% with operation up to 750kHz are becoming more common. Under these conditions, the voltage drop across the sense resistor's parasitic inductance is no longer negligible. A typical sensing circuit using a discrete resistor is shown in Figure 25b. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of the capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 100Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 200ns.

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This same RC filter with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 26 illustrates the voltage waveform across a 2mΩ resistor with a PCB footprint of 2010. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time, t_{ON}, and off-time, t_{OFF}, of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \bullet \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}} \quad (1)$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resultant waveform looks resistive, as shown in Figure 27. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use Equation 1 to determine the ESL. However, do not overfilter the signal. Keep the RC time constant less than or equal to the inductor time constant to maintain a sufficient ripple voltage on V_{RSENSE} for optimal operation of the current loop controller.

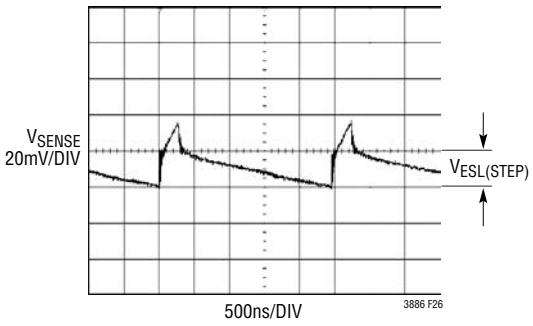

Figure 26. Voltage Measured Directly Across R_{SENSE}

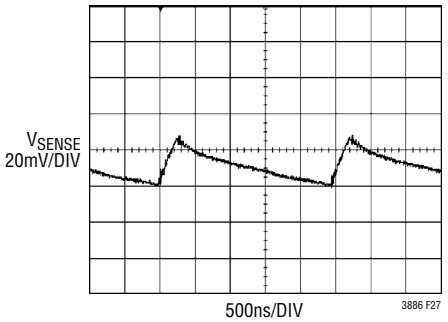

Figure 27. Voltage Measured After the R_{SENSE} Filter

INDUCTOR DCR CURRENT SENSING

For applications requiring the highest possible efficiency at high load currents, the LTC3886 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 25a. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would reduce the efficiency by a few percent compared to DCR sensing.

If R1 = R3 and the external (R1 + R3)||R2 • C1 time constant is chosen to be exactly equal to the 2 • L/DCR time constant, assuming R1 = R3, the voltage drop across the external capacitor,C1, is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2 + R3). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. The DCR value is entered as the IOUT_CAL_GAIN in mΩ unless R2 is required. If R2 is used:

$$IOUT_CAL_GAIN = DCR \bullet \frac{R2}{R1 + R2 + R3}$$

R2 can be removed if there is no need to attenuate the current sense signal in order to remain within the desired current sense range. To properly select the external filter components, the DCR of the inductor must be known. It can be measured using an accurate RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the inductor manufacturers' data sheets for detailed information. The LTC3886 will correct for temperature variation if the correct temperature coefficient value is entered into the MFR_IOUT_CAL_GAIN_TC command. Typically the resistance has a 3900ppm/°C coefficient.

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Assuming R1 = R3, C2 can be optimized for a flat frequency response using the following equation:

$$C2 = \frac{2R1 \bullet R2 \bullet C1 - \frac{L}{DCR}(2R1 + R2)}{R1^2}$$

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, be sure to pick the optimum I_{LIMIT} value accounting for tolerance in the DCR versus the MFR_IOUT_CAL_GAIN parameter entered.

Next, determine the DCR of the inductor. Use the manufacturer's maximum value, which is usually specified at 20°C. Increase this value to account for tolerances in the temperature sensing element of 3°C to 5°C and any additional temperature differences associated with the proximity of the temperature sensor element to the inductor.

C1 is usually selected to be in the range of 0.047µF to 4.7µF. This forces (R1 + R3)||R2 to be approximately 2k. Adding optional elements R3 and C2 shown in Figure 18a will minimize offset errors associated with the I_{SENSE} leakage currents. Set R3 equal to the value of R1. Set C2 to a value of 1µF or greater to ensure adequate noise filtering.

The equivalent resistance (R1 + R3)||R2 is scaled to the room temperature inductance and maximum DCR:

$$(R1 + R3)||R2 = \frac{2 \bullet L}{(DCR \text{ at } 20°C) \bullet C1}$$

The maximum power loss in R1 is related to the duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reducing conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method. Selecting discontinuous mode will improve the converter efficiency at light loads regardless of the current sensing method.

To maintain a good signal-to-noise ratio for the current sense signal, use a minimum ΔV_{ISENSE} of 10mV to 15mV. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{ISENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \bullet \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

SLOPE COMPENSATION AND INDUCTOR PEAK CURRENT

Slope compensation provides stability in constant frequency current mode architectures by preventing subharmonic oscillations at high duty cycles. This is accomplished internally by adding a compensation ramp to the inductor current signal at duty cycles in excess of 35%. The LTC3886 uses a patented current limit technique that cancels the effect of the compensating ramp. This allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

INDUCTOR VALUE CALCULATION

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \bullet f_{OSC} \bullet L}$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at the lowest frequency with a small ripple current. Achieving this, however, requires a large inductor.

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A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that the ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN} \bullet f_{OSC} \bullet I_{RIPPLE}}$$

INDUCTOR CORE SELECTION

Once the inductor value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance. As the inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate hard, which means that the inductance collapse abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

POWER MOSFET AND OPTIONAL SCHOTTKY DIODE SELECTION

Two external power MOSFETs must be selected for each output channel in the LTC3886: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V. Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f_{OSC}$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low

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or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes connected from ground to SW*n* conduct during the dead time between the conduction of the two power MOSFETs. These prevent the body diodes of the bottom MOSFETs from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} AND C_{OUT} SELECTION

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}} \left[(V_{OUT})(V_{IN} - V_{OUT}) \right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2 \bullet V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3886, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of using a LTC3886 in 2-phase operation can be calculated by using the equation above for the higher power channel and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both channels are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case scenario is adequate for the dual controller design. Also, if applicable the power losses due to the input protection fuse resistance, V_{IN} source impedance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the V_{IN} power supply/battery is included in the efficiency testing. The drain terminals of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances on V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3886, is also suggested. A 2.2Ω to 10Ω R_{VIN} resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation if multiple LTC3886s are used.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE} \left(ESR + \frac{1}{8 f C_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTC3886 must enter the run state prior to soft-start. The RUN*n* pin is released after the part initializes and V_{IN} is greater than the VIN_ON threshold. If multiple LTC3886s are used in an application, they should be configured to share the same RUN*n* pins. They all hold their respective RUN*n* pins low until all devices initialize and V_{IN} exceeds the VIN_ON threshold for all devices. The SHARE_CLK

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pin assures all the devices connected to the signal use the same time base for time delay operations.

After the RUN*n* pin releases, the controller waits for the user-specified turn-on delay (TON_DELAY) prior to initiating an output voltage ramp. Multiple LTC3886s and other ADI parts can be configured to start with equal or unique delay times. To work within a desired synchronization scheme all devices must use the same timing clock (SHARE_CLK) and all devices must share the RUN*n* pin. This allows the relative delay of all parts to be synchronized. The actual variation in the delays will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Analog Devices ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±10% in frequency, thus the actual time delays will have proportional variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0.0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISE to any value less than 0.250ms. The LTC3886 will perform the necessary math to assure the voltage ramp is controlled to the desired slope. However, the voltage slope can not be any faster than the fundamental limits of the power stage. The shorter TON_RISE time is set, the larger the discrete steps in the TON_RISE ramp will appear. The number of steps in the ramp is equal to TON_RISE/0.1ms.

The LTC3886 PWM will always use discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom gate is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load.

The LTC3886 does not include a traditional tracking feature. However, two outputs can be given the same TON_RISE and TON_DELAY times to effectively ramp up at the same time. If the RUN pin is released at the same time and both LTC3886s use the same time base, the outputs will track very closely. If the circuit is in a PolyPhase configuration, all timing parameters for that rail must be the same.

The previously described method of start-up sequencing is time based. For concatenated events it is possible to control the RUN*n* pins based on the $\overline{\text{FAULT}}$*n* pin of a different controller, or the PGOODn pin(s) of the LTC3886. The $\overline{\text{FAULT}}$*n* pins can be configured to release when the output voltage of the converter is greater than the VOUT_UV_FAULT_LIMIT. It is recommended to use the deglitched V_{OUT} UV fault limit because there is little appreciable time delay between the converter crossing the UV threshold and the $\overline{\text{FAULT}}$*n* pin releasing. The deglitched output can be enabled by setting the Mfr_FAULT_propagate_vout_uvuf bit in the MFR_FAULT_PROPAGATE_LTC3886 command. Refer to the MFR section of the PMBus commands in this document. The UV comparator output signal may have some glitching as the V_{OUT} signal transitions through the comparator threshold. The LTC3886 includes a 70µs digital deglitch filter to greatly reduce the probability of multiple transitions. To minimize the risk of $\overline{\text{FAULT}}$*n* pins glitching, make the TON_RISE times less than 100ms. If unwanted transitions still occur on $\overline{\text{FAULT}}$*n*, place a capacitor to ground on the $\overline{\text{FAULT}}$*n* pin to filter the waveform. The RC time-constant of the filter should be set sufficiently fast to assure no appreciable delay is incurred. A delay of 300µs to 500µs will provide some additional filtering without significantly delaying the trigger event.

DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the MFR_PWM_MODE_LTC3886 command. In digital servo mode the LTC3886 will adjust the regulated output voltage based on the ADC voltage reading. Every 90ms the digital servo loop will step the LSB of the DAC (nominally 4mV or 2mV depending on the voltage range bit) until the output is at the correct ADC reading. At power-up this mode engages after TON_MAX_FAULT_LIMIT unless the limit is set to 0 (infinite). If the TON_MAX_FAULT_LIMIT is set to 0 (infinite), the servo begins after TON_RISE is complete and V_{OUT} has exceeded the VOUT_UV_FAULT_LIMIT. This same point in time is when the output changes from discontinuous to the programmed mode as indicated in MFR_PWM_MODE_LTC3886 bit 0. Refer to Figure 28 for details on the V_{OUT} waveform under time-based sequencing.

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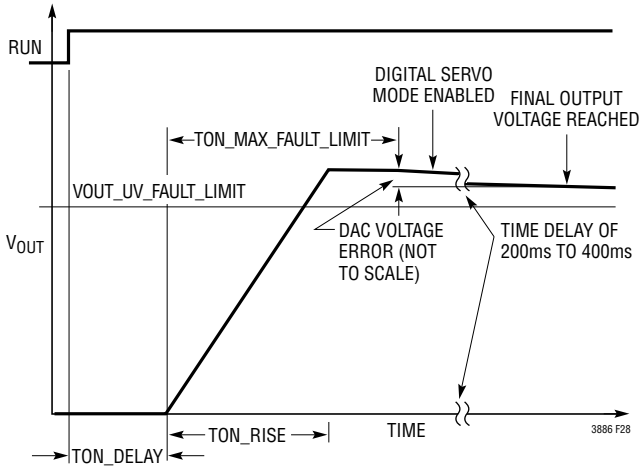

Figure 28. Timing Controlled VOUT Rise

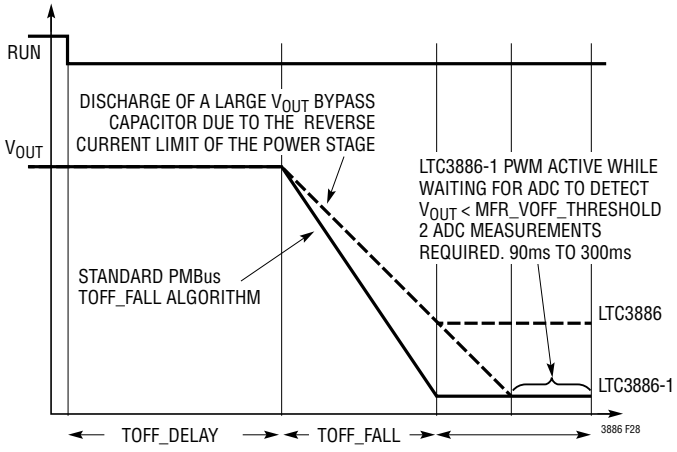

Figure 29. TOFF_DELAY and TOFF_FALL

If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is set to ignore (0x00), the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time is reached.
3. After the VOUT_UV_FAULT_LIMIT has been exceed or the IOUT_OC_FAULT_LIMIT is not longer active.

If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is not set to ignore 0X00, the servo begins:

1. After the TON_RISE sequence is complete;
2. After the TON_MAX_FAULT_LIMIT time has expired and both VOUT_UV_FAULT and IOUT_OC_FAULT are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase application only one phase should have digital servo mode enabled. This will ensure the phases servo to the same output regulation point.

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTC3886 also supports controlled turn-off. The TOFF_DELAY and TOFF_FALL functions are shown in Figure 29. TOFF_FALL is processed when the RUN pin goes low or if the part is commanded off. If the part faults off or $\overline{\text{FAULT}}n$ is pulled low externally and the part is programmed to respond to $\overline{\text{FAULT}}n$, the output will three-state by turning off both the main and synchronous MOSFETs turned off. The output will decay as a function of the load rather than exhibiting a controlled ramp.

The output voltage will ramp as shown in Figure 29 so long as the part is in forced continuous mode and the TOFF_FALL time is slow enough that the power stage can achieve the desired slope. The TOFF_FALL time can only be met if the power stage and controller can sink sufficient current to assure the output is at zero volts by the end of the fall time interval. If the TOFF_FALL time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero volt state. At the end of TOFF_FALL, the controller will cease to sink current and V_{OUT} will decay at the natural rate determined by the load impedance. The LTC3886-1 sequence off feature is enabled by bit[5] of the MFR_CHAN_CONFIG_LTC3886 command. When enabled, the sequence off feature keeps the power stage on until the output voltage has ramped below the MFR_VOFF_THRESHOLD value. This allows the LTC3886-1, in continuous mode, to fully discharge very large output capacitors regardless if the controller power stage can sink enough current to meet the TOFF_FALL time. If the controller is in discontinuous mode, the controller will not pull negative current and the output will be

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pulled low by the load, not the power stage. The maximum fall time is limited to 1.3 seconds. The shorter TOFF_FALL time is set, the larger the discrete steps of the TOFF_FALL ramp will appear. The number of steps in the ramp is typically TOFF_FALL/0.1ms.

$INTV_{CC}$ REGULATOR

The LTC3886 features a PMOS linear regulator that supplies power to $INTV_{CC}$ from the V_{IN} or $EXTV_{CC}$ supply. $INTV_{CC}$ powers the gate drivers, V_{DD33} and much of the LTC3886 internal circuitry. The linear regulator produces 5V at the $INTV_{CC}$ pin when V_{IN} or $EXTV_{CC}$ is greater than approximately 5.5V. The regulator can supply a peak current of 100mA and must be bypassed to ground with a minimum of 1µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and GND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage application in which large MOSFETs are being driven at high frequencies may cause the maximum die junction temperature rating for the LTC3886 to be exceeded. To reduce die temperature, the $INTV_{CC}$ current, of which a large percentage is due to the gate charge current, may be supplied from either the V_{IN} or $EXTV_{CC}$ pin. If the LTC3886 internal regulator is powered from the V_{IN} pin, the power through the IC is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations in Note 2 of the Electrical Characteristics. For example, at 70°C ambient, the LTC3886 $INTV_{CC}$ current is limited to less than 44mA from a 40V supply:

$$T_J = 70°C + 44mA \bullet 40V \bullet 31°C/W = 125°C$$

To prevent the maximum junction temperature from being exceeded, the LTC3886 internal LDO can be can powered from the $EXTV_{CC}$ pin. If the $EXTV_{CC}$ pin is not used to power $INTV_{CC}$, the $EXTV_{CC}$ pin must be tied to GND, do not float this pin. The V_{IN} current resulting from the gate driver and control circuitry will be reduced to a minimum by supplying the $INTV_{CC}$ current from the $EXTV_{CC}$ pin with an external supply or an output derived source.

Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + 44mA \bullet 5V \bullet 31°C/W + 2mA \bullet 40V \bullet 31°C/W = 80°C$$

Do not tie $INTV_{CC}$ on the LTC3886 to an external supply because $INTV_{CC}$ will attempt to pull the external supply high and hit current limit, significantly increasing the die temperature.

Applying voltages below –0.3V to the $EXTV_{CC}$ pin may result in permanent damage to the device. If the $EXTV_{CC}$ pin is tied to an output of the controller and the external load can pull the output below –0.3V, a Schottky diode from GND to $EXTV_{CC}$ must be used to protect the $EXTV_{CC}$ pin.

For applications where V_{IN} is 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 30. To minimize the voltage drop caused by the gate charge current a low ESR capacitor must be connected to the V_{IN}/$INTV_{CC}$ pins. This configuration will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low. Make sure the $INTV_{CC}$ voltage exceeds the $R_{DS(ON)}$ test voltage for the MOSFETs which is typically 4.5V for logic level devices. The UVLO on $INTV_{CC}$ is set to approximately 4V.

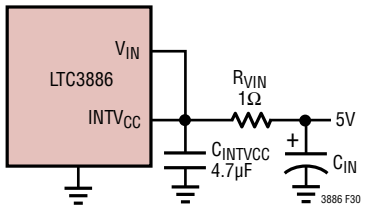

Figure 30. Setup for a 5V Input

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TOPSIDE MOSFET DRIVER SUPPLY (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST*n* pin supplies the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Block Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW*n* pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW*n*, rises to V_{IN} and the BOOST*n* pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$.

PWM jitter has been observed in some designs operating at higher V_{IN}/V_{OUT} ratios. This jitter does not substantially affect the circuit accuracy. Referring to Figure 31, PWM jitter can be removed by inserting a series resistor with a value of 1Ω to 5Ω between the cathode of the diode and the BOOST*n* pin.

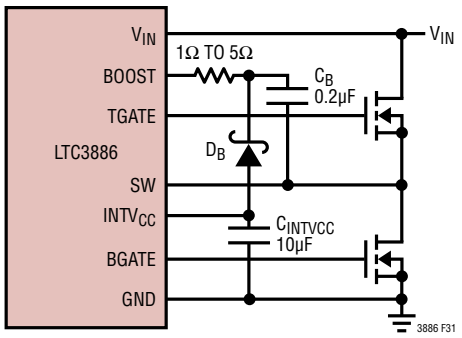

Figure 31. Boost Circuit to Minimize PWM Jitter

UNDERVOLTAGE LOCKOUT

The LTC3886 is initialized by an internal threshold-based UVLO where V_{IN} must be approximately 4V and $INTV_{CC}$, V_{DD33}, V_{DD25} must be within approximately 20% of the regulated values. In addition, V_{DD33} must be within approximately 7% of the targeted value before the RUN pin is released. After the part has initialized, an additional comparator monitors V_{IN}. The VIN_ON threshold must be exceeded before the power sequencing can begin. When V_{IN} drops below the VIN_OFF threshold, the SHARE_CLK pin will be pulled low and V_{IN} must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed. If $\overline{FAULT}n$ is held low when V_{IN} is applied, $\overline{ALERT}$ will be asserted low even if the part is programmed to not assert $\overline{ALERT}$ when $\overline{FAULT}n$ is held low. If I^2C communication occurs before the LTC3886 is out of reset and only a portion of the command is seen by the part, this can be interpreted as a CML fault. If a CML fault is detected, $\overline{ALERT}$ is asserted low.

It is possible to program the contents of the EEPROM in the application if the V_{DD33} supply is externally driven. This will activate the digital portion of the LTC3886 without engaging the high voltage sections. PMBus communications are valid in this supply configuration. If V_{IN} has not been applied to the LTC3886, bit 3 (EEPROM Not Initialized)in MFR_COMMON will be asserted low. If this condition is detected, the part will only respond to addresses 5A and 5B. To initialize the part issue the following set of commands: global address 0x5B command 0xBD data 0x2B followed by global address 5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired then issue a STORE_USER_ALL. When V_{IN} is applied a MFR_RESET command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

FAULT INDICATIONS

The LTC3886 $\overline{FAULT}n$ pins are configurable to indicate a variety of faults including OV, UV, OC, OT, timing faults, peak overcurrent faults. In addition the $\overline{FAULT}n$ pins can be pulled low by external sources indicating a fault in some other portion of the system. The fault response is configurable and allows the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Refer to the PMBus section of the data sheet and the PMBus specification for more details regarding fault responses.

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The OV response is always automatic. If an OV condition is detected, TG*n* goes low and BG*n* is asserted.

OPEN-DRAIN PINS

The LTC3886 has the following open-drain pins:

3.3V Pins

1. $\overline{\text{FAULT}}$*n*
2. SYNC
3. SHARE_CLK
4. PGOOD*n*

5V Pins (5V pins operate correctly when pulled to 3.3V.)

1. RUN*n*
2. $\overline{\text{ALERT}}$
3. SCL
4. SDA

All the above pins have on-chip pull-down transistors that can sink 3mA at 0.4V. Unless there are transient speed issues associated with the RC time constant of the resistor pull-up and parasitic capacitance to ground, a 10k resistor or larger is generally recommended.

For high speed signals such as the SDA, SCL and SYNC, a lower value resistor may be required. The RC time constant should be set to 1/3 to 1/5 the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA and SCL pins with the time constant set to 1/3 the rise time:

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k$$

Minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is one time constant.

The SYNC pin has an on-chip pull-down transistor with the output held low for nominally 500ns. If the internal oscillator is set for 500kHz and the load is 100pF and a 3x time constant is required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5k$$

If timing errors are occurring or if the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. If not reduce the pull up resistor sufficiently to assure proper timing. The SHARE_CLK pull-up resistor has a similar equation with a period of 10µs and a pull-down time of 1µs. The RC time constant should be approximately 3µs or faster.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTC3886 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the **falling** edge of the SYNC pin. The phase relationship between the PWM controller and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_CONFIG_LTC3886 command. For PolyPhase applications, it is recommended all the phases be spaced evenly. Thus for a 2-phase system the signals should be 180° out of phase and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 100kHz and 750kHz. Nominal parts will have a range beyond this; however, operation to a wider frequency range is not guaranteed.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{\text{ALERT}}$ pin is pulled low. The fault can be cleared by writing a 1 to the

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bit. If the user does not want the $\overline{\text{ALERT}}$ pin to assert if a PLL_FAULT occurs, the SMBALERT_MASK command can be used to prevent the alert.

If there is no external signal applied to the SYNC pin in the application, the nominal programmed frequency will control the PWM circuitry. If FREQUENCY_SWITCH is programmed to external oscillator, and no external SYNC signal is present, the LTC3886 PWM engine will run at the lowest free running frequency of the PLL oscillator. This may result in excess inductor current and undesirable operation. If multiple parts share the SYNC signal and the external SYNC signal is not present, the parts will not be synchronized and excess voltage ripple on the output may be present.

Multiple LTC3886s are required to share one SYNC signal in PolyPhase configurations, for other configurations connecting the SYNC pins to form a single SYNC signal is optional. If the SYNC pin is shared between LTC3886s, only one LTC3886 should be programmed with a frequency output. All the other LTC3886s should be programmed to disable their SYNC output. However their frequency should be programmed to the nominal desired value. If the LTC3886 is programmed with a frequency output, and an external signal is present. Bit 10 of MFR_PADS will be asserted low if this condition exists.

If the PWM signal appears to be running at too high a frequency, monitor the SYNC pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise versus the intended signal. Review routing of digital control signals and minimize crosstalk to the SYNC signal to avoid this problem.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3886 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn off the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3886 is approximately 90ns. Good PCB layout, minimum 30% inductor current ripple and at least 10mV to 15mV ripple on the current sense signal are required to avoid increasing the minimum on-time. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak current sense voltage decreases, the minimum on-time gradually increases to 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

EXTERNAL TEMPERATURE SENSE

The LTC3886 is capable of measuring the temperature of the power stage temperature of each channel. Multiple methods using silicon junction remote sensors are supported. The voltage produced by the remote sense circuit is digitized by the internal ADC, and the computed temperature value is returned by the paged READ_TEMPERATURE_1 telemetry command.

The most accurate external temperature measurement can be made using a diode-connected PNP transistor such as the MMBT3906 as shown in Figure 32. Bit 5 of MFR_PWM_MODE_LTC3886 should be set to 0 (ΔV_{BE} method) when using this sensor configuration. The transistor should be placed in contact with or immediately adjacent to the power stage inductor. Its emitter should be connected to the TSNS*n* pin while the base and collector terminals of the PNP transistor must be connected and returned directly to Pin 53 of the LTC3886 using a Kelvin connection. For best noise immunity, the connections should be routed differentially and a 10nF capacitor should be placed in parallel with the diode-connected PNP. Parasitic PCB trace inductance between the capacitor and transistor should be minimized. Avoid placing PCB vias between the transistor and capacitor.

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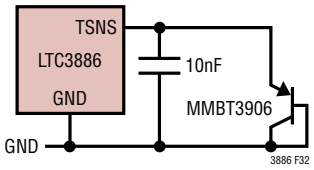

Figure 32. External ΔV_{BE} Temperature Sense

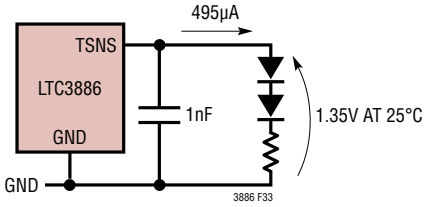

Figure 33. 2D+R Temperature Sense

The LTC3886 also supports direct junction voltage measurements when bit 5 of MFR_PWM_MODE_LTC3886 is set to one. The factory defaults support a resistor-trimmed dual diode network as shown in Figure 33. This second measurement method is not generally as accurate as the first, but it supports legacy power blocks or may prove necessary if high noise environments prevent use of the ΔV_{BE} approach with its lower signal levels.

For either method, the slope of the external temperature sensor can be modified with the coefficient stored in MFR_TEMP_1_GAIN. With the ΔV_{BE} approach, typical PNPs require temperature slope adjustments slightly less than 1. The MMBT3906 has a recommended value of approximately MFR_TEMP_1_GAIN = 0.991 based on the ideality factor of 1.01. Simply invert the ideality factor to calculate the MFR_TEMP_1_GAIN. Different manufacturers and different lots may have different ideality factors. Consult with the manufacturer to set this value. Characterization over temperature of a prototype or prototypes is recommended before selecting a final MFR_TEMP_1_GAIN value when using the direct p-n junction measurement method.

The offset of the external temperature sense can be adjusted using MFR_TEMP_1_OFFSET.

If an external temperature sense element is not used, the TSNS*n* pin must be shorted to GND. The UT_FAULT_LIMIT must be set to –275°C, the UT_FAULT_RESPONSE must be set to ignore, and the IOUT_CAL_GAIN_TC to a value of 0.

To ensure proper use of these temperature adjustment parameters, refer to the specific formulas given for the two methods in the MFR_PWM_MODE_LTC3886 command section.

Derating EEPROM Retention at Temperature

EEPROM read operations between –40°C and 125°C will not affect data storage. But retention will be degraded if the EEPROM is written above 85°C or stored or operated above 125°C. If an occasional fault log is generated above 85°C, the slight reduction in data retention in the EEPROM fault log area will not affect the use of the function or other EEPROM storage. See the Operation section for other high temperature EEPROM functional details. Degradation in data can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

$k = 8.617 \bullet 10^{-5}$ eV/°K

T_{USE} = is the specified junction temperature

T_{STRESS} = actual junction temperature in °C

As an example, if the device is stored at 130°C for 10 hours,

T_{STRESS} = 130°C, and

$$AF = e^{\left[\left(\frac{1.4}{8.617\bullet10^{-5}}\right)\bullet\left(\frac{1}{398}-\frac{1}{403}\right)\right]} = 1.66$$

indicating the effect is the same as operating the device at 125°C for 10 • 1.66 = 16.6 hours, resulting in a retention derating of 6.6 hours.

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INPUT CURRENT SENSE AMPLIFIER

The LTC3886 input current sense amplifier can sense the supply current into the V_{IN} pin using an external resistor as well as the power stage current using an external sense resistor. Unless care is taken to mitigate the frequency noise caused by the discontinuous input current, significant input current measurement error may occur. The noise will be the greatest in high current applications and at large step-down ratios. Careful layout and filtering at the V_{IN} pin is recommended to minimize measurement error. The V_{IN} pin should be filtered with a resistor and a ceramic capacitor. The filter should be located as close to the V_{IN} pin as possible. The supply side of the V_{IN} pin filter should be Kelvin connected to the supply side of the R_{IINSNS} resistor. A 2Ω resistor should be sufficient for most applications. The resistor will cause an IR voltage drop from the supply to the V_{IN} pin due to the current flowing into the V_{IN} pin. To compensate for this voltage drop, the MFR_RVIN command value should be set to the nominal resistor value. The LTC3886 will multiply the MFR_READ_ICHIP measurement value by the user defined MFR_RVIN value and add this voltage to the measured voltage at the V_{IN} pin.

$$READ_VIN = V_{VIN_PIN} + (MFR_READ_ICHIP \bullet MFR_RVIN)$$

Therefore, the READ_VIN command will return the value of the voltage at the supply side of the V_{IN} pin filter. If no V_{IN} filter element is used, set MFR_RVIN = 0.

The capacitor from the drain of the topside MOSFET to ground should be a low ESR ceramic capacitor. It should be placed as close as possible to the drain of the topside MOSFET to supply high frequency transient input current. This will help prevent noise from the top gate MOSFET from feeding into the input current sense amplifier inputs and supply.

If the input current sense amplifier is not used, short the V_{IN}, I_{IN}^+ and I_{IN}^- and pins together.

EXTERNAL RESISTOR CONFIGURATION PINS (RCONFIG)

The LTC3886 is factory programmed to use external resistor configuration. This allows output voltage, PWM frequency, PWM phasing, and the PMBus address to be set by the user without programming the part through the PMBus interface or purchasing custom programmed parts. To use resistor programming, the RCONFIG pin(s) require a resistor divider between V_{DD25} and GND. The RCONFIG pins are only interrogated at initial power up and during a reset, so modifying their values on the fly while the part is powered will have no effect. RCONFIG pins on the same IC can be shared with a single resistor divider if they require identical programming. Resistors with a tolerance of 1% or better must be used to assure proper operation. In the following tables, R_{TOP} is connected between V_{DD25} and the RCONFIG pin while R_{BOT} is connected between the pin and GND. Noisy clock signals should not be routed near these pins.

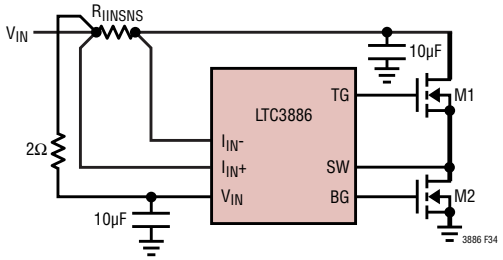

Figure 34. Low Noise Input Current Sense Circuit

Voltage Selection

When an output voltage is set using the VOUT_CFG*n* pins the following parameters are set as a percentage of the output voltage:

- VOUT_OV_FAULT_LIMIT ..... +10%
- VOUT_OV_WARN_LIMIT .....+7.5%
- VOUT_MAX.....+7.5%
- VOUT_MARGIN_HIGH .....+5%
- VOUT_MARGIN_LOW.....–5%
- VOUT_UV_WARN_LIMIT ..... –6.5%
- VOUT_UV_FAULT_LIMIT ..... –7%

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Refer to Table 3 to set the output voltage using the VOUT_CFG*n* pins. 1% resistors must be used to assure proper operation. If VOUT is seven volts or lower, low range is used. When VOUT is set using the VOUTn_CFG pins, the part will turn on the rail modifying the OPERATION command, if required, to respond to PMBus commands.

Table 3. VOUT_CFG*n*

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	V_{OUT} (V)	ON/OFF
0 or Open	Open	EEPROM	EEPROM
10	23.2	12.0	ON
10	15.8	8.0	ON
16.2	20.5	7.0	ON
16.2	17.4	6.0	ON
20	17.8	5.0	ON
20	15	3.3	ON
20	12.7	2.5	ON
20	11	1.8	ON
24.9	11.3	1.5	ON
24.9	9.09	1.2	ON
24.9	7.32	1.1	ON
24.9	5.76	1.0	ON
24.9	4.32	0.9	ON
30.1	3.57	0.75	ON
30.1	1.96	0.65	ON
Open	0	EEPROM	OFF

Frequency Selection

The PWM switching frequency is set according to Table 4. The SYNC pins must be shared in poly-phase configurations where multiple LTC3886s or multiple LTC3886s and LTC3870s are used to produce the output. If the configuration is not PolyPhase the SYNC pins do not have to be shared. If the SYNC pins are shared between LTC3886s only one SYNC pin should be enabled, all other SYNC pins should be disabled. A pull-up resistor to V_{DD33} is required on the SYNC pin.

For example in a 4-phase configuration clocked at 250kHz, all of the LTC3886s must be set to the desired frequency and phase and one LTC3886 should be set to the desired frequency with the SYNC pin disabled. All phasing is with respect to the falling edge of SYNC.

For LTC3886 chip 1, set the frequency to 250kHz with 90° and 270° phase shift with the SYNC pin enabled:

Frequency: R_{TOP} = 24.9kΩ and R_{BOT} = 11.3kΩ

Phase: R_{TOP} = 30.1kΩ and R_{BOT} = 1.96kΩ

For LTC3886 chip 2, set the frequency to 250kHz with 0° and 180° phase shift and the SYNC pin disabled:

Frequency: R_{TOP} = 24.9kΩ and R_{BOT} = 11.3kΩ

Phase: R_{TOP} = 24.9kΩ and R_{BOT} = 11.3kΩ

All configurations in frequency and phase can be achieved using the FREQ_CFG and PHAS_CFG pins. In the above application, if the SYNC pin connection is lost from chip 1, chip 2 will internally detect the frequency as missing and continue switching at 250kHz. However, because the SYNC pin is disconnected between the chips, the output voltage ripple will likely be higher than desired. Bit 10 of MFR_PADS will assert low on chip 2 indicating chip 2 is providing its own internal oscillator when it is expecting an external SYNC input.

Table 4. FREQ_CFG Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	SWITCHING FREQUENCY (kHz)
0 or Open	Open	EEPROM
10	23.2	EEPROM
10	15.8	750
16.2	20.5	650
16.2	17.4	575
20	17.8	500
20	15	425
20	12.7	350
20	11	300
24.9	11.3	250
24.9	9.09	225
24.9	7.32	200
24.9	5.76	175
24.9	4.32	150
30.1	3.57	125
30.1	1.96	100
Open	0	External SYNC Only

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Phase Selection

The phase of the channels with respect to the falling edge of SYNC is set using the values in Table 5.

Table 5. PHAS_CFG Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	θ_{SYNC} TO θ_0	θ_{SYNC} TO θ_1	SYNC OUTPUT
0 or Open	Open	EEPROM	EEPROM	EEPROM
10	23.2	EEPROM	EEPROM	EEPROM
10	15.8	EEPROM	EEPROM	EEPROM
16.2	20.5	120°	300°	DISABLED
16.2	17.4	60°	240°	
20	12.7	120°	240°	
20	15	0°	120°	
20	12.7	0°	240°	
20	11	90°	270°	
24.9	11.3	0°	180°	
24.9	9.09	120°	300°	ENABLED
24.9	7.32	60°	240°	
24.9	5.76	120°	240°	
24.9	4.32	0°	120°	
30.1	3.57	0°	240°	
30.1	1.96	90°	270°	
Open	0	0°	180°	

Address Selection Using RCONFIG

The LTC3886 address is selected based on the programming of the two configuration pins ASEL0 and ASEL1 according to Table 6. ASEL0 programs the bottom four bits of the device address for the LTC3886, and ASEL1 programs the three most-significant bits. Either portion of the address can also be retrieved from the MFR_ADDRESS value in EEPROM. If both pins are left open, the full 7-bit MFR_ADDRESS value stored in EEPROM is used to determine the device address. The LTC3886 always responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS should not be set to either of these values because these are global addresses and all parts will respond to them.

Table 6. ASEL*n* Resistor Programming

		ASEL1		ASEL0	
		LTC3886 DEVICE ADDRESS BITS[6:4]		LTC3886 DEVICE ADDRESS BITS[3:0]	
R_{TOP} (kΩ)	R_{BOT} (kΩ)	BINARY	HEX	BINARY	HEX
0 or Open	Open	EEPROM		EEPROM	
10	23.2			1111	F
10	15.8			1110	E
16.2	20.5			1101	D
16.2	17.4			1100	C
20	17.8			1011	B
20	15			1010	A
20	12.7			1001	9
20	11			1000	8
24.9	11.3	111	7	0111	7
24.9	9.09	110	6	0110	6
24.9	7.32	101	5	0101	5
24.9	5.76	100	4	0100	4
24.9	4.32	011	3	0011	3
30.1	3.57	010	2	0010	2
30.1	1.96	001	1	0001	1
Open	0	000	0	0000	0

EFFICIENCY CONSIDERATIONS

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3886 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

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1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. Supplying the $INTV_{CC}$ current from the $EXTV_{CC}$ pin with an external supply will reduce the V_{IN} current required to a minimum.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor and current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 10m\Omega$, $R_L = 10m\Omega$, $R_{SENSE} = 5m\Omega$, then the total resistance is $25m\Omega$. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = $(1.7)\ V_{IN}^2\ I_{O(MAX)}\ C_{RSS}\ f$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of $20m\Omega$ to $50m\Omega$ of ESR. The LTC3886 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

PROGRAMMABLE LOOP COMPENSATION

The LTC3886 offers programmable loop compensation to optimize the transient response without any hardware change. As shown in Figure 35, the error amplifier gain g_m varies from 1.0mmho to 5.73mmho, and the compensation resistor R_{TH} varies from $0k\Omega$ to $62k\Omega$ inside the controller. Two compensation capacitors, C_{TH} and C_{THP}, are required in the design and the typical ratio between C_{TH} and C_{THP} is 10.

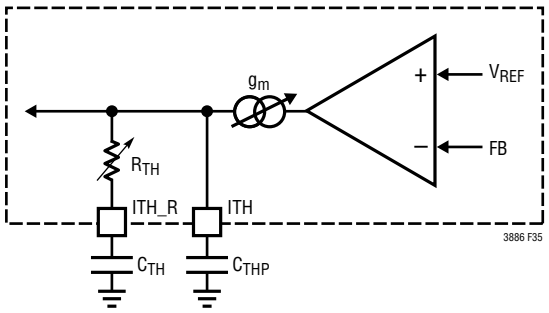

Figure 35. Programmable Loop Compensation

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By adjusting the g_m and R_{TH} only, the LTC3886 can provide a flexible type II compensation network to optimize the loop over a wide range of output capacitors. Adjusting the g_m will change the gain of the compensation over the whole frequency range without moving the pole and zero location, as shown in Figure 36.

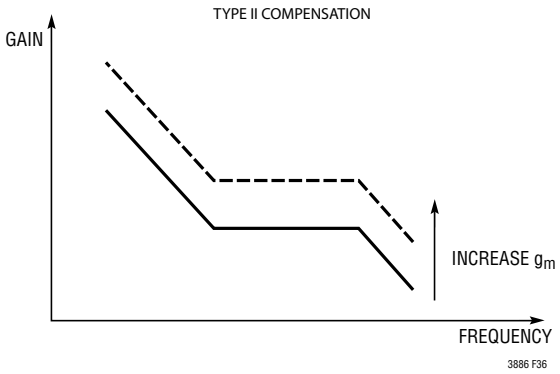

Figure 36. Error Amp g_m Adjust

Adjusting the R_{TH} will change the pole and zero location, as shown in Figure 37. It is recommended that the user determines the appropriate value for the g_m and R_{TH} using the LTpowerCAD® tool.

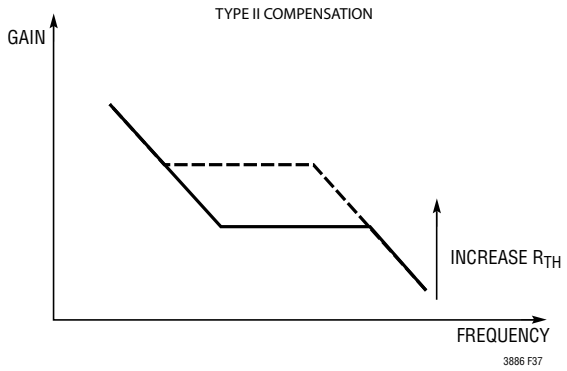

Figure 37. R_{ITH} Adjust

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{THR} external capacitor shown in the Typical Application circuit will provide an adequate starting point for most applications. The programmable parameters that affect loop gain are the voltage range, bit[1] of the MFR_PWM_CONFIG_LTC3886 command, the current range, bit 7 of the MFR_PWM_MODE_LTC3886 command, the gm of the PWM channel amplifier, bits [7:5] of MFR_PWM_COMP, and the internal R_{ITH} compensation resistor, bits[4:0] of MFR_PWM_COMP. Be sure to establish these settings prior to compensation calculation.

The I_{TH} series internal R_{ITH} - external C_C filter sets the dominant pole-zero loop compensation. The internal R_{ITH} value can be modified (from 0Ω to 62kΩ) using bits[4:0] of the MFR_PWM_COMP command. Adjust the value of R_{ITH} to optimize transient response once the final PC layout is done and the particular C_C filter capacitor and output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET with a resistor to ground directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to

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produce a load step. The MOSFET + R_{SERIES} will produce output currents approximately equal to V_{OUT}/R_{SERIES}. R_{SERIES} values from 0.1Ω to 2Ω are valid depending on the current limit settings and the programmed output voltage. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_{ITH} and the bandwidth of the loop will be increased by decreasing C_C. If R_{ITH} is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The gain of the loop will be proportional to the transconductance of the error amplifier which is set using bits[7:5] of the MFR_PWM_COMP command. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PolyPhase CONFIGURATION

When configuring a PolyPhase rail with multiple LTC3886s, the user must share the SYNC, ITH, SHARE_CLK, $\overline{FAULT}n$, PGOOD*n* and $\overline{ALERT}$ pins of both parts. Be sure to use pull-up resistors on $\overline{FAULT}n$, PGOOD*n*, SYNC, SHARE_CLK and $\overline{ALERT}$. One of the LTC3886's SYNC pin must be set to the desired switching frequency, and all other FREQUENCY_SWITCH commands must be set to External Clock. If an external oscillator is provided, set the FREQUENCY_SWITCH command to External Clock for all LTC3886s. The relative phasing of all the channels should be spaced equally. The MFR_RAIL_ADDRESS of all the devices should be set to the same value.

When connecting a PolyPhase rail with LTC3886s, connect the V_{IN} pins of the LTC3886s directly back to the supply voltage through the V_{IN} pin filter networks.

PC BOARD LAYOUT CHECKLIST

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 38. Figure 39 illustrates the current waveforms present in the various branches of the synchronous regulator operating in the continuous mode. Check the following in your layout:

1. Is the top N-channel MOSFET, M1, located within 1cm of C_{IN}?
2. Are signal ground and power ground kept separate? The ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals.
3. The I_{TH} trace should be as short as possible.
4. The loop formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths.
5. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described in item 4.
6. Are the I_{SENSE}^+ and I_{SENSE}^- leads routed together with minimum PC trace spacing? The filter capacitor between I_{SENSE}^+ and I_{SENSE}^- should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor or inductor, whichever is used for current sensing.

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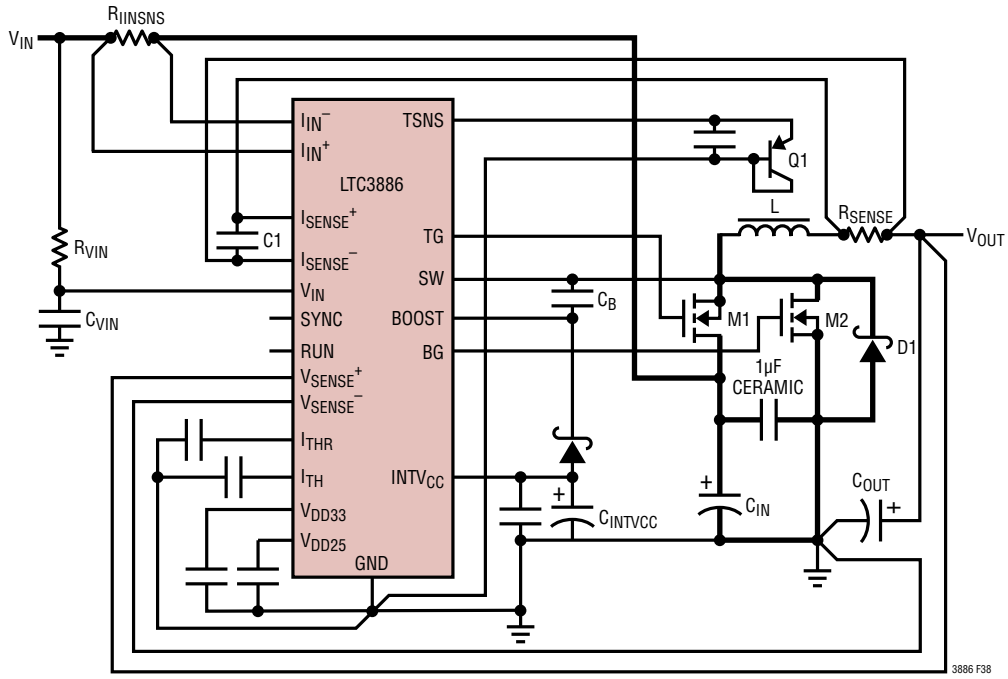

Figure 38. Recommended Printed Circuit Layout Diagram, Single Phase Shown

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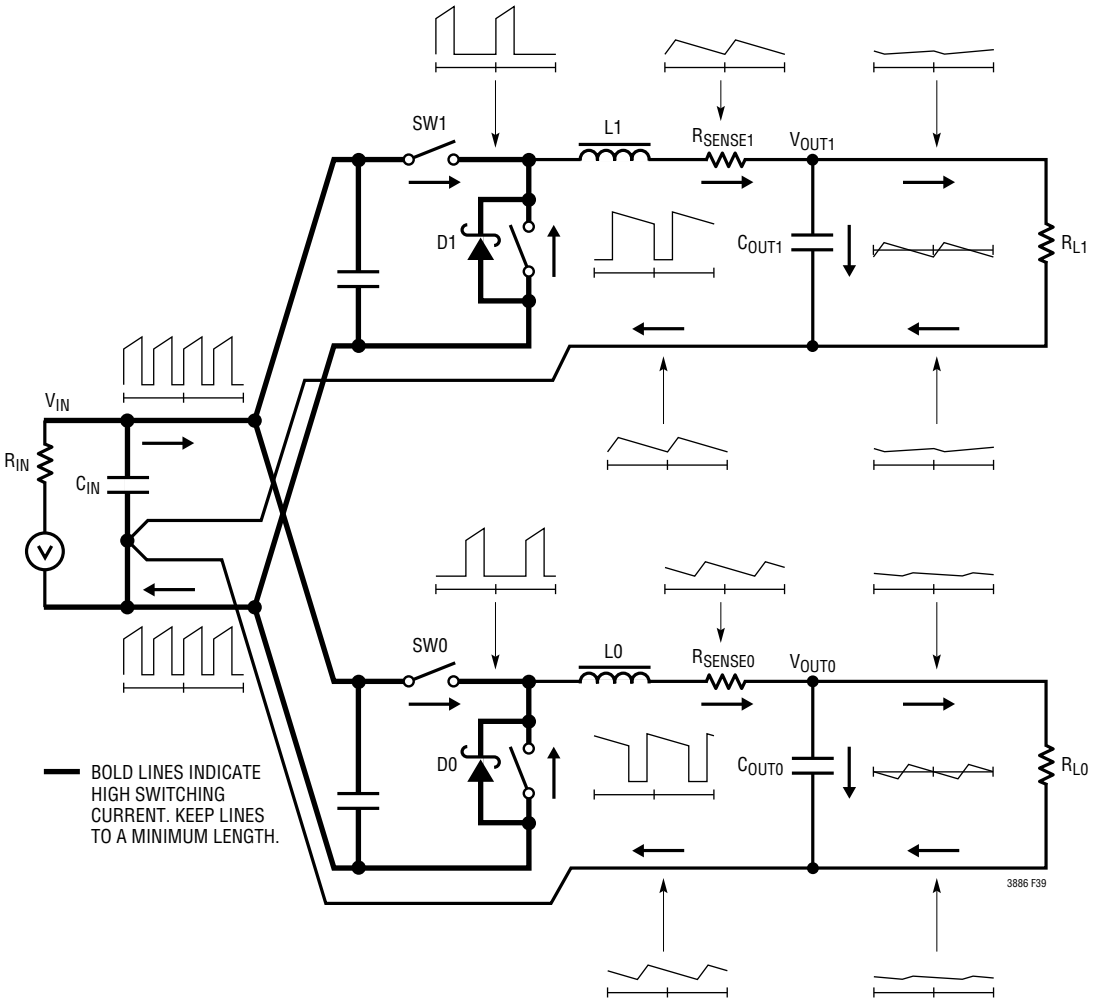

Figure 39. Branch Current Waveforms

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7. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET driver current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially.
8. Keep the switching nodes (SW*n*), top gate nodes (TG*n*), and boost nodes (BOOST*n*) away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3886 and occupy minimum PC trace area. If DCR sensing is used, place the top resistor (Figure 25a, R1) close to the switching node.
9. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ and $EXTV_{CC}$ decoupling capacitors, the bottom of the voltage feedback resistive divider and the GND pin of the IC.
10. Are the I_{IN}^+ and I_{IN}^- pins Kelvin connected to the $R_{SENSEIN}$ sense resistor? This will prevent the PCB trace resistance from causing errors in the input current measurement. These traces should be as short as possible and routed away from any noisy nodes such as the switching or boost nodes.
11. Is the V_{IN} filter Kelvin connected to the input side of the $R_{SENSEIN}$ resistor? This can help improve the noise performance of the input current sense amplifier by reducing the voltage transients between the amplifier inputs and amplifier supply caused by the discontinuous power stage current.

PC BOARD LAYOUT DEBUGGING

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW*n* pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST*n*, SW*n*, TG*n*, and possibly BG*n* connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

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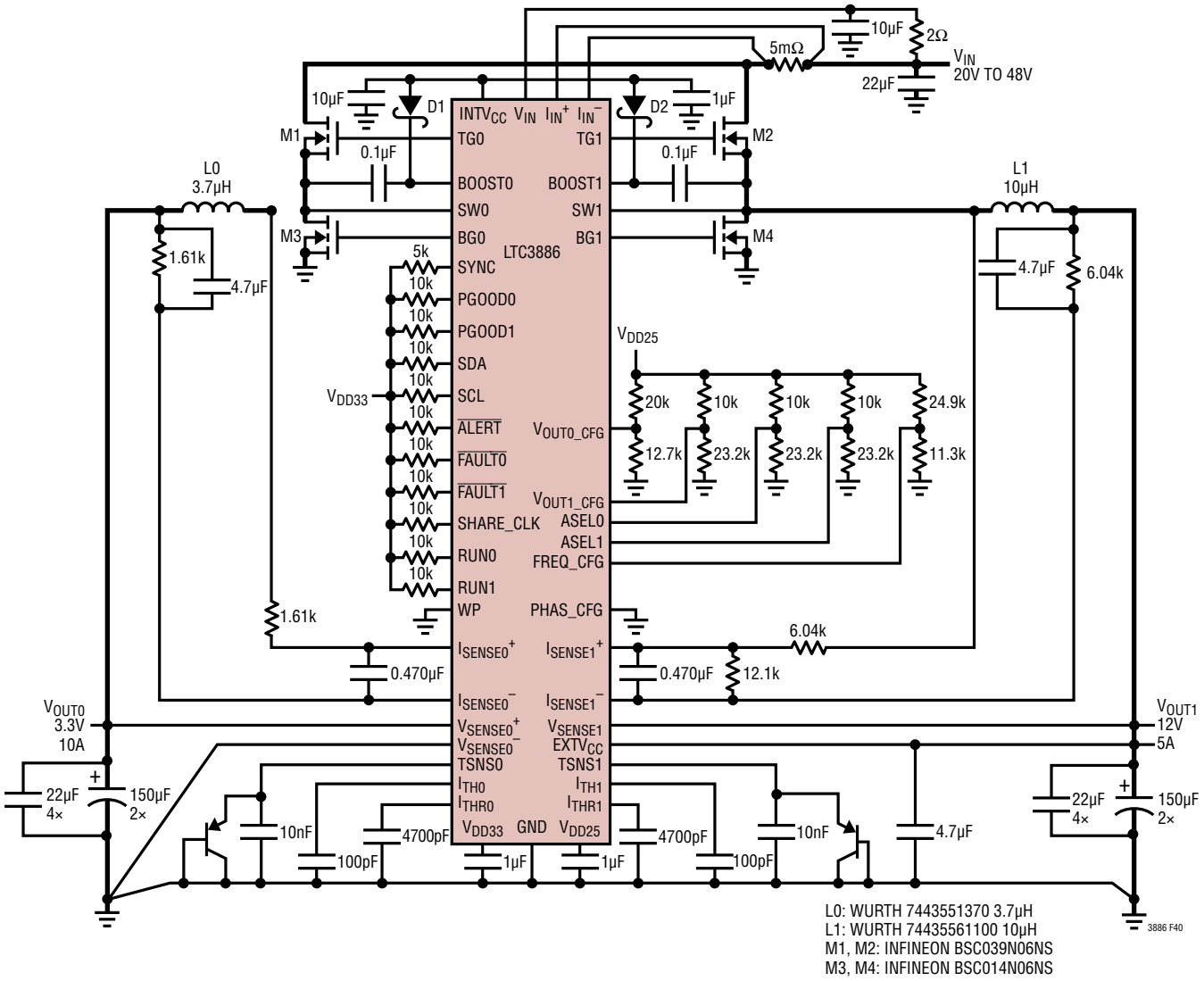

L0: WURTH 7443551370 3.7µH
L1: WURTH 74435561100 10µH
M1, M2: INFINEON BSC039N06NS
M3, M4: INFINEON BSC014N06NS

Figure 40. High Efficiency Dual 250kHz 12V/3.3V Step-Down Converter

DESIGN EXAMPLE

As a design example for a medium current regulator, assume V_{IN} = 48V nominal, V_{IN} = 55V maximum, V_{OUT0} = 3.3V, V_{OUT1} = 12V, $I_{MAX0,1}$ = 10A and f = 250kHz (see Figure 40).

The regulated outputs are established by the VOUT_ COMMAND stored in EEPROM or placing the following resistor divider between V_{DD25} the V_{OUTn_CFG} pin and GND:

1. V_{OUT0_CFG}, R_{TOP} = 20k, R_{BOTTOM} = 12.7k
2. V_{OUT1_CFG}, R_{TOP} = 10k, R_{BOTTOM} = 23.2k

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The frequency and phase are set by EEPROM or by setting the resistor dividers between V_{DD25} and GND.

1. FREQ_CFG, R_{TOP} = 24.9k, R_{BOTTOM} = 11.3k
2. PHAS_CFG, R_{TOP} = Open, R_{BOTTOM} = 0

The address is set to XF where X is the MSB stored in EEPROM.

The following parameters are set as a percentage of the output voltage if the resistor configuration pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT.....+10%
- VOUT_OV_WARN_LIMIT.....+7.5%
- VOUT_MAX.....+7.5%
- VOUT_MARGIN_HIGH.....+5%
- VOUT_MARGIN_LOW.....–5%
- VOUT_UV_WARN_LIMIT.....–6.5%
- VOUT_UV_FAULT_LIMIT.....–7%

All other user defined parameters must be programmed into the EEPROM. The GUI can be utilized to quickly set up the part with the desired operating parameters.

The inductance values are based on a 35% maximum ripple current assumption (3.5A). The highest value of ripple current occurs at the maximum input voltage:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Channel 0 will require 3.5µH and channel 1 will require 10.7µH. The nearest standard values are 3.7µH and 10µH respectively. At the nominal input the ripple will be:

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L}\left[1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right]$$

Channel 0 will have 3.32A (33%) ripple, and channel 1 will have 3.6A (36%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current or 11.6A for channel 0 and 11.8A for channel 1. The minimum on time occurs on channel 0 at the maximum V_{IN}, and should not be less than 90ns:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f} = \frac{3.3V}{55V(250kHz)} = 240ns$$

The Würth 7443551370 3.7µH (4.9mΩ DCR_{TYP} at 25°C) channel 0 and the Wurth 744355611000 10µH (7mΩ DCR_{TYP} at 25°C) channel 1 are the chosen inductors.

$$(R1+R3) = \frac{2 \bullet L}{(DCR \text{ at } 25°C) \bullet C1} = \frac{2 \bullet 3.7\mu H}{4.9m\Omega \bullet 0.47\mu F}$$

R1 = R3 = 1.61kΩ.

$$IOUT_CAL_GAIN = 4.9m\Omega$$

The maximum power loss in R1 is related to the duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS} \bullet R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

$$= \frac{(55 - 3.3) \bullet 3.3}{3.05k} = 55.9mW$$

The respective values for channel 1 are C1 = 0.47µF, R1 = R3 = 6.08kΩ, R2 = 12.1kΩ, IOUT_CAL_GAIN = 3.45mΩ and P_{LOSS}R1 = 84.9mW.

The current limit will be set 20% higher than the peak value to assure variation in components and noise in the system do not limit the average current.

V_{ILIMIT} = I_{PEAK} • $R_{DCR(MAX)}$ = 1.2 •11.3A •3.5mΩ = 47.46mV

The closest V_{ILIMIT} setting is 42.9mV or 48.2mV. The values are entered with the IOUT_OC_FAULT_LIMIT command. Based on expected variation and measurement in the lab across the sense capacitor the user can determine the optimal setting. For channel 1 the V_{ILIMIT} value is 49.56mV. The closest value is 53.6mV.

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The power dissipation on the topside MOSFET can be easily estimated. Choose an INFINEON BSC039N06NS topside MOSFET. $R_{DS(ON)}$ = 3.9mΩ, C_{MILLER} = 75pF. At maximum input voltage with T estimated = 50°C and a bottom side INFINEON BSC014N06NS MOSFET, $R_{DS(ON)}$ = 1.45mΩ:

$$P_{MAIN} = \frac{3.3V}{55V} \bullet (11.6)^2 \bullet \left[1+(0.005)(50°C-25°C)\right] \bullet 0.0039\Omega + (55V)^2(5.8A) \bullet \left(\frac{1}{5-2.8}+\frac{1}{2.8}\right)(59pF)(250kHz) = 0.245W$$

The loss in the bottom side MOSFET is:

$$P_{SYNC} = \frac{(55V-3.3V)}{55V} \bullet (11.6A)^2 \bullet \left[1+(0.005)(50°C-25°C)\right] \bullet 0.00145\Omega = 0.206W$$

Both MOSFETS have I^2R losses while the P_{MAIN} equation includes an additional term for transition losses, which are highest at high input voltages.

C_{IN} is chosen for an RMS current rating of:

$$I_{RMS} = \frac{11.8}{55}\left[(3.3) \bullet (55-3.3)\right]^{1/2} = 2.8A$$

at temperature. C_{OUT} is chosen with an ESR of 0.01Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is

$V_{ORIPPLE} = R(\Delta I_L) = 0.01\Omega \bullet 3.6A = 36mV.$

ADDITIONAL DESIGN CHECKS

Tie FAULT0 and FAULT1 together and pull up to V_{DD33} with a 10k resistor.

Tie RUN0 and RUN1 together and pull up to V_{DD33} with a 10k resistor.

If there are other ADI PSM parts, connect the RUN pins between chips and connect the FAULT pins between chips.

Be sure all PMBus pins have resistor pull-up to V_{DD33} and connect these inputs across all ADI PSM parts in the application.

Tie SHARE_CLK high with a 10k resistor to V_{DD33} and share between all ADI PSM parts in the application.

Be sure a unique address for each chip can be decoded with the ASEL0 and ASEL1 pins. Refer to Table 6.

For maximum flexibility, allow board space for R_{TOP} and R_{BOTTOM} for any parameter that is set with resistors such as ASEL0 and ASEL1.

CONNECTING THE USB TO I²C/SMBus/PMBus ADAPTER TO THE LTC3886 IN SYSTEM

The ADI USB to I^2C/SMBus/PMBus adapter (DC1613A or equivalent) can be interfaced to the LTC3886 on the user's board for programming, telemetry and system debug. The adapter, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status commands and the fault log. The final configuration can be quickly developed and stored to the LTC3886 EEPROM.

Figure 41 illustrates the application schematic for powering, programming and communication with one or more LTC3886s via the ADI I^2C/SMBus/PMBus adapter regardless of whether or not system power is present. If system power is not present, the adapter will power the LTC3886 through the V_{DD33} supply pin. To initialize the part when V_{IN} is not applied and the V_{DD33} pin is powered use global address 0x5B command 0xBD data 0x2B followed by address 0x5B command 0xBD data 0xC4. The LTC3886 will now communicate normally, and the project file can be updated. To write the updated project file to the EEPROM issue a STORE_USER_ALL command. When VIN is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

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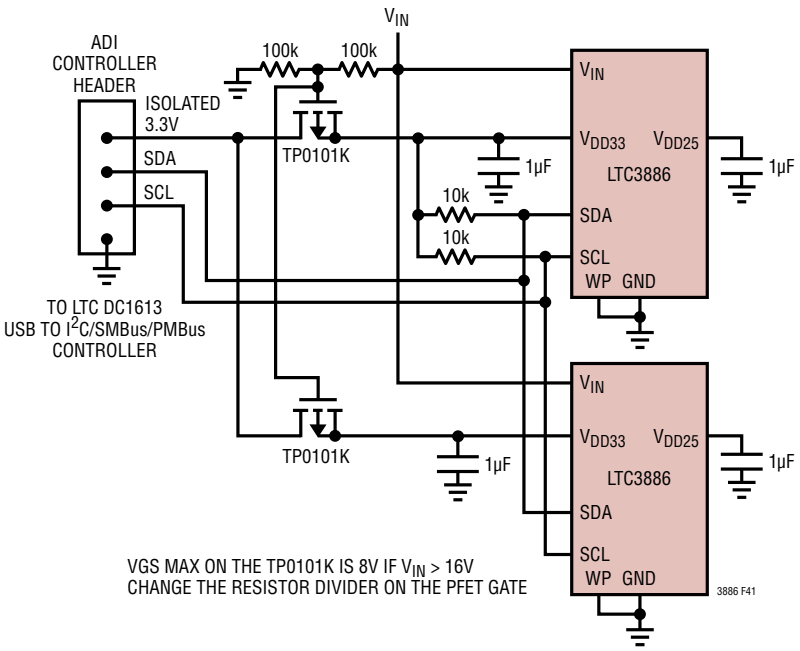

Figure 41. ADI Controller Connection

Because of the adapter's limited current sourcing capability, only the LTC3886s, their associated pull-up resistors and the I^2C pull-up resistors should be powered from the ORed 3.3V supply. In addition any device sharing the I^2C bus connections with the LTC3886 should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication in the absence of system power. If V_{IN} is applied the DC1613A will not supply power to the LTC3886s on the board. It is recommended the RUN*n* pins be held low or no voltage configuration resistors inserted to avoid providing power to the load until the part is fully configured.

The LTC3886 is fully isolated from the host PC's ground by the DC1613A. The 3.3V from the adapter and the LTC3886 V_{DD33} pin must be driven to each LTC3886 with a separate PFET. If V_{IN} is not applied, the V_{DD33} pins can be in parallel because the on-chip LDO is off. The DC1613A's 3.3V current limit is 100mA but typical V_{DD33} currents are under 15mA. The V_{DD33} does back drive the $INTV_{CC}$/$EXTV_{CC}$ pins. Normally this is not an issue if V_{IN} is open.

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER

LTpowerPlay is a powerful Windows-based development environment that supports Analog Devices digital power ICs including the LTC3886. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Analog Devices ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build multiple IC configuration files that can be saved and re-loaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bringing up rails. LTpowerPlay utilizes Analog Devices' USB-to-I^2C/SMBus/PMBus adapter to communication with one of the many potential targets including the DC2155A demo board, or a customer target system. The software also provides an automatic update feature to keep the revision current with the latest set of device drivers and documentation. A great deal of context sensitive help is available with LTpowerPlay along with several tutorial demos. Complete information is available at:

LTpowerPlay

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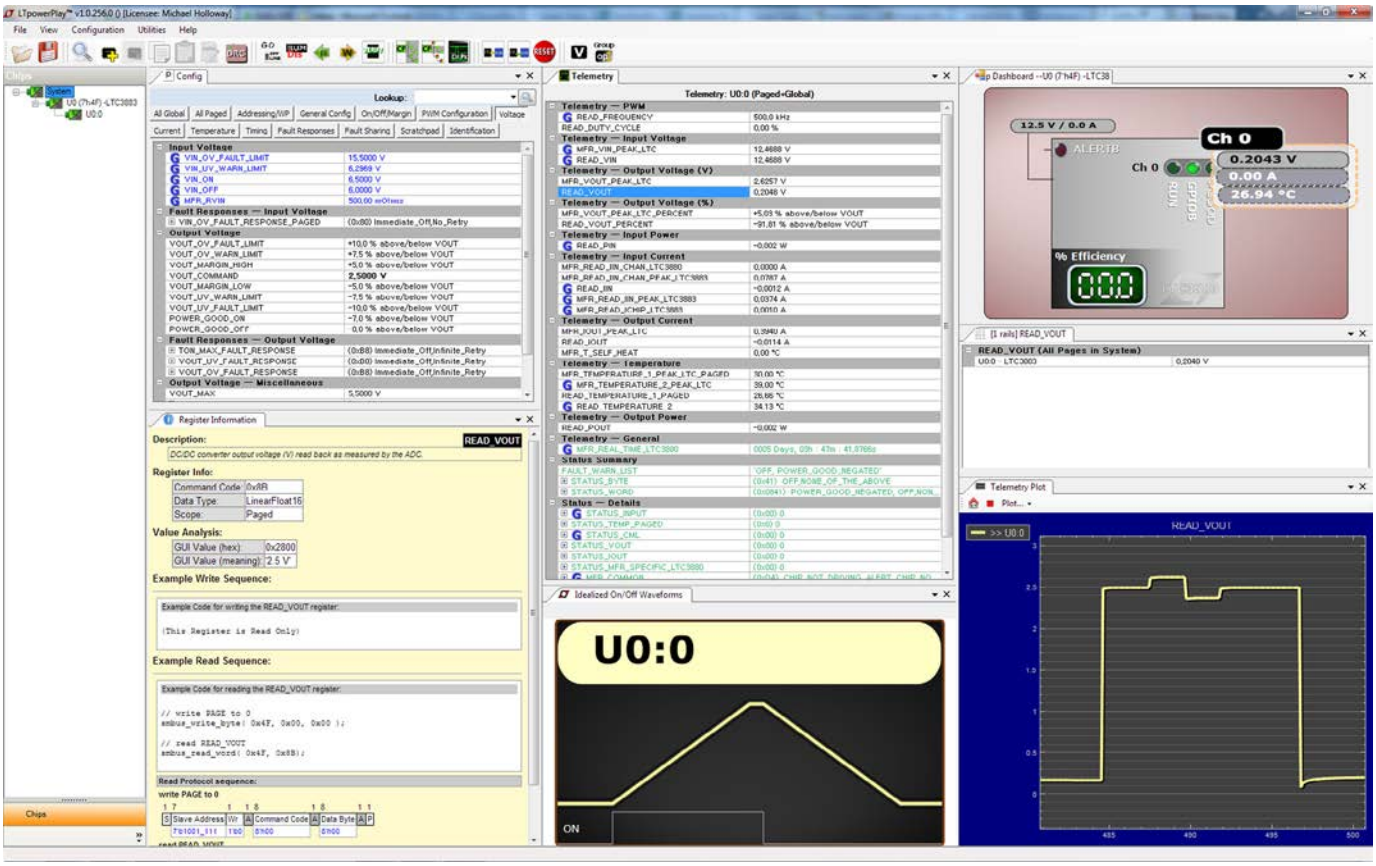

Figure 42. LTpowerPlay Screen Shot

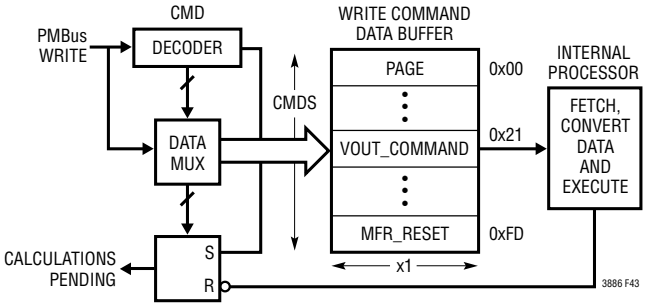

Figure 43. Write Command Data Processing

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTC3886 has a one deep buffer to hold the last data written for each supported command prior to processing as shown in Figure 43; Write Command Data Processing. When the part receives a new command from the bus, it copies the data into the Write Command Data Buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format so that it can be executed.

Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data to the Write Command Data Buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing.

Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long

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```
// wait until chip is not busy
do
{
        mfrCommonValue = PMBUS_READ_BYTE(0xEF);
        partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)

// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

Figure 44. Example of a Command Write of VOUT_COMMAND

relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process via bit 5 of MFR_COMMON ('calculations not pending'). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 44 which ensures that commands are processed in order while simplifying error handling routines.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL_LTC3886. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

PMBus busy protocols are well accepted standards, but can make writing system level software somewhat complex. The part provides three 'hand shaking' status bits which reduce complexity while enabling robust system level communication.

The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON ('chip not busy'). When the part is busy specifically because it is in a transitional VOUT state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.) it will clear bit 4 of MFR_COMMON ('output not in transition'). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON ('calculations not pending'). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault/$\overline{\text{ALERT}}$ notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 44.

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted $\overline{\text{ALERT}}$ notification. A simple way to achieve this is to create a SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutine. The above polling mechanism allows your software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases please refer to the application notes AN135 and AN152.

When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus master that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults is required.

The LTC3886 is not recommended in applications with bus speeds in excess of 400kHz.

PMBus COMMAND DETAILS

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00
PAGE_PLUS_WRITE	0x05	Write a supported command directly to a PWM channel.	W Block	N				
PAGE_PLUS_READ	0x06	Read a supported command directly from a PWM channel.	Block R/W	N				
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80

PAGE

The PAGE command provides the ability to configure, control and monitor both PWM channels through only one physical address, either the MFR_ADDRESS or GLOBAL device address. Each PAGE contains the operating commands for one PWM channel.

Pages 0x00 and 0x01 correspond to Channel 0 and Channel 1, respectively, in this device.

Setting PAGE to 0xFF applies any following paged commands to both outputs. Reading from the device with PAGE set to 0xFF is not recommended.

This command has one data byte.

PAGE_PLUS_WRITE

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command, and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command that has two data bytes is shown in Figure 45.

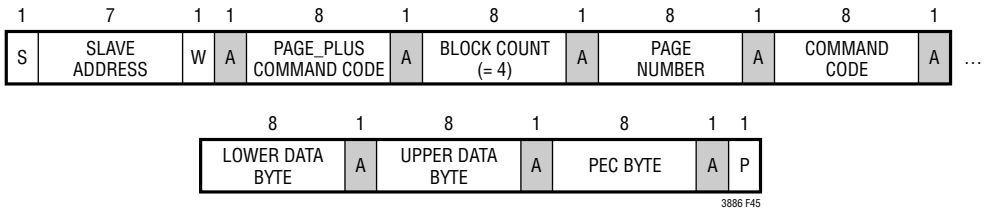

Figure 45. Example of PAGE_PLUS_WRITE

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PAGE_PLUS_READ

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command, and then read the data returned by the command, all in one communication packet .

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses Block Write-Block Read Process Call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 46.

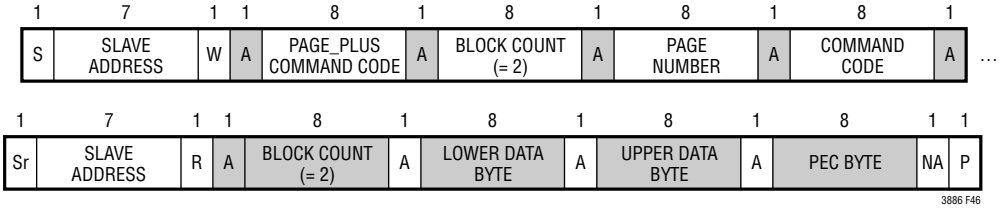

Figure 46. Example of PAGE_PLUS_READ

Note: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTC3886 will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the LTC3886 device. This command does not indicate the status of the WP pin which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command.

BYTE	MEANING
0x80	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL command.
0x40	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION and CLEAR_FAULTS command. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x20	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x10	Reserved, must be 0
0x08	Reserved, must be 0
0x04	Reserved, must be 0
0x02	Reserved, must be 0
0x01	Reserved, must be 0

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When WRITE_PROTECT is set to 0x00, writes to all commands are enabled.

If WP pin is high, PAGE, OPERATION, MFR_CLEAR_PEAKS, MFR_EE_UNLOCK, WRITE_PROTECT and CLEAR_FAULTS commands are supported. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.

MFR_ADDRESS

The MFR_ADDRESS command byte sets the 7 bits of the PMBus slave address for this device.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If RCONFIG is set to ignore, the ASEL0 and ASEL1 pins are still used to determine the LSB and MSB, respectively, of the channel address. If the ASEL0 and ASEL1 pins are both open, the LTC3886 will use the address value stored in EEPROM. If the ASEL0 pin is open, the LTC3886 will use the lower 4 bits of the MFR_ADDRESS value stored in EEPROM to construct the effective address of the part. If the ASEL1 pin is open, the LTC3886 will use the upper 3 bits of the MFR_ADDRESS value stored in EEPROM to construct the effective address of the part.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be common to all devices attached to a single power supply rail.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTC3886 will detect bus contention and may set a CML communications fault.

Setting this command to a value of 0x80 disables rail device addressing for the channel.

This command has one data byte.

GENERAL CONFIGURATION COMMANDS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_CHAN_CONFIG_LTC3886	0xD0	LTC3886 Channel specific configuration bits. LTC3886-1 Channel specific configuration bits.	R/W Byte R/W Byte	Y Y	Reg Reg		Y Y	0x1D 0x3D
MFR_CONFIG_ALL_LTC3886	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21

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MFR_CHAN_CONFIG_LTC3886

General purpose configuration command common to multiple ADI products.

BIT	MEANING
7	Reserved
6	Reserved
5	LTC3886: Reserved LTC3886-1: Asserting this bit enables the MFR_VOFF_THRESHOLD sequence off feature to discharge large output capacitors.
4	Disable RUN Low. When asserted the RUN pin is not pulsed low if commanded OFF.
3	Short Cycle. When asserted the output will immediate off if commanded ON while waiting for TOFF_DELAY or TOFF_FALL. TOFF_MIN of 120ms is honored then the part will command ON.
2	SHARE_CLOCK control. If SHARE_CLOCK is held low, the output is disabled.
1	$\overline{\text{ALERT}}$ is not pulled low if $\overline{\text{FAULT}}$ is pulled low externally.
0	Disables the V_{OUT} decay value requirement for MFR_RETRY_TIME processing. When this bit is set to a 0, the output must decay to less than 12.5% of the programmed value(LTC3886), or below the MFR_VOFF_THRESHOLD value (LTC3886-1) before the PWM will restart. This applies to any action that turns off the PWM including a fault, an OFF/ON command, or a RUN pin transition from high to low. A TOFF_MAX warning status will not be generated when this bit is set to a 1.

This command has one data byte.

MFR_CONFIG_ALL_LTC3886

General purpose configuration command common to multiple ADI products.

BIT	MEANING
7	Enable Fault Logging
6	Ignore Resistor Configuration Pins
5	Disable CML Fault for Quick Command Message.
4	Disable SYNC output
3	Enable 255ms PMBus timeout
2	PMBus command writes require a valid Packet Error Checking, PEC, byte to be accepted.*
1	Enable the use of PMBus clock stretching
0	Execute CLEAR_FAULTS on rising edge of either RUN pin.

*PMBus command writes that have a valid PEC byte are always processed. PMBus command writes that have an invalid PEC byte are not processed and set a CML status fault.

This command has one data byte.

ON/OFF/MARGIN

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x40
MFR_RESET	0xFD	Commanded reset without requiring a power-down.	Send Byte	N				NA

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ON_OFF_CONFIG

The ON_OFF_CONFIG command specifies the combination of RUN*n* pin input state and PMBus commands needed to turn the PWM channel on and off.

Supported Values:

VALUE	MEANING
0x1F	OPERATION value and RUN*n* pin must both command the device to start/run. Device executes immediate off when commanded off.
0x1E	OPERATION value and RUN*n* pin must both command the device to start/run. Device uses TOFF_ command values when commanded off.
0x17	RUN*n* pin control with immediate off when commanded off. OPERATION on/off control ignored.
0x16	RUN*n* pin control using TOFF_ command values when commanded off. OPERATION on/off control ignored.

Note: A high on the RUN pin is always required to start power conversion. Power conversion will always stop with a low on RUN.

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault and the command will be ignored.

This command has one data byte.

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the RUN*n* pins. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOLTAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the RUN*n* pin instructs the device to change to another mode. If the part is stored in the MARGIN_LOW/HIGH state, the next RESET or POWER_ON cycle will ramp to that state. If the OPERATION command is modified, for example ON is changed to MARGIN_LOW, the output will move at a fixed slope set by the VOUT_TRANSITION_RATE. The default operation command is sequence off. If V_{IN} is applied to a part with factory default programming and the VOUT_CONFIG resistor configuration pins are not installed, the outputs will be commanded off.

The part defaults to the Sequence Off state.

This command has one data byte.

Supported Values:

VALUE	MEANING
0xA8	Margin high.
0x98	Margin low.
0x80	On (V_{OUT} back to nominal even if bit 3 of ON_OFF_CONFIG is not set).
0x40*	Soft off (with sequencing).
0x00*	Immediate off (no sequencing).

*Device does not respond to these commands if bit 3 of ON_OFF_CONFIG is not set.

Programming an unsupported OPERATION value will generate a CML fault and the command will be ignored.

This command has one data byte.

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MFR_RESET

This command provides a means to reset the LTC3886 from the serial bus. This forces the LTC3886 to turn off both PWM channels, load the operating memory from internal EEPROM, clear all faults and then perform a soft-start of both PWM channels, if enabled.

This write-only command has no data bytes.

PWM CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0x70
MFR_PWM_MODE_LTC3886	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC1
MFR_PWM_CONFIG_LTC3886	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	350 0xFABC

MFR_PWM_MODE_LTC3886

The MFR_PWM_MODE_LTC3886 command sets important PWM controls for each channel. Bits [0] and [6] may be changed when the addressed channel(s) is on,however the channel(s) must be turned off if any other bits are changed when the command is issued. The LTC3886 will issue a CML fault and ignore the command and its data if the channel is on and any bits other than [0] and [6] are changed.

The MFR_PWM_MODE_LTC3886 command allows the user to program the PWM controller to use discontinuous (pulse-skipping mode), or forced continuous conduction mode.

BIT	MEANING
7	Use High Range of I_{LIMIT}
0b	Low Current Range
1b	High Current Range
6	Enable Servo Mode
5	External temperature sense:
	0: ΔV_{BE} measurement.
	1: Direct voltage measurement.
[4:2]	Reserved
1	V_{OUT} Range
0b	The maximum output voltage is 13.2V
1b	The maximum output voltage is 7V
Bit[0]	Mode
0b	Discontinuous
1b	Forced Continuous

Bit [7] of this command determines if the part is in high range or low range of the IOUT_OC_FAULT_LIMIT command. Changing this bit value changes the PWM loop gain and compensation. This bit value cannot be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

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Bit [6] The LTC3886 will not servo while the part is OFF, ramping on or ramping off. When set to a one, the output servo is enabled. The output set point DAC will be slowly adjusted to minimize the difference between the READ_VOUT_ADC and the VOUT_COMMAND (or the appropriate margined value).

When Bit[5] is cleared, the LTC3886 computes temperature in °C from ΔV_{BE} measured by the ADC at the TSNS*n* pin as

$$T = (G \bullet \Delta V_{BE} \bullet q/(K \bullet \ln(16))) - 273.15 + O$$

When Bit[5] is set, the LTC3886 computes temperature in °C from TSNS*n* voltage measured by the ADC as

$$T = (G \bullet (1.35 - V_{TSNSn} + O)/4.3e\text{-}3) + 25$$

For both equations,

G = MFR_TEMP_1_GAIN $\bullet 2^{-14}$, and

O = MFR_TEMP_1_OFFSET

Bit[1] of this command determines if the part is in high range or low voltage range. Changing this bit value changes the PWM loop gain and compensation. This bit value cannot be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit[0] determines if the PWM mode of operation is discontinuous (pulse-skipping mode), or forced continuous conduction mode. This command has one data byte. Whenever the channel is ramping on, the PWM mode will be discontinuous, regardless of the value of this command.

MFR_PWM_COMP

The MFR_PWM_COMP command sets the gm of the PWM channel error amplifiers and the value of the internal R_{ITHn} compensation resistors. This command affects the loop gain of the PWM output which may require modifications to the external compensation network.

BIT	MEANING
BIT [7:5]	**EA_{gm} (mS)**
000b	1.00
001b	1.68
010b	2.35
011b	3.02
100b	3.69
101b	4.36
110b	5.04
111b	5.73
BIT [4:0]	**R_{ITH} (kΩ)**
00000b	0
00001b	0.25
00010b	0.5
00011b	0.75
00100b	1
00101b	1.25

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BIT	MEANING
00110b	1.5
00111b	1.75
01000b	2
01001b	2.5
01010b	3
01011b	3.5
01100b	4
01101b	4.5
01110b	5
01111b	5.5
10000b	6
10001b	7
10010b	8
10011b	9
10100b	11
10101b	13
10110b	15
10111b	17
11000b	20
11001b	24
11010b	28
11011b	32
11100b	38
11101b	46
11110b	54
11111b	62

This command has one data byte.

MFR_PWM_CONFIG_LTC3886

The MFR_PWM_CONFIG_LTC3886 command sets the switching frequency phase offset with respect to the falling edge of the SYNC signal. The part must be in the OFF state to process this command. Either the RUN pins must be low or the part must be commanded off. If either channel is in the RUN state and this command is written, the command will be NACK'd and a BUSY fault will be asserted.

BIT	MEANING
7	Use VFBO
0b	Feedback nodes of both channels are independent.
1b	Channel 1 uses the Channel 0 feedback node.
[6:5]	Input current sense gain.
00b	2x gain. 0mV to 50mV range.
01b	4x gain. 0mV to 20mV range.
10b	8x gain. 0mV to 5mV range.
11b	

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BIT	MEANING	
4	Share Clock Enable : If this bit is 1, the SHARE_CLK pin will not be released until V_{IN} > VIN_ON. The SHARE_CLK pin will be pulled low when V_{IN} < VIN_OFF. If this bit is 0, the SHARE_CLK pin will not be pulled low when VIN < VIN_OFF except for the initial application of VIN.	
BIT [2:0]	**CHANNEL 0 (DEGREES)**	**CHANNEL 1 (DEGREES)**
000b	0	180
001b	90	270
010b	0	240
011b	0	120
100b	120	240
101b	60	240
110b	120	300

Do not assert Bit[7] except for use in a PolyPhase configuration. The $V_{SENSE}n^+n$, $I_{TH}n$, PGOOD*n* and RUN*n* must be shared between channels when this bit is asserted.

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the switching frequency, in kHz, of a PMBus device.

Supported Frequencies:

VALUE [15:0]	RESULTING FREQUENCY (TYP)
0x0000	External Oscillator
0xEB20	100kHz
0xFBE8	125kHz
0xF258	150kHz
0xF2BC	175kHz
0xF320	200kHz
0xF384	225kHz
0xF3E8	250kHz
0xFA58	300kHz
0xFABC	350kHz
0xFB52	425kHz
0xFBE8	500kHz
0x023F	575kHz
0x028A	650kHz
0x02EE	750kHz

The part must be in the OFF state to process this command. The RUN pin must be low or both channels must be commanded off. If the part is in the RUN state and this command is written, the command will be NACK'd and a BUSY fault will be asserted. When the part is commanded off and the frequency is changed, a PLL_UNLOCK status may be detected as the PLL locks onto the new frequency.

This command has two data bytes and is formatted in Linear_5s_11s format.

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VOLTAGE

Input Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	48.0 0xE300
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	6.3 0xCB26
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	6.5 0xCB40
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	6.0 0xCB00
MFR_RVIN	0xF7	The resistance value of the V_{IN} pin filter element in milliohms	R/W Word	N	L11	mΩ	Y	3000 0x12EE

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured by the ADC, in volts, that causes an input overvoltage fault.

This command has two data bytes in Linear_5s_11s format.

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of input voltage measured by the ADC that causes an input undervoltage warning. This warning is disabled until the input exceeds the input startup threshold value set by the VIN_ON command and the unit has been enabled. If the VIN_UV_WARN_LIMIT is then exceeded, the device:

- Sets the INPUT Bit Is the STATUS_WORD
- Sets the V_{IN} Undervoltage Warning Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

VIN_ON

The VIN_ON command sets the input voltage, in volts, at which the unit should start power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_OFF

The VIN_OFF command sets the input voltage, in volts, at which the unit should stop power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_RVIN

The MFR_RVIN command is used to set the resistance value of the V_{IN} pin filter element in milliohms. (See also READ_VIN). Set MFR_RVIN equal to 0 if no filter element is used.

This command has two data bytes and is formatted in Linear_5s_11s format.

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Output Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	14.0 0xE000
VOUT_OV_FAULT_ LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A
VOUT_OV_WARN_ LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33
VOUT_UV_WARN_ LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD
VOUT_UV_FAULT_ LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage.	R Word	Y	L16	V		14.0 0xE000
MFR_VOFF_THRESHOLD	0xDA	The PWM channel remains active until the ADC measures V_{OUT} below this value during sequencing OFF (LTC3886-1 only)	R/W Word	Y	L16	V	Y	0.1 0x019A

VOUT_MODE

The data byte for VOUT_MODE command, used for commanding and reading output voltage, consists of a 3-bit mode (only linear format is supported) and a 5-bit parameter representing the exponent used in output voltage Read/Write commands.

This read-only command has one data byte.

VOUT_MAX

The VOUT_MAX command sets an upper limit on any voltage, including VOUT_MARGIN_HIGH, the unit can command regardless of any other commands or combinations. The maximum allowed value of this command is 14 volts. The maximum output voltage the LTC3886 can produce is 14 volts including VOUT_MARGIN_HIGH. However, the VOUT_OV_FAULT_LIMIT can only be commanded as high as 14 volts.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured by the OV supervisor comparator at the sense pins, in volts, which causes an output overvoltage fault.

If the VOUT_OV_FAULT_LIMIT is modified and the part is in the RUN state, allow 10ms after the command is modified to assure the new value is being honored. The part indicates if it is busy making a calculation. Monitor bits 5 and 6 of MFR_COMMON. Either bit is low if the part is busy. If this wait time is not met, and the VOUT_COMMAND is modified

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above the old overvoltage limit, an OV condition might temporarily be detected resulting in undesirable behavior and possible damage to the switcher.

If VOUT_OV_FAULT_RESPONSE is set to OV_PULLDOWN or 0x00, the $\overline{\text{FAULT}}$ pin will not assert if VOUT_OV_FAULT is propagated. The LTC3886 will pull the TG low and assert the BG bit as soon as the overvoltage condition is detected.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage high warning. The MFR_VOUT_PEAK value will be used to determine if this limit has been exceeded.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This condition is detected by the ADC so the response time may be up to 120ms.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin High”. The value must be greater than VOUT_COMMAND. The maximum guaranteed value on VOUT_MARGIN_HIGH is 13.8 volts.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_COMMAND

The VOUT_COMMAND consists of two bytes and is used to set the output voltage, in volts. The maximum guaranteed value on VOUT is 13.2 volts.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin Low”. The value must be less than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

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VOUT_UV_WARN_LIMIT

The VOUT_UV_ WARN_LIMIT command reads the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage low warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Undervoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command reads the value of the output voltage measured by the UV supervisor comparator at the sense pins, in volts, which causes an output undervoltage fault.

This command has two data bytes and is formatted in Linear_16u format.

MFR_VOUT_MAX

The MFR_VOUT_MAX command is the maximum output voltage in volts for each channel, including VOUT_OV_FAULT_LIMIT. If the output voltages are set to high range (Bit 1 of MFR_PWM_MODE_LTC3886 set to a 0) MFR_VOUT_MAX is 14.0V. If the output voltage is set to low range (Bit 1 of MFR_PWM_MODE_LTC3886 set to a 1) the MFR_VOUT_MAX is 7.0V. Entering a VOUT_COMMAND value greater than this will result in a CML fault and the output voltage setting will be clamped to the maximum level. This will also result in Bit 3 VOUT_MAX_Warning in the STATUS_VOUT command being set.

This read only command has 2 data bytes and is formatted in Linear_16u format.

MFR_VOFF_THRESHOLD

The MFR_VOFF_THRESHOLD is used to determine the presence of residual voltage on the channel's PWM output. The presence of residual voltage is determine by the ADC and is defined by VOUT > MFR_VOFF_THRESHOLD. The function of the MFR_VOFF_THRESHOLD is dependent upon the value of the EnableMfrVoffThreshold bit (MFR_CHAN_CONFIG_LTC3886 bit #5).

This command has two data bytes and is formatted in Linear_16u format.

LTC3886-1 Only.

For EnableMfrVoffThreshold = 0

Residual Voltage on the channel's output will not prevent the PWM from shutting down. When the IgnoreResidualVoltage bit (i.e. MFR_CHAN_CONFIG_LTC3886 bit #0) is set to 0, residual Voltage is used to determine when a TOFF_MAX Warning conditions exist. Once residual voltage is no longer determined to be present, a TOFF_MAX Warning event is prevented from being generated. If the IgnoreResidualVoltage bit is set to 0, the channel will not attempt to turn-on until the channel output residual voltage is no longer present.

It is recommended that the value of the MFR_VOFF_THRESHOLD command is set to 12.5% of the programmed VOUT_COMMAND. It is also recommended that most users set the IgnoreResidualVoltage bit to a value of 1.

PMBus COMMAND DETAILS

For EnableMfrVoffThreshold = 1

Residual Voltage on the channel's output will prevent the PWM from shutting down. The ADC must measure at least 2 samples of VOUT < MFR_VOFF_THRESHOLD before the PWM will shut down. The ADC will not begin to look for the VOUT < MFR_VOFF_THRESHOLD until the PWM sequence off operation has reached the end of the TOFF_FALL sequencing. When the IgnoreResidualVoltage bit is set to 0, the MFR_VOFF_THRESHOLD is used to determine when TOFF_MAX Warning conditions exist. Only one VOUT < MFR_VOFF_THRESHOLD is required to consider residual voltage on the channel output to not be present and prevent a TOFF_MAX Warning event from being generated. The channel will not attempt to turn-on until the channel output residual voltage is not present when the IgnoreResidualVoltage bit is set to 0.

This command is not used during fault events. If a fault occurs, the PWM channel will immediately shutoff without attempting to discharge any energy storage remaining on the corresponding rail.

OUTPUT CURRENT AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R/W Word	Y	L11	mΩ	Y	1.8 0xBB9A
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF		Y	3900 0x0F3C
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	29.75 0xDBB8
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	20.0 0xDA80

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the resistance value of the current sense resistor in milliohms. (see also MFR_IOUT_CAL_GAIN_TC).

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C.

This command has two data bytes and is formatted in 16-bit 2's complement integer ppm. N = –32768 to 32767 • 10^{-6}. Nominal temperature is 27°C. The IOUT_CAL_GAIN is multiplied by:

[1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1-27)]. DCR sensing will have a typical value of 3900.

The IOUT_CAL_GAIN and MFR_IOUT_CAL_GAIN_TC impact all current parameters including: READ_IOUT, MFR_READ_IIN_CHAN, IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT.

PMBus COMMAND DETAILS

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the peak output current limit, in amperes. When the controller is in current limit, the overcurrent detector will indicate an overcurrent fault condition. The programmed overcurrent fault limit value is rounded up to the nearest one of the following set of discrete values:

25mV/IOUT_CAL_GAIN	Low Range (1.5x Nominal Loop Gain)
28.6mV/IOUT_CAL_GAIN	MFR_PWM_MODE_LTC3886 [7]=0
32.1mV/IOUT_CAL_GAIN	
35.7mV/IOUT_CAL_GAIN	
39.3mV/IOUT_CAL_GAIN	
42.9mV/IOUT_CAL_GAIN	
46.4mV/IOUT_CAL_GAIN	
50mV/IOUT_CAL_GAIN	
37.5mV/IOUT_CAL_GAIN	High Range (Nominal Loop Gain)
42.9mV/IOUT_CAL_GAIN	MFR_PWM_MODE_LTC3886 [7]=1
48.2mV/IOUT_CAL_GAIN	
53.6mV/IOUT_CAL_GAIN	
58.9mV/IOUT_CAL_GAIN	
64.3mV/IOUT_CAL_GAIN	
69.6mV/IOUT_CAL_GAIN	
75mV/IOUT_CAL_GAIN	

Note: This is the peak of the current waveform. The READ_IOUT command returns the average current. The peak output current limits are adjusted with temperature based on the MFR_IOUT_CAL_GAIN_TC using the equation:

Peak Current Limit = IOUT_CAL_GAIN • (1 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERTURE_1-27.0)).

The LTpowerPlay GUI automatically convert the voltages to currents.

The I_{OUT} range is set with bit 7 of the MFR_PWM_MODE_LTC3886 command.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

If the IOUT_OC_FAULT_LIMIT is exceeded, the device:

- Sets the IOUT bit in the STATUS word
- Sets the IOUT Overcurrent fault bit in the STATUS_IOUT
- Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

IOUT_OC_WARN_LIMIT

This command sets the value of the output current measured by the ADC that causes an output overcurrent warning in amperes. The READ_IOUT value will be used to determine if this limit has been exceeded.

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Warning bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format

Input Current and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	L11	mΩ	Y	5.000 0xCA80

MFR_IIN_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the resistance value of the input current sense resistor in milliohms. (see also READ_IIN).

This command has two data bytes and is formatted in Linear_5s_11s format.

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
IIN_OC_WARN_LIMIT	0x5D	Input overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280

IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC, in amperes, that causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the IIN Overcurrent Warning bit[1] in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TEMPERATURE

External Temperature Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	1.0 0x4000
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor.	R/W Word	Y	L11	C	Y	0.0 0x8000

MFR_TEMP_1_GAIN

The MFR_TEMP_1_GAIN command will modify the slope of the external temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in 16-bit 2's complement integer. The effective gain adjustment is $N \bullet 2^{-14}$. The nominal value is 1.

MFR_TEMP_1_OFFSET

The MFR_TEMP_1_OFFSET command will modify the offset of the external temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in Linear_5s_11s format.

External Temperature Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	100.0 0xEB20
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	85.0 0xEAA8
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–40.0 0xE580

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an overtemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This command has two data bytes and is formatted in Linear_5s_11s format.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an overtemperature warning. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

In response to the OT_WARN_LIMIT being exceeded, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Warning bit in the STATUS_TEMPERATURE command, and

PMBus COMMAND DETAILS

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

UT_FAULT_LIMIT

The UT_FAULT_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an undertemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

Note: If the temp sensors are not installed, the UT_FAULT_LIMIT can be set to –275°C and UT_FAULT_LIMIT response set to ignore to avoid $\overline{\text{ALERT}}$ being asserted.

This command has two data bytes and is formatted in Linear_5s_11s format.

TIMING

Timing—On Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	8.0 0xD200
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10.0 0xD280
VOUT_TRANSITION_RATE	0x27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xAA00

TON_DELAY

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. Values from 0ms to 83 seconds are valid. The resulting turn-on delay will have a typical delay of 270µs for TON_DELAY = 0 and an uncertainty of ±50µs for all values of TON_DELAY.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_RISE

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. Values from 0 to 1.3 seconds are valid. The part will be in discontinuous mode during TON_RISE events. If TON_RISE is less than 0.25ms, the LTC3886 digital slope will be bypassed and the output voltage transition will only be controlled by the analog performance of the PWM switcher. The number of steps in TON_RISE is equal to TON_RISE (in ms)/0.1ms with an uncertainty of ±0.1ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit, or output overcurrent limit.

PMBus COMMAND DETAILS

A data value of 0ms means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely. The maximum limit is 83 seconds.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOUT_TRANSITION_RATE

When a PMBus device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low) that causes the output voltage to change this command set the rate in V/ms at which the output voltage changes. This commanded rate of change does not apply when the unit is commanded on or off. The maximum allowed slope is 4V/ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

Timing—Off Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	8.0 0xD200
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5% (LTC3886), MFR_VOFF_THRESHOLD (LTC3886-1).	R/W Word	Y	L11	ms	Y	150 0xF258

TOFF_DELAY

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. Values from 0 to 83 seconds are valid. The resulting turn off delay will have a typical delay of 270µs for TOFF_DELAY = 0 and an uncertainty of ±50µs for all values of TOFF_DELAY. TOFF_DELAY is not applied when a fault event occurs

This command has two data bytes and is formatted in Linear_5s_11s format.

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. It is the ramp time of the V_{OUT} DAC. When the V_{OUT} DAC is zero, the PWM output will be set to high impedance state.

The part will maintain the mode of operation programmed. For defined TOFF_FALL times, the user should set the part to continuous conduction mode. Loading the max value indicates the part will ramp down at the slowest possible rate. The minimum supported fall time is 0.25ms. A value less than 0.25ms will result in a 0.25ms ramp. The maximum fall time is 1.3 seconds. The number of steps in TOFF_FALL is equal to TOFF_FALL (in ms)/0.1ms with an uncertainty of ±0.1ms.

In discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to turn off the output until a warning is asserted. The LTC3886 output is considered off when the V_{OUT} voltage is less than 12.5% of the programmed VOUT_COMMAND value. The LTC3886-1 output is considered off when the V_{OUT} voltage is less than the programmed MFR_VOFF_THRESHOLD value. The calculation begins after TOFF_FALL is complete. MFR_CHAN_CONFIG_LTC3886 bit #0 must be 0 for TOFF_MAX warning status messages to be generated.

A data value of 0ms means that there is no limit and that the unit can attempt to turn off the output voltage indefinitely. Other than 0, values from 120ms to 524 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

Precondition for Restart

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_RESTART_ DELAY	0xDC	Minimum time the RUN pin is held low by the LTC3886.	R/W Word	Y	L11	ms	Y	500 0xFBE8

MFR_RESTART_DELAY

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The minimum recommended value is 136ms.

Note: The restart delay is different than the retry delay. The restart delay pulls RUN low for the specified time, after which a standard start-up sequence is initiated. The minimum restart delay should be equal to TOFF_DELAY + TOFF_FALL + 136ms. Valid values are from 136ms to 65.52 seconds in 16ms increments. To assure a minimum off time, set the MFR_RESTART_DELAY 16ms longer than the desired time. The LTC3886 output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the IgnoreResidualVoltage bit is set to 0 in the MFR_CHAN_CONFIG_LTC3886 command and the output takes a long time to decay below 12.5% of the programmed value. The LTC3886-1 output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the IgnoreResidualVoltage bit is set to 0 in the MFR_CHAN_CONFIG_LTC3886 command and the output takes a long time to decay below the MFR_VOFF_THRESHOLD.

This command has two data bytes and is formatted in Linear_5s_11s format.

FAULT RESPONSE

Fault Responses All Faults

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_RETRY_ DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350 0xFABC

MFR_RETRY_DELAY

This command sets the time in milliseconds between retries if the fault response is to retry the controller at specified intervals. This command value is used for all fault responses that require retry. The retry time starts once the fault has been detected by the offending channel. Valid values are from 120ms to 83.88 seconds in 1ms increments.

PMBus COMMAND DETAILS

Note: The LTC3886 retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value when bit[5] of the MFR_CHAN_CONFIG_LTC3886 command is set to 1. The LTC3886-1 retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below the MFR_VOFF_THRESHOLD for one ADC cycle when bit[5] of the MFR_CHAN_CONFIG command is set to 0. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG_LTC3886.

This command has two data bytes and is formatted in Linear_5s_11s format.

Fault Responses Input Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input supply overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The data byte is in the format given in Table 11.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN Overvoltage Fault bit in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

Fault Responses Output Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. The data byte is in the format given in Table 7.

The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD

PMBus COMMAND DETAILS

• Sets the VOUT Overvoltage Fault bit in the STATUS_VOUT command

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The only values recognized for this command are:

0x00–Part performs OV pull down only, or OV_PULLDOWN.

0x80–The device shuts down (disables the output) and the unit does not attempt to retry. (PMBus, Part II, Section 10.7).

0xB8–The device shuts down (disables the output) and device attempts to retry continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.

0x4n The device shuts down and the unit does not attempt to retry. The output remains disabled until the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

0x78+n The device shuts down and the unit attempts to retry continuously until either the fault condition is cleared or the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

Any other value will result in a CML fault and the write will be ignored.

This command has one data byte.

Table 7. VOUT_OV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3886: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC3886.	00	Part performs OV pull down only or OV_PULLDOWN (i.e., turns off the top MOSFET and turns on lower MOSFET while V_{OUT} is > VOUT_OV_FAULT).
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The data byte is in the format given in Table 8.

PMBus COMMAND DETAILS

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT undervoltage fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The UV fault and warn are masked until the following criteria are achieved:

1) The TON_MAX_FAULT_LIMIT has been reached
2) The TON_DELAY sequence has completed
3) The TON_RISE sequence has completed
4) The VOUT_UV_FAULT_LIMIT threshold has been reached
5) The IOUT_OC_FAULT_LIMIT is not present

The UV fault and warn are masked whenever the channel is not active.

The UV fault and warn are masked during TON_RISE and TOFF_FALL sequencing.

This command has one data byte.

Table 8. VOUT_UV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3886: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The PMBus device continues operation without interruption. (Ignores the fault functionally)
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

PMBus COMMAND DETAILS

TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The data byte is in the format given in Table 11.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0.

This command has one data byte.

Fault Responses Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The data byte is in the format given in Table 9.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Fault bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

PMBus COMMAND DETAILS

Table 9. IOUT_OC_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3886: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The LTC3886 continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage (known as constant-current or brick-wall limiting).
		01	Not supported.
		10	The LTC3886 continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage, for the delay time set by bits [2:0]. If the device is still operating in current limit at the end of the delay time, the device responds as programmed by the Retry Setting in bits [5:3].
		11	The LTC3886 shuts down immediately and responds as programmed by the Retry Setting in bits [5:3].
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared by cycling the RUN pin or removing bias power.
		111	The device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The number of delay time units in 16ms increments. This delay time is used to determine the amount of time a unit is to continue operating after a fault is detected before shutting down. Only valid for deglitched off response.

Fault Responses IC Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0

MFR_OT_FAULT_RESPONSE

The MFR_OT_FAULT_RESPONSE command byte instructs the device on what action to take in response to an internal overtemperature fault. The data byte is in the format given in Table 10.

The LTC3886 also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD, and
- Sets the Overtemperature Fault bit in the STATUS_MFR_SPECIFIC command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

PMBus COMMAND DETAILS

Table 10. Data Byte Contents MFR_OT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3886: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC3886.	00	Not supported. Writing this value will generate a CML fault.
		01	Not supported. Writing this value will generate a CML fault
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001-111	Not supported. Writing this value will generate CML fault.
2:0	Delay Time	XXX	Not supported. Value ignored

Fault Responses External Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
OT_FAULT_ RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8
UT_FAULT_ RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an external overtemperature fault on the external temp sensors. The data byte is in the format given in Table 11.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Overtemperature Fault bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

UT_FAULT_RESPONSE

The UT_FAULT_RESPONSE command instructs the device on what action to take in response to an external undertemperature fault on the external temp sensors. The data byte is in the format given in Table 11.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Undertemperature Fault bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

PMBus COMMAND DETAILS

This condition is detected by the ADC so the response time may be up to 90ms.

This command has one data byte.

Table 11. Data Byte Contents: TON_MAX_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3886: • Sets the corresponding fault bit in the status commands, and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The PMBus device continues operation without interruption.
		01	Not supported. Writing this value will generate a CML fault.
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	Not supported. Values ignored

FAULT SHARING

Fault Sharing Propagation

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_FAULT_PROPAGATE_LTC3886	0xD2	Configuration that determines which faults are propagated to the FAULT pins.	R/W Word	Y	Reg		Y	0x6993

MFR_FAULT_PROPAGATE_LTC3886

The MFR_FAULT_PROPAGATE_LTC3886 command enables the faults that can cause the $\overline{\text{FAULT}}$*n* pin to assert low. The command is formatted as shown in Table 12. Faults can only be propagated to the $\overline{\text{FAULT}}$*n* pin if they are programmed to respond to faults.

This command has two data bytes.

PMBus COMMAND DETAILS

Table 12. $\overline{\text{FAULT}}n$ Propagate Fault Configuration

The $\overline{\text{FAULT0}}$ and $\overline{\text{FAULT1}}$ pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

BIT(S)	SYMBOL	OPERATION
B[15]	VOUT disabled while not decayed.	This is used in a PolyPhase configuration when bit 0 of the MFR_CHAN_CONFIG_LTC3886 is a zero. If the channel is turned off, by toggling the RUN pin or commanding the part OFF, and then the RUN is reasserted or the part is commanded back on before the output has decayed, VOUT will not restart until the 12.5% decay is honored. The $\overline{\text{FAULT}}$ pin is asserted during this condition if bit 15 is asserted.
B[14]	Mfr_FAULT_propagate_short_CMD_cycle	0: No action 1: Asserts low if commanded off then on before the output has sequenced off. Re-asserts high 120ms after sequence off.
b[13]	Mfr_FAULT_propagate_ton_max_fault	0: No action if a TON_MAX_FAULT fault is asserted 1: Associated output will be asserted low if a TON_MAX_FAULT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 TON_MAX_FAULT faults $\overline{\text{FAULT1}}$ is associated with page 1 TON_MAX_FAULT faults
b[12]	Reserved	Must be 0
b[11]	Mfr_FAULT0_propagate_int_ot, Mfr_FAULT1_propagate_int_ot	0: No action if the MFR_OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the MFR_OT_FAULT_LIMIT fault is asserted
b[10]	Reserved	Must be 0
b[9]	Reserved	Must be 0
b[8]	Mfr_FAULT0_propagate_ut, Mfr_FAULT1_propagate_ut	0: No action if the UT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the UT_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 UT faults $\overline{\text{FAULT1}}$ is associated with page 1 UT faults
b[7]	Mfr_FAULT0_propagate_ot, Mfr_FAULT1_propagate_ot	0: No action if the OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the OT_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OT faults $\overline{\text{FAULT1}}$ is associated with page 1 OT faults
b[6]	Reserved	
b[5]	Reserved	
b[4]	Mfr_FAULT0_propagate_input_ov, Mfr_FAULT1_propagate_input_ov	0: No action if the VIN_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VIN_OV_FAULT_LIMIT fault is asserted
b[3]	Reserved	
b[2]	Mfr_FAULT0_propagate_iout_oc, Mfr_FAULT1_propagate_iout_oc	0: No action if the IOUT_OC_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the IOUT_OC_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OC faults $\overline{\text{FAULT1}}$ is associated with page 1 OC faults
b[1]	Mfr_FAULT0_propagate_vout_uv, Mfr_FAULT1_propagate_vout_uv	0: No action if the VOUT_UV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_UV_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 UV faults $\overline{\text{FAULT1}}$ is associated with page 1 UV faults
b[0]	Mfr_FAULT0_propagate_vout_ov, Mfr_FAULT1_propagate_vout_ov	0: No action if the VOUT_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_OV_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OV faults $\overline{\text{FAULT1}}$ is associated with page 1 OV faults

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Fault Sharing Response

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the FAULT pin is asserted low.	R/W Byte	Y	Reg		Y	0xC0

MFR_FAULT_RESPONSE

The MFR_FAULT_RESPONSE command instructs the device on what action to take in response to the $\overline{\text{FAULT}}n$ pin being pulled low by an external source.

Supported Values:

VALUE	MEANING
0xC0	FAULT_INHIBIT The LTC3886 will disable the respective PWM channel in response to the $\overline{\text{FAULT}}$ pin pulled low.
0x00	FAULT_IGNORE The LTC3886 continues operation without interruption.

The device also:

- Sets the MFR_SPECIFIC Bit in the STATUS_WORD.
- Sets Bit 0 in the STATUS_MFR_SPECIFIC Command to Indicate $\overline{\text{FAULT}}n$ Is Being Pulled Low
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
USER_DATA_00	0xB0	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA
USER_DATA_02	0xB2	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_03	0xB3	A EEPROM word available for the user.	R/W Word	Y	Reg		Y	0x0000
USER_DATA_04	0xB4	A EEPROM word available for the user.	R/W Word	N	Reg		Y	0x0000

USER_DATA_00 through *USER_DATA_04*

These commands are non-volatile memory locations for customer storage. The customer has the option to write any value to the USER_DATA_nn at any time. However, the LTpowerPlay software and contract manufacturers use some of these commands for inventory control. Modifying the reserved USER_DATA_nn commands may lead to undesirable inventory control and incompatibility with these products.

These commands have 2 data bytes and are in register format.

PMBus COMMAND DETAILS

IDENTIFICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg		FS	0x22
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0
MFR_ID	0x99	The manufacturer ID of the LTC3886 in ASCII.	R String	N	ASC			LTC
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTC3886
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC3886. Manufacturer code representing the LTC3886-1.	R Word	N	Reg			0x460X 0x461X
IC_DEVICE_ID	0xAD	Identification of the IC (LTC3886-1 only)	R Block	N	ASC		Y	LTC3886-1
IC_DEVICE_REV	0xAE	Revision of the IC (LTC3886-1 only)	R Block	N	ASC		Y	ACA0

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTC3886 is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

CAPABILITY

This command provides a way for a host system to determine some key capabilities of a PMBus device.

The LTC3886 supports packet error checking, 400kHz bus speeds, and $\overline{\text{ALERT}}$ pin.

This read-only command has one data byte.

MFR_ID

The MFR_ID command indicates the manufacturer ID of the LTC3886 using ASCII characters.

This read-only command is in block format.

MFR_MODEL

The MFR_MODEL command indicates the manufacturer's part number of the LTC3886 using ASCII characters.

This read-only command is in block format.

MFR_SPECIAL_ID

The 16-bit word representing the part name and revision. 0x46 denotes the part is an LTC3886, X is adjustable by the manufacturer.

This read-only command has two data bytes.

IC_DEVICE_ID

The IC_DEVICE_ID command indicates the manufacturer's ID of the LTC3886-1 using ASCII characters.

This read-only command is in block format.

LTC3886-1 Only.

PMBus COMMAND DETAILS

IC_DEVICE_REV

The IC_DEVICE_REV command indicates the revision of the LTC3886-1 using ASCII characters.

This read-only command is in block format.

LTC3886-1 Only

FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA
SMBALERT_MASK	0x1B	Mask activity.	Block R/W	Y	Reg		Y	See CMD Details
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				NA
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA
STATUS_ TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA
STATUS_MFR_ SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA
MFR_INFO	0xB6	Manufacturing Specific Information	R Word	N	Reg			NA

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{ALERT}}$ pin signal output if the device is asserting the $\overline{\text{ALERT}}$ pin signal. If the fault is still present when the bit is cleared, the fault bit will remain set and the host notified by asserting the $\overline{\text{ALERT}}$ pin low. CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame it may be cleared before the status register is set.

This write-only command has no data bytes.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted when:

- The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or
- MFR_RESET command is issued.
- Bias power is removed and reapplied to the integrated circuit

PMBus COMMAND DETAILS

SMBALERT_MASK

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from asserting $\overline{\text{ALERT}}$ as they are asserted.

Figure 47 shows an example of the Write Word format used to set an $\overline{\text{ALERT}}$ mask, in this case without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ if set.

Figure 48 shows an example of the Block Write – Block Read Process Call protocol used to read back the present state of any supported status register, again without PEC.

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON or MFR_PADS. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

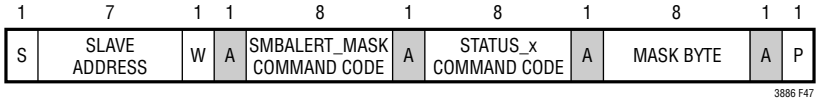

Figure 47. Example of Setting SMBALERT_MASK

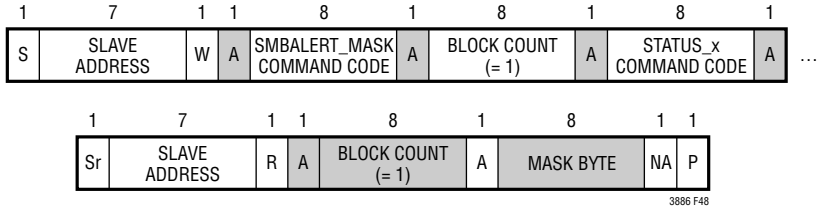

Figure 48. Example of Reading SMBALERT_MASK

SMBALERT_MASK Default Setting: (Refer Also to Figure 2)

STATUS RESISTER	ALERT Mask Value	MASKED BITS
STATUS_VOUT	0x00	None
STATUS_IOUT	0x00	None
STATUS_TEMPERATURE	0x00	None
STATUS_CML	0x00	None
STATUS_INPUT	0x00	None
STATUS_MFR_SPECIFIC	0x11	Bit 4 (internal PLL unlocked), bit 0 ($\overline{\text{FAULT}}$ pulled low by external device)

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values. A MFR_RESET command will also clear the MFR_*_PEAK data values.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. This is the lower byte of the status word.

STATUS_BYTE Message Contents:

BIT	STATUS BIT NAME	MEANING
7*	BUSY	A fault was declared because the LTC3886 was unable to respond.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	VIN_UV	Not supported (LTC3886 returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0*	NONE OF THE ABOVE	A fault Not listed in bits[7:1] has occurred.

*$\overline{\text{ALERT}}$ can be asserted if either of these bits is set. They may be cleared by writing a 1 to their bit position in the STATUS_BYTE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

STATUS_WORD High Byte Message Contents:

BIT	STATUS BIT NAME	MEANING
15	V_{OUT}	An output voltage fault or warning has occurred.
14	I_{OUT}	An output current fault or warning has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LTC3886 has occurred.
11	POWER_GOOD#	The POWER_GOOD state is false if this bit is set.
10	FANS	Not supported (LTC3886 returns 0).
9	OTHER	Not supported (LTC3886 returns 0).
8	UNKNOWN	Not supported (LTC3886 returns 0).

If any of the bits in the upper byte are set, NONE_OF_THE_ABOVE is asserted.

This command has two data bytes.

PMBus COMMAND DETAILS

STATUS_VOUT

The STATUS_VOUT command returns one byte of V_{OUT} status information.

STATUS_VOUT Message Contents:

BIT	MEANING
7	V_{OUT} overvoltage fault.
6	V_{OUT} overvoltage warning.
5	V_{OUT} undervoltage warning.
4	V_{OUT} undervoltage fault.
3	V_{OUT} max warning.
2	TON max fault.
1	TOFF max fault.
0	Not supported (LTC3886 returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT command returns one byte of I_{OUT} status information.

STATUS_IOUT Message Contents:

BIT	MEANING
7	I_{OUT} overcurrent fault.
6	Not supported (LTC3886 returns 0).
5	I_{OUT} overcurrent warning.
4:0	Not supported (LTC3886 returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. This command has one data byte.

PMBus COMMAND DETAILS

STATUS_INPUT

The STATUS_INPUT command returns one byte of V_{IN} (VINSNS) status information.

STATUS_INPUT Message Contents:

BIT	MEANING
7	V_{IN} overvoltage fault.
6	Not supported (LTC3886 returns 0).
5	V_{IN} undervoltage warning.
4	Not supported (LTC3886 returns 0).
3	Unit off for insufficient V_{IN}.
2	Not supported (LTC3886 returns 0).
1	I_{IN} overcurrent warning.
0	Not supported (LTC3886 returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. Bit 3 of this command is not latched and will not generate an $\overline{\text{ALERT}}$ even if it is set. This command has one data byte.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE commands returns one byte with status information on temperature. This is a paged command and is related to the respective READ_TEMPERATURE_1 value.

STATUS_TEMPERATURE Message Contents:

BIT	MEANING
7	External overtemperature fault.
6	External overtemperature warning.
5	Not supported (LTC3886 returns 0).
4	External undertemperature fault.
3:0	Not supported (LTC3886 returns 0).

.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

This command has one data byte.

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STATUS_CML

The STATUS_CML command returns one byte of status information on received commands, internal memory and logic.

STATUS_CML Message Contents:

BIT	MEANING
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	Packet error check failed.
4	Memory fault detected.
3	Processor fault detected.
2	Reserved (LTC3886 returns 0).
1	Other communication fault.
0	Other memory or logic fault.

If either bit 3 or bit 4 of this command is set, a serious and significant internal error has been detected. Continued operation of the part is not recommended if these bits are continuously set.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC commands returns one byte with the manufacturer specific status information.

The format for this byte is:

BIT	MEANING
7	Internal Temperature Fault Limit Exceeded.
6	Internal Temperature Warn Limit Exceeded.
5	Factory Trim Area EEPROM CRC Fault.
4	PLL is Unlocked
3	Fault Log Present
2	V_{DD33} UV or OV Fault
0	$\overline{\text{FAULT}}$ Pin Asserted Low by External Device

If any of these bits are set, the MFR bit in the STATUS_WORD will be set, and $\overline{\text{ALERT}}$ may be asserted.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command. However, the fault log present bit can only be cleared by issuing the MFR_FAULT_LOG_CLEAR command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

PMBus COMMAND DETAILS

MFR_PADS

This command provides the user a means of directly reading the digital status of the I/O pins of the device. The bit assignments of this command are as follows:

BIT	ASSIGNED DIGITAL PIN
15	V_{DD33} OV Fault
14	V_{DD33} UV Fault
13	Reserved
12	Reserved
11	ADC Values Invalid, Occurs During Start-Up. May Occur Briefly on Current Measurement Channels During Normal Operation
10	SYNC clocked by external device (when LTC3886 configured to drive SYNC pin)
9	Channel 1 Power Good
8	Channel 0 Power Good
7	LTC3886 Driving RUN1 Low
6	LTC3886 Driving RUN0 Low
5	RUN1 Pin State
4	RUN0 Pin State
3	LTC3886 Driving $\overline{\text{FAULT1}}$ Low
2	LTC3886 Driving $\overline{\text{FAULT0}}$ Low
1	$\overline{\text{FAULT1}}$ Pin State
0	$\overline{\text{FAULT0}}$ Pin State

A 1 indicates the condition is true.

This read-only command has two data bytes.

MFR_COMMON

The MFR_COMMON command contains bits that are common to all ADI digital power and telemetry products.

BIT	MEANING
7	Chip Not Driving $\overline{\text{ALERT}}$ Low
6	LTC3886 Not Busy
5	Calculations Not Pending
4	LTC3886 Outputs Not in Transition
3	EEPROM Initialized
2	Reserved
1	SHARE_CLK Timeout
0	WP Pin Status

This read-only command has one data byte.

PMBus COMMAND DETAILS

MFR_INFO

The MFR_INFO command contains the EEPROM status bit.

MFR_INFO Data Contents:

BIT	MEANING
15:5	Reserved
4	EEPROM ECC status
0b	Corrections made in the EEPROM user space
1b	No corrections made in the EEPROM user space
3:0	Reserved

EEPROM ECC status is updated after each RESTORE_USER_ALL or RESET command, a power-on reset or a EEPROM bulk read operation. This read-only command has two data bytes.

TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA
READ_TEMPERATURE_2	0x8E	Internal junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	kHz		NA
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		NA
READ_PIN	0x97	Calculated input power.	R Word	N	L11	W		NA
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back	R/W Byte	N	Reg			0x00
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA
MFR_READ_IIN_PEAK	0xE1	Maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS.	R Word	N	L11	A		NA
MFR_READ_ICHIP	0xE4	Measured current used by the LTC3886.	R Word	N	L11	A		NA
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA

PMBus COMMAND DETAILS

READ_VIN

The READ_VIN command returns the measured V_{IN} pin voltage, in volts added to READ_ICHIP • MFR_RVIN. This compensates for the IR voltage drop across the V_{IN} filter element due to the supply current of the LTC3886.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_VOUT

The READ_VOUT command returns the measured output voltage in the same format as set by the VOUT_MODE command.

This read-only command has two data bytes and is formatted in Linear_16u format.

READ_IIN

The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor (see also MFR_IIN_CAL_GAIN).

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_IOUT

The READ_IOUT command returns the average output current in amperes. The IOUT value is a function of:

a) the differential voltage measured across the I_{SENSE} pins

b) the IOUT_CAL_GAIN value

c) the MFR_IOUT_CAL_GAIN_TC value, and

d) READ_TEMPERATURE_1 value

e) The MFR_TEMP_1_GAIN and the MFR_TEMP_1_OFFSET

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the external sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the LTC3886's die temperature, in degrees Celsius, of the internal sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_FREQUENCY

The READ_FREQUENCY command is a reading of the PWM switching frequency in kHz.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

READ_POUT

The READ_POUT command is a reading of the DC/DC converter output power in Watts. POUT is calculated based on the most recent correlated output voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

READ_PIN

The READ_PIN command is a reading of the DC/DC converter input power in Watts. PIN is calculated based on the most recent input voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_ADC_CONTROL

The MFR_ADC_CONTROL command determines the ADC read back selection. A default value of 0 in the command runs the standard telemetry loop with all parameters updated in a round robin fashion with a typical latency of 90ms. The user can command a non-zero value to monitored a single parameter with an approximate update rate of 8ms. This command has a latency of up to 2 ADC conversions or approximately 16ms (external temperature conversions may have a latency of up to 3 ADC conversion or approximately 24ms). It is recommended the part remain in standard telemetry mode except for special cases where fast ADC updates of a single parameter is required. The part should be commanded to monitor the desired parameter for a limited period of time (less then 1 second) then set the command back to standard round robin mode. If this command is set to any value except standard round robin telemetry (0) all warnings and faults associated with telemetry other than the selected parameter are effectively disabled and voltage servoing is disabled. When round robin is reasserted, all warnings and faults and servo mode are re-enabled.

COMMANDED VALUE	TELEMETRY COMMAND NAME	DESCRIPTION
0x0F		Reserved
0x0E		Reserved
0x0D		Reserved
0x0C	READ_TEMPERATURE_1	Channel 1 external temperature
0x0B		Reserved
0x0A	READ_IOUT	Channel 1 measured output current
0x09	READ_VOUT	Channel 1 measured output voltage
0x08	READ_TEMPERATURE_1	Channel 0 external temperature
0x07		Reserved
0x06	READ_IOUT	Channel 0 measured output current
0x05	READ_VOUT	Channel 0 measured output voltage
0x04	READ_TEMPERATURE_2	Internal junction temperature
0x03	READ_IIN	Measured input supply current
0x02	MFR_READ_ICHIP	Measured supply current of the LTC3886
0x01	READ_VIN	Measured input supply voltage
0x00		Standard ADC round robin telemetry

PMBus COMMAND DETAILS

If a reserved command value is entered, the telemetry will default to Internal IC Temperature and issue a CML fault. CML faults will continue to be issued by the LTC3886 until a valid command value is entered. The accuracy of the measured input supply voltage is only guaranteed if the MFR_ADC_CONTROL command is set to standard round robin telemetry. This write-only command has 1 data byte and is formatted in register format.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_16u format.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_IIN_PEAK

The MFR_READ_IIN_PEAK command reports the highest current, in Amperes, reported by the READ_IIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_ICHIP

The MFR_READ_ICHIP command returns the measured input current, in Amperes, used by the LTC3886.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_2_PEAK

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

EEPROM MEMORY COMMANDS

Store/Restore

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with EEPROM.	Send Byte	N				NA

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the non-volatile user contents of the Operating Memory to the matching locations in the non-volatile User EEPROM memory.

Executing this command if the die temperature exceeds 85°C or is below 0°C is not recommended and the data retention of 10 years cannot be guaranteed. If the die temperature exceeds 130°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 125°C.

Communication with the LTC3886 and programming of the EEPROM can be initiated when VDD33 is available and VIN is not applied. To enable the part in this state, using global address 0x5B write MFR_EE_UNLOCK to 0x2B followed by 0xC4. The LTC3886 will now communicate normally, and the project file can be updated. To write the updated project file to the EEPROM issue a STORE_USER_ALL command. When VIN is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

This write-only command has no data bytes.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the PMBus device to copy the contents of the non-volatile User memory to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the User commands. The LTC3886 ensures both channels are off, loads the operating memory from the internal EEPROM, clears all faults, reads the resistor configuration pins, and then performs a soft-start of both PWM channels if applicable.

STORE_USER_ALL, MFR_COMPARE_USER_ALL and RESTORE_USER_ALL commands are disabled if the die exceeds 130°C and are not re-enabled until the die temperature drops below 125°C.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in non-volatile memory. If the compare operation detects differences, a CML fault will be generated.

This write-only command has no data bytes.

Fault Logging

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	CF		Y	NA
MFR_FAULT_LOG_ STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA

Fault Log Operation

A conceptual diagram of the fault log is shown in Figure 49. The fault log provides black box capability for the LTC3886. During normal operation the contents of the status registers, the output voltage/current/temperature readings, the input voltage readings, as well as the peak values of these quantities, are stored in a continuously updated buffer in RAM. You can think of the operation as being similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for non volatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time.

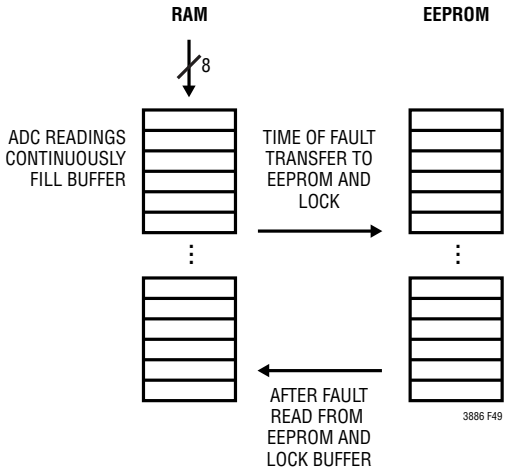


Figure 49. Fault Log Conceptual Diagram

PMBus COMMAND DETAILS

MFR_FAULT_LOG

The MFR_FAULT_LOG command allows the user to read the contents of the FAULT_LOG after the first fault occurrence since the last MFR_FAULT_LOG_CLEAR command was written. The contents of this command are stored in non-volatile memory, and are cleared by the MFR_FAULT_LOG_CLEAR command. The length and content of this command are listed in Table 13. If the user accesses the MFR_FAULT_LOG command and no fault log is present, the command will return a data length of 0. If a fault log is present, the MFR_FAULT_LOG will return a block of data 147 bytes long. The area available for the fault log in EEPROM is smaller than the area in RAM. When reading the fault log from RAM all six events of cyclical data remain. However, when the fault log is read from EEPROM (after a reset), the last two events are lost. The read length of 147 bytes remains the same, but the fifth and sixth events are a repeat of the fourth event. If a fault occurs within the first second of applying power, some of the earlier pages in the fault log may not contain valid data.

NOTE: The approximate transfer time for this command is 3.4ms using a 400kHz clock.

This read-only command is in block format.

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces the fault log operation to be written to EEPROM just as if a fault event occurred. This command will set bit 3 of the STATUS_MFR_SPECIFIC fault if bit 7 “Enable Fault Logging” is set in the MFR_CONFIG_ALL_LTC3886 command.

If the die temperature exceeds 130°C, the MFR_FAULT_LOG_STORE command is disabled until the IC temperature drops below 125°C.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

Table 13. Fault Logging
This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

Data Format Definitions				
				BYTE = 8 bits interpreted per definition of this command
DATA	**BITS**	**DATA FORMAT**	**BYTE NUM**	**BLOCK READ COMMAND**
Block Length		BYTE	147	The MFR_FAULT_LOG command is a fixed length of 147 bytes The block length will be zero if a data log event has not been captured
HEADER INFORMATION				
Fault Log Preface	[7:0]	ASC	0	Returns LTxx beginning at byte 0 if a partial or complete fault log exists. Word xx is a factory identifier that may vary part to part.
	[7:0]		1	
	[15:8]	Reg	2	
	[7:0]		3	
Fault Source	[7:0]	Reg	4	Refer to Table 13a.
MFR_REAL_TIME	[7:0]	Reg	5	48 bit share-clock counter value when fault occurred (200µs resolution).
	[15:8]		6	
	[23:16]		7	
	[31:24]		8	
	[39:32]		9	
	[47:40]		10	
MFR_VOUT_PEAK (PAGE 0)	[15:8]	L16	11	Peak READ_VOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		12	
MFR_VOUT_PEAK (PAGE 1)	[15:8]	L16	13	Peak READ_VOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		14	
MFR_IOUT_PEAK (PAGE 0)	[15:8]	L11	15	Peak READ_IOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		16	
MFR_IOUT_PEAK (PAGE 1)	[15:8]	L11	17	Peak READ_IOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		18	
MFR_VIN_PEAK	[15:8]	L11	19	Peak READ_VIN since last power-on or CLEAR_PEAKS command.
	[7:0]		20	
READ_TEMPERATURE1 (PAGE 0)	[15:8]	L11	21	External temperature sensor 0 during last event.
	[7:0]		22	
READ_TEMPERATURE1 (PAGE 1)	[15:8]	L11	23	External temperature sensor 1 during last event.
	[7:0]		24	
READ_TEMPERATURE2	[15:8]	L11	25	LTC3886 die temperature sensor during last event.
	[7:0]		26	

PMBus COMMAND DETAILS

CYCLICAL DATA

EVENT n **(Data at Which Fault Occurred; Most Recent Data)**				Event "n" represents one complete cycle of ADC reads through the MUX at time of fault. Example: If the fault occurs when the ADC is processing step 15, it will continue to take readings through step 25 and then store the header and all 6 event pages to EEPROM
READ_VOUT (PAGE 0)	[15:8]	LIN 16	27	
	[7:0]	LIN 16	28	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	29	
	[7:0]	LIN 16	30	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	31	
	[7:0]	LIN 11	32	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	33	
	[7:0]	LIN 11	34	
READ_VIN	[15:8]	LIN 11	35	
	[7:0]	LIN 11	36	
READ_IIN	[15:8]	LIN 11	37	
	[7:0]	LIN 11	38	
STATUS_VOUT (PAGE 0)		BYTE	39	
STATUS_VOUT (PAGE 1)		BYTE	40	
STATUS_WORD (PAGE 0)	[15:8]	WORD	41	
	[7:0]	WORD	42	
STATUS_WORD (PAGE 1)	[15:8]	WORD	43	
	[7:0]	WORD	44	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	45	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	46	
EVENT n-1 **(data measured before fault was detected)**				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	47	
	[7:0]	LIN 16	48	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	49	
	[7:0]	LIN 16	50	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	51	
	[7:0]	LIN 11	52	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	53	
	[7:0]	LIN 11	54	
READ_VIN	[15:8]	LIN 11	55	
	[7:0]	LIN 11	56	
READ_IIN	[15:8]	LIN 11	57	
	[7:0]	LIN 11	58	

PMBus COMMAND DETAILS

STATUS_VOUT (PAGE 0)		BYTE	59	
STATUS_VOUT (PAGE 1)		BYTE	60	
STATUS_WORD (PAGE 0)	[15:8]	WORD	61	
	[7:0]	WORD	62	
STATUS_WORD (PAGE 1)	[15:8]	WORD	63	
	[7:0]	WORD	64	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	65	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	66	
*				
*				
*				
EVENT n-5 (Oldest Recorded Data)				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	127	
	[7:0]	LIN 16	128	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	129	
	[7:0]	LIN 16	130	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	131	
	[7:0]	LIN 11	132	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	133	
	[7:0]	LIN 11	134	
READ_VIN	[15:8]	LIN 11	135	
	[7:0]	LIN 11	136	
READ_IIN	[15:8]	LIN 11	137	
	[7:0]	LIN 11	138	
STATUS_VOUT (PAGE 0)		BYTE	139	
STATUS_VOUT (PAGE 1)		BYTE	140	
STATUS_WORD (PAGE 0)	[15:8]	WORD	141	
	[7:0]	WORD	142	
STATUS_WORD (PAGE 1)	[15:8]	WORD	143	
	[7:0]	WORD	144	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	145	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	146	

PMBus COMMAND DETAILS

Table 13a. Explanation of Position_Fault Values

POSITION_FAULT VALUE	SOURCE OF FAULT LOG
0xFF	MFR_FAULT_LOG_STORE
0x00	TON_MAX_FAULT Channel 0
0x01	VOUT_OV_FAULT Channel 0
0x02	VOUT_UV_FAULT Channel 0
0x03	IOUT_OC_FAULT Channel 0
0x05	TEMP_OT_FAULT Channel 0
0x06	TEMP_UT_FAULT Channel 0
0x07	VIN_OV_FAULT
0x0A	MFR_TEMPERATURE_2_OT_FAULT
0x10	TON_MAX_FAULT Channel 1
0x11	VOUT_OV_FAULT Channel 1
0x12	VOUT_UV_FAULT Channel 1
0x13	IOUT_OC_FAULT Channel 1
0x15	OT_FAULT Channel 1
0x16	UT_FAULT Channel 1
0x17	VIN_OV_FAULT
0x1A	MFR_TEMPERATURE_2_OT_FAULT

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command will erase the fault log file stored values. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command. After a clear is issued, the status can take up to 8ms to clear.

This write-only command is send bytes.

Block Memory Write/Read

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA

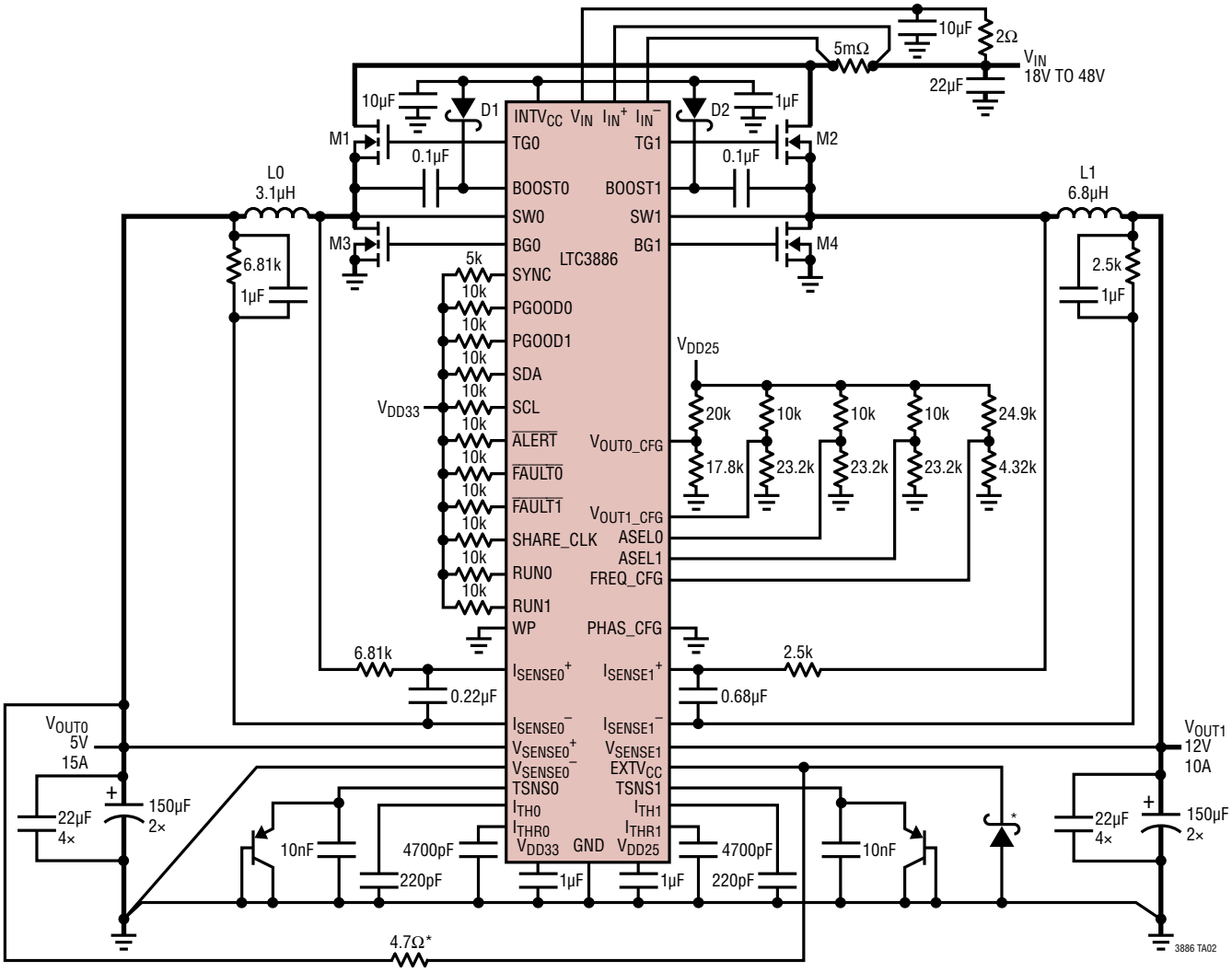
All the EEPROM commands are disabled if the die temperature exceeds 130°C. EEPROM commands are re-enabled when the die temperature drops below 125°C.

MFR_EE_xxxx

The MFR_EE_xxxx commands facilitate bulk programming of the LTC3886 internal EEPROM. Contact the factory for details.

TYPICAL APPLICATIONS

High Efficiency 150kHz/5V and 12V Step-Down Converter with DCR Sense

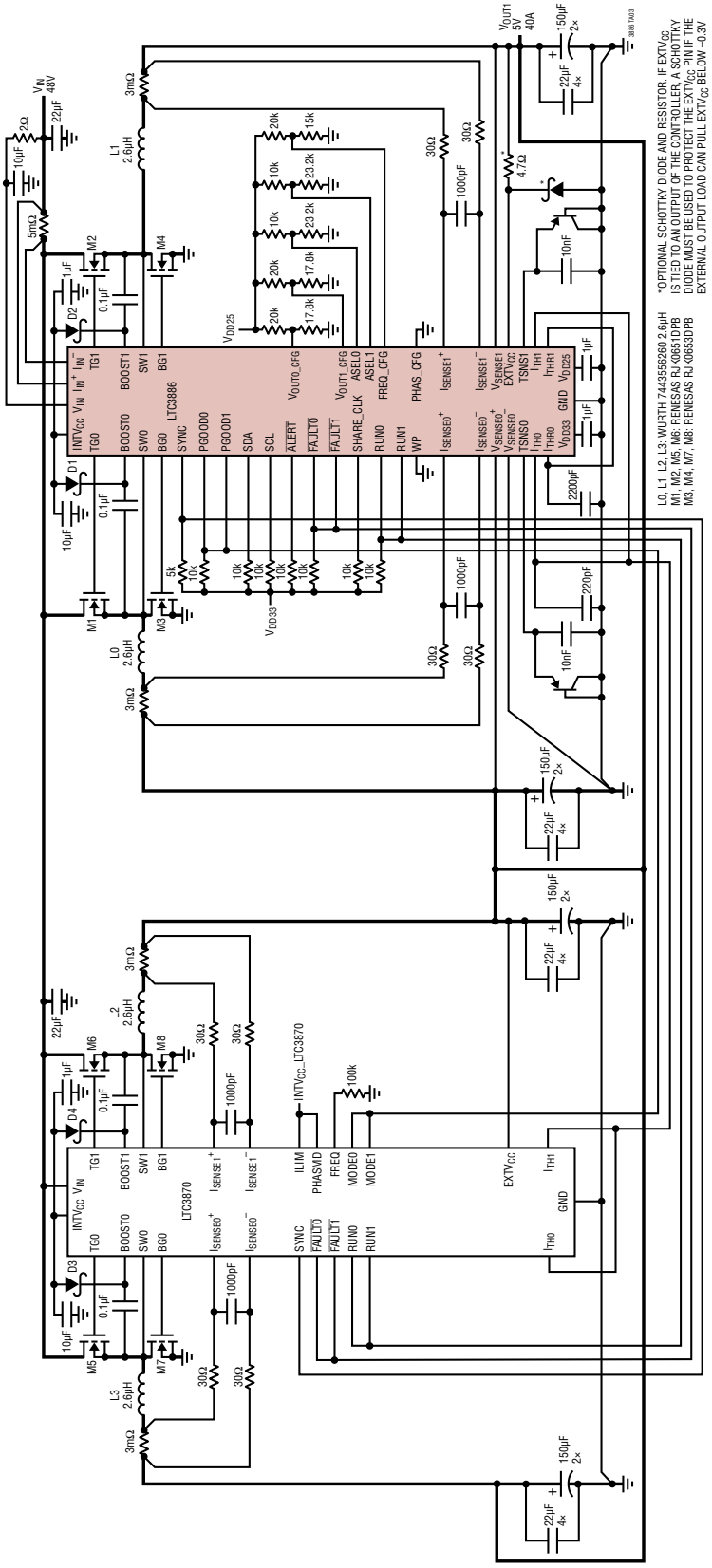


L0: WURTH 7443630310 3.1µH
L1: WURTH 7443556680 6.8µH
M1, M2: RENESAS RJK0651DPB
M3, M4: RENESAS RJK0653DPB

*OPTIONAL SCHOTTKY DIODE AND RESISTOR. IF $EXTV_{CC}$ IS TIED TO AN OUTPUT OF THE CONTROLLER, A SCHOTTKY DIODE MUST BE USED TO PROTECT THE $EXTV_{CC}$ PIN IF THE EXTERNAL OUTPUT LOAD CAN PULL $EXTV_{CC}$ BELOW –0.3V

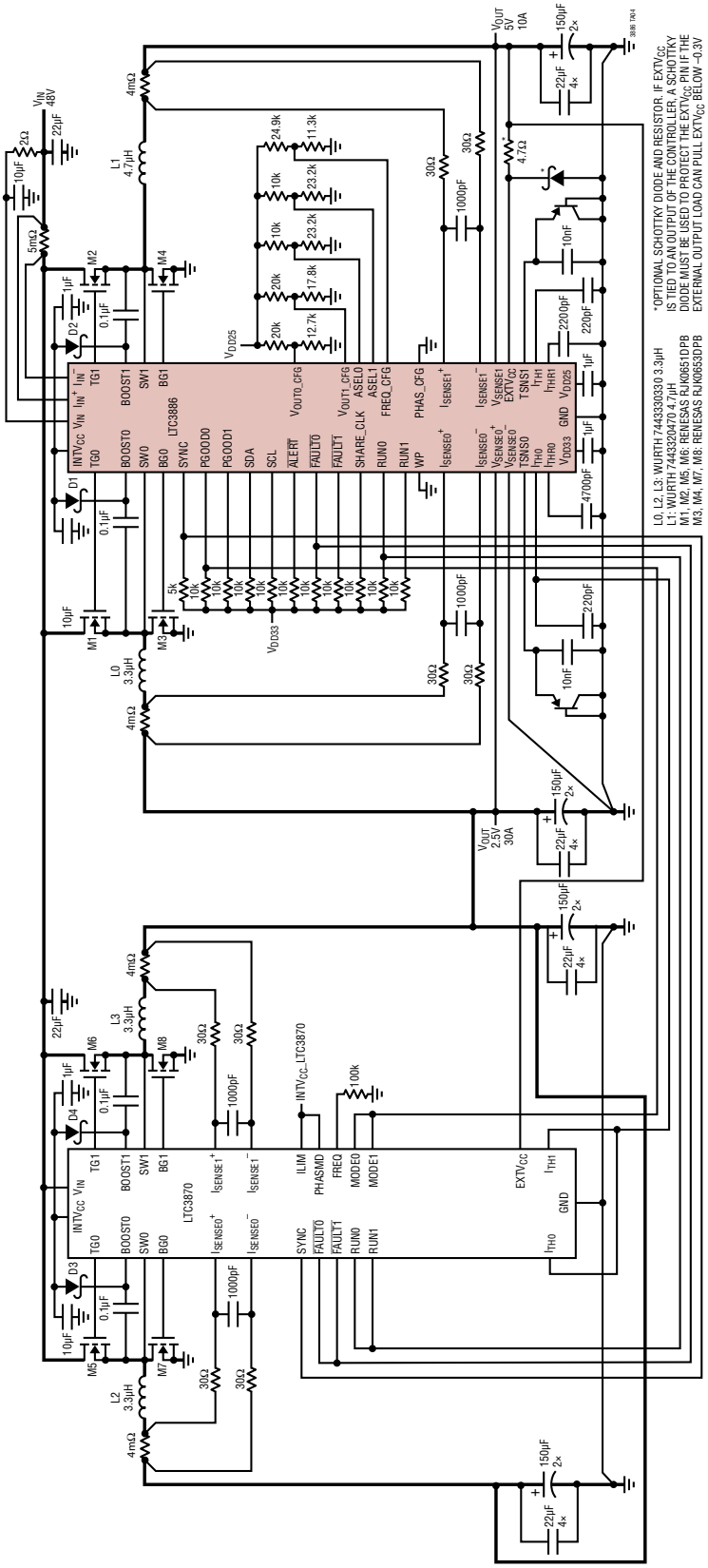
TYPICAL APPLICATIONS

High Efficiency 425kHz 4-phase 5V Step-Down Converter



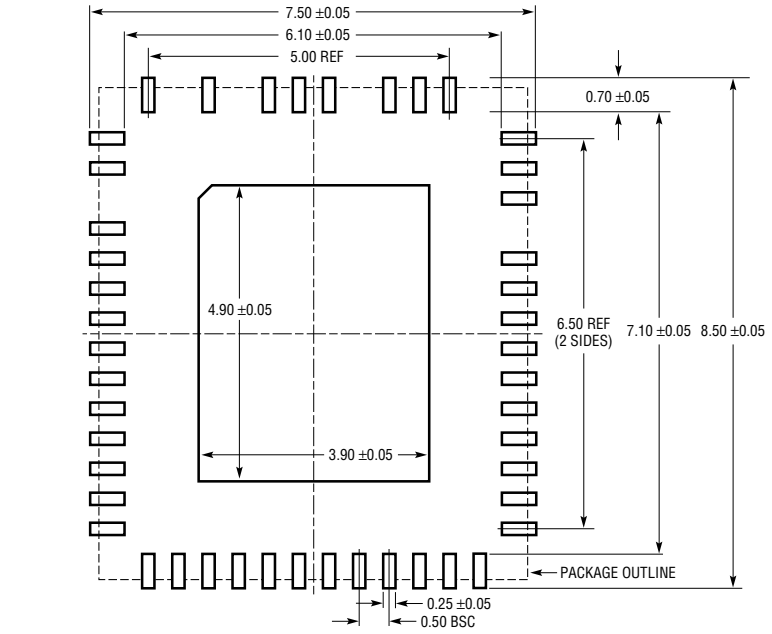
TYPICAL APPLICATIONS

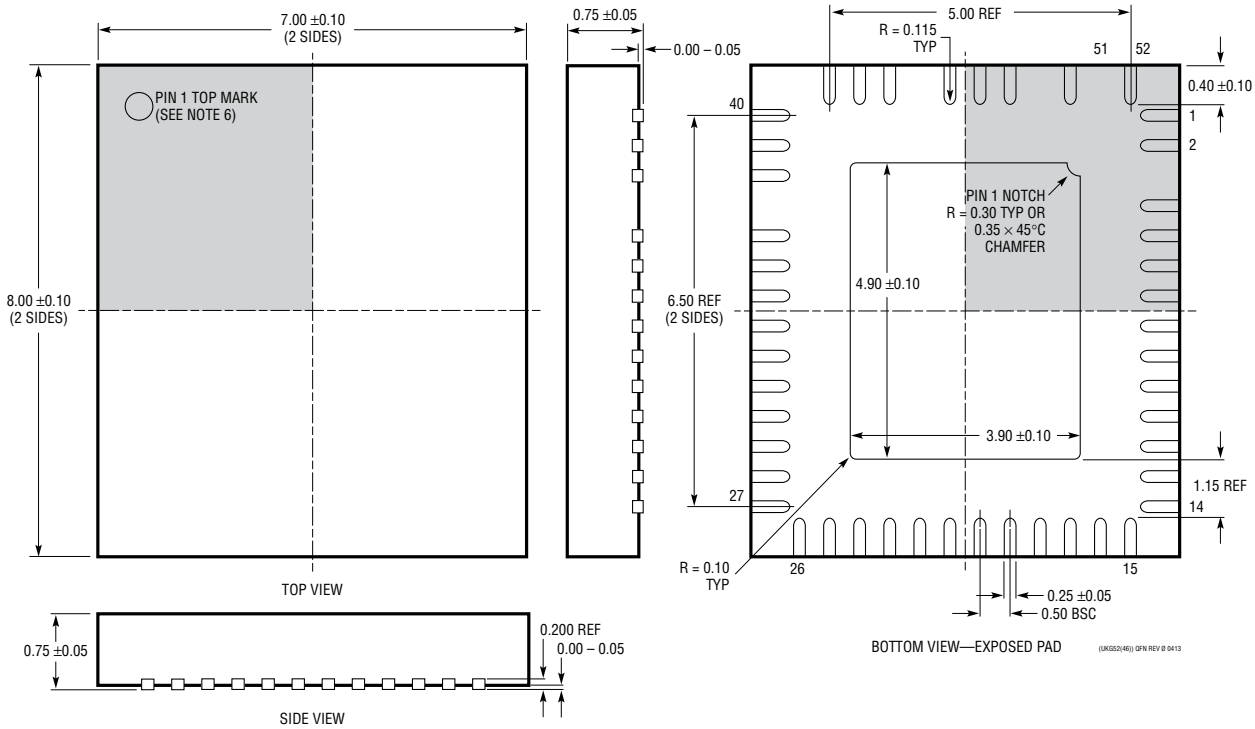
High Efficiency 250kHz 3-Phase 2.5V Plus 1-Phase 5V Step-Down Converter with Sense Resistors



PACKAGE DESCRIPTION

UKG Package
Variation: UKG52(46)
52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1947 Rev Ø)





NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Changed target voltage	12
		Corrected B60/B61 pin numbers	14
B	4/16	Modified R1 + R3||R2 formula	44
		Modified schematics	62, 113, 114, 115, 116
		Added Fault Log Operation	109
C	6/16	Deleted $V_{SENSE0(RIN)}$ and $V_{SENSE1(RIN)}$ lines	5
		Electrical Characteristics Table changes	6, 7
		Revised Input Current Sensing and PolyPhase Load Sharing sections	21
		Replaced Figures 28, 29	48
		Revised Table 6	56
D	8/16	$EXTV_{CC}$ Pin Functions clarification	14, 49
		Schematic modifications – optional Schottky diode	115, 116, 117, 120
E	5/17	Added ECC	1, 16, 17
		Reduced initialization time	5
		Reduced conversion time	6, 7
		Added I_{IN} input current to Electrical Characteristics Table	7
		Changed V_{IH} and V_{IL} threshold limits	8
F	9/18	Added LTC3886-1	1, 4, 7, 16, 19, 37-39, 48, 71, 72, 81, 86-89, 98, 99

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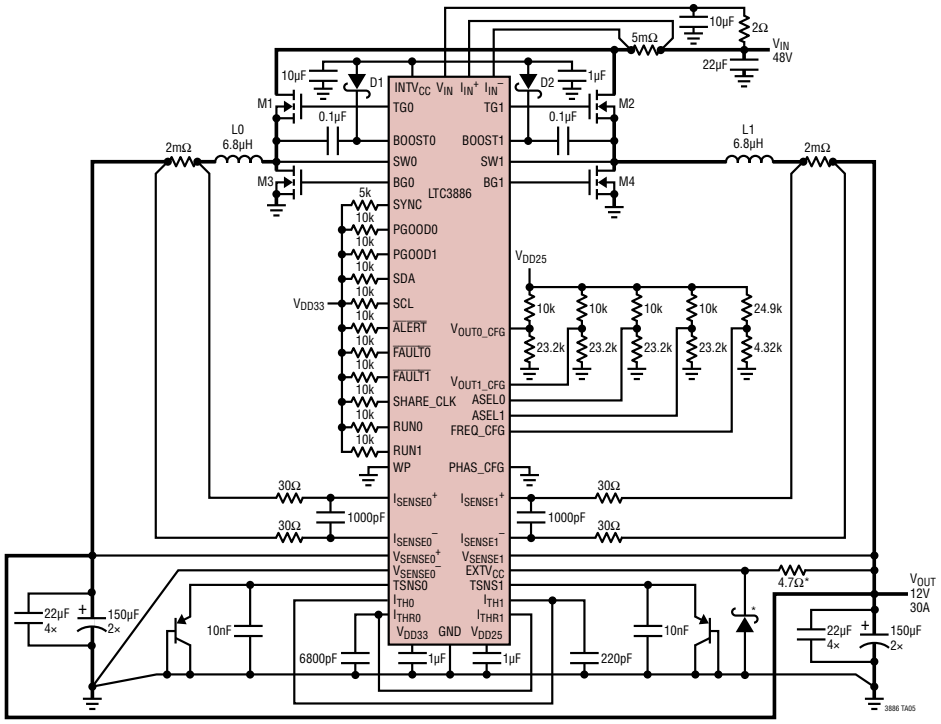
TYPICAL APPLICATION

High Efficiency 150kHz 2-Phase12V Step-Down Converter with Sense Resistors



L0, L1: COILCRAFT SER2915H-682KL 6.8µH
M1, M2: RENESAS RJK0651DPB
M3, M4: RENESAS RJK0653DPB

*OPTIONAL SCHOTTKY DIODE AND RESISTOR. IF $EXTV_{CC}$ IS TIED TO AN OUTPUT OF THE CONTROLLER, A SCHOTTKY DIODE MUST BE USED TO PROTECT THE $EXTV_{CC}$ PIN IF THE EXTERNAL OUTPUT LOAD CAN PULL $EXTV_{CC}$ BELOW –0.3V

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM®4676A	Dual 13A or Single 26A Step-Down DC/DC µModule Regulator with Digital Power System Management	V_{IN} Up to 26.5V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.4V, ±2% I_{OUT} ADC Accuracy, Fault Logging, I^2C/PMBus Interface, 16mm × 16mm × 5mm, BGA Package
LTM4675	Dual 9A or Single 18A Step-Down DC/DC µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤17V; 0.5V ≤ V_{OUT} ≤ 5.5V, ±0.5% V_{OUT} Accuracy I^2C/PMBus Interface, 11.9mm × 16mm × 3.51mm, BGA Package
LTM4677	Dual 18A or Single 36A µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤16V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 1.8V, I^2C/PMBus Interface, 16mm × 16mm × 5.01mm, BGA Package
LTC3870/LTC3870-1	60V Dual Output Multiphase Step-Down Slave Controller for Current Mode Control Applications with Digital Power System Management	V_{IN} Up to 60V, 0.5V ≤ V_{OUT} ≤ 14V, Very High Output Current Applications with Accurate Current Share Between Phases Supporting LTC3880/ LTC3880-1, LTC3883/ LTC3883-1, LTC3886, LTC3887/ LTC3887-1
LTC3884	Dual Output MultiPhase Step-Down Controller with Sub MilliOhm DCR Sensing Current Mode Control and Digital Power System Management	4.5V ≤ V_{IN} ≤ 38V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, I^2C/PMBus Interface, Programmable Analog Loop Compensation, Input Current Sense
LTC3887/LTC3887-1	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ $V_{OUT0,1}$ ≤ 5.5V, Analog Control Loop, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3882/LTC3882-1	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	V_{IN} Up to 38V, 0.5V ≤ $V_{OUT1,2}$ ≤ 5.25V, ±0.5% V_{OUT} Accuracy I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3883/LTC3883-1	Single Phase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Input Current Sense Amplifier, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3889	60V Dual Output Multiphase Step-Down Controller with Digital Power System Management	5V < V_{IN} < 60V, 3V ≤ V_{OUT} (±0.5%) ≤ 38V, Input Current Sense, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3815	6A Monolithic Synchronous DC/DC Step-Down Converter with Digital Power System Management	2.25V ≤ V_{IN} ≤ 5.5V, 0.4V ≤ V_{OUT} ≤ 0.72V_{IN}, Programmable V_{OUT} Range ±25% with 0.1% Resolution, Up to 3MHz Operation with 13-Bit ADC

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