maxim integrated™

MAX15026

Low-Cost, Small, 4.5V to 28V Wide Operating Range, DC-DC Synchronous Buck Controller

General Description

The MAX15026 synchronous step-down controller operates from a 4.5V to 28V input voltage range and generates an adjustable output voltage from 85% of the input voltage down to 0.6V while supporting loads up to 25A. The device allows monotonic startup into a prebiased bus without discharging the output and features adaptive internal digital soft-start.

The MAX15026 offers the ability to adjust the switching frequency from 200kHz to 2MHz with an external resistor. The MAX15026's adaptive synchronous rectification eliminates the need for an external freewheeling Schottky diode. The device also utilizes the external low-side MOSFET's on-resistance as a current-sense element, eliminating the need for a current-sense resistor. This protects the DC-DC components from damage during output overloaded conditions or output short-circuit faults without requiring a current-sense resistor. Hiccup-mode current limit reduces power dissipation during short-circuit conditions. The MAX15026 includes a power-good output and an enable input with precise turn-on/turn-off threshold, which can be used for input supply monitoring and for power sequencing.

Additional protection features include sink-mode current limit and thermal shutdown.

Sink-mode current limit prevents reverse inductor current from reaching dangerous levels when the device is sinking current from the output.

The MAX15026 is available in a space-saving and thermally enhanced 3mm x 3mm, 14-pin TDFN-EP package. The MAX15026 operates over the extended -40°C to +85°C and automotive -40°C to +125°C temperature ranges.

The MAX15026C is designed to provide additional margin for break-before-make times.

The MAX15026B/MAX15026C provide a soft-stop feature to ramp down the output voltage at turn-off. The soft-stop function is disabled in the MAX15026D.

Applications

Set-Top Boxes

LCD TV Secondary Supplies

Switches/Routers

Power Modules

DSP Power Supplies

Points-of-Load Regulators

Features

- **4.5V to 28V or 5V ±10% Input Supply Range**
- **0.6V to (0.85 x V_{IN}) Adjustable Output**
- **Adjustable 200kHz to 2MHz Switching Frequency**
- **Ability to Start into a Prebiased Load**
- **Lossless, Cycle-by-Cycle Valley Mode Current Limit with Adjustable, Temperature-Compensated Threshold**
- **Sink-Mode Current-Limit Protection**
- **Adaptive Internal Digital Soft-Start**
- **±1% Accurate Voltage Reference**
- **Internal Boost Diode**
- **Adaptive Synchronous Rectification Eliminates External Freewheeling Schottky Diode**
- **Hiccup-Mode Short-Circuit Protection**
- **Thermal Shutdown**
- **Power-Good Output and Enable Input for Power Sequencing**
- **±5% Accurate Enable Input Threshold**
- **AEC-Q100 Qualified (MAX15026B)**

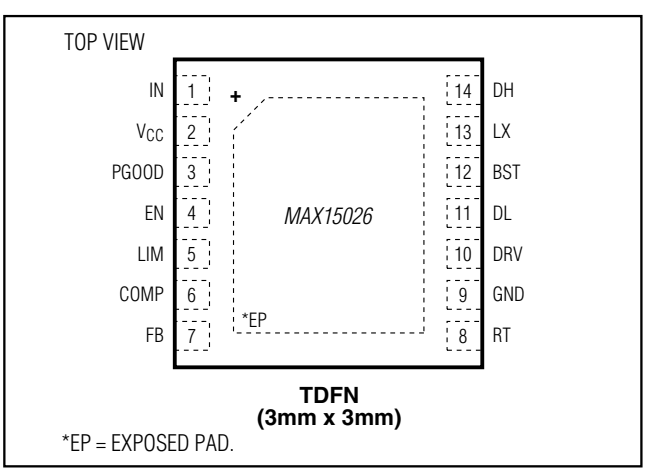
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15026BETD+	-40°C to +85°C	14 TDFN-EP*
MAX15026BETD/V+T	-40°C to +85°C	14 TDFN-EP*
MAX15026CETD+	-40°C to +85°C	14 TDFN-EP*
MAX15026BATD+	-40°C to +125°C	14 TDFN-EP*
MAX15026CATD+	-40°C to +125°C	14 TDFN-EP*
MAX15026DATD+	-40°C to +125°C	14 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad. T = Tape and reel.*
/V denotes an automotive qualified part.
MAX15026D recommended for new designs.

Pin Configuration



TDFN
(3mm x 3mm)

*EP = EXPOSED PAD.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-4108; Rev 5; 11/12

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V
BST to GND .....-0.3V to +36V
LX to GND .....-1V to +30V
EN to GND .....-0.3V to +6V
PGOOD to GND .....-0.3V to +30V
BST to LX .....-0.3V to +6V
DH to LX .....-0.3V to (V_{BST} + 0.3V)
DRV to GND .....-0.3V to +6V
DL to GND .....-0.3V to (V_{DRV} + 0.3V)
V_{CC} to GND .....-0.3V to the lower of +6V and (V_{IN} + 0.3V)
All Other Pins to GND .....-0.3V to (V_{CC} + 0.3V)
V_{CC} Short Circuit to GND .....Continuous
DRV Input Current 600mA
PGOOD Sink Current 5mA
Continuous Power Dissipation (T_A = +70°C) (Note 1)
14-Pin TDFN-EP, Multilayer Board
(derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range
MAX15026B/CETD+, MAX15026BETD/V+ .....-40°C to +85°C
MAX15026B/C/DATD+ .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Dissipation wattage values are based on still air with no heatsink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher. Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, R_{RT} = 27kΩ, R_{LIM} = 30kΩ, C_{VCC} = 4.7µF, C_{IN} = 1µF, T_A = -40°C to +85°C (MAX15026B/CETD+, MAX15026BETD/V+), T_A = T_J = -40°C to +125°C (MAX15026B/C/DATD+), unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{IN}		4.5		28	V
		V_{IN} = V_{CC} = V_{DRV}	4.5		5.5	
Quiescent Supply Current		V_{FB} = 0.9V, no switching		1.75	2.75	mA
Shutdown Supply Current	I_{IN_SBY}	EN = GND		290	500	µA
Enable to Output Delay				480		µs
V_{CC} High to Output Delay		EN = V_{CC}		375		µs
V_{CC} REGULATOR						
Output Voltage	V_{CC}	6V < V_{IN} < 28V, I_{LOAD} = 25mA	5.0	5.25	5.5	V
		V_{IN} = 12V, 1mA < I_{LOAD} < 70mA				
V_{CC} Regulator Dropout		V_{IN} = 4.5V, I_{LOAD} = 70mA			0.28	V
V_{CC} Short-Circuit Output Current		V_{IN} = 5V	100	200	300	mA
V_{CC} Undervoltage Lockout	V_{CC_UVLO}	V_{CC} rising	3.8	4.0	4.2	V
V_{CC} Undervoltage Lockout Hysteresis				400		mV
ERROR AMPLIFIER (FB, COMP)						
FB Input Voltage Set-Point	V_{FB}		585	591	597	mV
FB Input Bias Current	I_{FB}	V_{FB} = 0.6V	-250		+250	nA
FB to COMP Transconductance	g_M	I_{COMP} = ±20µA	600	1200	1800	µS
Amplifier Open-Loop Gain				80		dB
Amplifier Unity-Gain Bandwidth		Capacitor from COMP to GND = 50pF		4		MHz
$V_{COMP-RAMP}$ Minimum Voltage				160		mV
COMP Source/Sink Current	I_{COMP}	V_{COMP} = 1.4V	50	80	110	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, R_{RT} = 27kΩ, R_{LIM} = 30kΩ, C_{VCC} = 4.7µF, C_{IN} = 1µF, T_A = -40°C to +85°C (MAX15026B/CETD+, MAX15026BETD/V+), T_A = T_J = -40°C to +125°C (MAX15026B/C/DATD+), unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ENABLE (EN)							
EN Input High	V_{EN_H}	V_{EN} rising		1.14	1.20	1.26	V
EN Input Low	V_{EN_L}	V_{EN} falling		0.997	1.05	1.103	V
EN Input Leakage Current	I_{LEAK_EN}	V_{EN} = 5.5V		-1		+1	µA
OSCILLATOR							
Switching Frequency	f_{SW}	R_{RT} = 27kΩ		540	600	660	kHz
1MHz Switching Frequency		R_{RT} = 15.7kΩ		0.9	1	1.1	MHz
2MHz Switching Frequency		R_{RT} = 7.2kΩ		1.8	2.0	2.4	MHz
Switching Frequency Adjustment Range (Note 3)				200		2000	kHz
RT Voltage	V_{RT}			1.19	1.205	1.22	V
PWM Ramp Peak-to-Peak Amplitude	V_{RAMP}				1.8		V
PWM Ramp Valley	V_{VALLEY}				0.8		V
Minimum Controllable On-Time					65	100	ns
Maximum Duty Cycle		f_{SW} = 600kHz		85	88		%
Minimum Low-Side On-Time		R_{RT} = 15.7kΩ		75	110	150	ns
OUTPUT DRIVERS/DRIVER SUPPLY (DRV)							
DRV Undervoltage Lockout	V_{DRV_UVLO}	V_{DRV} rising		4.0	4.2	4.4	V
DRV Undervoltage Lockout Hysteresis					400		mV
DH On-Resistance		Low, sinking 100mA, V_{BST} = 5V			1	3	Ω
		High, sourcing 100mA, V_{BST} = 5V			1.5	4.5	
DL On-Resistance		Low, sinking 100mA, V_{BST} = 5.2V			1	3	Ω
		High, sourcing 100mA, V_{BST} = 5.2V			1.5	4.5	
DH Peak Current		C_{LOAD} = 10nF	Sinking		4		A
			Sourcing		3		
DL Peak Current		C_{LOAD} = 10nF	Sinking		4		A
			Sourcing		3		
DH/DL Break-Before-Make Time		DH at 1V (falling) to DL at 1V (rising)			10 (18, Note 5)		ns
DL/DH Break-Before-Make Time		DL at 1V (falling) to DH at 1V (rising)			10 (20, Note 6)		ns
SOFT-START							
Soft-Start Duration					2048		Switching Cycles
Reference Voltage Steps					64		Steps
CURRENT LIMIT/HICCUP							
Current-Limit Threshold Adjustment Range		Cycle-by-cycle valley current-limit threshold adjustment range valley limit = V_{LIM}/10		30		300	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, R_{RT} = 27kΩ, R_{LIM} = 30kΩ, C_{VCC} = 4.7µF, C_{IN} = 1µF, T_A = -40°C to +85°C (MAX15026B/CETD+, MAX15026BETD/V+), T_A = T_J = -40°C to +125°C (MAX15026B/C/DATD+), unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LIM Reference Current	I_{LIM}	V_{LIM} = 0.3V to 3V (Note 4)	45	50	55	µA
LIM Reference Current Tempco		V_{LIM} = 0.3V to 3V		2300		ppm/°C
Number of Consecutive Current-Limit Events to Hiccup				7		Events
Soft-Start Timeout				4096		Switching Cycles
Soft-Start Restart Timeout				8192		Switching Cycles
Hiccup Timeout		Out of soft-start		4096		Switching Cycles
Peak Low-Side Sink Current Limit		Sink limit = 1.5V, R_{LIM} = 30kΩ (Note 4)		75		mV
BOOST						
Boost Switch Resistance		V_{IN} = V_{CC} = 5V, I_{BST} = 10mA		3	8	Ω
POWER-GOOD OUTPUT						
PGOOD Threshold Rising			90	94.5	97.5	$\%V_{FB}$
PGOOD Threshold Falling			88	92	94.5	$\%V_{FB}$
PGOOD Output Leakage	I_{LEAK_PGD}	V_{IN} = V_{PGOOD} = 28V, V_{EN} = 5V, V_{FB} = 1V	-1		+1	µA
PGOOD Output Low Voltage	V_{PGOOD_L}	I_{PGOOD} = 2mA, EN = GND			0.4	V
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		+150		°C
Thermal-Shutdown Hysteresis		Temperature falling		20		°C

Note 2: All devices are 100% tested at room temperature and guaranteed by design over the specified temperature range.

Note 3: Select R_{RT} as: $R_{RT} = \frac{17.3 \times 10^9}{f_{SW} + (1x10^{-7})x(f_{SW}^2)}$ where f_{SW} is in Hertz.

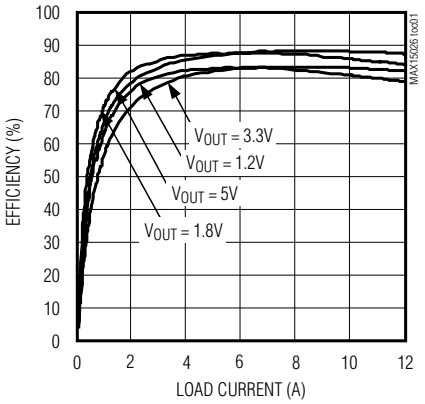
Note 4: T_A = +25°C.
Note 5: 10ns for MAX15026B, 18ns for the MAX15026C/D.
Note 6: 10ns for MAX15026B, 20ns for the MAX15026C/D.

Low-Cost, Small, 4.5V to 28V Wide Operating Range, DC-DC Synchronous Buck Controller

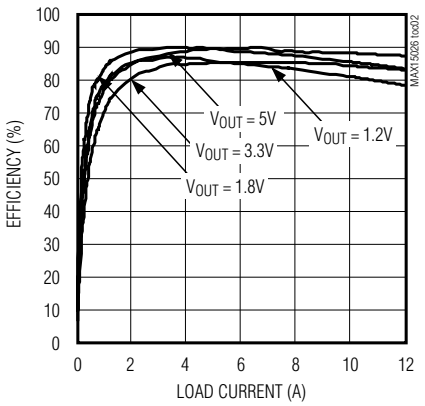
Typical Operating Characteristics

(V_{IN} = 12V, T_A = +25°C. The following TOCs are for MAX15026B/C/D, unless otherwise noted.) (See the circuit of Figure 5.)

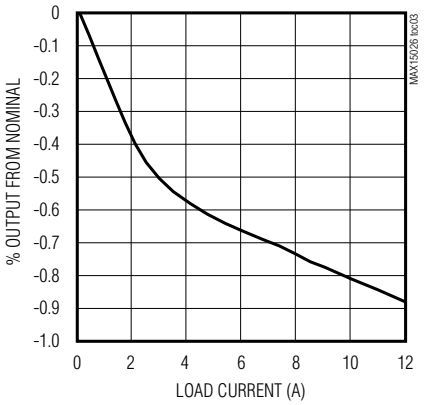
EFFICIENCY vs. LOAD CURRENT (MAX15026B/C)



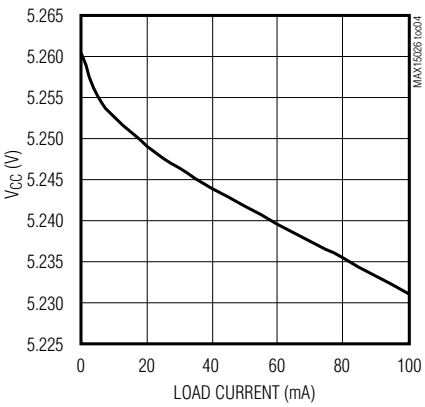
EFFICIENCY vs. LOAD CURRENT (V_{IN} = 12V, V_{CC} = V_{DRV} = 5V)



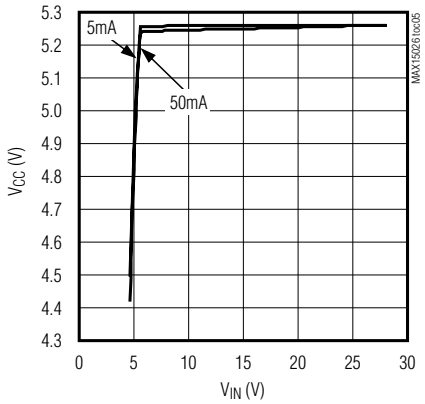
V_{OUT} vs. LOAD CURRENT



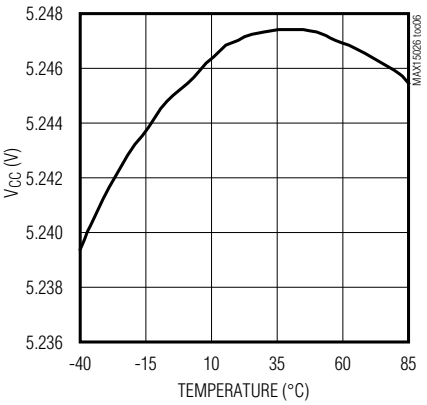
V_{CC} vs. LOAD CURRENT



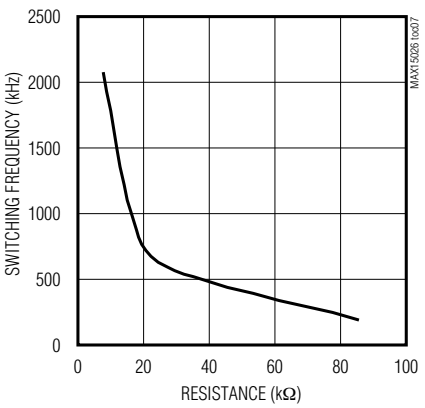
V_{CC} LINE REGULATION



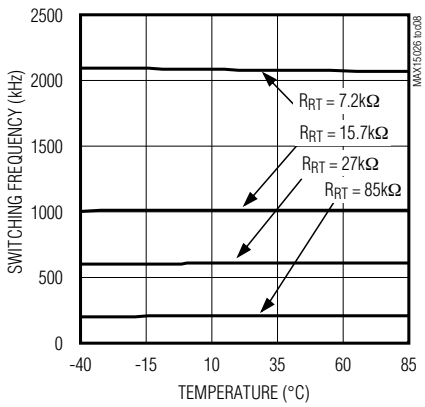
V_{CC} vs. TEMPERATURE



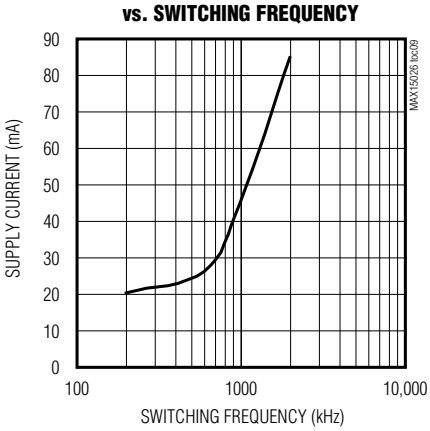
SWITCHING FREQUENCY vs. RESISTANCE



SWITCHING FREQUENCY vs. TEMPERATURE



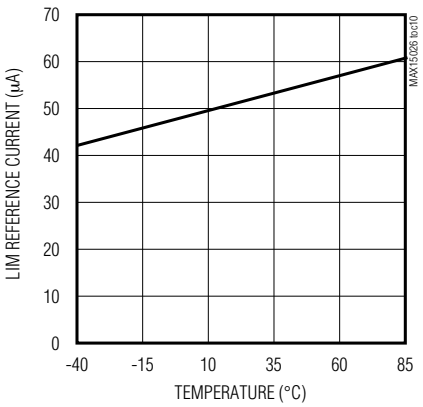
SUPPLY CURRENT vs. SWITCHING FREQUENCY



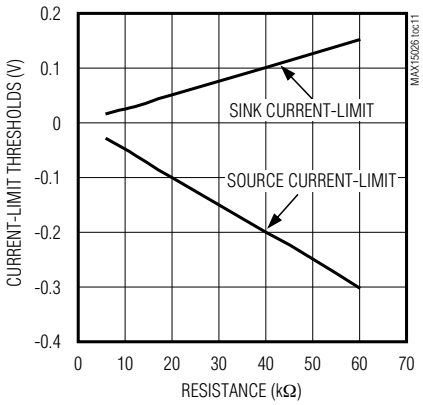
Typical Operating Characteristics (continued)

(V_{IN} = 12V, T_A = +25°C. The following TOCs are for MAX15026B/C/D, unless otherwise noted.) (See the circuit of Figure 5.)

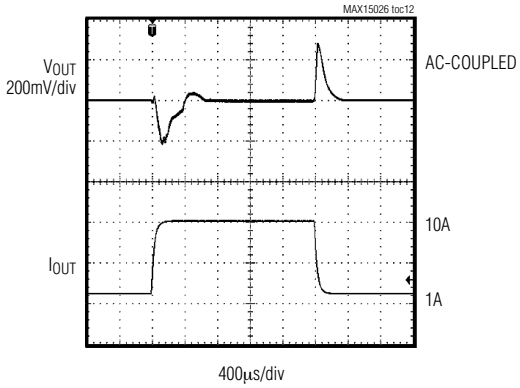
LIM REFERENCE CURRENT vs. TEMPERATURE



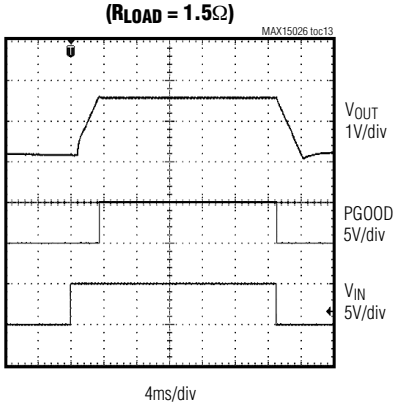
SINK AND SOURCE CURRENT-LIMIT THRESHOLDS vs. RESISTANCE (R_{ILIM})



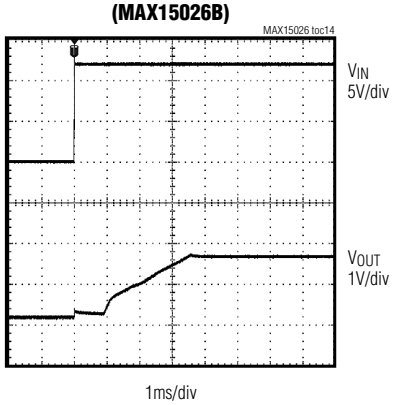
LOAD TRANSIENT ON OUT



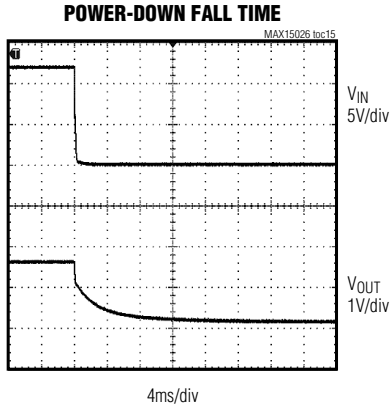
STARTUP AND DISABLE FROM EN (R_{LOAD} = 1.5Ω)



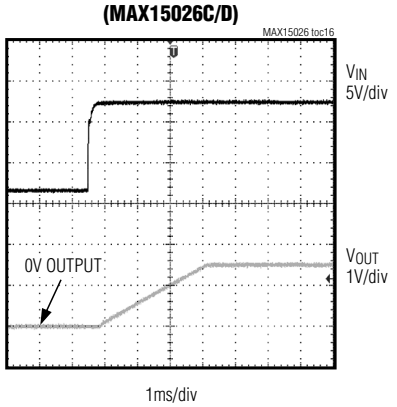
STARTUP RISE TIME (MAX15026B)



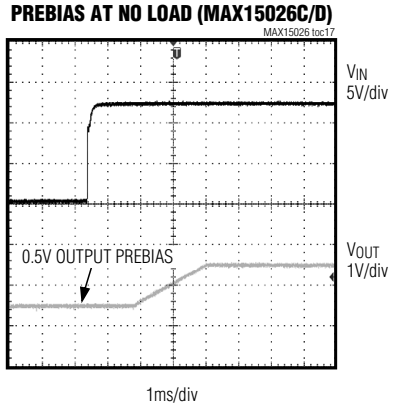
POWER-DOWN FALL TIME



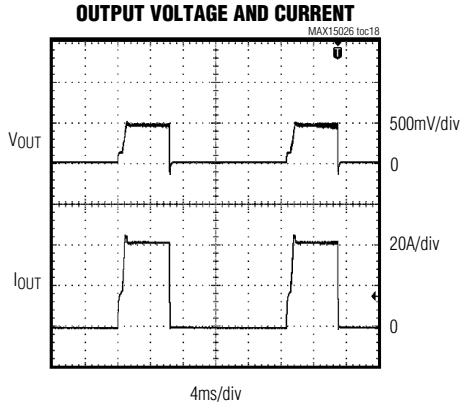
STARTUP RISE TIME (MAX15026C/D)



SOFT-START WITH 0.5V PREBIAS AT NO LOAD (MAX15026C/D)



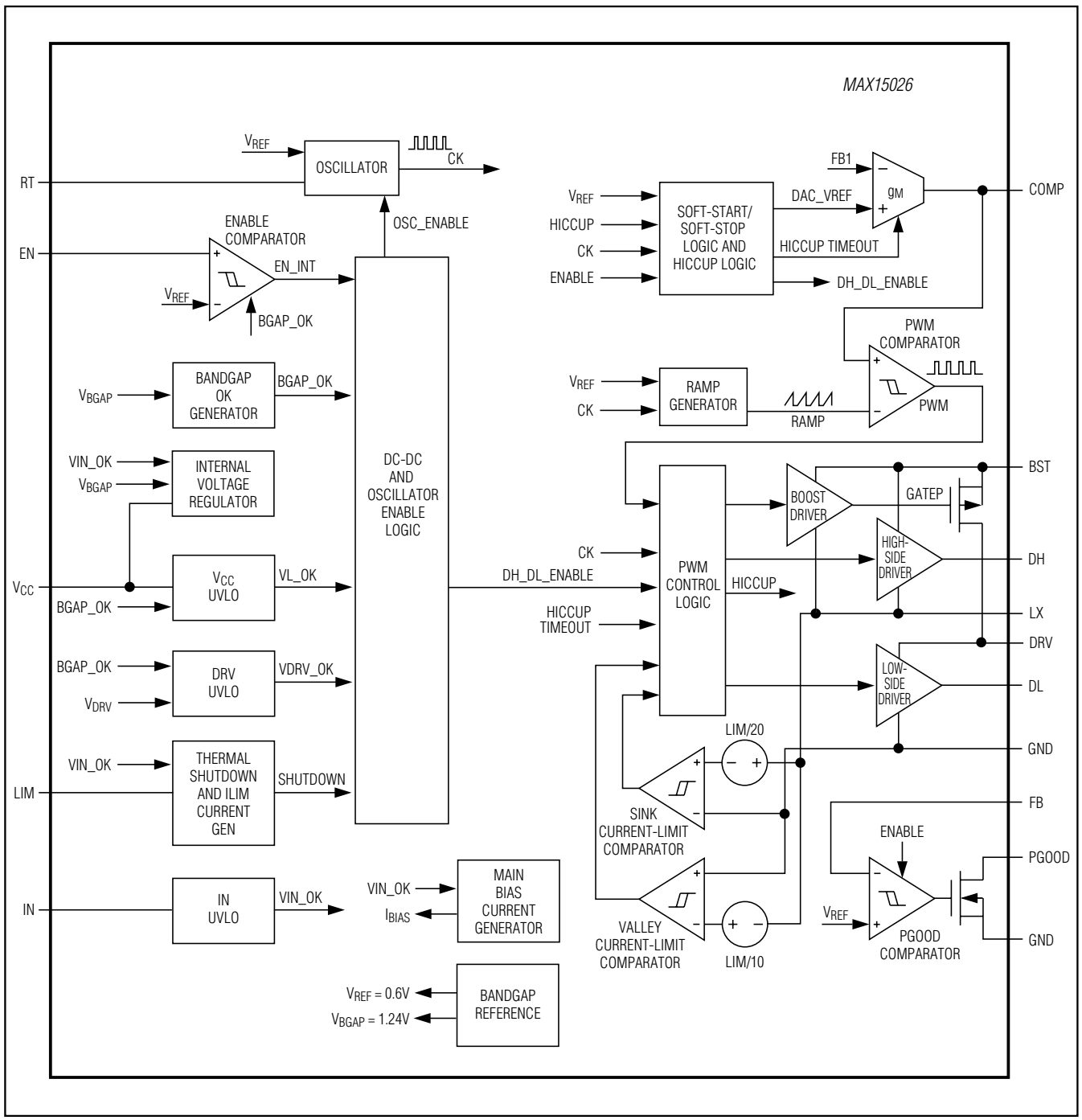
OUTPUT SHORT-CIRCUIT BEHAVIOR MONITOR OUTPUT VOLTAGE AND CURRENT



Pin Description

PIN	NAME	FUNCTION
1	IN	Regulator Input. Bypass IN to GND with a 1µF minimum ceramic capacitor. Connect IN to V_{CC} when operating in the 5V ±10% range.
2	V_{CC}	5.25V Linear Regulator Output. Bypass V_{CC} to GND with a minimum of 4.7µF low-ESR ceramic capacitor to ensure stability up to the regulated rated current when V_{CC} supplies the drive current at DRV. Bypass V_{CC} to GND when V_{CC} supplies the device core quiescent current with a 2.2µF minimum ceramic capacitor.
3	PGOOD	Open-Drain Power-Good Output. Connect PGOOD with an external resistor to any supply voltage.
4	EN	Active-High Enable Input. Pull EN to GND to disable the output. Connect EN to V_{CC} for always-on operation. EN can be used for power sequencing and as a UVLO adjustment input.
5	LIM	Current-Limit Adjustment. Connect a resistor from LIM to GND to adjust current-limit threshold from 30mV (R_{LIM} = 6kΩ) to 300mV (R_{LIM} = 60kΩ). See the *Setting the Valley Current Limit* section.
6	COMP	Compensation Input. Connect compensation network from COMP to FB or from COMP to GND. See the *Compensation* section.
7	FB	Feedback Input. Connect FB to a resistive divider between output and GND to adjust the output voltage between 0.6V and (0.85 x Input Voltage). See the *Setting the Output Voltage* section.
8	RT	Oscillator Timing Resistor Input. Connect a resistor from RT to GND to set the oscillator frequency from 200kHz to 2MHz. See the *Setting the Switching Frequency* section.
9	GND	Ground
10	DRV	Drive Supply Voltage. DRV is internally connected to the anode terminal of the internal boost diode. Bypass DRV to GND with a 2.2µF minimum ceramic capacitor (see the *Typical Application Circuits*).
11	DL	Low-Side Gate-Driver Output. DL swings from DRV to GND. DL is low during UVLO.
12	BST	Boost Flying Capacitor. Connect a ceramic capacitor with a minimum value of 100nF between BST and LX.
13	LX	External Inductor Connection. Connect LX to the switching side of the inductor. LX serves as the lower supply rail for the high-side gate driver and as a sensing input of the drain to source voltage drop of the synchronous MOSFET.
14	DH	High-Side Gate-Driver Output. DH swings from LX to BST. DH is low during UVLO.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large copper plane at GND potential to improve thermal dissipation. Do not use EP as the only GND ground connection.

Functional Diagram



Detailed Description

The MAX15026 synchronous step-down controller operates from a 4.5V to 28V input voltage range and generates an adjustable output voltage from 85% of the input voltage down to 0.6V while supporting loads up to 25A. As long as the device supply voltage is within 5.0V to 5.5V, the input power bus (V_{IN}) can be as low as 3.3V.

The MAX15026 offers adjustable switching frequency from 200kHz to 2MHz with an external resistor. The adjustable switching frequency provides design flexibility in selecting passive components. The MAX15026 adopts an adaptive synchronous rectification to eliminate an external freewheeling Schottky diode and improve efficiency. The device utilizes the on-resistance of the external low-side MOSFET as a current-sense element. The current-limit threshold voltage is resistor-adjustable from 30mV to 300mV and is temperature-compensated, so that the effects of the MOSFET $R_{DS(ON)}$ variation over temperature are reduced. This current-sensing scheme protects the external components from damage during output overloaded conditions or output short-circuit faults without requiring a current-sense resistor. Hiccup-mode current limit reduces power dissipation during short-circuit conditions. The MAX15026 includes a power-good output and an enable input with precise turn-on/-off threshold to be used for monitoring and for power sequencing.

The MAX15026 features internal digital soft-start that allows prebias startup without discharging the output. The digital soft-start function employs sink current limiting to prevent the regulator from sinking excessive current when the prebias voltage exceeds the programmed steady-state regulation level. The digital soft-start feature prevents the synchronous rectifier MOSFET and the body diode of the high-side MOSFET from experiencing dangerous levels of current while the regulator is sinking current from the output. The MAX15026 shuts down at a junction temperature of +150°C to prevent damage to the device.

DC-DC PWM Controller

The MAX15026 step-down controller uses a PWM voltage-mode control scheme (see the *Functional Diagram*). Control-loop compensation is external for providing maximum flexibility in choosing the operating frequency and output LC filter components. An internal transconductance error amplifier produces an integrated error voltage at COMP that helps to provide higher DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and a ramp generator. On the rising edge of an internal clock, the high-side n-channel MOSFET turns on and remains on until either the appropriate duty cycle or the maximum duty cycle is reached. During the on-time of the high-side MOSFET, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side n-channel MOSFET turns on. The inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, when the inductor current exceeds the selected valley current-limit threshold (see the *Current-Limit Circuit (LIM)* section), the high-side MOSFET does not turn on at the subsequent clock rising edge and the low-side MOSFET remains on to let the inductor current ramp down.

Internal 5.25V Linear Regulator

An internal linear regulator (V_{CC}) provides a 5.25V nominal supply to power the internal functions and to drive the low-side MOSFET. Connect IN and V_{CC} together when using an external 5V ±10% power supply. The maximum regulator input voltage (V_{IN}) is 28V. Bypass IN to GND with a 1µF ceramic capacitor. Bypass the output of the linear regulator (V_{CC}) with a 4.7µF ceramic capacitor to GND. The V_{CC} dropout voltage is typically 125mV. When V_{IN} is higher than 5.5V, V_{CC} is typically 5.25V. The MAX15026 also employs an undervoltage lockout circuit that disables the internal linear regulator when V_{CC} falls below 3.6V (typ). The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

The internal V_{CC} linear regulator can source up to 70mA to supply the IC, power the low-side gate driver, recharge the external boost capacitor, and supply small external loads. The current available for external loads depends on the current consumed by the MOSFET gate drivers.

For example, when switching at 600kHz, a MOSFET with 18nC total gate charge (at V_{GS} = 5V) requires (18nC x 600kHz) = 11mA. The internal control functions consume 5mA maximum. The current available for external loads is:

$$(70 - (2 \times 11) - 5)mA \cong 43mA$$

MOSFET Gate Drivers (DH, DL)

DH and DL are optimized for driving large-size n-channel power MOSFETs. Under normal operating conditions and after startup, the DL low-side drive waveform is always the complement of the DH high-side drive waveform, with controlled dead-time to prevent cross-conduction or shoot-through. An adaptive dead-time circuit monitors the DH and DL outputs and prevents the opposite-side MOSFET from turning on until the other MOSFET is fully off. Thus, the circuit allows the high-side driver to turn on only when the DL gate driver has turned off, preventing the low-side (DL) from turning on until the DH gate driver has turned off.

The adaptive driver dead-time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from DL and DH to the MOSFET gates for the adaptive dead-time circuits to function properly. The stray impedance in the gate discharge path can cause the sense circuitry to interpret the MOSFET gate as off while the V_{GS} of the MOSFET is still high. To minimize stray impedance, use very short, wide traces.

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal low-side Schottky catch diode with a low-resistance MOSFET switch. The MAX15026 features a robust internal pulldown transistor with a typical 1Ω $R_{DS(ON)}$ to drive DL low. This low on-resistance prevents DL from being pulled up during the fast rise time of the LX node, due to capacitive coupling from the drain to the gate of the low-side synchronous rectifier MOSFET.

High-Side Gate-Drive Supply (BST) and Internal Boost Switch

An internal switch between BST and DH turns on to boost the gate voltage above V_{IN} providing the necessary gate-to-source voltage to turn on the high-side MOSFET. The boost capacitor connected between BST and LX holds up the voltage across the gate driver during the high-side MOSFET on-time.

The charge lost by the boost capacitor for delivering the gate charge is replenished when the high-side MOSFET turns off and LX node goes to ground. When LX is low, an internal high-voltage switch connected between V_{DRV} and BST recharges the boost capacitor. See the *Boost Capacitor* section in the *Applications Information* to choose the right size of the boost capacitor.

Enable Input (EN), Soft-Start, and Soft-Stop

Drive EN high to turn on the MAX15026. A soft-start sequence starts to increase step-wise the reference voltage of the error amplifier. The duration of the soft-start ramp is 2048 switching cycles and the resolution is 1/64th of the steady-state regulation voltage allowing a smooth increase of the output voltage. A logic-low on EN initiates a soft-stop sequence by stepping down the reference voltage of the error amplifier. After the soft-stop sequence is completed, the MOSFET drivers are both turned off. See Figure 1. The soft-stop feature is disabled in the MAX15026D.

Connect EN to V_{CC} for always-on operation. Owing to the accurate turn-on/-off thresholds, EN can be used as UVLO adjustment input, and for power sequencing together with the PGOOD output.

When the valley current limit is reached during soft-start the MAX15026 regulates to the output impedance times the limited inductor current and turns off after 4096 clock cycles. When starting up into a large capacitive load (for example) the inrush current will not exceed the current-limit value. If the soft-start is not completed before 4096 clock cycles, the device will turn off. The device remains off for 8192 clock cycles before trying to soft-start again. This implementation allows the soft-start time to be automatically adapted to the time necessary to keep the inductor current below the limit while charging the output capacitor.

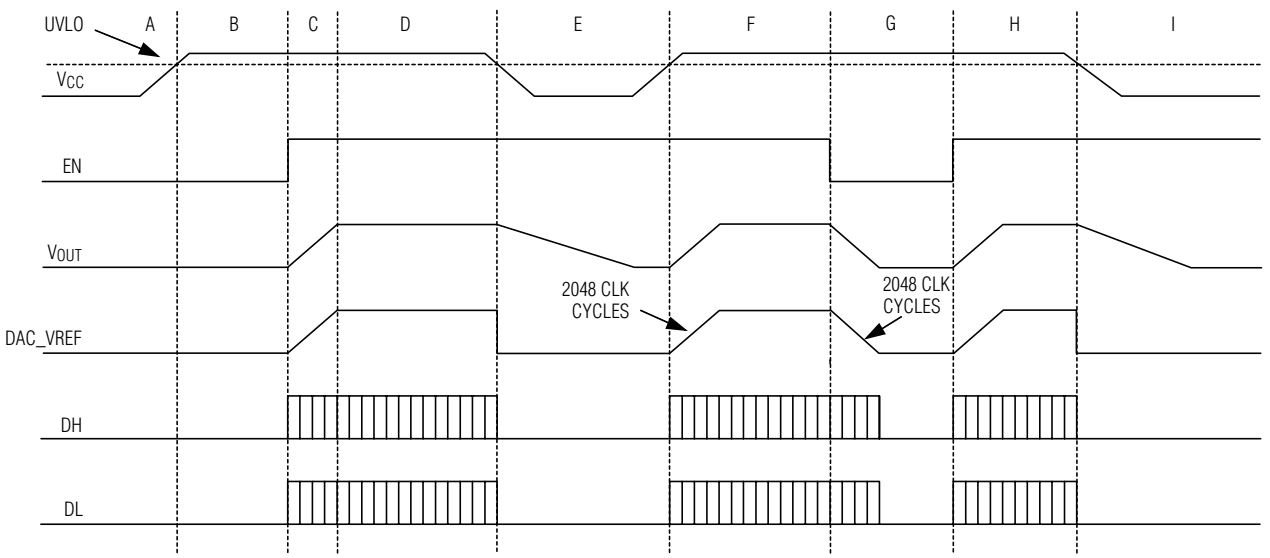
Power-Good Output (PGOOD)

The MAX15026 includes a power-good comparator to monitor the output voltage and detect the power-good threshold, fixed at 94.5% of the nominal FB voltage. The open-drain PGOOD output requires an external pullup resistor. PGOOD sinks up to 2mA of current while low.

PGOOD goes high (high-impedance) when the regulator output increases above 94.5% of the designed nominal regulated voltage. PGOOD goes low when the regulator output voltage drops to below 92% of the nominal regulated voltage. PGOOD asserts low during hiccup timeout period.

Startup into a Prebiased Output

When the MAX15026 starts into a prebiased output, DH and DL are off so that the converter does not sink current from the output. DH and DL do not start switching until the PWM comparator commands the first PWM pulse. The first PWM pulse occurs when the ramping reference voltage increases above the FB voltage.



SYMBOL	DEFINITION
UVLO	Undervoltage threshold value is provided in the *Electrical Characteristics* table.
V_{CC}	Internal 5.25V linear regulator output.
EN	Active-high enable input.
V_{OUT}	Regulator output voltage.
DAC_VREF	Regulator internal soft-start and soft-stop signal.
DH	Regulator high-side gate-driver output.
DL	Regulator low-side gate-driver output.
A	V_{CC} rising while below the UVLO threshold. EN is low.

SYMBOL	DEFINITION
B	V_{CC} is higher than the UVLO threshold. EN is low.
C	EN is pulled high. DH and DL start switching.
D	Normal operation.
E	V_{CC} drops below UVLO.
F	V_{CC} goes above the UVLO threshold. DH and DL start switching. Normal operation.
G	EN is pulled low. V_{OUT} enters soft-stop.
H	EN is pulled high. DH and DL start switching. Normal operation.
I	V_{CC} drops below UVLO.

Figure 1. Power-On/-Off Sequencing for MAX15026B/C.

Current-Limit Circuit (LIM)

The current-limit circuit employs a valley and sink current-sensing algorithm that uses the on-resistance of the low-side MOSFET as a current-sensing element, to eliminate costly sense resistors. The current-limit circuit is also temperature compensated to track the on-resistance variation of the MOSFET over temperature. The current limit is adjustable with an external resistor at LIM, and accommodates MOSFETs with a wide range of on-resistance characteristics (see the *Setting the Valley Current Limit* section). The adjustment range is from 30mV to 300mV for the valley current limit, corresponding to resistor values of 6kΩ to 60kΩ. The valley current-limit threshold across the low-side MOSFET is precisely 1/10th of the voltage at LIM, while the sink current-limit threshold is 1/20th of the voltage at LIM.

Valley current limit acts when the inductor current flows towards the load, and LX is more negative than GND during the low-side MOSFET on-time. If the magnitude of current-sense signal exceeds the valley current-limit threshold at the end of the low-side MOSFET on-time, the MAX15026 does not initiate a new PWM cycle and lets the inductor current decay in the next cycle. The controller also rolls back the internal reference voltage so that the controller finds a regulation point determined by the current-limit value and the resistance of the short. In this manner, the controller acts as a constant current source. This method greatly reduces inductor ripple current during the short event, which reduces inductor sizing restrictions, and reduces the possibility for audible noise. After a timeout, the device goes into hiccup mode. Once the short is removed, the internal reference voltage soft-starts back up to the normal reference voltage and regulation continues.

Sink current limit is implemented by monitoring the voltage drop across the low-side MOSFET when LX is more positive than GND. When the voltage drop across the low-side MOSFET exceeds 1/20th of the voltage at LIM at any time during the low-side MOSFET on-time, the low-side MOSFET turns off, and the inductor current flows from the output through the body diode of the high-side MOSFET. When the sink current limit activates, the DH/DL switching sequence is no longer complementary.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals at LX and GND. Mount the MAX15026 close to the low-side MOSFET with short, direct traces making a Kelvin-sense connection so that trace resistance does not add to the intended sense resistance of the low-side MOSFET.

Hiccup-Mode Overcurrent Protection

Hiccup-mode overcurrent protection reduces power dissipation during prolonged short-circuit or deep overload conditions. An internal three-bit counter counts up on each switching cycle when the valley current-limit threshold is reached. The counter counts down on each switching cycle when the threshold is not reached, and stops at zero (000). The counter reaches 111 (= 7 events) when the valley mode current-limit condition persists. The MAX15026 stops both DL and DH drivers and waits for 4096 switching cycles (hiccup timeout delay) before attempting a new soft-start sequence. The hiccup-mode protection remains active during the soft-start time.

Undervoltage Lockout

The MAX15026 provides an internal undervoltage lockout (UVLO) circuit to monitor the voltage on V_{CC}. The UVLO circuit prevents the MAX15026 from operating when V_{CC} is lower than V_{UVLO}. The UVLO threshold is 4V, with 400mV hysteresis to prevent chattering on the rising/falling edge of the supply voltage. DL and DH stay low to inhibit switching when the device is in undervoltage lockout.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX15026. When the junction temperature of the device exceeds +150°C, an on-chip thermal sensor shuts down the device, forcing DL and DH low, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C. The regulator shuts down and soft-start resets during thermal shutdown. Power dissipation in the LDO regulator and excessive driving losses at DH/DL trigger thermal-overload protection. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal-overload protection in normal operation.

Applications Information

Effective Input Voltage Range

The MAX15026 operates from input supplies up to 28V and regulates down to 0.6V. The minimum voltage conversion ratio (V_{OUT}/V_{IN}) is limited by the minimum controllable on-time. For proper fixed-frequency PWM operation, the voltage conversion ratio must obey the following condition,

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(MIN)} \times f_{SW}$$

where $t_{ON(MIN)}$ is 125ns and f_{SW} is the switching frequency in Hertz. Pulse-skipping occurs to decrease the effective duty cycle when the desired voltage conversion does not meet the above condition. Decrease the switching frequency or lower V_{IN} to avoid pulse skipping.

The maximum voltage conversion ratio is limited by the maximum duty cycle (D_{max}):

$$\frac{V_{OUT}}{V_{IN}} < D_{max} - \frac{D_{max} \times V_{DROP2} + (1 - D_{max}) \times V_{DROP1}}{V_{IN}}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistance. V_{DROP2} is the sum of the resistance in the charging path, including high-side switch, inductor, and PCB resistance. In practice, provide adequate margin to the above conditions for good load-transient response.

Setting the Output Voltage

Set the MAX15026 output voltage by connecting a resistive divider from the output to FB to GND (Figure 2). Select R_2 from between 1kΩ and 50kΩ. Calculate R_1 with the following equation:

$$R_1 = R_2 \left[\left(\frac{V_{OUT}}{V_{FB}} \right) - 1 \right]$$

where V_{FB} = 0.591V (see the *Electrical Characteristics* table) and V_{OUT} can range from 0.591V to (0.85 x V_{IN}).

Resistor R_1 also plays a role in the design of the Type III compensation network. Review the values of R_1 and R_2 when using a Type III compensation network (see the *Type III Compensation Network (See Figure 4)* section).

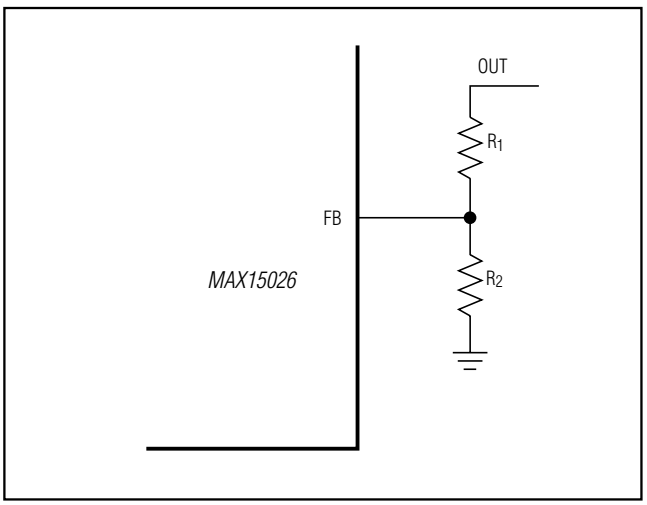


Figure 2. Adjustable Output Voltage

Setting the Switching Frequency

An external resistor connecting RT to GND sets the switching frequency (f_{SW}). The relationship between f_{SW} and R_{RT} is:

$$R_{RT} = \frac{17.3 \times 10^9}{f_{SW} + (1 \times 10^{-7}) \times (f_{SW}^2)}$$

where f_{SW} is in Hz and R_{RT} is in Ω. For example, a 600kHz switching frequency is set with R_{RT} = 27.2kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15026: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). To determine the inductance value, select the ratio of inductor peak-to-peak AC current to DC average current (LIR) first. For LIR values which are too high, the RMS currents are high, and therefore I^2R losses are high. Use high-valued inductors to achieve low LIR values. Typically, inductance is proportional to resistance for a given package type, which again makes I^2R losses high for very low LIR values. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows,

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUT} LIR}$$

where V_{IN}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{RT} (see the *Setting the Switching Frequency* section). The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but also improve transient response and reduce efficiency due to higher peak currents. On the other hand, higher inductance increases efficiency by reducing the RMS current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The saturation current rating (I_{SAT}) must be high enough to ensure that saturation can occur only above the maximum current-limit value ($I_{CL(MAX)}$), given the tolerance of the on-resistance of the low-side MOSFET and of the LIM reference current (I_{LIM}). Combining these conditions, select an inductor with a saturation current (I_{SAT}) of:

$$I_{SAT} \geq 1.35 \times I_{CL(TYP)}$$

where $I_{CL(TYP)}$ is the typical current-limit set-point. The factor 1.35 includes $R_{DS(ON)}$ variation of 25% and 10% for the LIM reference current error. A variety of inductors from different manufacturers are available to meet this requirement (for example, Coilcraft MSS1278-142ML and other inductors from the same series).

Setting the Valley Current Limit

The minimum current-limit threshold must be high enough to support the maximum expected load current with the worst-case low-side MOSFET on-resistance value as the $R_{DS(ON)}$ of the low-side MOSFET is used as the current-sense element. The inductor's valley current occurs at $I_{LOAD(MAX)}$ minus one half of the ripple current. The minimum value of the current-limit threshold voltage (V_{ITH}) must be higher than the voltage on the low-side MOSFET during the ripple-current valley:

$$V_{ITH} > R_{DS(ON,MAX)} \times I_{LOAD(MAX)} \times \left(1 - \frac{LIR}{2}\right)$$

where $R_{DS(ON)}$ is the on-resistance of the low-side MOSFET in ohms. Use the maximum value for $R_{DS(ON)}$ from the data sheet of the low-side MOSFET.

Connect an external resistor (R_{LIM}) from LIM to GND to adjust the current-limit threshold. The relationship between the current-limit threshold (V_{ITH}) and R_{LIM} is:

$$R_{LIM} = \frac{10 \times V_{ITH}}{50\mu A}$$

where R_{LIM} is in kΩ and V_{ITH} is in mV.

An R_{LIM} resistance range of 6kΩ to 60kΩ corresponds to a current-limit threshold of 30mV to 300mV. Use 1% tolerance resistors when adjusting the current limit to minimize error in the current-limit threshold.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents as defined by the following equation,

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} attains a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$. For most applications, non-tantalum capacitors (ceramic, aluminum, polymer, or OS-CON) are preferred at the inputs due to the robustness of non-tantalum capacitors to accommodate high inrush currents of systems being powered from very low-impedance sources. Additionally, two (or more) smaller-value low-ESR capacitors can be connected in parallel for lower cost.

Output Capacitor

The key selection parameters for the output capacitor are capacitance value, ESR, and voltage rating. These parameters affect the overall stability, output ripple voltage, and transient response. The output ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current flowing into and out of the capacitor:

$$\Delta V_{RIPPLE} \cong \Delta V_{ESR} + \Delta V_Q$$

The output voltage ripple as a consequence of the ESR and the output capacitance is:

$$\Delta V_{ESR} = I_{P-P} \times ESR$$

$$\Delta V_Q = \frac{I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current ripple (see the *Inductor Selection* section). Use these equations for initial capacitor selection. Decide on the final values by testing a prototype or an evaluation circuit.

Check the output capacitor against load-transient response requirements. The allowable deviation of the output voltage during fast load transients determines the capacitor output capacitance, ESR, and equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a higher duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter (see the *Compensation* section). The resistive drop across the ESR of the output capacitor, the voltage drop across the ESL (ΔV_{ESL}) of the capacitor, and the capacitor discharge, cause a voltage droop during the load step.

Use a combination of low-ESR tantalum/aluminum electrolytic and ceramic capacitors for improved transient load and voltage ripple performance. Nonleaded capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output voltage deviation below the tolerable limits of the load. Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

$$t_{RESPONSE} \cong \frac{1}{3 \times f_O}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, $t_{RESPONSE}$ is the response time of the controller and f_O is the closed-loop crossover frequency.

Compensation

The MAX15026 provides an internal transconductance amplifier with the inverting input and the output available for external frequency compensation. The flexibility of external compensation offers a wide selection of output filtering components, especially the output capacitor. Use high-ESR aluminum electrolytic capacitors for cost-sensitive applications. Use low-ESR tantalum or ceramic capacitors at the output for size sensitive applications. The high switching frequency of the MAX15026 allows the use of ceramic capacitors at the output. Choose all passive power components to meet the output ripple, component size, and component cost

requirements. Choose the small-signal components for the error amplifier to achieve the desired closed-loop bandwidth and phase margin.

To choose the appropriate compensation network type, the power-supply poles and zeros, the zero crossover frequency, and the type of the output capacitor must be determined.

In a buck converter, the LC filter in the output stage introduces a pair of complex poles at the following frequency:

$$f_{PO} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The output capacitor introduces a zero at:

$$f_{ZO} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

where ESR is the equivalent series resistance of the output capacitor.

The loop-gain crossover frequency (f_O), where the loop gain equals 1 (0dB) should be set below 1/10th of the switching frequency:

$$f_O \le \frac{f_{SW}}{10}$$

Choosing a lower crossover frequency reduces the effects of noise pick-up into the feedback loop, such as jittery duty cycle.

To maintain a stable system, two stability criteria must be met:

1) The phase shift at the crossover frequency f_O, must be less than 180°. In other words, the phase margin of the loop must be greater than zero.
2) The gain at the frequency where the phase shift is -180° (gain margin) must be less than 1.

Maintain a phase margin of around 60° to achieve a robust loop stability and well-behaved transient response.

When using an electrolytic or large-ESR tantalum output capacitor the capacitor ESR zero f_{ZO} typically occurs between the LC poles and the crossover frequency f_O ($f_{PO} < f_{ZO} < f_O$). Choose Type II (PI—proportional-integral) compensation network.

When using a ceramic or low-ESR tantalum output capacitor, the capacitor ESR zero typically occurs above the desired crossover frequency f_O, that is $f_{PO} < f_O < f_{ZO}$. Choose Type III (PID—proportional, integral, and derivative) compensation network.

Type II Compensation Network (Figure 3)

If f_{ZO} is lower than f_O and close to f_{PO}, the phase lead of the capacitor ESR zero almost cancels the phase loss of one of the complex poles of the LC filter around the crossover frequency. Use a Type II compensation network with a midband zero and a high-frequency pole to stabilize the loop. In Figure 3, R_F and C_F introduce a midband zero (f_{Z1}). R_F and C_{CF} in the Type II compensation network provide a high-frequency pole (f_{P1}), which mitigates the effects of the output high-frequency ripple.

Follow the instructions below to calculate the component values for the Type II compensation network in Figure 3:

1) Calculate the gain of the modulator ($GAIN_{MOD}$), comprised of the regulator's pulse-width modulator, LC filter, feedback divider, and associated circuitry at the crossover frequency:

$$GAIN_{MOD} = \frac{V_{IN}}{V_{RAMP}} \times \frac{ESR}{(2\pi \times f_O \times L_{OUT})} \times \frac{V_{FB}}{V_{OUT}}$$

where V_{IN} is the input voltage of the regulator, V_{RAMP} is the amplitude of the ramp in the pulse-width modulator, V_{FB} is the FB input voltage set-point (0.591V typically, see the *Electrical Characteristics* table), and V_{OUT} is the desired output voltage.

The gain of the error amplifier ($GAIN_{EA}$) in midband frequencies is:

$$GAIN_{EA} = g_M \times R_F$$

where g_M is the transconductance of the error amplifier.

The total loop gain, which is the product of the modulator gain and the error amplifier gain at f_O, is 1.

$$GAIN_{MOD} \times GAIN_{EA} = 1$$

So:

$$\frac{V_{IN}}{V_{RAMP}} \times \frac{ESR}{(2\pi \times f_O \times L_{OUT})} \times \frac{V_{FB}}{V_{OUT}} \times g_M \times R_F = 1$$

Solving for R_F:

$$R_F = \frac{V_{RAMP} \times (2\pi \times f_O \times L_{OUT}) \times V_{OUT}}{V_{FB} \times V_{IN} \times g_M \times ESR}$$

2) Set a midband zero (f_{Z1}) at 0.75 x f_{PO} (to cancel one of the LC poles):

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F} = 0.75 \times f_{PO}$$

Solving for C_F:

$$C_F = \frac{1}{2\pi \times R_F \times f_{PO} \times 0.75}$$

3) Place a high-frequency pole at f_{P1} = 0.5 x f_{SW} (to attenuate the ripple at the switching frequency, f_{SW}) and calculate C_{CF} using the following equation:

$$C_{CF} = \frac{1}{\pi \times R_F \times f_{SW} - \frac{1}{C_F}}$$

Type III Compensation Network (See Figure 4)

When using a low-ESR tantalum or ceramic type, the ESR-induced zero frequency is usually above the targeted zero crossover frequency (f_O). Use Type III compensation. Type III compensation provides three poles and two zeros at the following frequencies:

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F}$$

$$f_{Z2} = \frac{1}{2\pi \times C_I \times (R_1 + R_I)}$$

Two midband zeros (f_{Z1} and f_{Z2}) cancel the pair of complex poles introduced by the LC filter:

$$f_{P1} = 0$$

f_{P1} introduces a pole at zero frequency (integrator) for nulling DC output voltage errors:

$$f_{P2} = \frac{1}{2\pi \times R_I \times C_I}$$

Depending on the location of the ESR zero (f_{ZO}), use f_{P2} to cancel f_{ZO}, or to provide additional attenuation of the high-frequency output ripple:

$$f_{P3} = \frac{1}{2\pi \times R_F \times \frac{C_F \times C_{CF}}{C_F + C_{CF}}}$$

f_{P3} attenuates the high-frequency output ripple.

Place the zeros and poles so the phase margin peaks around f_O.

Ensure that $R_F >> 2/g_M$ and the parallel resistance of R_1, R_2, and R_I is greater than $1/g_M$. Otherwise, a 180° phase shift is introduced to the response making the loop unstable.

Use the following compensation procedure:

1) With $R_F \geq 10k\Omega$, place the first zero (f_{Z1}) at 0.8 x f_{PO}.

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F} = 0.8 \times f_{PO}$$

So:

$$GAIN_{MOD} = \frac{V_{IN}}{V_{RAMP}} \times \frac{}{(2\pi}$$

2) The gain of the modulator ($GAIN_{MOD}$), comprises the pulse-width modulator, LC filter, feedback divider, and associated circuitry at the crossover frequency is:

$$GAIN_{MOD} = \frac{V_{IN}}{V_{RAMP}} \times \frac{1}{(2\pi \times f_O)^2 \times L_{OUT} \times C_{OUT}}$$

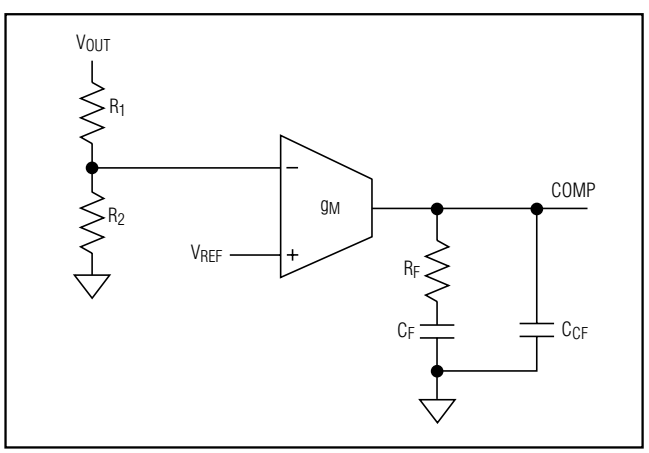


Figure 3. Type II Compensation Network

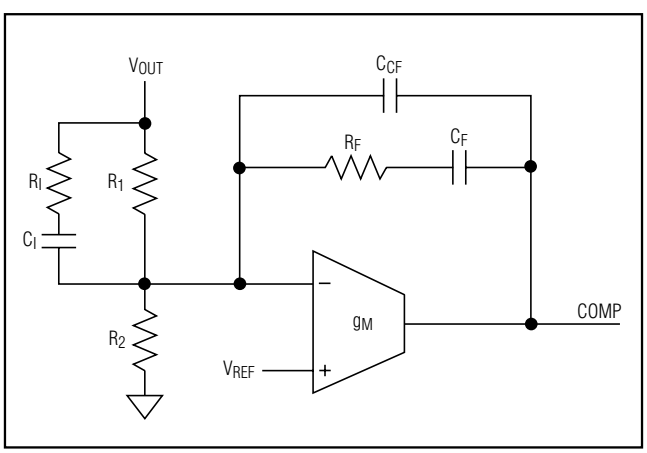


Figure 4. Type III Compensation Network

The gain of the error amplifier ($GAIN_{EA}$) in midband frequencies is:

$$GAIN_{EA} = 2\pi \times f_O \times C_1 \times R_F$$

The total loop gain as the product of the modulator gain and the error amplifier gain at f_O is 1.

$$GAIN_{MOD} \times GAIN_{EA} = 1$$

So:

$$\frac{V_{IN}}{V_{RAMP}} \times \frac{1}{(2\pi \times f_O)^2 \times C_{OUT} \times L_{OUT}}$$

Solving for C_I:

$$C_I = \frac{V_{RAMP} \times (2\pi \times f_O \times L_{OUT} \times C_{OUT})}{V_{IN} \times R_F}$$

3) Use the second pole (f_{P2}) to cancel f_{ZO} when $f_{PO} < f_O < f_{ZO} < f_{SW}/2$. The frequency response of the loop gain does not flatten out soon after the 0dB crossover, and maintains a -20dB/decade slope up to 1/2 of the switching frequency. This is likely to occur if the output capacitor is a low-ESR tantalum. Set $f_{P2} = f_{ZO}$.

When using a ceramic capacitor, the capacitor ESR zero f_{ZO} is likely to be located even above 1/2 the switching frequency, $f_{PO} < f_O < f_{SW}/2 < f_{ZO}$. In this case, place the frequency of the second pole (f_{P2}) high enough to not significantly erode the phase margin at the crossover frequency. For example, set f_{P2} at 5 x f_O so that the contribution to phase loss at the crossover frequency f_O is only about 11°:

$$f_{P2} = 5 \times f_{PO}$$

Once f_{P2} is known, calculate R_I:

$$R_I = \frac{1}{2\pi \times f_{P2} \times C_I}$$

4) Place the second zero (f_{Z2}) at 0.2 x f_O or at f_{PO}, whichever is lower, and calculate R_1 using the following equation:

$$R_1 = \frac{1}{2\pi \times f_{Z2} \times C_I} - R_I$$

5) Place the third pole (f_{P3}) at 1/2 the switching frequency and calculate C_{CF}:

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F) - 1}$$

6) Calculate R_2 as:

$$R_2 = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_1$$

MOSFET Selection

The MAX15026 step-down controller drives two external logic-level n-channel MOSFETs. The key selection parameters to choose these MOSFETs include:

- On-Resistance ($R_{DS(ON)}$)
- Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)
- Minimum Threshold Voltage ($V_{TH(MIN)}$)
- Total Gate Charge (Q_G)
- Reverse Transfer Capacitance (C_{RSS})
- Power Dissipation

The two n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V. For maximum efficiency, choose a high-side MOSFET that has conduction losses equal to the switching losses at the typical input voltage. Ensure that the conduction losses at minimum input voltage do not exceed the MOSFET package thermal limits, or violate the overall thermal budget. Also, ensure that the conduction losses plus switching losses at the maximum input voltage do not exceed package ratings or violate the overall thermal budget. Ensure that the DL gate driver can drive the low-side MOSFET. In particular, check that the dv/dt caused by the high-side MOSFET turning on does not pull up the low-side MOSFET gate through the drain-to-gate capacitance of the low-side MOSFET, which is the most frequent cause of cross-conduction problems.

Check power dissipation when using the internal linear regulator to power the gate drivers. Select MOSFETs with low gate charge so that V_{CC} can power both drivers without overheating the device.

$$P_{DRIVE} = V_{CC} \times Q_{G_TOTAL} \times f_{SW}$$

where Q_{G_TOTAL} is the sum of the gate charges of the two external MOSFETs.

Boost Capacitor

The MAX15026 uses a bootstrap circuit to generate the necessary gate-to-source voltage to turn on the high-side MOSFET. The selected n-channel high-side MOSFET determines the appropriate boost capacitance value (C_{BST} in the *Typical Application Circuits*) according to the following equation:

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}}$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} so the available gate-drive voltage is not significantly degraded (e.g. ΔV_{BST} = 100mV to 300mV) when determining C_{BST}. Use a low-ESR ceramic capacitor as the boost flying capacitor with a minimum value of 100nF.

Power Dissipation

The maximum power dissipation of the device depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the device package, PCB copper area, other thermal mass, and airflow.

The power dissipated into the package (P_T) depends on the supply configuration (see the *Typical Application Circuits*). Use the following equation to calculate power dissipation:

$$P_T = (V_{IN} - V_{CC}) \times I_{LDO} + V_{DRV} \times I_{DRV} + V_{CC} \times I_{IN}$$

where I_{LDO} is the current supplied by the internal regulator, I_{DRV} is the supply current consumed by the drivers at DRV, and I_{IN} is the supply current of the MAX15026 without the contribution of the I_{DRV}, as given in the *Typical Operating Characteristics*. For example, in the application circuit of Figure 5, $I_{LDO} = I_{DRV} + I_{IN}$ and $V_{DRV} = V_{CC}$ so that $P_T = V_{IN} \times (I_{DRV} + I_{IN})$.

Use the following equation to estimate the temperature rise of the die:

$$T_J = T_A + (P_T \times \theta_{JA})$$

where θ_{JA} is the junction-to-ambient thermal impedance of the package, P_T is power dissipated in the device, and T_A is the ambient temperature. The θ_{JA} is 24.4°C/W for 14-pin TDFN package on multilayer boards, with the conditions specified by the respective JEDEC standards (JESD51-5, JESD51-7). An accurate estimation of the junction temperature requires a direct measurement of the case temperature (T_C) when actual operating conditions significantly deviate from those described in the JEDEC standards. The junction temperature is then:

$$T_J = T_C + (P_T \times \theta_{JC})$$

Use 8.7°C/W as θ_{JC} thermal impedance for the 14-pin TDFN package. The case-to-ambient thermal impedance (θ_{CA}) is dependent on how well the heat is transferred from the PCB to the ambient. Solder the exposed pad of the TDFN package to a large copper area to spread heat through the board surface, minimizing the case-to-ambient thermal impedance. Use large copper areas to keep the PCB temperature low.

PCB Layout Guidelines

Place all power components on the top side of the board, and run the power stage currents using traces or copper fills on the top side only. Make a star connection on the top side of traces to GND to minimize voltage drops in signal paths.

Keep the power traces and load connections short, especially at the ground terminals. This practice is essential for high efficiency and jitter-free operation. Use thick copper PCBs (2oz or above) to enhance efficiency.

Place the MAX15026 adjacent to the synchronous rectifier MOSFET, preferably on the back side, to keep LX, GND, DH, and DL traces short and wide. Use multiple small vias to route these signals from the top to the bottom side. Use an internal quiet copper plane to shield the analog components on the bottom side from the power components on the top side.

Make the MAX15026 ground connections as follows: create a small analog ground plane near the device. Connect this plane to GND and use this plane for the ground connection for the V_{IN} bypass capacitor, compensation components, feedback dividers, V_{CC} capacitor, RT resistor, and LIM resistor.

Use Kelvin sense connections for LX and GND to the synchronous rectifier MOSFET for current limiting to guarantee the current-limit accuracy.

Route high-speed switching nodes (BST, LX, DH, and DL) away from the sensitive analog areas (RT, COMP, LIM, and FB). Group all GND-referred and feedback components close to the device. Keep the FB and compensation network as small as possible to prevent noise pickup.

Typical Application Circuits

Single 4.5V to 28V Supply Operation

Figure 5 shows an application circuit for a single 4.5V to 28V power-supply operation.

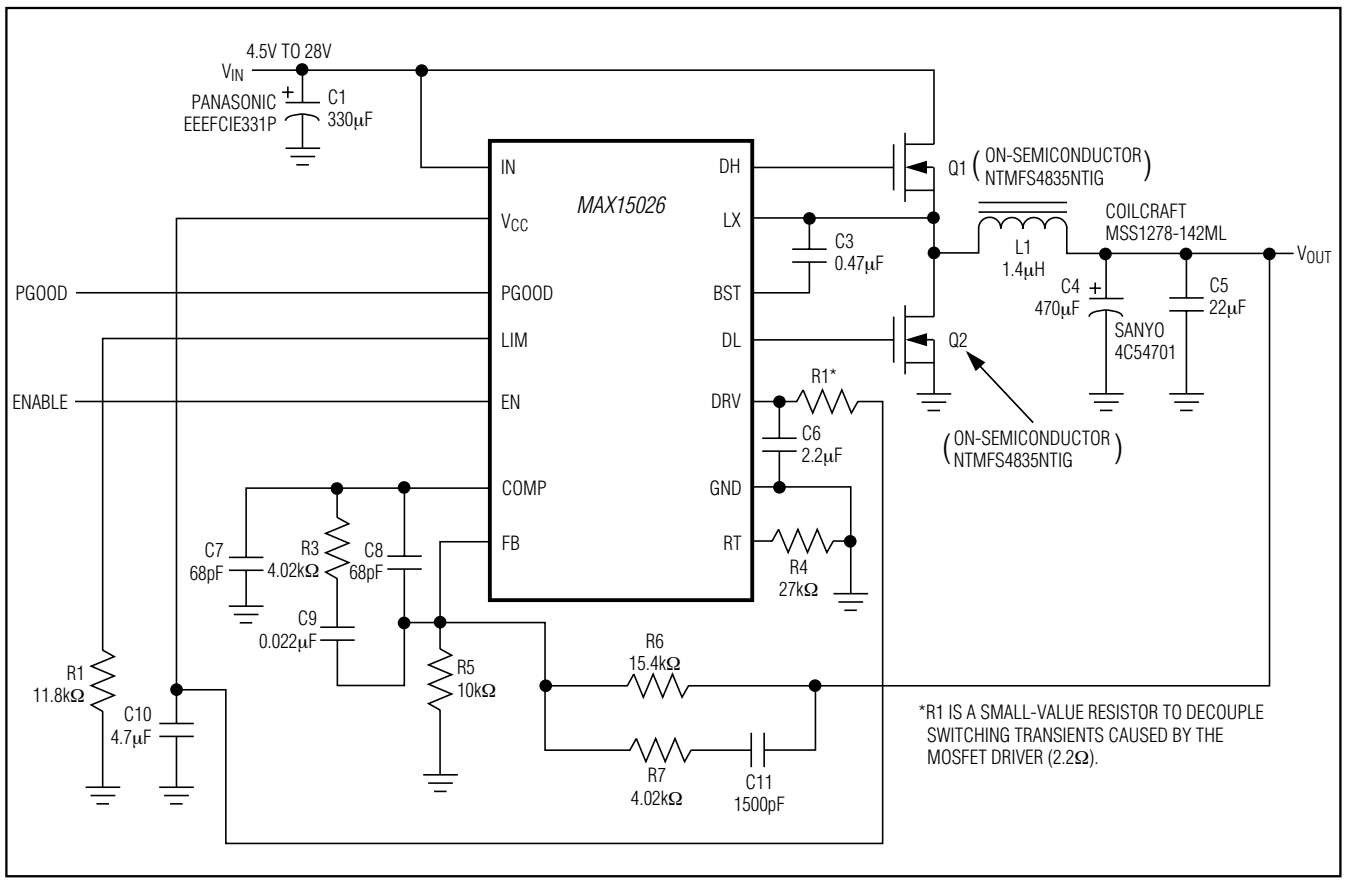


Figure 5. V_{IN} = 4.5V to 28V

Typical Application Circuits (continued)

Single 4.5V to 5.5V Supply Operation

Figure 6 shows an application circuit for a single 4.5V to 5.5V power-supply operation.

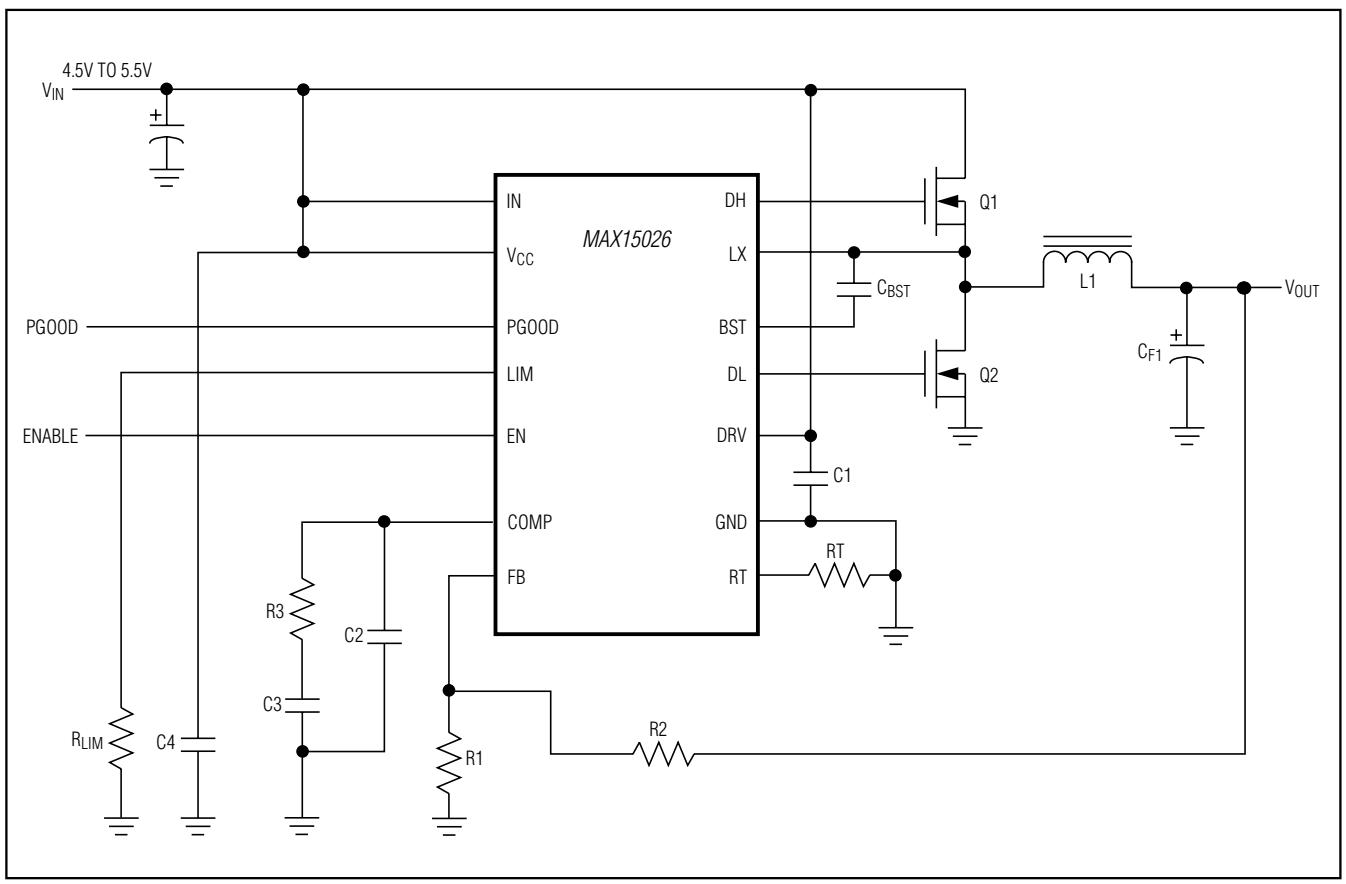


Figure 6. V_{CC} = V_{IN} = V_{DRV} = 4.5V to 5.5V

Low-Cost, Small, 4.5V to 28V Wide Operating Range, DC-DC Synchronous Buck Controller

Typical Application Circuits (continued)

Auxiliary 5V Supply Operation

Figure 7 shows an application circuit for a +12V supply to drive the external MOSFETs and an auxiliary +5V supply to power the device.

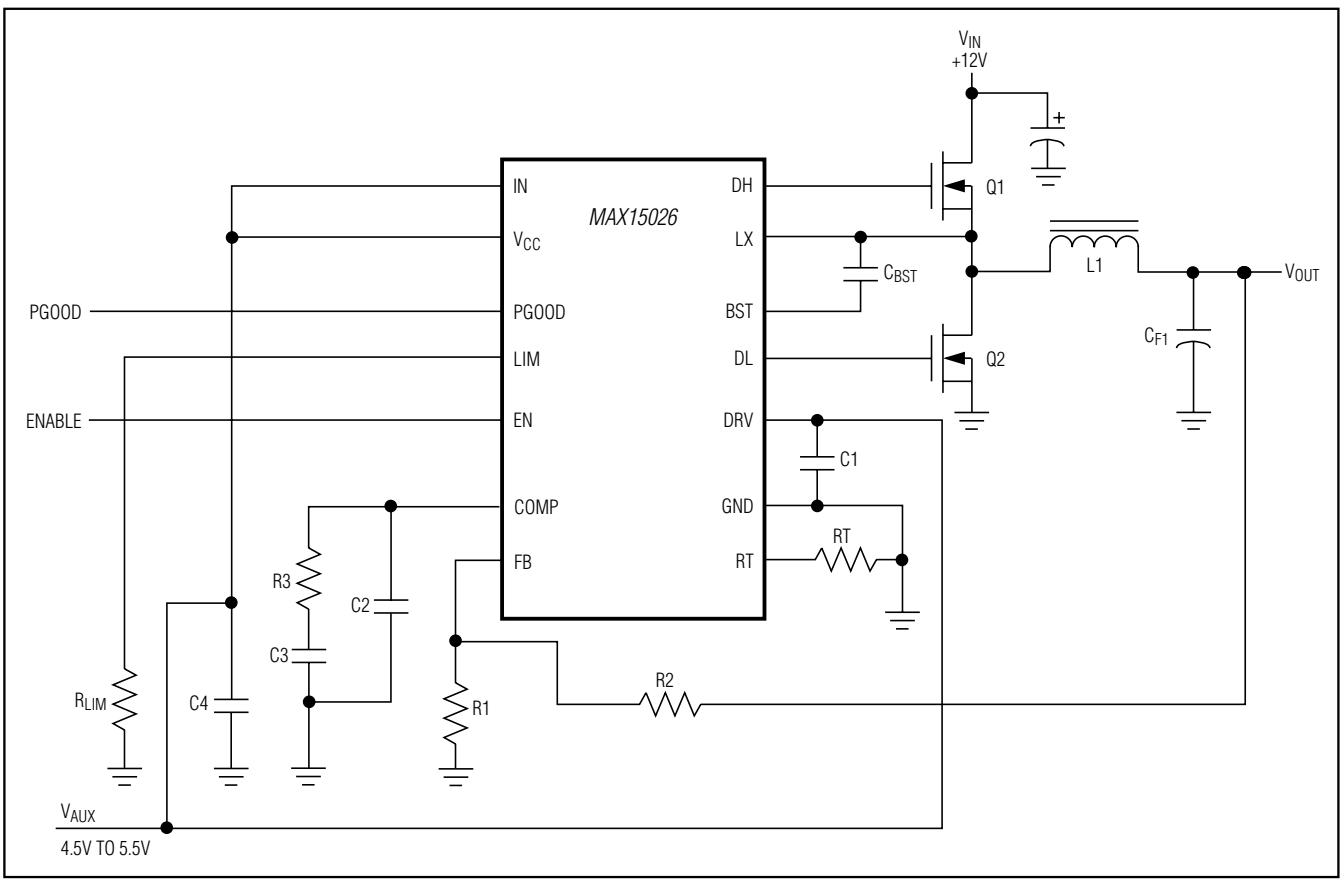


Figure 7. Operation with Auxiliary 5V Supply

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TDFN-EP	T1433+2	21-0137	90-0063

Low-Cost, Small, 4.5V to 28V Wide Operating Range, DC-DC Synchronous Buck Controller

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	5/09	Revised *General Description*, *Ordering Information*, *Absolute Maximum Ratings*, *Electrical Characteristics*, *Power-Good Output (PGOOD)* section, and *Typical Application Circuits*	1–4, 10, 15, 19
2	9/10	Added MAX15026C; revised *General Description*, *Ordering Information*, *Electrical Characteristics*, *Typical Operating Characteristics*, and *Startup into a Prebiased Output* sections	1–6, 10
3	4/11	Added automotive part to *Ordering Information*, *Absolute Maximum Ratings*, and *Electrical Characteristics*	1, 2, 3
4	2/12	Design modified to meet customer requirements and new OPN added to *Ordering Information*	1–6, 10, 11
5	11/12	Changed recommended part number for new designs to MAX15026D	1

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