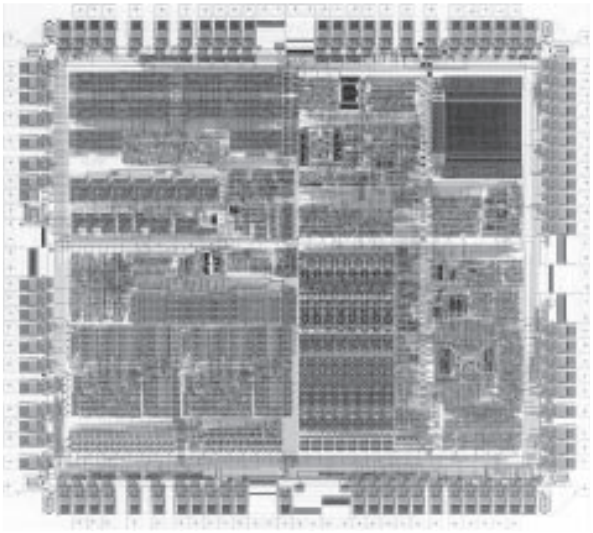
# 80C186EB/80C188E B AND 80L186EB/80L188EB 16-BIT HIGH-INTEGRATION EMBEDDED PROCESSORS

- Full Static Operation
- True CMOS Inputs and Outputs

- Integrated Feature Set
  - Low-Power Static CPU Core
  - Two Independent UARTs each with an Integral Baud Rate Generator
  - Two 8-Bit Multiplexed I/O Ports
  - Programmable Interrupt Controller
  - Three Programmable 16-Bit Timer/Counters
  - Clock Generator
  - Ten Programmable Chip Selects with Integral Wait-State Generator
  - Memory Refresh Control Unit
  - System Level Testing Support (ONCE Mode)
- Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O
- Speed Versions Available (5V):
  - 25 MHz (80C186EB25/80C188EB25)
  - 20 MHz (80C186EB20/80C188EB20)
  - 13 MHz (80C186EB13/80C188EB13)
- Available in Extended Temperature Range (- 40°C to + 85°C)
- Speed Versions Available (3V):
  - 16 MHz (80L186EB16/80L188EB16)
  - 13 MHz (80L186EB13/80L188EB13)
- Low-Power Operating Modes:
  - Idle Mode Freezes CPU Clocks but keeps Peripherals Active
  - Powerdown Mode Freezes All Internal Clocks
- Supports 80C187 Numeric Coprocessor Interface (80C186EB PLCC Only)
- Available In:
  - 80-Pin Quad Flat Pack (QFP)
  - 84-Pin Plastic Leaded Chip Carrier (PLCC)
  - 80-Pin Shrink Quad Flat Pack (SQFP)

The 80C186EB is a second generation CHMOS High-Integration microprocessor. It has features that are new to the 80C186 family and include a STATIC CPU core, an enhanced Chip Select decode unit, two independent Serial Channels, I/O ports, and the capability of Idle or Powerdown low power modes.



272433–1

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July, 2004 Order Number: 272433-006

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# 80C186EB/80C188EB and 80L186EB/80L188EB 16-Bit High-Integration Embedded Processors

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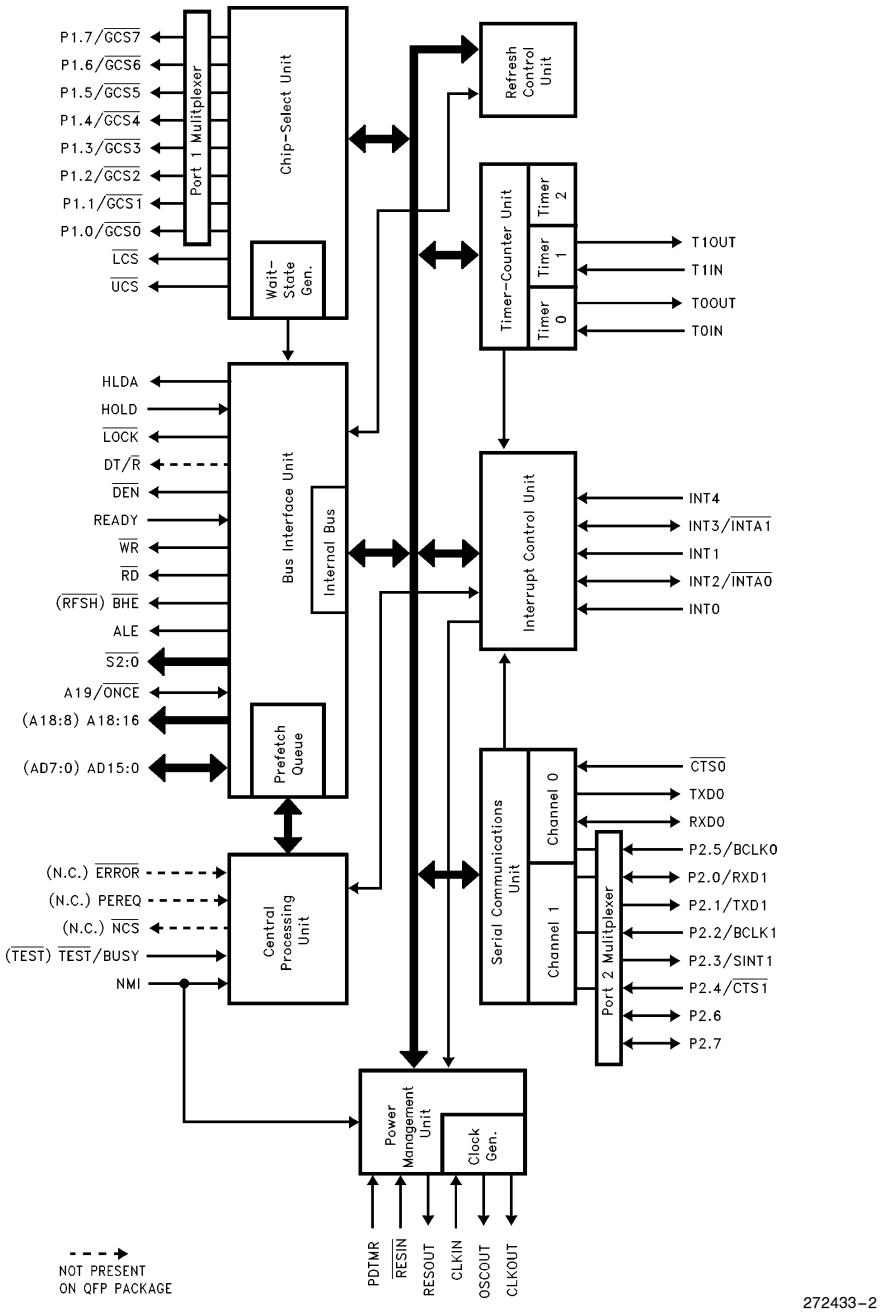
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**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB

**Figure 1. 80C186EB/80C188EB Block Diagram**

## INTRODUCTION

Unless specifically noted, all references to the 80C186EB apply to the 80C188EB, 80L186EB, and 80L188EB. References to pins that differ between the 80C186EB/80L186EB and the 80C188EB/80L188EB are given in parentheses. The ''L'' in the part number denotes low voltage operation. Physically and functionally, the ''C'' and ''L'' devices are identical.

The 80C186EB is the first product in a new generation of low-power, high-integration microprocessors. It enhances the existing 186 family by offering new features and new operating modes. The 80C186EB is object code compatible with the 80C186XL/80C188XL microprocessors.

The 80L186EB is the 3V version of the 80C186EB. The 80L186EB is functionally identical to the 80C186EB embedded processor. Current 80C186EB users can easily upgrade their designs to use the 80L186EB and benefit from the reduced power consumption inherent in 3V operation.

The feature set of the 80C186EB meets the needs of low power, space critical applications. Low-Power applications benefit from the static design of the CPU core and the integrated peripherals as well as low voltage operation. Minimum current consumption is achieved by providing a Powerdown mode that halts operation of the device, and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space critical applications benefit from the integration of commonly used system peripherals. Two serial channels are provided for services such as diagnostics, inter-processor communication, modem interface, terminal display interface, and many others. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 129 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters and sixteen multiplexed I/O port pins round out the feature set of the 80C186EB.

Figure 1 shows a block diagram of the 80C186EB/80C188EB. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instruction, and fully static operation. The Bus Interface Unit (BIU) is the same as that found on the original 186 family products, except the queue status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used to allow communication between the BIU and internal peripherals.

## CORE ARCHITECTURE

### Bus Interface Unit

The 80C186EB core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information, and data (for write operations) information. It is also responsible for reading data off the local bus during a read operation. A READY input pin is provided to extend a bus cycle beyond the minimum four states (clocks).

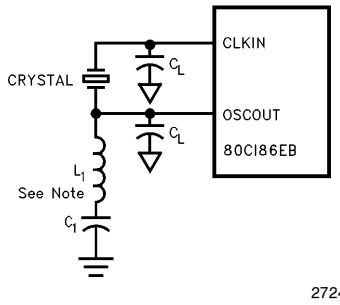
The local bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. (Both $\overline{DEN}$ and DT/$\overline{R}$ are available on the PLCC devices, only $\overline{DEN}$ is available on the QFP and SQFP devices.) This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

### Clock Generator

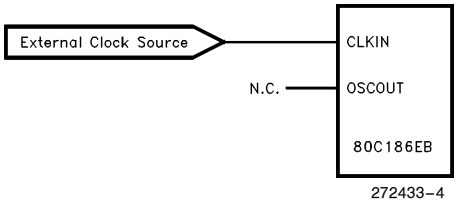
The processor provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, and two low-power operating modes.

The oscillator circuit is designed to be used with either a **parallel resonant** fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.




**(A) Crystal Connection**




**(B) Clock Connection**

**NOTE:**
The $L_1C_1$ network is **only** required when using a third-overtone crystal.

**Figure 2. Clock Configurations**

The following parameters are recommended when choosing a crystal:

| | |
|---|---|
| Temperature Range: | Application Specific |
| ESR (Equivalent Series Resistance): | 40Ω max |
| C0 (Shunt Capacitance of Crystal): | 7.0 pF max |
| $C_L$ (Load Capacitance): | 20 pF ± 2 pF |
| Drive Level: | 1 mW max |

## 80C186EB PERIPHERAL ARCHITECTURE

The 80C186EB has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or serial channels).

The list of integrated peripherals includes:

- 7-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel Serial Communications Unit
- 10-Output Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 x 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256 Byte address boundary.

Figure 3 provides a list of the registers associated with the PCB. The Register Bit Summary at the end of this specification individually lists all of the registers and identifies each of their programming attributes.

### Interrupt Control Unit

The 80C186EB can receive interrupts from a number of sources, both internal and external. The interrupt control unit serves to merge these requests on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit (ICU) or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and Serial channel 0. External interrupt sources come from the five input pins INT4:0. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the Timer and Serial channel each have only one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer and Serial channel units.

### Timer/Counter Unit

The 80C186EB Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts. etc.

| PCB Offset | Function |
|---|---|
| 00H | Reserved |
| 02H | End Of Interrupt |
| 04H | Poll |
| 06H | Poll Status |
| 08H | Interrupt Mask |
| 0AH | Priority Mask |
| 0CH | In-Service |
| 0EH | Interrupt Request |
| 10H | Interrupt Status |
| 12H | Timer Control |
| 14H | Serial Control |
| 16H | INT4 Control |
| 18H | INT0 Control |
| 1AH | INT1 Control |
| 1CH | INT2 Control |
| 1EH | INT3 Control |
| 20H | Reserved |
| 22H | Reserved |
| 24H | Reserved |
| 26H | Reserved |
| 28H | Reserved |
| 2AH | Reserved |
| 2CH | Reserved |
| 2EH | Reserved |
| 30H | Timer0 Count |
| 32H | Timer0 Compare A |
| 34H | Timer0 Compare B |
| 36H | Timer0 Control |
| 38H | Timer1 Count |
| 3AH | Timer1 Compare A |
| 3CH | Timer1 Compare B |
| 3EH | Timer1 Control |

| PCB Offset | Function |
|---|---|
| 40H | Timer2 Count |
| 42H | Timer2 Compare |
| 44H | Reserved |
| 46H | Timer2 Control |
| 48H | Reserved |
| 4AH | Reserved |
| 4CH | Reserved |
| 4EH | Reserved |
| 50H | Port 1 Direction |
| 52H | Port 1 Pin |
| 54H | Port 1 Control |
| 56H | Port 1 Latch |
| 58H | Port 2 Direction |
| 5AH | Port 2 Pin |
| 5CH | Port 2 Control |
| 5EH | Port 2 Latch |
| 60H | Serial0 Baud |
| 62H | Serial0 Count |
| 64H | Serial0 Control |
| 66H | Serial0 Status |
| 68H | Serial0 RBUF |
| 6AH | Serial0 TBUF |
| 6CH | Reserved |
| 6EH | Reserved |
| 70H | Serial1 Baud |
| 72H | Serial1 Count |
| 74H | Serial1 Control |
| 76H | Serial1 Status |
| 78H | Serial1 RBUF |
| 7AH | Serial1 TBUF |
| 7CH | Reserved |
| 7EH | Reserved |

| PCB Offset | Function |
|---|---|
| 80H | GCS0 Start |
| 82H | GCS0 Stop |
| 84H | GCS1 Start |
| 86H | GCS1 Stop |
| 88H | GCS2 Start |
| 8AH | GCS2 Stop |
| 8CH | GCS3 Start |
| 8EH | GCS3 Stop |
| 90H | GCS4 Start |
| 92H | GCS4 Stop |
| 94H | GCS5 Start |
| 96H | GCS5 Stop |
| 98H | GCS6 Start |
| 9AH | GCS6 Stop |
| 9CH | GCS7 Start |
| 9EH | GCS7 Stop |
| A0H | LCS Start |
| A2H | LCS Stop |
| A4H | UCS Start |
| A6H | UCS Stop |
| A8H | Relocation |
| AAH | Reserved |
| ACH | Reserved |
| AEH | Reserved |
| B0H | Refresh Base |
| B2H | Refresh Time |
| B4H | Refresh Control |
| B6H | Reserved |
| B8H | Power Control |
| BAH | Reserved |
| BCH | Step ID |
| BEH | Reserved |

| PCB Offset | Function |
|---|---|
| C0H | Reserved |
| C2H | Reserved |
| C4H | Reserved |
| C6H | Reserved |
| C8H | Reserved |
| CAH | Reserved |
| CCH | Reserved |
| CEH | Reserved |
| D0H | Reserved |
| D2H | Reserved |
| D4H | Reserved |
| D6H | Reserved |
| D8H | Reserved |
| DAH | Reserved |
| DCH | Reserved |
| DEH | Reserved |
| E0H | Reserved |
| E2H | Reserved |
| E4H | Reserved |
| E6H | Reserved |
| E8H | Reserved |
| EAH | Reserved |
| ECH | Reserved |
| EEH | Reserved |
| F0H | Reserved |
| F2H | Reserved |
| F4H | Reserved |
| F6H | Reserved |
| F8H | Reserved |
| FAH | Reserved |
| FCH | Reserved |
| FEH | Reserved |

**Figure 3. Peripheral Control Block Registers**

## Serial Communications Unit

The Serial Control Unit (SCU) of the 80C186EB contains two independent channels. Each channel is identical in operation except that only channel 0 is supported by the integrated interrupt controller (channel 1 has an external interrupt pin). Each channel has its own baud rate generator that is independent of the Timer/Counter Unit, and can be internally or externally clocked at up to one half the 80C186EB operating frequency.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit register logic. A 1x baud clock is provided in the synchronous mode.

## Chip-Select Unit

The 80C186EB Chip-Select Unit (CSU) integrates logic which provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically insert additional clocks (wait-states) into the current bus cycle and automatically terminate a bus cycle independent of the condition of the READY input pin.

## I/O Port Unit

The I/O Port Unit (IPU) on the 80C186EB supports two 8-bit channels of input, output, or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Most of Port 2 is multiplexed with the serial channel pins. Port 2 pins are limited to either an output or input function depending on the operation of the serial pin it is multiplexed with.

## Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the A12:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

## Power Management Unit

The 80C186EB Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides three power modes: Active, Idle, and Powerdown.

Active Mode indicates that all units on the 80C186EB are functional and the device consumes maximum power (depending on the level of peripheral operation). Idle Mode freezes the clocks of the Execution and Bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided $V_{CC}$ is maintained. Current consumption is reduced to just transistor junction leakage.

## 80C187 Interface (80C186EB Only)

The 80C186EB (PLCC package only) supports the direct connection of the 80C187 Numerics Coprocessor.

## ONCE Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186EB has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the A19/$\overline{\text{ONCE}}$ pin LOW (0) during a processor reset (this pin is weakly held to a HIGH (1) level) while $\overline{\text{RESIN}}$ is active.

## PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80C186EB in the Plastic Leaded Chip Carrier (PLCC) package, Shrink Quad Flat Pack (SQFP), and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

### Prefix Identification

With the extended temperature range, operational characteristics are guaranteed over the temperature range corresponding to - 40°C to + 85°C ambient. Package types are identified by a two-letter prefix to the part number. The prefixes are listed in Table 1.

**Table 1. Prefix Identification**

| Prefix | Note | Package Type | Temperature Type |
|---|---|---|---|
| XX | 1 | PLCC | Extended |
| XX | 1 | QFP (EIAJ) | Extended |
| XX | 1, 2 | SQFP | Extended/Commercial |
| X | 1, 2 | PLCC | Commercial |
| X | 1, 2 | QFP (EIAJ) | Commercial |

**NOTE**:

1. To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".
2. The 5V 25 MHz and 3V 16 MHz versions are only available in commercial temperature range corresponding to 0°C to a 70°C ambient.

### Pin Descriptions

Each pin or logical set of pins is described in Table 3. There are three columns for each entry in the Pin Description Table.

The **Pin Name** column contains a mnemonic that describes the pin function. Negation of the signal name (for example, $\overline{\text{RESIN}}$) denotes a signal that is active low.

The **Pin Type** column contains two kinds of information. The first symbol indicates whether a pin is power (P), ground (G), input only (I), output only (O) or input/output (I/O). Some pins have multiplexed functions (for example, A19/S6). Additional symbols indicate additional characteristics for each pin. Table 2 lists all the possible symbols for this column.

The **Input Type** column indicates the type of input (Asynchronous or Synchronous).

Asynchronous pins require that setup and hold times be met only in order to guarantee *recognition* at a particular clock edge. Synchronous pins require that setup and hold times be met to guarantee proper *operation*. For example, missing the setup or hold time for the SRDY pin (a synchronous input) will result in a system failure or lockup. Input pins may also be edge- or level-sensitive. The possible characteristics for input pins are S(E), S(L), A(E) and A(L).

The **Output States** column indicates the output state as a function of the device operating mode. Output states are dependent upon the current activity of the processor. There are four operational states that are different from regular operation: bus hold, reset, Idle Mode and Powerdown Mode. Appropriate characteristics for these states are also indicated in this column, with the legend for all possible characteristics in Table 2.

The **Pin Description** column contains a text description of each pin.

As an example, consider AD15.0. I/O signifies the pins are bidirectional. S(L) signifies that the input function is synchronous and level-sensitive. H(Z) signifies that, as outputs, the pins are high-impedance upon acknowledgement of bus hold. R(Z) signifies that the pins float during reset. P(X) signifies that the pins retain their states during Powerdown Mode.

**Table 2. Pin Description Nomenclature**

| Symbol | Description |
|---|---|
| P | Power Pin (Apply $+V_{CC}$ Voltage) |
| G | Ground (Connect to $V_{SS}$) |
| I | Input Only Pin |
| O | Output Only Pin |
| I/O | Input/Output Pin |
| S(E) | Synchronous, Edge Sensitive |
| S(L) | Synchronous, Level Sensitive |
| A(E) | Asynchronous, Edge Sensitive |
| A(L) | Asynchronous, Level Sensitive |
| H(1) | Output Driven to $V_{CC}$ during Bus Hold |
| H(0) | Output Driven to $V_{SS}$ during Bus Hold |
| H(Z) | Output Floats during Bus Hold |
| H(Q) | Output Remains Active during Bus Hold |
| H(X) | Output Retains Current State during Bus Hold |
| R(WH) | Output Weakly Held at $V_{CC}$ during Reset |
| R(1) | Output Driven to $V_{CC}$ during Reset |
| R(0) | Output Driven to $V_{SS}$ during Reset |
| R(Z) | Output Floats during Reset |
| R(Q) | Output Remains Active during Reset |
| R(X) | Output Retains Current State during Reset |
| I(1) | Output Driven to $V_{CC}$ during Idle Mode |
| I(0) | Output Driven to $V_{SS}$ during Idle Mode |
| I(Z) | Output Floats during Idle Mode |
| I(Q) | Output Remains Active during Idle Mode |
| I(X) | Output Retains Current State during Idle Mode |
| P(1) | Output Driven to $V_{CC}$ during Powerdown Mode |
| P(0) | Output Driven to $V_{SS}$ during Powerdown Mode |
| P(Z) | Output Floats during Powerdown Mode |
| P(Q) | Output Remains Active during Powerdown Mode |
| P(X) | Output Retains Current State during Powerdown Mode |

**Table 3. Pin Descriptions**

| Pin Name | Pin Type | Input Type | Output States | Description |
|---|---|---|---|---|
| $V_{CC}$ | P | — | — | **POWER** connections consist of four pins which must be shorted externally to a $V_{CC}$ board plane. |
| $V_{SS}$ | G | — | — | **GROUND** connections consist of six pins which must be shorted externally to a $V_{SS}$ board plane. |
| CLKIN | I | A(E) | — | **CLocK INput** is an input for an external clock. An external oscillator operating at two times the required processor operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator. |
| OSCOUT | O | — | H(Q)<br>R(Q)<br>P(Q) | **OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode. |
| CLKOUT | O | — | H(Q)<br>R(Q)<br>P(Q) | **CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN. |
| $\overline{RESIN}$ | I | A(L) | — | **RESet IN** causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the processor begins fetching opcodes at memory location 0FFFF0H. |
| RESOUT | O | — | H(0)<br>R(1)<br>P(0) | **RESet OUTput** that indicates the processor is currently in the reset state. RESOUT will remain active as long as $\overline{RESIN}$ remains active. |
| PDTMR | I/O | A(L) | H(WH)<br>R(Z)<br>P(1) | **Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the processor waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator. |
| NMI | I | A(E) | — | **Non-Maskable Interrupt** input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally. |
| $\overline{TEST}$/BUSY ($\overline{TEST}$) | I | A(E) | — | **TEST** is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW). $\overline{TEST}$ is alternately known as BUSY when interfacing with an 80C187 numerics coprocessor (80C186EB only). |
| AD15:0 (AD7:0) | I/O | S(L) | H(Z)<br>R(Z)<br>P(X) | These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 (0 through 7 on the 80C188EB) are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle. |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.

**Table 3. Pin Descriptions** (Continued)

| Pin Name | Pin Type | Input Type | Output States | Description |
|---|---|---|---|---|
| A18:16<br>A19/$\overline{\text{ONCE}}$<br>(A15:A8)<br>(A18:16)<br>(A19/ONCE) | I/O | A(L) | H(Z)<br>R(WH)<br>P(X) | These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle. On the 80C188EB, A15–A8 provide valid address information for the entire bus cycle. During a processor reset ($\overline{\text{RESIN}}$ active), A19/$\overline{\text{ONCE}}$ is used to enable ONCE mode. A18:16 must not be driven low during reset or improper operation may result. |
| $\overline{\text{S2:0}}$ | O | — | H(Z)<br>R(Z)<br>P(1) | Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{\text{S2:0}}$ are encoded as follows:<br>$\overline{\text{S2}}$ $\overline{\text{S1}}$ $\overline{\text{S0}}$ — **Bus Cycle Initiated**<br>0 0 0 — Interrupt Acknowledge<br>0 0 1 — Read I/O<br>0 1 0 — Write I/O<br>0 1 1 — Processor HALT<br>1 0 0 — Queue Instruction Fetch<br>1 0 1 — Read Memory<br>1 1 0 — Write Memory<br>1 1 1 — Passive (no bus activity) |
| ALE | O | — | H(0)<br>R(0)<br>P(0) | **Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle. |
| $\overline{\text{BHE}}$<br>($\overline{\text{RFSH}}$) | O | — | H(Z)<br>R(Z)<br>P(X) | **Byte High Enable** output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{\text{BHE}}$ and A0 have the following logical encoding<br>**A0** — $\overline{\text{BHE}}$ — **Encoding** (for the 80C186EB/80L186EB only)<br>0 — 0 — Word Transfer<br>0 — 1 — Even Byte Transfer<br>1 — 0 — Odd Byte Transfer<br>1 — 1 — Refresh Operation<br>On the 80C188EB/80L188EB, $\overline{\text{RFSH}}$ is asserted low to indicate a refresh bus cycle. |
| $\overline{\text{RD}}$ | O | — | H(Z)<br>R(Z)<br>P(1) | **ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus. |
| $\overline{\text{WR}}$ | O | — | H(Z)<br>R(Z)<br>P(1) | **WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device. |
| READY | I | A(L)<br>S(L) | — | **READY** input to signal the completion of a bus cycle. READY must be active to terminate any bus cycle, unless it is ignored by correctly programming the Chip-Select Unit. |
| $\overline{\text{DEN}}$ | O | — | H(Z)<br>R(Z)<br>P(1) | **Data ENable** output to control the enable of bi-directional transceivers in a buffered system. $\overline{\text{DEN}}$ is active only when data is to be transferred on the bus. |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.

**Table 3. Pin Descriptions** (Continued)

| Pin Name | Pin Type | Input Type | Output States | Description |
|---|---|---|---|---|
| DT/$\overline{R}$ | O | — | H(Z)<br>R(Z)<br>P(X) | **Data Transmit/Receive** output controls the direction of a bi-directional buffer in a buffered system. DT/$\overline{R}$ is only available for the PLCC package. |
| $\overline{LOCK}$ | O | — | H(Z)<br>R(WH)<br>P(1) | **LOCK** output indicates that the bus cycle in progress is not to be interrupted. The processor will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low. |
| HOLD | I | A(L) | — | **HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The processor will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix. |
| HLDA | O | — | H(1)<br>R(0)<br>P(0) | **HoLD Acknowledge** output to indicate that the processor has relinquished control of the local bus. When HLDA is asserted, the processor will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly. |
| $\overline{NCS}$<br>(N.C.) | O | — | H(1)<br>R(1)<br>P(1) | **Numerics Coprocessor Select** output is generated when accessing a numerics coprocessor. $\overline{NCS}$ is not provided on the QFP or SQFP packages. This signal does not exist on the 80C188EB/80L188EB. |
| $\overline{ERROR}$<br>(N.C.) | I | A(L) | — | **ERROR** input that indicates the last numerics coprocessor operation resulted in an exception condition. An interrupt TYPE 16 is generated if $\overline{ERROR}$ is sampled active at the beginning of a numerics operation. $\overline{ERROR}$ is not provided on the QFP or SQFP packages. This signal does not exist on the 80C188EB/80L188EB. |
| PEREQ<br>(N.C.) | I | A(L) | — | **CoProcessor REQuest** signals that a data transfer between an External Numerics Coprocessor and Memory is pending. PEREQ is not provided on the QFP or SQFP packages. This signal does not exist on the 80C188EB/80L188EB. |
| $\overline{UCS}$ | O | — | H(1)<br>R(1)<br>P(1) | **Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. |
| $\overline{LCS}$ | O | — | H(1)<br>R(1)<br>P(1) | **Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset. |
| P1.0/$\overline{GCS0}$<br>P1.1/$\overline{GCS1}$<br>P1.2/$\overline{GCS2}$<br>P1.3/$\overline{GCS3}$<br>P1.4/$\overline{GCS4}$<br>P1.5/$\overline{GCS5}$<br>P1.6/$\overline{GCS6}$<br>P1.7/$\overline{GCS7}$ | O | — | H(X)/H(1)<br>R(1)<br>P(X)/P(1) | These pins provide a multiplexed function. If enabled, each pin can provide a **Generic Chip Select** output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general purpose output **Port.** As an output port pin, the value of the pin can be read internally. |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.

**Table 3. Pin Descriptions** (Continued)

| Pin Name | Pin Type | Input Type | Output States | Description |
|---|---|---|---|---|
| T0OUT<br>T1OUT | O | — | H(Q)<br>R(1)<br>P(Q) | **Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected. |
| T0IN<br>T1IN | I | A(L)<br>A(E) | — | **Timer INput** is used either as clock or control signals, depending on the timer mode selected. |
| INT0<br>INT1<br>INT4 | I | A(E,L) | — | Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{\text{INTA0}}$ and $\overline{\text{INTA1}}$ to interface with an external slave controller. |
| INT2/$\overline{\text{INTA0}}$<br>INT3/$\overline{\text{INTA1}}$ | I/O | A(E,L) | H(1)<br>R(Z)<br>P(1) | These pins provide a multiplexed function. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an INTERRUPT ACKNOWLEDGE handshake signal to allow interrupt expansion. |
| P2.7<br>P2.6 | I/O | A(L) | H(X)<br>R(Z)<br>P(X) | BI-DIRECTIONAL, open-drain **Port** pins. |
| $\overline{\text{CTSO}}$<br>P2.4/$\overline{\text{CTS1}}$ | I | A(L) | — | **Clear-To-Send** input is used to prevent the transmission of serial data on their respective TXD signal pin. $\overline{\text{CTS1}}$ is multiplexed with an input only port function. |
| TXD0<br>P2.1/TXD1 | O | — | H(X)/H(Q)<br>R(1)<br>P(X)/P(Q) | **Transmit Data** output provides serial data information. TXD1 is multiplexed with an output only **Port** function. During synchronous serial communications, TXD will function as a clock output. |
| RXD0<br>P2.0/RXD1 | I/O | A(L) | R(Z)<br>H(Q)<br>P(X) | **Receive Data** input accepts serial data information. RXD1 is multiplexed with an input only **Port** function. During synchronous serial communications, RXD is bi-directional and will become an output for transmission or data (TXD becomes the clock). |
| P2.5/BCLK0<br>P2.2/BCLK1 | I | A(L)/A(E) | — | **Baud CLocK** input can be used as an alternate clock source for each of the integrated serial channels. BCLKx is multiplexed with an input only **Port** function, and cannot exceed a clock rate greater than one-half the operating frequency of the processor. |
| P2.3/SINT1 | O | — | H(X)/H(Q)<br>R(0)<br>P(X)/P(X) | **Serial INTerrupt** output will go active to indicate serial channel 1 requires service. SINT1 is multiplexed with an output only **Port** function. |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.

## 80C186EB PINOUT

Tables 4 and 5 list the 80C186EB/80C188EB pin names with package location for the 84-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 5 depicts the complete 80C186EB/80C188EB pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 6 and 7 list the 80C186EB/80C188EB pin names with package location for the 80-pin Quad Flat Pack (QFP) component. Figure 6 depicts the complete 80C186EB/80C188EB (QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 8 and 9 list the 80186EB/80188EB pin names with package location for the 80-pin Shrink Quad Flat Pack (SQFP) component. Figure 7 depicts the complete 80C186EB/80C188EB (SQFP package) as viewed from the top side of the component (i.e., contacts facing down).

**Table 4. PLCC Pin Names with Package Location**

| Address/Data Bus | |
|---|---|
| **Name** | **Location** |
| AD0 | 61 |
| AD1 | 66 |
| AD2 | 68 |
| AD3 | 70 |
| AD4 | 72 |
| AD5 | 74 |
| AD6 | 76 |
| AD7 | 78 |
| AD8 (A8) | 62 |
| AD9 (A9) | 67 |
| AD10 (A10) | 69 |
| AD11 (A11) | 71 |
| AD12 (A12) | 73 |
| AD13 (A13) | 75 |
| AD14 (A14) | 77 |
| AD15 (A15) | 79 |
| A16 | 80 |
| A17 | 81 |
| A18 | 82 |
| A19/$\overline{\text{ONCE}}$ | 83 |

| Bus Control | |
|---|---|
| **Name** | **Location** |
| ALE | 6 |
| $\overline{\text{BHE}}$ ($\overline{\text{RFSH}}$) | 7 |
| $\overline{\text{S0}}$ | 10 |
| $\overline{\text{S1}}$ | 9 |
| $\overline{\text{S2}}$ | 8 |
| $\overline{\text{RD}}$ | 4 |
| $\overline{\text{WR}}$ | 5 |
| READY | 18 |
| $\overline{\text{DEN}}$ | 11 |
| DT/$\overline{\text{R}}$ | 16 |
| $\overline{\text{LOCK}}$ | 15 |
| HOLD | 13 |
| HLDA | 12 |

| Power | |
|---|---|
| **Name** | **Location** |
| $V_{SS}$ | 2, 22, 43<br>63, 65, 84 |
| $V_{CC}$ | 1, 23<br>42, 64 |

| Processor Control | |
|---|---|
| **Name** | **Location** |
| $\overline{\text{RESIN}}$ | 37 |
| RESOUT | 38 |
| CLKIN | 41 |
| OSCOUT | 40 |
| CLKOUT | 44 |
| $\overline{\text{TEST}}$/BUSY | 14 |
| $\overline{\text{NCS}}$ (N.C.) | 60 |
| PEREQ (N.C.) | 39 |
| $\overline{\text{ERROR}}$ (N.C.) | 3 |
| PDTMR | 36 |
| NMI | 17 |
| INT0 | 31 |
| INT1 | 32 |
| INT2/$\overline{\text{INTA0}}$ | 33 |
| INT3/$\overline{\text{INTA1}}$ | 34 |
| INT4 | 35 |

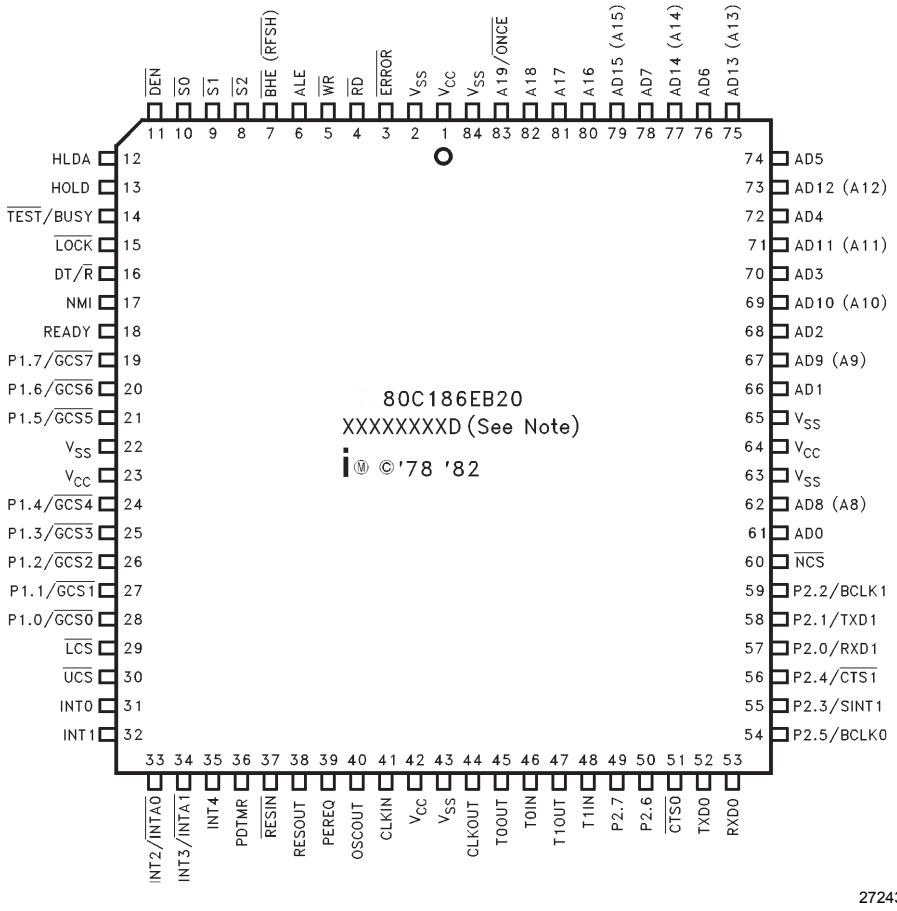
| I/O | |
|---|---|
| **Name** | **Location** |
| $\overline{\text{UCS}}$ | 30 |
| $\overline{\text{LCS}}$ | 29 |
| P1.0/$\overline{\text{GCS0}}$ | 28 |
| P1.1/$\overline{\text{GCS1}}$ | 27 |
| P1.2/$\overline{\text{GCS2}}$ | 26 |
| P1.3/$\overline{\text{GCS3}}$ | 25 |
| P1.4/$\overline{\text{GCS4}}$ | 24 |
| P1.5/$\overline{\text{GCS5}}$ | 21 |
| P1.6/$\overline{\text{GCS6}}$ | 20 |
| P1.7/$\overline{\text{GCS7}}$ | 19 |
| T0OUT | 45 |
| T0IN | 46 |
| T1OUT | 47 |
| T1IN | 48 |
| RXD0 | 53 |
| TXD0 | 52 |
| P2.5/BCLK0 | 54 |
| $\overline{\text{CTS0}}$ | 51 |
| P2.0/RXD1 | 57 |
| P2.1/TXD1 | 58 |
| P2.2/BCLK1 | 59 |
| P2.3/SINT1 | 55 |
| P2.4/$\overline{\text{CTS1}}$ | 56 |
| P2.6 | 50 |
| P2.7 | 49 |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.

**Table 5. PLCC Package Locations with Pin Name**

| Location | Name | Location | Name | Location | Name | Location | Name |
|---|---|---|---|---|---|---|---|
| 1 | $V_{CC}$ | 22 | $V_{SS}$ | 43 | $V_{SS}$ | 64 | $V_{CC}$ |
| 2 | $V_{SS}$ | 23 | $V_{CC}$ | 44 | CLKOUT | 65 | $V_{SS}$ |
| 3 | $\overline{\text{ERROR}}$ (N.C.) | 24 | P1.4/$\overline{\text{GCS4}}$ | 45 | T0OUT | 66 | AD1 |
| 4 | $\overline{\text{RD}}$ | 25 | P1.3/$\overline{\text{GCS3}}$ | 46 | T0IN | 67 | AD9 (A9) |
| 5 | $\overline{\text{WR}}$ | 26 | P1.2/$\overline{\text{GCS2}}$ | 47 | T1OUT | 68 | AD2 |
| 6 | ALE | 27 | P1.1/$\overline{\text{GCS1}}$ | 48 | T1IN | 69 | AD10 (A10) |
| 7 | $\overline{\text{BHE}}$ ($\overline{\text{RFSH}}$) | 28 | P1.0/$\overline{\text{GCS0}}$ | 49 | P2.7 | 70 | AD3 |
| 8 | $\overline{\text{S2}}$ | 29 | $\overline{\text{LCS}}$ | 50 | P2.6 | 71 | AD11 (A11) |
| 9 | $\overline{\text{S1}}$ | 30 | $\overline{\text{UCS}}$ | 51 | $\overline{\text{CTS0}}$ | 72 | AD4 |
| 10 | $\overline{\text{S0}}$ | 31 | INT0 | 52 | TXD0 | 73 | AD12 (A12) |
| 11 | $\overline{\text{DEN}}$ | 32 | INT1 | 53 | RXD0 | 74 | AD5 |
| 12 | HLDA | 33 | INT2/$\overline{\text{INTA0}}$ | 54 | P2.5/BCLK0 | 75 | AD13 (A13) |
| 13 | HOLD | 34 | INT3/$\overline{\text{INTA1}}$ | 55 | P2.3/SINT1 | 76 | AD6 |
| 14 | $\overline{\text{TEST}}$/BUSY | 35 | INT4 | 56 | P2.4/$\overline{\text{CTS1}}$ | 77 | AD14 (A14) |
| 15 | $\overline{\text{LOCK}}$ | 36 | PDTMR | 57 | P2.0/RXD1 | 78 | AD7 |
| 16 | DT/$\overline{\text{R}}$ | 37 | $\overline{\text{RESIN}}$ | 58 | P2.1/TXD1 | 79 | AD15 (A15) |
| 17 | NMI | 38 | RESOUT | 59 | P2.2/BCLK1 | 80 | A16 |
| 18 | READY | 39 | PEREQ (N.C.) | 60 | $\overline{\text{NCS}}$ (N.C.) | 81 | A17 |
| 19 | P1.7/$\overline{\text{GCS7}}$ | 40 | OSCOUT | 61 | AD0 | 82 | A18 |
| 20 | P1.6/$\overline{\text{GCS6}}$ | 41 | CLKIN | 62 | AD8 (A8) | 83 | A19/$\overline{\text{ONCE}}$ |
| 21 | P1.5/$\overline{\text{GCS5}}$ | 42 | $V_{CC}$ | 63 | $V_{SS}$ | 84 | $V_{SS}$ |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.




**NOTE:**
This is the FPO number location (indicated by X's).
Pin names in parentheses apply to the 80C188EB/80L188EB.

**Figure 4. 84-Pin Plastic Leaded Chip Carrier Pinout Diagram**

**Table 6. QFP Pin Name with Package Location**

| Address/Data Bus | |
|---|---|
| **Name** | **Location** |
| AD0 | 10 |
| AD1 | 15 |
| AD2 | 17 |
| AD3 | 19 |
| AD4 | 21 |
| AD5 | 23 |
| AD6 | 25 |
| AD7 | 27 |
| AD8 (A8) | 11 |
| AD9 (A9) | 16 |
| AD10 (A10) | 18 |
| AD11 (A11) | 20 |
| AD12 (A12) | 22 |
| AD13 (A13) | 24 |
| AD14 (A14) | 26 |
| AD15 (A15) | 28 |
| A16 | 29 |
| A17 | 30 |
| A18 | 31 |
| A19/$\overline{\text{ONCE}}$ | 32 |

| Bus Control | |
|---|---|
| **Name** | **Location** |
| ALE | 38 |
| $\overline{\text{BHE}}$ ($\overline{\text{RFSH}}$) | 39 |
| $\overline{\text{S0}}$ | 42 |
| $\overline{\text{S1}}$ | 41 |
| $\overline{\text{S2}}$ | 40 |
| $\overline{\text{RD}}$ | 36 |
| $\overline{\text{WR}}$ | 37 |
| READY | 49 |
| $\overline{\text{DEN}}$ | 43 |
| $\overline{\text{LOCK}}$ | 47 |
| HOLD | 45 |
| HLDA | 44 |

| Power | |
|---|---|
| **Name** | **Location** |
| $V_{SS}$ | 12, 14, 33 |
| | 35, 53, 73 |
| $V_{CC}$ | 13, 34 |
| | 54, 72 |

| Processor Control | |
|---|---|
| **Name** | **Location** |
| $\overline{\text{RESIN}}$ | 68 |
| RESOUT | 69 |
| CLKIN | 71 |
| OSCOUT | 70 |
| CLKOUT | 74 |
| $\overline{\text{TEST}}$ | 46 |
| PDTMR | 67 |
| NMI | 48 |
| INT0 | 62 |
| INT1 | 63 |
| INT2/$\overline{\text{INTA0}}$ | 64 |
| INT3/$\overline{\text{INTA1}}$ | 65 |
| INT4 | 66 |

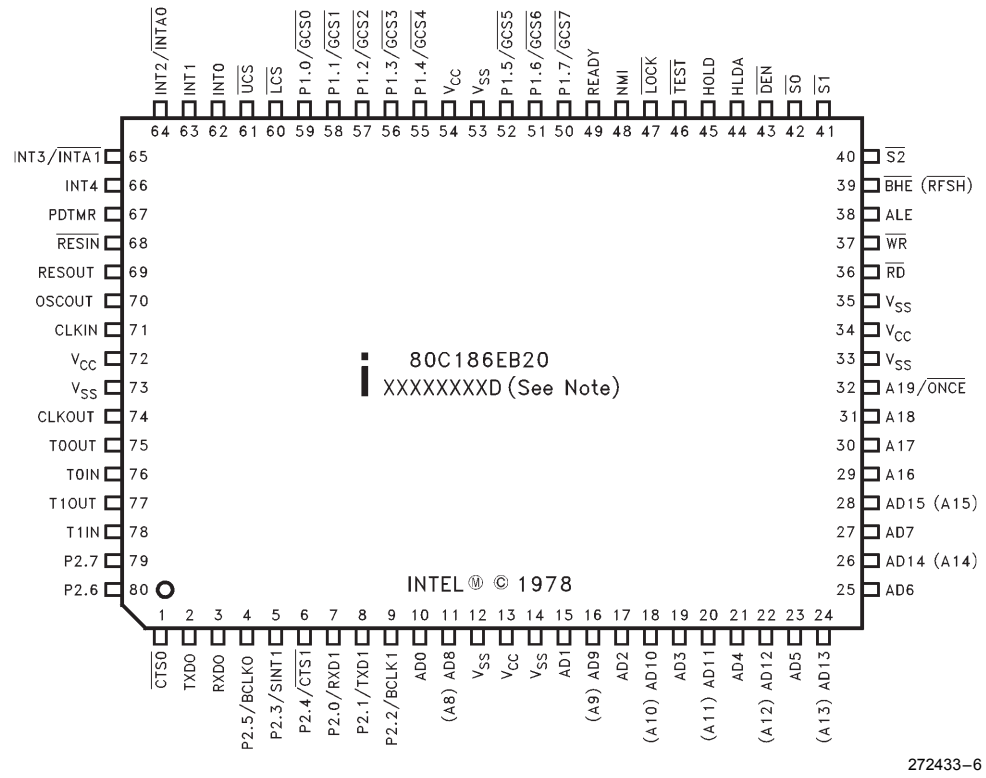
| I/O | |
|---|---|
| **Name** | **Location** |
| $\overline{\text{UCS}}$ | 61 |
| $\overline{\text{LCS}}$ | 60 |
| P1.0/$\overline{\text{GCS0}}$ | 59 |
| P1.1/$\overline{\text{GCS1}}$ | 58 |
| P1.2/$\overline{\text{GCS2}}$ | 57 |
| P1.3/$\overline{\text{GCS3}}$ | 56 |
| P1.4/$\overline{\text{GCS4}}$ | 55 |
| P1.5/$\overline{\text{GCS5}}$ | 52 |
| P1.6/$\overline{\text{GCS6}}$ | 51 |
| P1.7/$\overline{\text{GCS7}}$ | 50 |
| T0OUT | 75 |
| T0IN | 76 |
| T1OUT | 77 |
| T1IN | 78 |
| RXD0 | 3 |
| TXD0 | 2 |
| P2.5/BCLK0 | 4 |
| $\overline{\text{CTS0}}$ | 1 |
| P2.0/RXD1 | 7 |
| P2.1/TXD1 | 8 |
| P2.2/BCLK1 | 9 |
| P2.3/SINT1 | 5 |
| P2.4/$\overline{\text{CTS1}}$ | 6 |
| P2.6 | 80 |
| P2.7 | 79 |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.

**Table 7. QFP Package Location with Pin Names**

| Location | Name | Location | Name | Location | Name | Location | Name |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{CTS0}$ | 21 | AD4 | 41 | $\overline{S1}$ | 61 | $\overline{UCS}$ |
| 2 | TXD0 | 22 | AD12 (A12) | 42 | $\overline{S0}$ | 62 | INT0 |
| 3 | RXD0 | 23 | AD5 | 43 | $\overline{DEN}$ | 63 | INT1 |
| 4 | P2.5/BCLK0 | 24 | AD13 (A13) | 44 | HLDA | 64 | INT2/$\overline{INTA0}$ |
| 5 | P2.3/SINT1 | 25 | AD6 | 45 | HOLD | 65 | INT3/$\overline{INTA1}$ |
| 6 | P2.4/$\overline{CTS1}$ | 26 | AD14 (A14) | 46 | $\overline{TEST}$ | 66 | INT4 |
| 7 | P2.0/RXD1 | 27 | AD7 | 47 | $\overline{LOCK}$ | 67 | PDTMR |
| 8 | P2.1/TXD1 | 28 | AD15 (A15) | 48 | NMI | 68 | $\overline{RESIN}$ |
| 9 | P2.2/BCLK1 | 29 | A16 | 49 | READY | 69 | RESOUT |
| 10 | AD0 | 30 | A17 | 50 | P1.7/$\overline{GCS7}$ | 70 | OSCOUT |
| 11 | AD8 (A8) | 31 | A18 | 51 | P1.6/$\overline{GCS6}$ | 71 | CLKIN |
| 12 | $V_{SS}$ | 32 | A19/$\overline{ONCE}$ | 52 | P1.5/$\overline{GCS5}$ | 72 | $V_{CC}$ |
| 13 | $V_{CC}$ | 33 | $V_{SS}$ | 53 | $V_{SS}$ | 73 | $V_{SS}$ |
| 14 | $V_{SS}$ | 34 | $V_{CC}$ | 54 | $V_{CC}$ | 74 | CLKOUT |
| 15 | AD1 | 35 | $V_{SS}$ | 55 | P1.4/$\overline{GCS4}$ | 75 | T0OUT |
| 16 | AD9 (A9) | 36 | $\overline{RD}$ | 56 | P1.3/$\overline{GCS3}$ | 76 | T0IN |
| 17 | AD2 | 37 | $\overline{WR}$ | 57 | P1.2/$\overline{GCS2}$ | 77 | T1OUT |
| 18 | AD10 (A10) | 38 | ALE | 58 | P1.1/$\overline{GCS1}$ | 78 | T1IN |
| 19 | AD3 | 39 | $\overline{BHE}$ ($\overline{RFSH}$) | 59 | P1.0/$\overline{GCS0}$ | 79 | P2.7 |
| 20 | AD11 (A11) | 40 | $\overline{S2}$ | 60 | $\overline{LCS}$ | 80 | P2.6 |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.




**NOTE:**
This is the FPO number location (indicated by X's).
Pin names in parentheses apply to the 80C188EB/80L188EB.

**Figure 5. Quad Flat Pack Pinout Diagram**

**Table 8. SQFP Pin Functions with Location**

| AD Bus | |
|---|---|
| AD0 | 47 |
| AD1 | 52 |
| AD2 | 54 |
| AD3 | 56 |
| AD4 | 58 |
| AD5 | 60 |
| AD6 | 62 |
| AD7 | 64 |
| AD8 (A8) | 48 |
| AD9 (A9) | 53 |
| AD10 (A10) | 55 |
| AD11 (A11) | 57 |
| AD12 (A12) | 59 |
| AD13 (A13) | 61 |
| AD14 (A14) | 63 |
| AD15 (A15) | 65 |
| A16 | 66 |
| A17 | 67 |
| A18 | 68 |
| A19/ONCE | 69 |

| Bus Control | |
|---|---|
| ALE | 75 |
| BHE# (RFSH#) | 76 |
| S0# | 79 |
| S1# | 78 |
| S2# | 77 |
| RD# | 73 |
| WR# | 74 |
| READY | 6 |
| DEN# | 80 |
| LOCK# | 4 |
| HOLD | 2 |
| HLDA | 1 |

| Processor Control | |
|---|---|
| RESIN# | 25 |
| RESOUT | 26 |
| CLKIN | 28 |
| OSCOUT | 27 |
| CLKOUT | 31 |
| TEST#/BUSY | 3 |
| NMI | 5 |
| INT0 | 19 |
| INT1 | 20 |
| INT2/INTA0# | 21 |
| INT3/INTA1# | 22 |
| INT4 | 23 |
| PDTMR | 24 |

| Power and Ground | |
|---|---|
| $V_{CC}$ | 11 |
| $V_{CC}$ | 29 |
| $V_{CC}$ | 50 |
| $V_{CC}$ | 71 |
| $V_{SS}$ | 10 |
| $V_{SS}$ | 30 |
| $V_{SS}$ | 49 |
| $V_{SS}$ | 51 |
| $V_{SS}$ | 70 |
| $V_{SS}$ | 72 |

| I/O | |
|---|---|
| UCS# | 18 |
| LCS# | 17 |
| | |
| P1.0/GCS0# | 16 |
| P1.1/GCS1# | 15 |
| P1.2/GCS2# | 14 |
| P1.3/GCS3# | 13 |
| P1.4/GCS4# | 12 |
| P1.5/GCS5# | 9 |
| P1.6/GCS6# | 8 |
| P1.7/GCS7# | 7 |
| | |
| P2.0/RXD1 | 44 |
| P2.1/TXD1 | 45 |
| P2.2/BCLK1 | 46 |
| P2.3/SINT1 | 42 |
| P2.4/CTS1# | 43 |
| P2.5/BCLK0 | 41 |
| P2.6 | 37 |
| P2.7 | 36 |
| | |
| CTS0# | 38 |
| TXD0 | 39 |
| RXD0 | 40 |
| | |
| T0IN | 33 |
| T1IN | 35 |
| T0OUT | 32 |
| T1OUT | 34 |

**Table 9. SQFP Pin Locations with Pin Names**

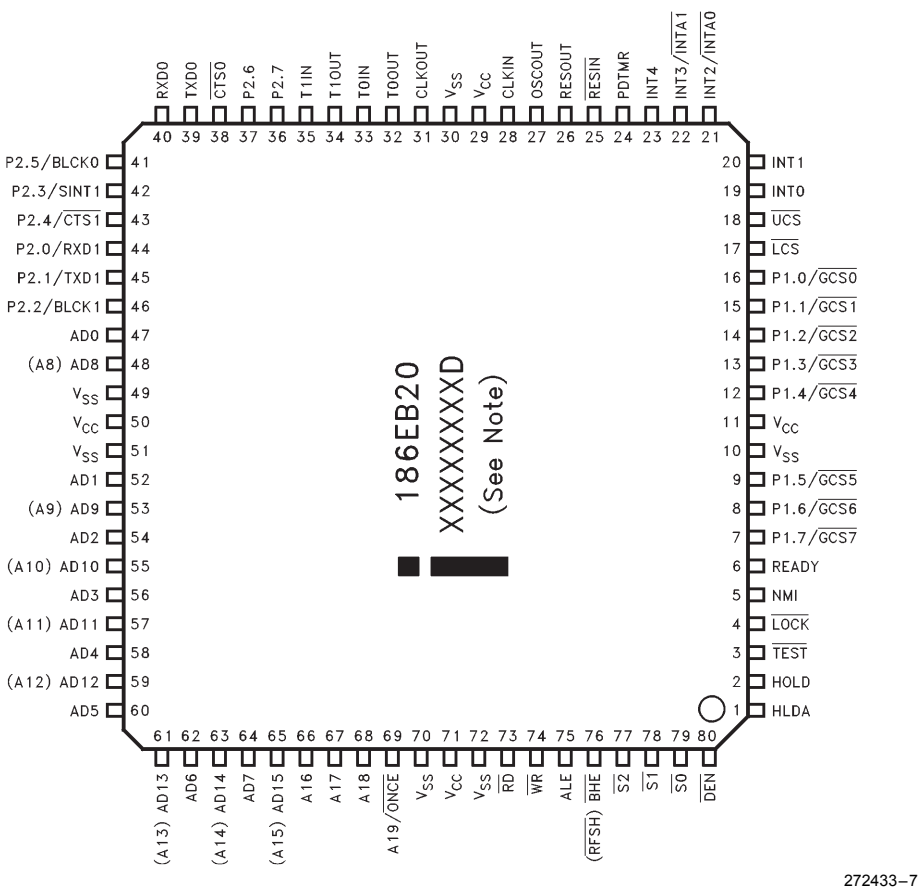
| | |
|---|---|
| 1 | HLDA |
| 2 | HOLD |
| 3 | TEST# |
| 4 | LOCK# |
| 5 | NMI |
| 6 | READY |
| 7 | P1.7/GCS7# |
| 8 | P1.6/GCS6# |
| 9 | P1.5/GCS5# |
| 10 | $V_{SS}$ |
| 11 | $V_{CC}$ |
| 12 | P1.4/GCS4# |
| 13 | P1.3/GCS3# |
| 14 | P1.2/GCS2# |
| 15 | P1.1/GCS1# |
| 16 | P1.0/GCS0# |
| 17 | LCS# |
| 18 | UCS# |
| 19 | INT0 |
| 20 | INT1 |

| | |
|---|---|
| 21 | INT1/INTA0# |
| 22 | INT3/INTA1# |
| 23 | INT4 |
| 24 | PDTMR |
| 25 | RESIN# |
| 26 | RESOUT |
| 27 | OSCOUT |
| 28 | CLKIN |
| 29 | $V_{CC}$ |
| 30 | $V_{SS}$ |
| 31 | CLKOUT |
| 32 | T0OUT |
| 33 | T0IN |
| 34 | T1OUT |
| 35 | T1IN |
| 36 | P2.7 |
| 37 | P2.6 |
| 38 | CTS0# |
| 39 | TXD0 |
| 40 | RXD0 |

| | |
|---|---|
| 41 | P2.5/BCLK0 |
| 42 | P2.3/SINT1 |
| 43 | P2.4/CTS1# |
| 44 | P2.0/RXD1 |
| 45 | P2.1/TXD1 |
| 46 | P2.2/BCLK1 |
| 47 | AD0 |
| 48 | AD8 (A8) |
| 49 | $V_{SS}$ |
| 50 | $V_{CC}$ |
| 51 | $V_{SS}$ |
| 52 | AD1 |
| 53 | AD9 (A9) |
| 54 | AD2 |
| 55 | AD10 (A10) |
| 56 | AD3 |
| 57 | AD11 (A11) |
| 58 | AD4 |
| 59 | AD12 (A12) |
| 60 | AD5 |

| | |
|---|---|
| 61 | AD13 (A13) |
| 62 | AD6 |
| 63 | AD14 (A14) |
| 64 | AD7 |
| 65 | AD15 (A15) |
| 66 | A16 |
| 67 | A17 |
| 68 | A18 |
| 69 | A19/ONCE |
| 70 | $V_{SS}$ |
| 71 | $V_{CC}$ |
| 72 | $V_{SS}$ |
| 73 | RD# |
| 74 | WR# |
| 75 | ALE |
| 76 | BHE# (RFSH#) |
| 77 | S2# |
| 78 | S1# |
| 79 | S0# |
| 80 | DEN# |

**NOTE:**
Pin names in parentheses apply to the 80C188EB/80L188EB.




NOTE:
XXXXXXXXC indicates Intel FPO number.
Pin names in parentheses apply to the 80C188EB/80L188EB.

Figure 6. SQFP Package

## PACKAGE THERMAL SPECIFICATIONS

The 80C186EB/80L186EB is specified for operation when $T_C$ (the case temperature) is within the range of −40°C to +100°C (PLCC package) or −40°C to +114°C (QFP package). $T_C$ may be measured in any environment to determine whether the processor is within the specified operating range. The case temperature must be measured at the center of the top surface.

$T_A$ (the ambient temperature) can be calculated from $\theta_{CA}$ (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P^*\theta_{CA}$$

Typical values for $\theta_{CA}$ at various airflows are given in Table 10. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and $V_{CC}$ of 5.5V.

**Table 10. Thermal Resistance ($\theta_{CA}$) at Various Airflows (in °C/Watt)**

| | Airflow Linear ft/min (m/sec) | | | | | |
|---|---|---|---|---|---|---|
| | **0 (0)** | **200 (1.01)** | **400 (2.03)** | **600 (3.04)** | **800 (4.06)** | **1000 (5.07)** |
| $\theta_{CA}$ (PLCC) | 30 | 24 | 21 | 19 | 17 | 16.5 |
| $\theta_{CA}$ (QFP) | 58 | 47 | 43 | 40 | 38 | 36 |
| $\theta_{CA}$ (SQFP) | 70 | TBD | TBD | TBD | TBD | TBD |

## ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

### Absolute Maximum Ratings

Storage Temperature . . . . . −65°C to +150°C

Case Temp under Bias . . . . . −65°C to +120°C

Supply Voltage
with Respect to $V_{SS}$ . . . . . −0.5V to + 6.5V

Voltage on other Pins
with Respect to $V_{SS}$ . . . . . −0.5V to $V_{CC}$ + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### Recommended Connections

Power and ground connections must be made to multiple $V_{CC}$ and $V_{SS}$ pins. Every 80C186EB-based circuit board should include separate power ($V_{CC}$) and ground ($V_{SS}$) planes. Every $V_{CC}$ pin must be connected to the power plane, and every $V_{SS}$ pin must be connected to the ground plane. Pins identified as "NC" must not be connected in the system. Liberal decoupling capacitance should be placed near the processor. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the processor $V_{CC}$ and $V_{SS}$ package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (INT0:4) should be connected to $V_{CC}$ through a pull-up resistor (in the range of 50 KΩ). **Leave any unused output pin or any NC pin unconnected.**

## DC SPECIFICATIONS (80C186EB/80C188EB)

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.5 | V | |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.3 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 3 mA (Min) |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ − 0.5 | | V | $I_{OH}$ = −2 mA (MIn) |
| $V_{HYR}$ | Input Hysterisis on $\overline{RESIN}$ | 0.50 | | V | |
| $I_{LI1}$ | Input Leakage Current for Pins: AD15:0 (AD7:0), READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, P2.6, P2.7 | | ±15 | μA | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $I_{LI2}$ | Input Leakage Current for Pins: $\overline{ERROR}$, PEREQ | ±0.275 | ±7 | mA | 0V ≤ $V_{IN}$ < $V_{CC}$ |
| $I_{LI3}$ | Input Leakage Current for Pins: A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$ | −0.275 | −5.0 | mA | $V_{IN}$ = 0.7 $V_{CC}$ (Note 1) |
| $I_{LO}$ | Output Leakage Current | | ±15 | μA | 0.45 ≤ $V_{OUT}$ ≤ $V_{CC}$ (Note 2) |
| $I_{CC}$ | Supply Current Cold (RESET) 80C186EB25 | | 115 | mA | (Notes 3, 7) |
| | 80C186EB20 | | 108 | mA | (Note 3) |
| | 80C186EB13 | | 73 | mA | (Note 3) |
| $I_{ID}$ | Supply Current Idle 80C186EB25 | | 91 | mA | (Notes 4, 7) |
| | 80C186EB20 | | 76 | mA | (Note 4) |
| | 80C186EB13 | | 48 | mA | (Note 4) |
| $I_{PD}$ | Supply Current Powerdown 80C186EB25 | | 100 | μA | (Notes 5, 7) |
| | 80C186EB20 | | 100 | μA | (Note 5) |
| | 80C186EB13 | | 100 | μA | (Note 5) |
| $C_{IN}$ | Input Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz |
| $C_{OUT}$ | Output Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz (Note 6) |

**NOTES:**
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
6. Output Capacitance is the capacitive load of a floating output pin.
7. Operating temperature for 25 MHz is 0°C to 70°C, $V_{CC}$ = 5.0 ±10%.

## DC SPECIFICATIONS (80L186EB16) (operating temperature, 0°C to 70°C)

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 5.5 | V | |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.3 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 1.6 mA (Min) (Note 1) |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ − 0.5 | | V | $I_{OH}$ = −1 mA (Min) (Note 1) |
| $V_{HYR}$ | Input Hysterisis on $\overline{RESIN}$ | 0.50 | | V | |
| $I_{LI1}$ | Input Leakage Current for pins: AD15:0 (AD7:0), READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, SINT1, P2.6, P2.7 | | ±15 | μA | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $I_{LI2}$ | Input Leakage Current for Pins: A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$ | −0.275 | −2 | mA | $V_{IN}$ = 0.7 $V_{CC}$ (Note 2) |
| $I_{LO}$ | Output Leakage Current | | ±15 | μA | 0.45 ≤ $V_{OUT}$ ≤ $V_{CC}$ (Note 3) |
| $I_{CC3}$ | Supply Current (RESET, 3.3V) 80L186EB16 | | 54 | mA | (Note 4) |
| $I_{ID3}$ | Supply Current Idle (3.3V) 80L186EB16 | | 38 | mA | (Note 5) |
| $I_{PD3}$ | Supply Current Powerdown (3.3V) 80L186EB16 | | 40 | μA | (Note 6) |
| $C_{IN}$ | Input Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz |
| $C_{OUT}$ | Output Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz (Note 7) |

**NOTES:**
1. $I_{OL}$ and $I_{OH}$ measured at $V_{CC}$ = 3.0V.
2. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
3. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
4. Measured with the device in RESET and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
5. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
6. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
7. Output Capacitance is the capacitive load of a floating output pin.

## DC SPECIFICATIONS (80L186EB13/80L188EB13

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.7 | 5.5 | V | |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.3 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 1.6 mA (Min) (Note 1) |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ − 0.5 | | V | $I_{OH}$ = −1 mA (Min) (Note 1) |
| $V_{HYR}$ | Input Hysterisis on $\overline{RESIN}$ | 0.50 | | V | |
| $I_{LI1}$ | Input Leakage Current for pins: AD15:0 (AD7:0), READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, SINT1, P2.6, P2.7 | | ±15 | μA | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $I_{LI2}$ | Input Leakage Current for Pins: A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$ | −0.275 | −2 | mA | $V_{IN}$ = 0.7 $V_{CC}$ (Note 2) |
| $I_{LO}$ | Output Leakage Current | | ±15 | μA | 0.45 ≤ $V_{OUT}$ ≤ $V_{CC}$ (Note 3) |
| $I_{CC5}$ | Supply Current (RESET, 5.5V)<br>80L186EB13<br>80L186EB8 | | <br>73<br>45 | <br>mA<br>mA | <br>(Note 4)<br>(Note 4) |
| $I_{CC3}$ | Supply Current (RESET, 2.7V)<br>80L186EB13<br>80L186EB8 | | <br>36<br>22 | <br>mA<br>mA | <br>(Note 4)<br>(Note 4) |
| $I_{ID5}$ | Supply Current Idle (5.5V)<br>80L186EB13<br>80L186EB8 | | <br>48<br>31 | <br>mA<br>mA | <br>(Note 5)<br>(Note 5) |
| $I_{ID3}$ | Supply Current Idle (2.7V)<br>80L186EB13<br>80L186EB8 | | <br>24<br>15 | <br>mA<br>mA | <br>(Note 5)<br>(Note 5) |
| $I_{PD5}$ | Supply Current Powerdown (5.5V)<br>80L186EB13<br>80L186EB8 | | <br>100<br>100 | <br>μA<br>μA | <br>(Note 6)<br>(Note 6) |
| $I_{PD3}$ | Supply Current Powerdown (2.7V)<br>80L186EB13<br>80L186EB8 | | <br>30<br>30 | <br>μA<br>μA | <br>(Note 6)<br>(Note 6) |
| $C_{IN}$ | Input Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz |
| $C_{OUT}$ | Output Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz (Note 7) |

**NOTES:**
1. $I_{OL}$ and $I_{OH}$ measured at $V_{CC}$ = 2.7V.
2. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
3. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
4. Measured with the device in RESET and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
5. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
6. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
7. Output Capacitance is the capacitive load of a floating output pin.

## $I_{CC}$ VERSUS FREQUENCY AND VOLTAGE

The current ($I_{CC}$) consumption of the processor is essentially composed of two components; $I_{PD}$ and $I_{CCS}$.

$I_{PD}$ is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or $V_{CC}$ (no clock applied to the device). $I_{PD}$ is equal to the Powerdown current and is typically less than 50 $\mu$A.

$I_{CCS}$ is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since $I_{CCS}$ is typically much greater than $I_{PD}$, $I_{PD}$ can often be ignored when calculating $I_{CC}$.

$I_{CCS}$ is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: $V$ = Device operating voltage ($V_{CC}$)

$C_{DEV}$ = Device capacitance

$f$ = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring $C_{DEV}$ on a device like the 80C186EB would be difficult. Instead, $C_{DEV}$ is calculated using the above formula by measuring $I_{CC}$ at a known $V_{CC}$ and frequency (see Table 11). Using this $C_{DEV}$ value, $I_{CC}$ can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical $I_{CC}$ when operating at 10 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.583 \times 10 \approx 28 \text{ mA}$$

## PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

**NOTE:**
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: $t$ = desired delay in **seconds**

$C_{PD}$ = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 $\mu$s, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ $\mu$F is required. Round up to standard (available) capacitive values.

**NOTE:**
The above equation applies to delay times greater than 10 $\mu$s and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher $V_{CC}$ and/or lower temperature will decrease delay time, while lower $V_{CC}$ and/or higher temperature will increase delay time.

**Table 11. Device Capacitance ($C_{DEV}$) Values**

| Parameter | Typ | Max | Units | Notes |
|---|---|---|---|---|
| $C_{DEV}$ (Device in Reset) | 0.583 | 1.02 | mA/V*MHz | 1, 2 |
| $C_{DEV}$ (Device in Idle) | 0.408 | 0.682 | mA/V*MHz | 1, 2 |

1. Max $C_{DEV}$ is calculated at −40°C, all floating outputs driven to $V_{CC}$ or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical $C_{DEV}$ is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

## AC SPECIFICATIONS

### AC Characteristics—80C186EB25

| Symbol | Parameter | 25 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **INPUT CLOCK** | | | | | |
| $T_F$ | CLKIN Frequency | 0 | 50 | MHz | 1 |
| $T_C$ | CLKIN Period | 20 | ∞ | ns | 1 |
| $T_{CH}$ | CLKIN High Time | 8 | ∞ | ns | 1, 2 |
| $T_{CL}$ | CLKIN Low Time | 8 | ∞ | ns | 1, 2 |
| $T_{CR}$ | CLKIN Rise Time | 1 | 7 | ns | 1, 3 |
| $T_{CF}$ | CLKIN Fall Time | 1 | 7 | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 16 | ns | 1, 4 |
| T | CLKOUT Period | | $2*T_C$ | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 6 | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 6 | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | |
| $T_{CHOV1}$ | ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$, A19:16 | 3 | 17 | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | $\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$ | 3 | 20 | ns | 1, 4, 6, 8 |
| $T_{CLOV1}$ | $\overline{BHE}$ ($\overline{RFSH}$), $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16 | 3 | 17 | ns | 1, 4, 6 |
| $T_{CLOV2}$ | $\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0 (AD7:0, A15:8), $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$ | 3 | 20 | ns | 1, 4, 6 |
| $T_{CHOF}$ | $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16 | 0 | 20 | ns | 1 |
| $T_{CLOF}$ | $\overline{DEN}$, AD15:0 (AD7:0, A15:8) | 0 | 20 | ns | 1 |

## AC SPECIFICATIONS

### AC Characteristics—80C186EB25 (Continued)

| Symbol | Parameter | 25 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **SYNCHRONOUS INPUTS** | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7 | 10 | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$ | 3 | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 10 | | ns | 1, 10 |
| $T_{CLIH}$ | READY, AD15:0 (AD7:0) | 3 | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD, PEREQ, $\overline{ERROR}$ | 10 | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD, PEREQ, $\overline{ERROR}$ | 3 | | ns | 1, 9 |

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## AC SPECIFICATIONS

### AC Characteristics—80C186EB20/80C186EB13

| Symbol | Parameter | 20 MHz | | 13 MHz | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| **INPUT CLOCK** | | | | | | | |
| $T_F$ | CLKIN Frequency | 0 | 40 | 0 | 26 | MHz | 1 |
| $T_C$ | CLKIN Period | 25 | ∞ | 38.5 | ∞ | ns | 1 |
| $T_{CH}$ | CLKIN High Time | 10 | ∞ | 12 | ∞ | ns | 1, 2 |
| $T_{CL}$ | CLKIN Low Time | 10 | ∞ | 12 | ∞ | ns | 1, 2 |
| $T_{CR}$ | CLKIN Rise Time | 1 | 8 | 1 | 8 | ns | 1, 3 |
| $T_{CF}$ | CLKIN Fall Time | 1 | 8 | 1 | 8 | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 17 | 0 | 23 | ns | 1, 4 |
| T | CLKOUT Period | | $2*T_C$ | | $2*T_C$ | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) − 5 | (T/2) + 5 | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) − 5 | (T/2) + 5 | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 6 | 1 | 6 | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 6 | 1 | 6 | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | | | |
| $T_{CHOV1}$ | ALE, S2:0, DEN, DT/R, BHE (RFSH), LOCK, A19:16 | 3 | 22 | 3 | 25 | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | GCS0:7, LCS, UCS, NCS, RD, WR | 3 | 27 | 3 | 30 | ns | 1, 4, 6, 8 |
| $T_{CLOV1}$ | BHE (RFSH), DEN, LOCK, RESOUT, HLDA, T0OUT, T1OUT, A19:16 | 3 | 22 | 3 | 25 | ns | 1, 4, 6 |
| $T_{CLOV2}$ | RD, WR, GCS7:0, LCS, UCS, AD15:0 (AD7:0, A15:8), NCS, INTA1:0, S2:0 | 3 | 27 | 3 | 30 | ns | 1, 4, 6 |
| $T_{CHOF}$ | RD, WR, BHE (RFSH), DT/R, LOCK, S2:0, A19:16 | 0 | 25 | 0 | 25 | ns | 1 |
| $T_{CLOF}$ | DEN, AD15:0 (AD7:0, A15:8) | 0 | 25 | 0 | 25 | ns | 1 |

## AC SPECIFICATIONS

### AC Characteristics—80C186EB20/80C186EB13 (Continued)

| Symbol | Parameter | 20 MHz | | 13 MHz | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| **SYNCHRONOUS INPUTS** | | | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7 | 10 | | 10 | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$ | 3 | | 3 | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 10 | | 10 | | ns | 1, 10 |
| $T_{CLIH}$ | READY, AD15:0 (AD7:0) | 3 | | 3 | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD, PEREQ, $\overline{ERROR}$ | 10 | | 10 | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD, PEREQ, $\overline{ERROR}$ | 3 | | 3 | | ns | 1, 9 |

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## AC SPECIFICATIONS

### AC Characteristics—80L186EB16

| Symbol | Parameter | 16 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **INPUT CLOCK** | | | | | |
| $T_F$ | CLKIN Frequency | 0 | 32 | MHz | 1 |
| $T_C$ | CLKIN Period | 31.25 | ∞ | ns | 1 |
| $T_{CH}$ | CLKIN High Time | 13 | ∞ | ns | 1, 2 |
| $T_{CL}$ | CLKIN Low Time | 13 | ∞ | ns | 1, 2 |
| $T_{CR}$ | CLKIN Rise Time | 1 | 8 | ns | 1, 3 |
| $T_{CF}$ | CLKIN Fall Time | 1 | 8 | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 30 | ns | 1, 4 |
| T | CLKOUT Period | | $2*T_C$ | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 9 | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 9 | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | |
| $T_{CHOV1}$ | DT/$\overline{R}$, $\overline{LOCK}$, A19:16, $R_{\overline{FSH}}$ | 3 | 22 | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | $\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$ | 3 | 27 | ns | 1, 4, 6, 8 |
| $T_{CHOV3}$ | $\overline{BHE}$, $\overline{DEN}$ | 3 | 25 | ns | 1, 4 |
| $T_{CHOV4}$ | ALE | 3 | 30 | ns | 1, 4 |
| $T_{CHOV5}$ | $\overline{S2:0}$ | 3 | 33 | ns | 1, 4 |
| $T_{CLOV1}$ | $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16 | 3 | 22 | ns | 1, 4, 6 |
| $T_{CLOV2}$ | $\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{INTA1:0}$, AD15:0 (AD7:0, A15:8) | 3 | 27 | ns | 1, 4, 6 |
| $T_{CHOF}$ | $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16 | 0 | 25 | ns | 1 |
| $T_{CLOF}$ | $\overline{DEN}$, AD15:0 (AD7:0, A15:8) | 0 | 25 | ns | 1 |
| $T_{CLOV3}$ | $\overline{BHE}$, $\overline{DEN}$ | 3 | 25 | ns | 1, 4, 6 |
| $T_{CLOV5}$ | $\overline{S2:0}$ | 3 | 33 | ns | 1, 4, 6 |

## AC SPECIFICATIONS

### AC Characteristics—80L186EB16 (Continued)

| Symbol | Parameter | 16 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **SYNCHRONOUS INPUTS** | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7 | 15 | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, INT4:0, T1:0IN, BCLK1:0, READY, $\overline{CTS1:0}$ | 3 | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 15 | | ns | 1, 10 |
| $T_{CLIH}$ | READY, AD15:0 (AD7:0) | 3 | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD | 15 | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD | 3 | | ns | 1, 9 |

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## AC SPECIFICATIONS

### AC Characteristics—80L186EB13

| Symbol | Parameter | 13 MHz | | 8 MHz | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | No Longer | Available | | |
| **INPUT CLOCK** | | | | | | | |
| $T_r$ | CLKIN Frequency | 0 | 26 | | | MHz | 1 |
| $T_C$ | CLKIN Period | 38.5 | % | | | ns | 1 |
| $T_{CH}$ | CLKIN High Time | 15 | % | | | ns | 1, 2 |
| $T_{CL}$ | CLKIN Low Time | 15 | % | | | ns | 1, 2 |
| $T_{CR}$ | CLKIN Rise Time | 1 | 8 | | | ns | 1, 3 |
| $T_{CF}$ | CLKIN Fall Time | 1 | 8 | | | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 10 | | | ns | 1, 4 |
| T | CLKOUT Period | | $2*T_C$ | | | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) b 5 | (T/2) a5 | | | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) b 5 | (T/2) a 5 | | | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 10 | | | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 10 | | | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | | | |
| $T_{CHOV1}$ | ALE, $\overline{S2\text{-}0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$, A19:16 | 3 | 25 | | | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | $\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$ | 3 | 30 | | | ns | 1, 4,6, 8 |
| $T_{CLOV1}$ | $\overline{BHE}$ ($\overline{RFSH}$), $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16 | 3 | 25 | | | ns | 1, 4, 6 |
| $T_{CLOV2}$ | $\overline{S2:0}$, $\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{INTA1:0}$, AD15:0 (AD7:0, A15:8) | 3 | 30 | | | ns | 1, 4, 6 |
| $T_{CHOF}$ | $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16 | 0 | 30 | | | ns | 1 |
| $T_{CLOF}$ | $\overline{DEN}$, AD15:0 (AD7:0, A15:8) | 0 | 30 | | | ns | 1 |

## AC SPECIFICATIONS

### AC Characteristics—80L186EB13/80L186EB8 (Continued)

| Symbol | Parameter | 13 MHz | | 8 MHz | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Not | Available | | |
| **SYNCHRONOUS INPUTS** | | | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY $\overline{CTS1:0}$, P2.6, P2.7 | 20 | | | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, INT4:0, T1:0IN, BCLK1:0, READY, $\overline{CTS1:0}$ | 3 | | | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 20 | | | | ns | 1, 10 |
| $T_{CLIH}$ | READY, AD15:0 (AD7:0) | 3 | | | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD | 20 | | | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD | 3 | | | | ns | 1, 9 |

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## AC SPECIFICATIONS (Continued)

### Relative Timings (80C186EB25, 20, 13/80L186EB16, 13, 8)

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| **RELATIVE TIMINGS** | | | | | |
| $T_{LHLL}$ | ALE Rising to ALE Falling | T − 15 | | ns | |
| $T_{AVLL}$ | Address Valid to ALE Falling | ½T − 10 | | ns | |
| $T_{PLLL}$ | Chip Selects Valid to ALE Falling | ½T − 10 | | ns | 1 |
| $T_{LLAX}$ | Address Hold from ALE Falling | ½T − 10 | | ns | |
| $T_{LLWL}$ | ALE Falling to $\overline{WR}$ Falling | ½T − 15 | | ns | 1 |
| $T_{LLRL}$ | ALE Falling to $\overline{RD}$ Falling | ½T − 15 | | ns | 1 |
| $T_{WHLH}$ | $\overline{WR}$ Rising to ALE Rising | ½T − 10 | | ns | 1 |
| $T_{AFRL}$ | Address Float to $\overline{RD}$ Falling | 0 | | ns | |
| $T_{RLRH}$ | $\overline{RD}$ Falling to $\overline{RD}$ Rising | (2*T) − 5 | | ns | 2 |
| $T_{WLWH}$ | $\overline{WR}$ Falling to $\overline{WR}$ Rising | (2*T) − 5 | | ns | 2 |
| $T_{RHAV}$ | $\overline{RD}$ Rising to Address Active | T − 15 | | ns | |
| $T_{WHDX}$ | Output Data Hold after $\overline{WR}$ Rising | T − 15 | | ns | |
| $T_{WHPH}$ | $\overline{WR}$ Rising to Chip Select Rising | ½T − 10 | | ns | 1 |
| $T_{RHPH}$ | $\overline{RD}$ Rising to Chip Select Rising | ½T − 10 | | ns | 1 |
| $T_{PHPL}$ | $\overline{CS}$ Inactive to $\overline{CS}$ Active | ½T − 10 | | ns | 1 |
| $T_{OVRH}$ | $\overline{ONCE}$ Active to $\overline{RESIN}$ Rising | T | | ns | 3 |
| $T_{RHOX}$ | $\overline{ONCE}$ Hold from $\overline{RESIN}$ Rising | T | | ns | 3 |

**NOTES:**
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested

## AC SPECIFICATIONS (Continued)

### Serial Port Mode 0 Timings (80C186EB25, 20, 13/80L186EB16, 13, 8)

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $T_{XLXL}$ | TXD Clock Period | T (n + 1) | | ns | 1, 2 |
| $T_{XLXH}$ | TXD Clock Low to Clock High (n > 1) | 2T − 35 | 2T + 35 | ns | 1 |
| $T_{XLXH}$ | TXD Clock Low to Clock High (n = 1) | T − 35 | T + 35 | ns | 1 |
| $T_{XHXL}$ | TXD Clock High to Clock Low (n > 1) | (n − 1) T − 35 | (n − 1) T + 35 | ns | 1, 2 |
| $T_{XHXL}$ | TXD Clock High to Clock Low (n = 1) | T − 35 | T + 35 | ns | 1 |
| $T_{QVXH}$ | RXD Output Data Setup to TXD Clock High (n > 1) | (n − 1) T − 35 | | ns | 1, 2 |
| $T_{QVXH}$ | RXD Output Data Setup to TXD Clock High (n = 1) | T − 35 | | ns | 1 |
| $T_{XHQX}$ | RXD Output Data Hold after TXD Clock High (n > 1) | 2T − 35 | | ns | 1 |
| $T_{XHQX}$ | RXD Output Data Hold after TXD Clock High (n = 1) | T − 35 | | ns | 1 |
| $T_{XHQZ}$ | RXD Output Data Float after Last TXD Clock High | | T + 20 | ns | 1 |
| $T_{DVXH}$ | RXD Input Data Setup to TXD Clock High | T + 20 | | ns | 1 |
| $T_{XHDX}$ | RXD Input Data Hold after TXD Clock High | 0 | | ns | 1 |

**NOTES:**
1. See Figure 12 for waveforms.
2. n is the value of the BxCMP register ignoring the ICLK Bit (i.e., ICLK = 0).

## AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 7. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

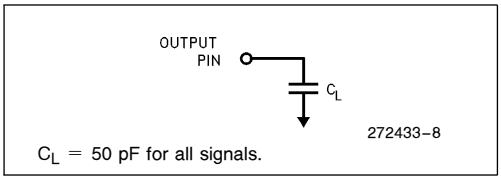



**Figure 7. AC Test Load**

## AC TIMING WAVEFORMS

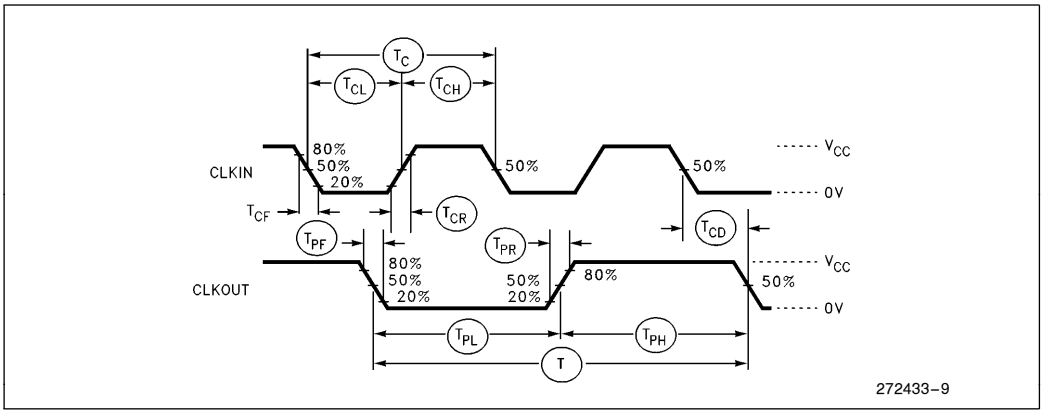
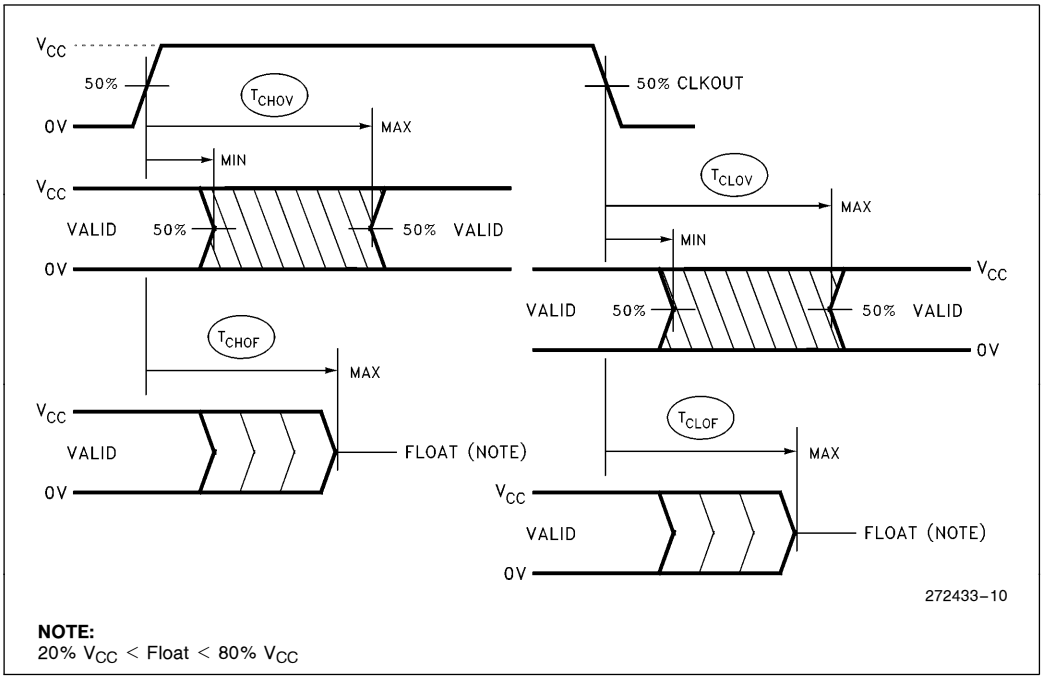



**Figure 8. Input and Output Clock Waveform**




**NOTE:**
20% $V_{CC}$ < Float < 80% $V_{CC}$

**Figure 9. Output Delay and Float Waveform**

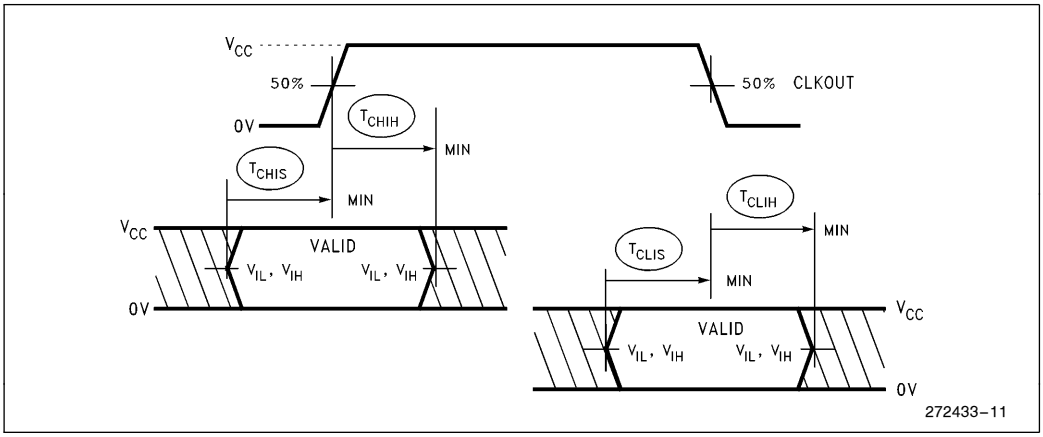
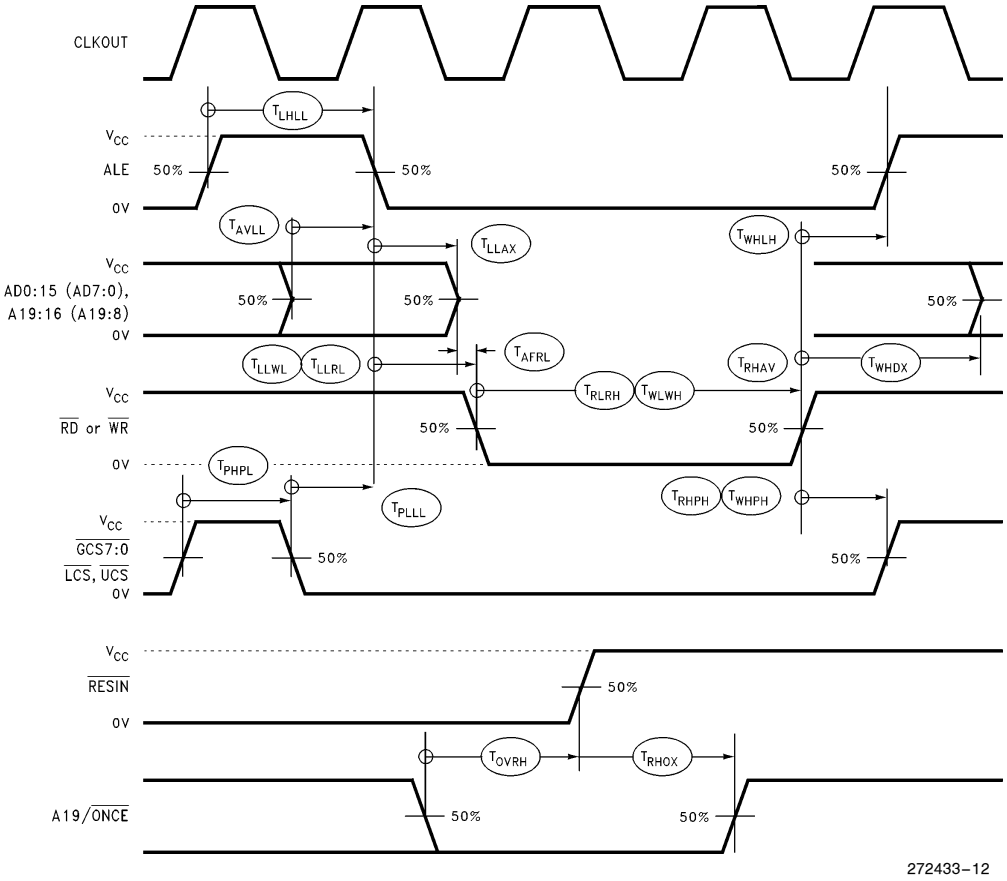



**Figure 10. Input Setup and Hold**




**NOTE:**
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 11. Relative Signal Waveform**

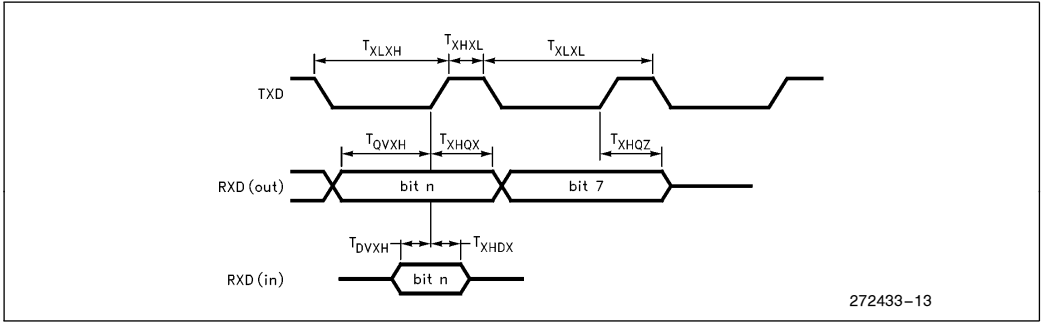



**Figure 12. Serial Port Mode 0 Waveform**

## DERATING CURVES

### TYPICAL OUTPUT DELAY VARIATIONS VERSUS LOAD CAPACITANCE

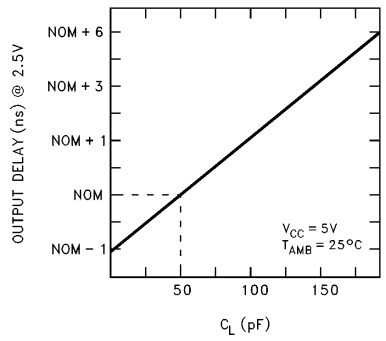



**Figure 13**

### TYPICAL RISE AND FALL VARIATIONS VERSUS LOAD CAPACITANCE

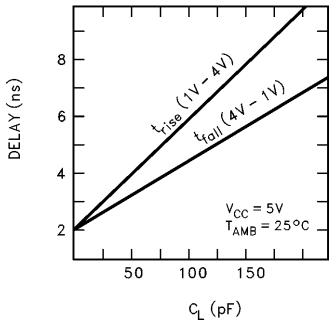



**Figure 14**

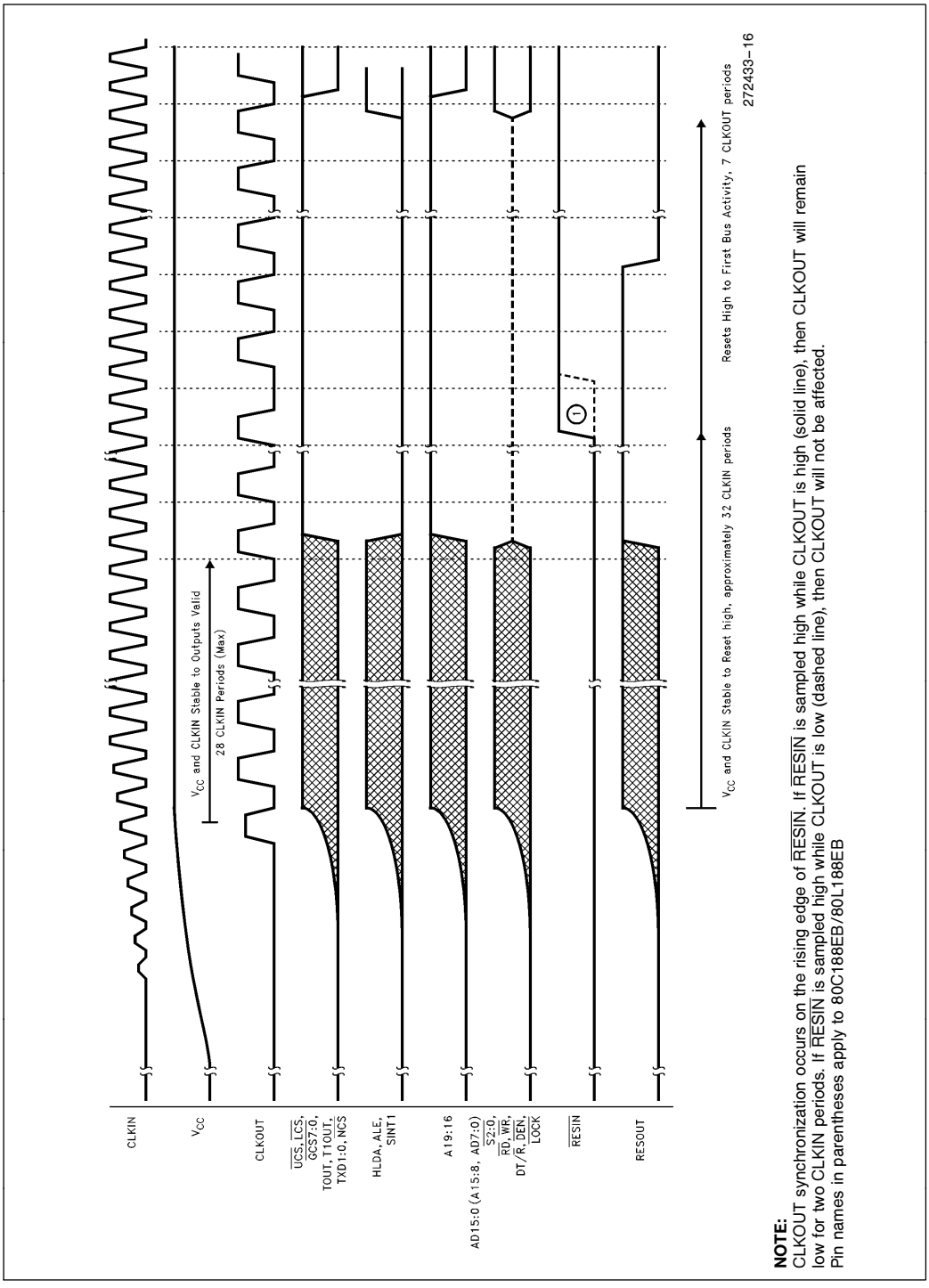
## RESET

The processor will perform a reset operation any time the RESIN pin active. The RESIN pin is actually synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, RESIN must be held active (low) in order to guarantee correct initialization of the processor. **Failure to provide RESIN while the device is powering up will result in unspecified operation of the device.**

Figure 14 shows the correct reset sequence when first applying power to the processor. An external clock connected to CLKIN must not exceed the $V_{CC}$ threshold being applied to the processor. This is normally not a problem if the clock driver is supplied with the same $V_{CC}$ that supplies the processor. When attaching a crystal to the device, RESIN must remain active until both $V_{CC}$ and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The RESIN pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for $V_{CC}$ is not so long that RESIN is never really sampled at a logic low level when $V_{CC}$ reaches minimum operating conditions.

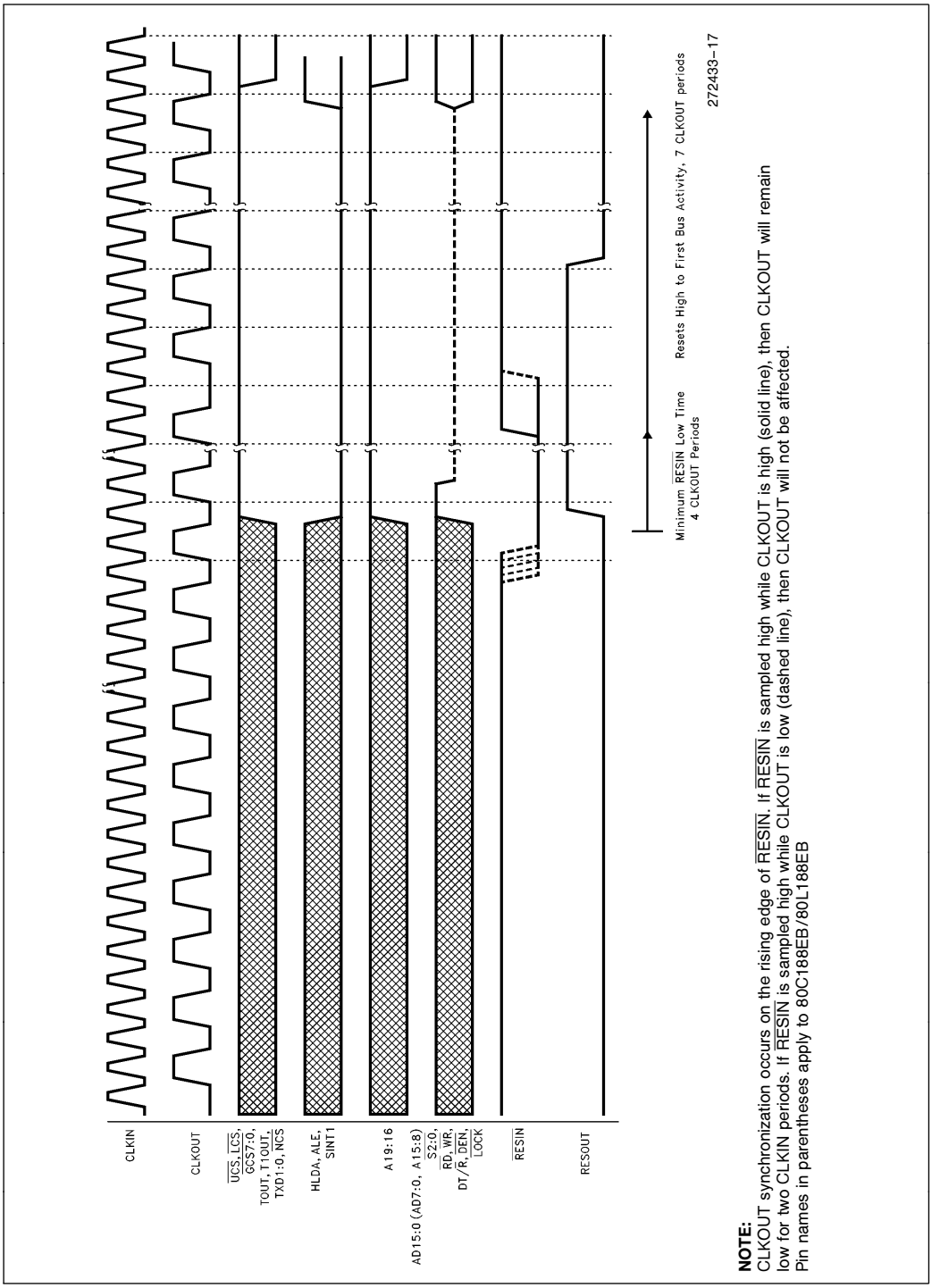
Figure 16 shows the timing sequence when RESIN is applied after $V_{CC}$ is stable and the device has been operating. Note that a reset will terminate all activity and return the processor to a known operating state. Any bus operation that is in progress at the time RESIN is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While RESIN is active, bus signals LOCK, A19/ONCE, and A18:16 are configured as inputs and weakly held high by internal pullup transistors. Only 19/ONCE can be overdriven to a low and is used to enable ONCE Mode. Forcing LOCK or A18:16 low at any time while RESIN is low is prohibited and will cause unspecified device operation.




**NOTE:**
CLKOUT synchronization occurs on the rising edge of $\overline{RESIN}$. If $\overline{RESIN}$ is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If $\overline{RESIN}$ is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 15. Cold Reset Waveforms**

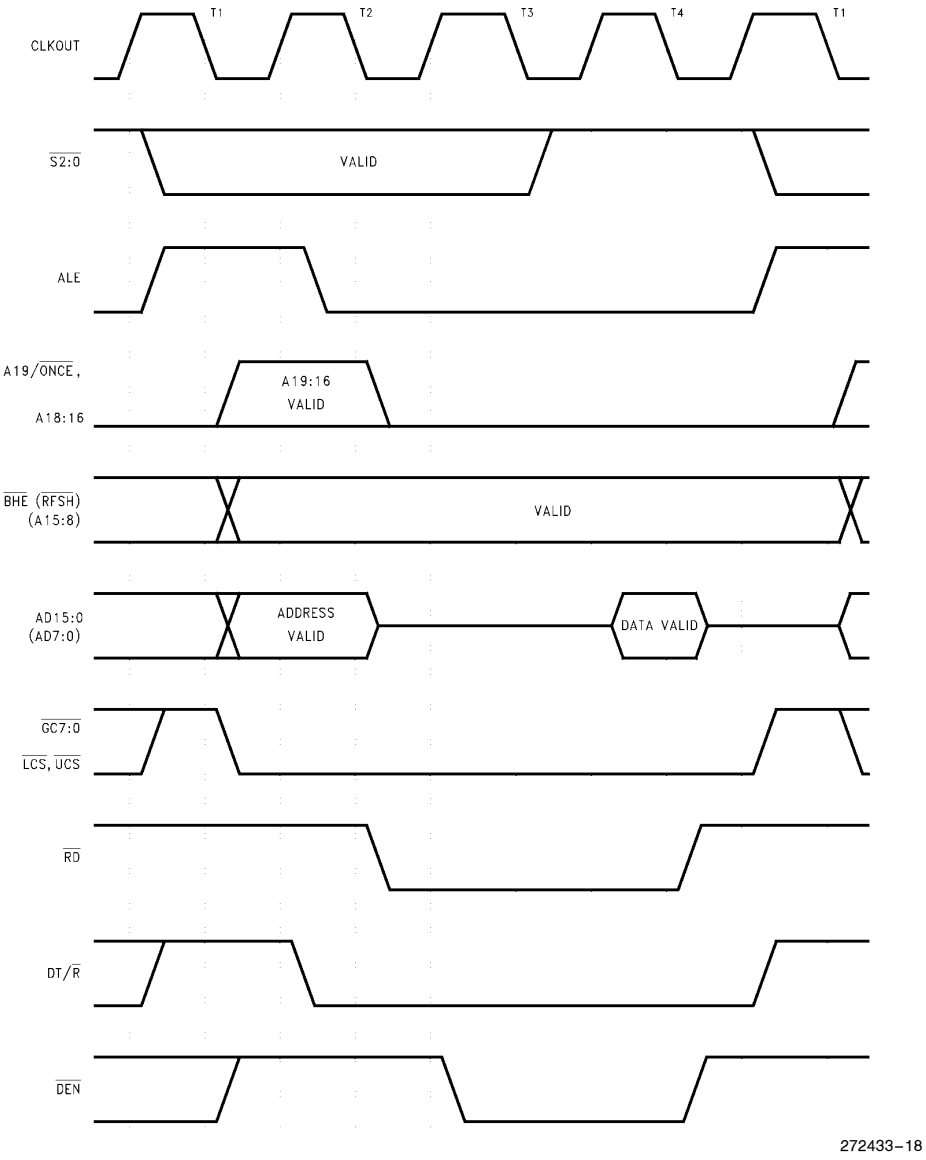



**NOTE:**
CLKOUT synchronization occurs on the rising edge of $\overline{\text{RESIN}}$. If $\overline{\text{RESIN}}$ is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If $\overline{\text{RESIN}}$ is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 16. Warm Reset Waveforms**

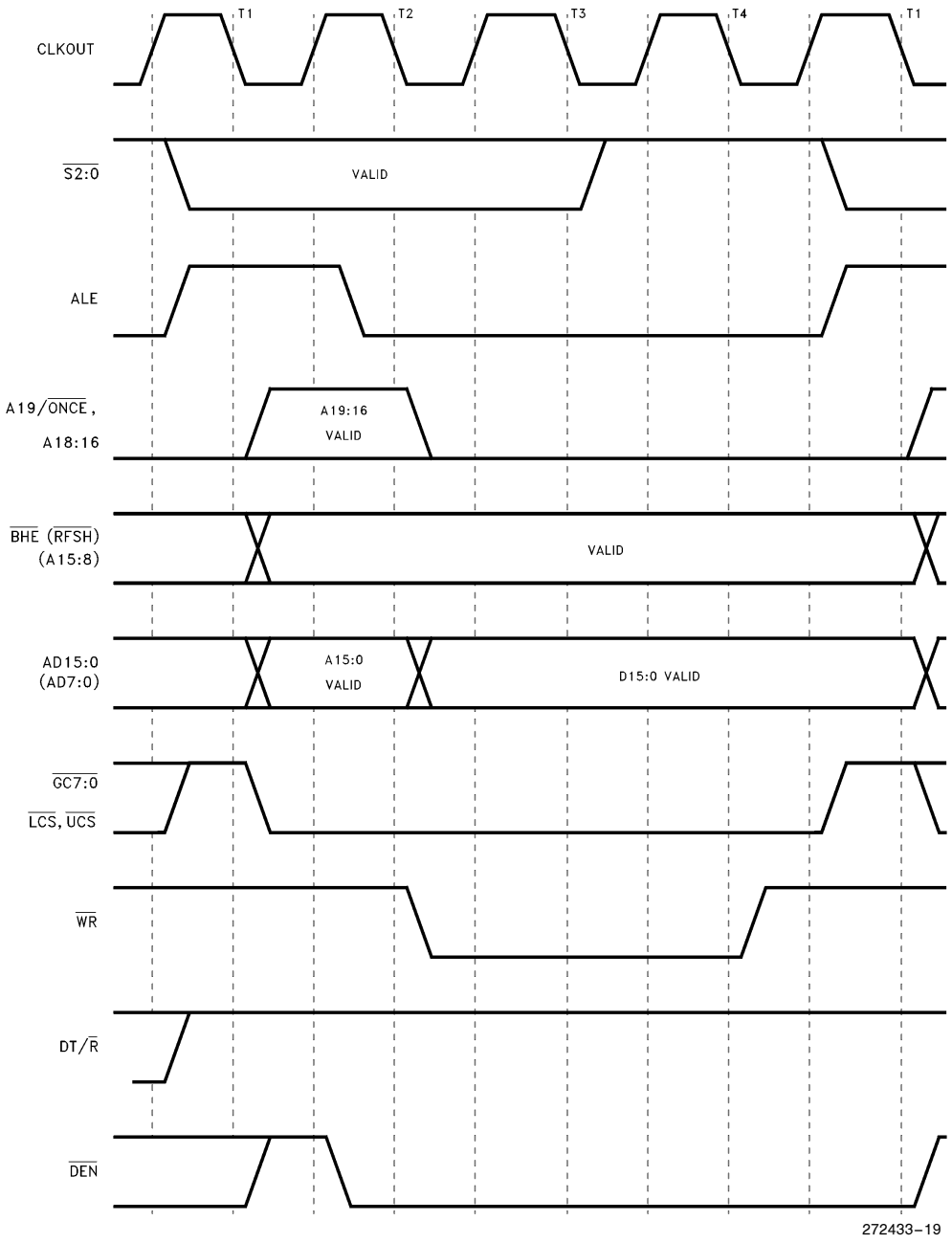
## BUS CYCLE WAVEFORMS

Figures 17 through 23 present the various bus cycles that are generated by the processor. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in **AC Specifications** allow the user to determine all the critical timing analysis needed for a given application.



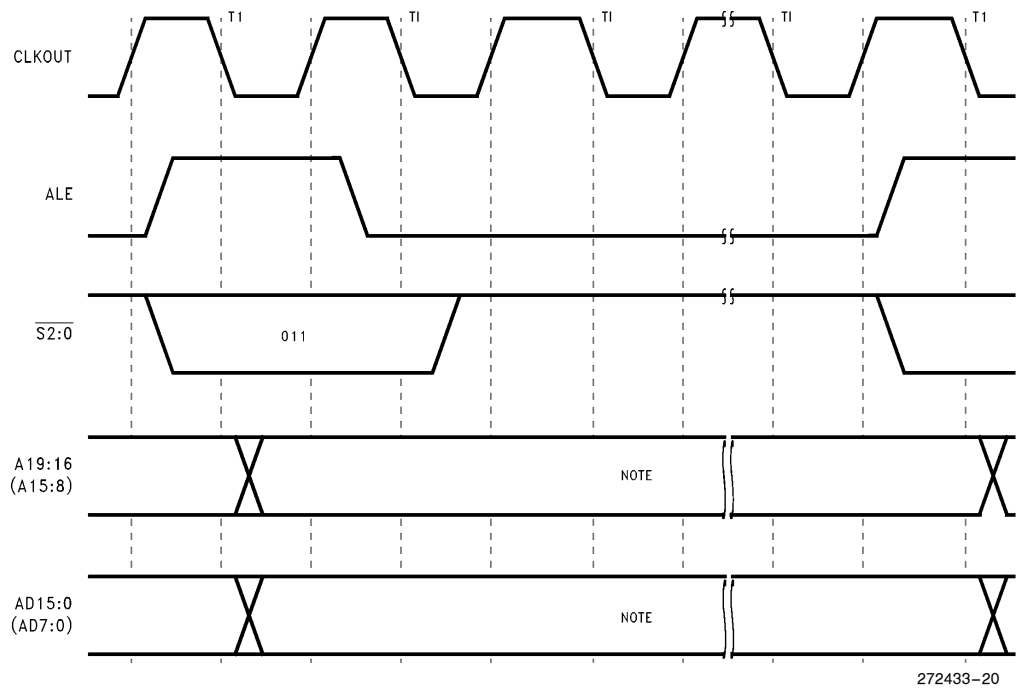

**NOTE:**
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 17. Read, Fetch, and Refresh Cycle Waveforms**



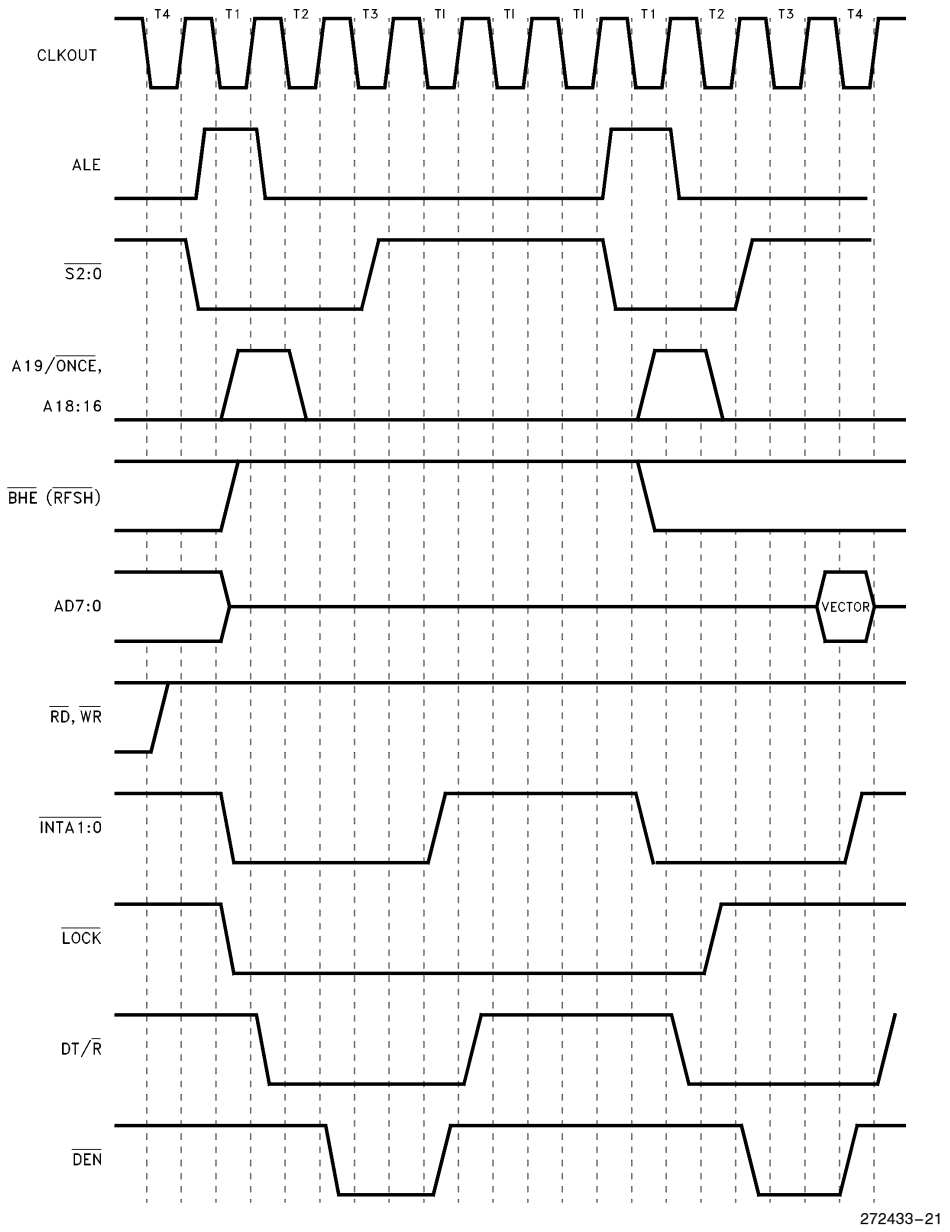

**NOTE:**
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 18. Write Cycle Waveforms**



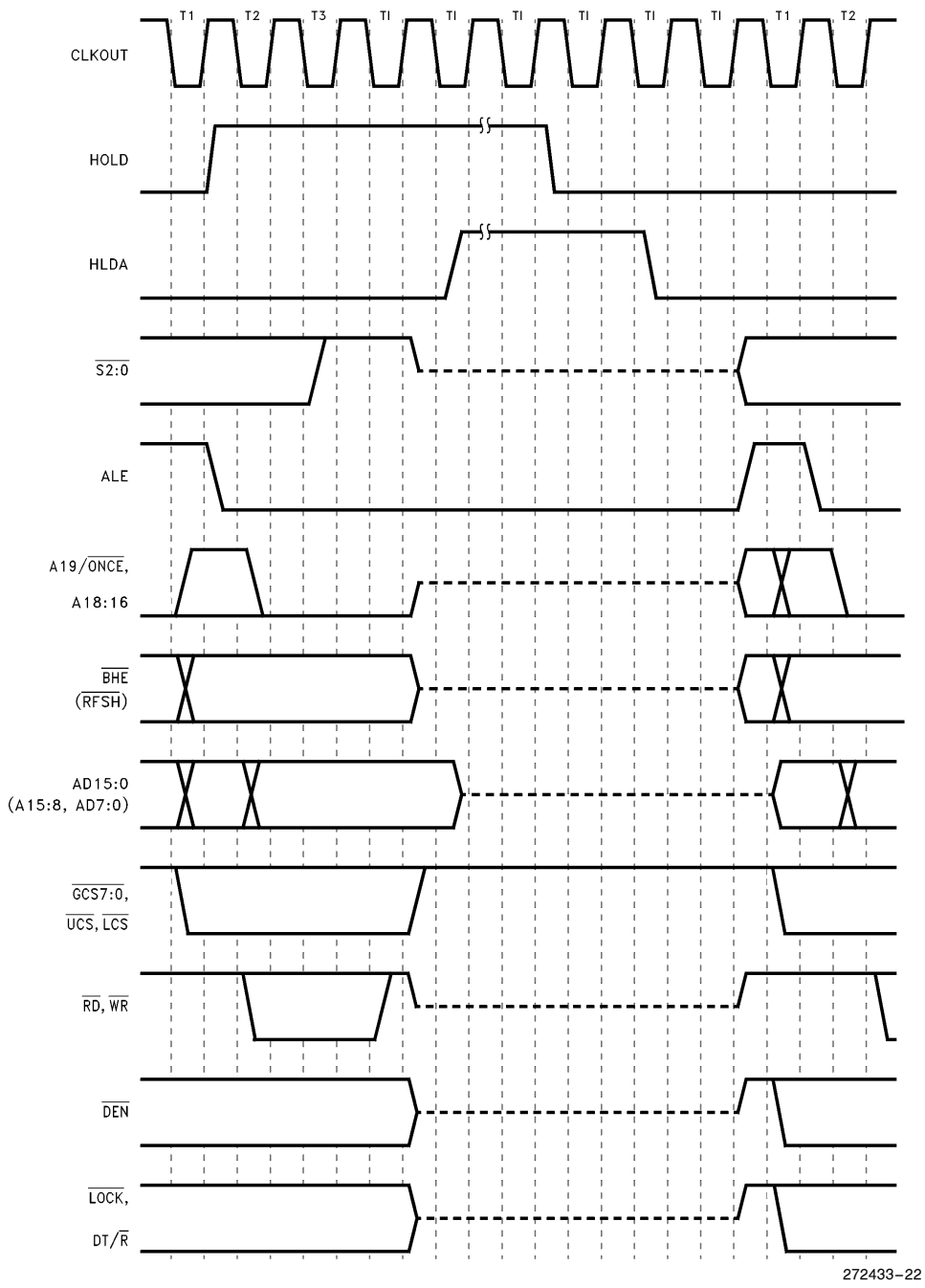

**NOTE:**
The address driven is typically the location of the next instruction prefetch. Under a majority of instruction sequences the AD15:0 (AD7:0) bus will float, while the A19:16 (A19:8) bus remains driven and all bus control signals are driven to their inactive state.
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 19. Halt Cycle Waveforms**



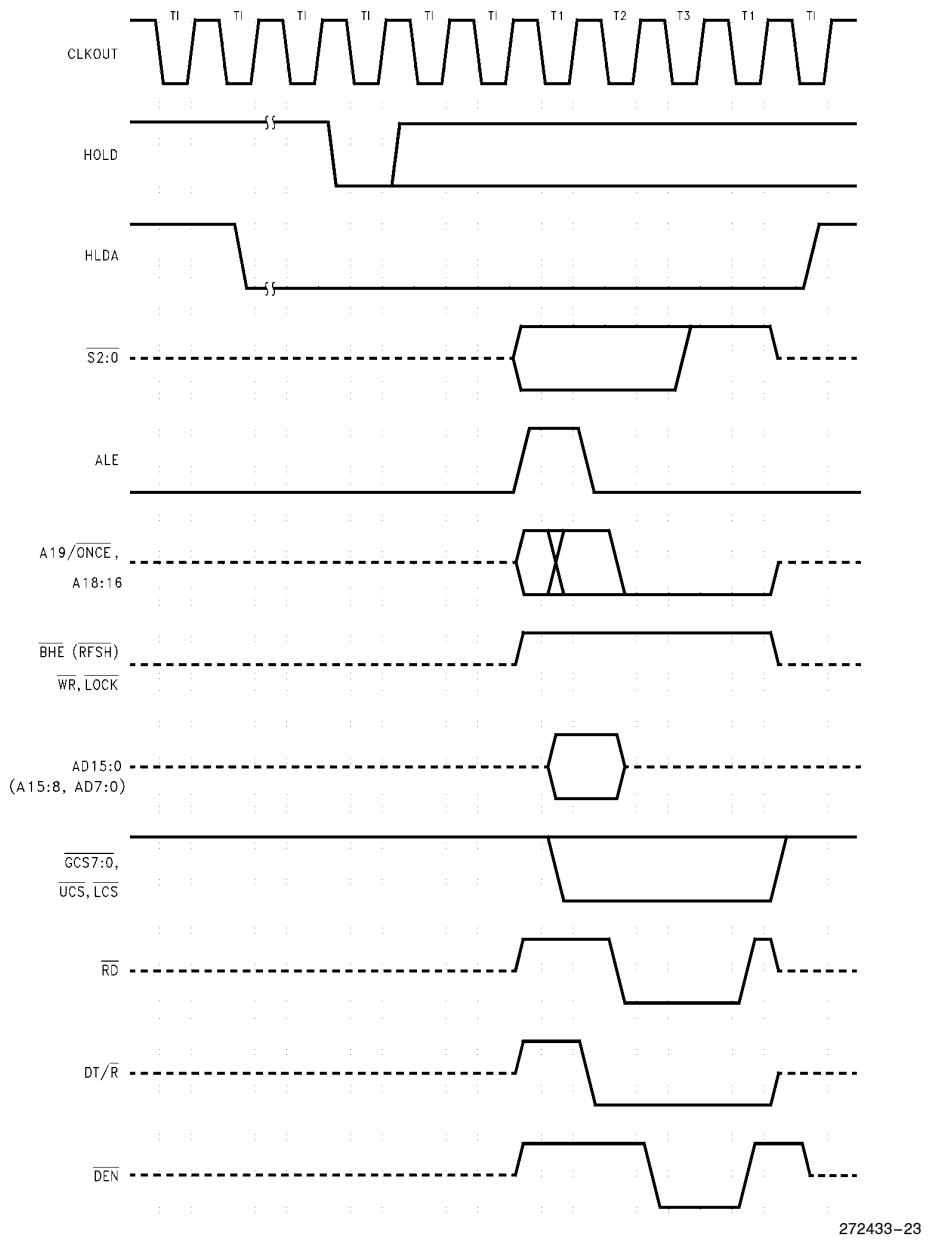

**NOTE:**
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 20. Interrupt Acknowledge Cycle Waveform**



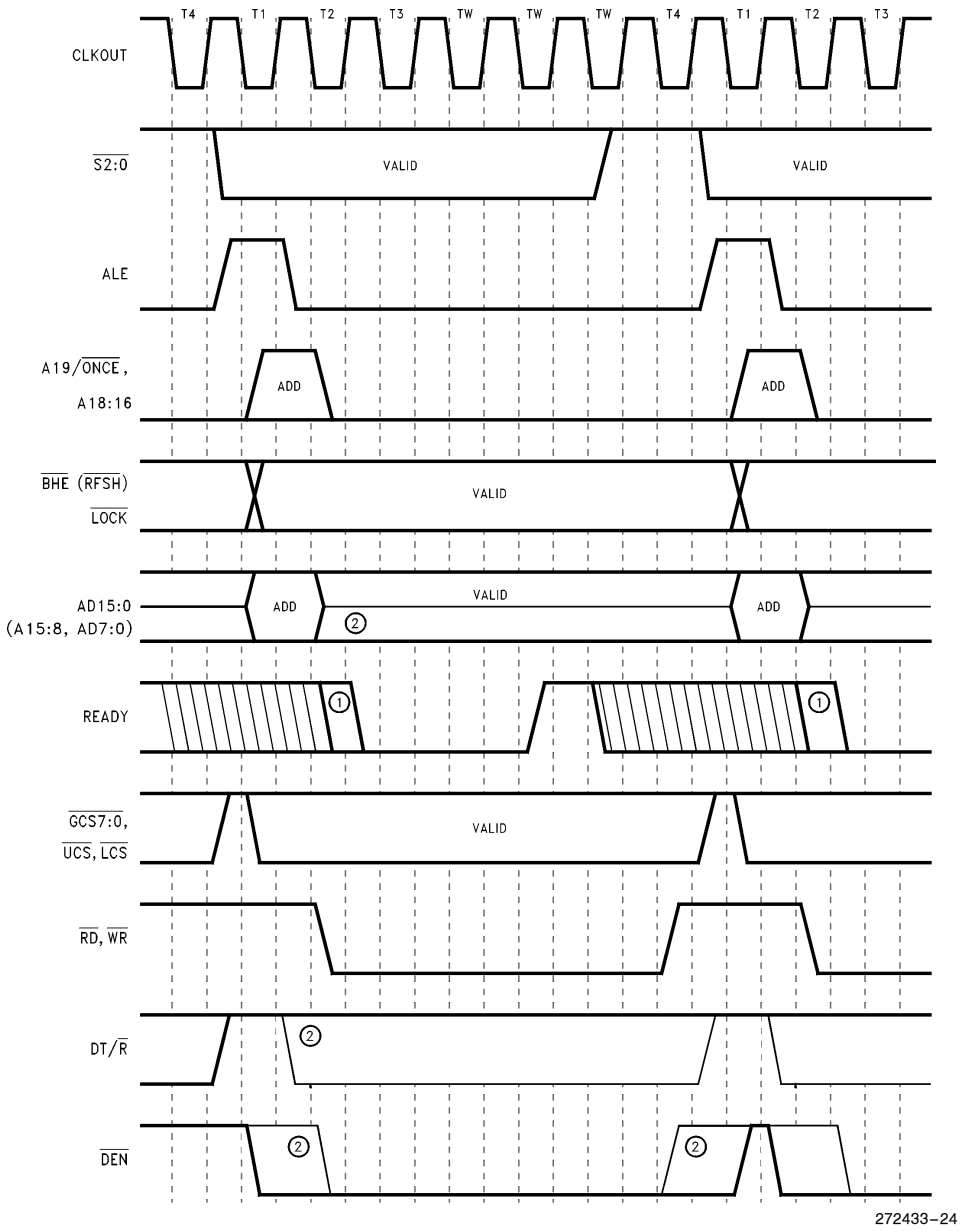

**NOTE:**
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 21. HOLD/HLDA Waveforms**




**NOTES:**
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 22. Refresh during Hold Acknowledge**




**NOTES:**
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.
Pin names in parentheses apply to 80C188EB/80L188EB

**Figure 23. Ready Waveforms**

## EXECUTION TIMINGS

A determination of program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries (80C186EB only).

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186EB has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue (6 bytes) most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

The 80C188EB 8-bit BIU is limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue (4 bytes) much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

## INSTRUCTION SET SUMMARY

| Function | Format | | | | 80C186EB Clock Cycles | 80C188EB Clock Cycles | Comments |
|---|---|---|---|---|---|---|---|
| **DATA TRANSFER** | | | | | | | |
| **MOV = Move:** | | | | | | | |
| Register to Register/Memory | 1 0 0 0 1 0 0 w | mod reg r/m | | | 2/12 | 2/12* | |
| Register/memory to register | 1 0 0 0 1 0 1 w | mod reg r/m | | | 2/9 | 2/9* | |
| Immediate to register/memory | 1 1 0 0 0 1 1 w | mod 000 r/m | data | data if w = 1 | 12/13 | 12/13 | 8/16-bit |
| Immediate to register | 1 0 1 1 w reg | data | data if w = 1 | | 3/4 | 3/4 | 8/16-bit |
| Memory to accumulator | 1 0 1 0 0 0 0 w | addr-low | addr-high | | 8 | 8* | |
| Accumulator to memory | 1 0 1 0 0 0 1 w | addr-low | addr-high | | 9 | 9* | |
| Register/memory to segment register | 1 0 0 0 1 1 1 0 | mod 0 reg r/m | | | 2/9 | 2/13 | |
| Segment register to register/memory | 1 0 0 0 1 1 0 0 | mod 0 reg r/m | | | 2/11 | 2/15 | |
| **PUSH = Push:** | | | | | | | |
| Memory | 1 1 1 1 1 1 1 1 | mod 1 1 0 r/m | | | 16 | 20 | |
| Register | 0 1 0 1 0 reg | | | | 10 | 14 | |
| Segment register | 0 0 0 reg 1 1 0 | | | | 9 | 13 | |
| Immediate | 0 1 1 0 1 0 s 0 | data | data if s = 0 | | 10 | 14 | |
| **PUSHA = Push All** | 0 1 1 0 0 0 0 0 | | | | 36 | 68 | |
| **POP = Pop:** | | | | | | | |
| Memory | 1 0 0 0 1 1 1 1 | mod 0 0 0 r/m | | | 20 | 24 | |
| Register | 0 1 0 1 1 reg | | | | 10 | 14 | |
| Segment register | 0 0 0 reg 1 1 1 | (reg≠01) | | | 8 | 12 | |
| POPA = Pop All | 0 1 1 0 0 0 0 1 | | | | 51 | 83 | |
| **XCHG = Exchange:** | | | | | | | |
| Register/memory with register | 1 0 0 0 0 1 1 w | mod reg r/m | | | 4/17 | 4/17* | |
| Register with accumulator | 1 0 0 1 0 reg | | | | 3 | 3 | |
| **IN = Input from:** | | | | | | | |
| Fixed port | 1 1 1 0 0 1 0 w | port | | | 10 | 10* | |
| Variable port | 1 1 1 0 1 1 0 w | | | | 8 | 8* | |
| **OUT = Output to:** | | | | | | | |
| Fixed port | 1 1 1 0 0 1 1 w | port | | | 9 | 9* | |
| Variable port | 1 1 1 0 1 1 1 w | | | | 7 | 7* | |
| **XLAT** = Translate byte to AL | 1 1 0 1 0 1 1 1 | | | | 11 | 15 | |
| **LEA** = Load EA to register | 1 0 0 0 1 1 0 1 | mod reg r/m | | | 6 | 6 | |
| **LDS** = Load pointer to DS | 1 1 0 0 0 1 0 1 | mod reg r/m | (mod≠11) | | 18 | 26 | |
| **LES** = Load pointer to ES | 1 1 0 0 0 1 0 0 | mod reg r/m | (mod≠11) | | 18 | 26 | |
| **LAHF** = Load AH with flags | 1 0 0 1 1 1 1 1 | | | | 2 | 2 | |
| **SAHF** = Store AH into flags | 1 0 0 1 1 1 1 0 | | | | 3 | 3 | |
| **PUSHF** = Push flags | 1 0 0 1 1 1 0 0 | | | | 9 | 13 | |
| **POPF** = Pop flags | 1 0 0 1 1 1 0 1 | | | | 8 | 12 | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | 80C186EB Clock Cycles | 80C188EB Clock Cycles | Comments |
|---|---|---|---|---|
| **DATA TRANSFER** (Continued) | | | | |
| **SEGMENT = Segment Override:** | | | | |
| **CS** | 00101110 | 2 | 2 | |
| **SS** | 00110110 | 2 | 2 | |
| **DS** | 00111110 | 2 | 2 | |
| **ES** | 00100110 | 2 | 2 | |
| **ARITHMETIC** | | | | |
| **ADD = Add:** | | | | |
| Reg/memory with register to either | 000000dw \| mod reg r/m | 3/10 | 3/10* | |
| Immediate to register/memory | 100000sw \| mod 000 r/m \| data \| data if s w=01 | 4/16 | 4/16* | |
| Immediate to accumulator | 0000010w \| data \| data if w=1 | 3/4 | 3/4 | 8/16-bit |
| **ADC = Add with carry:** | | | | |
| Reg/memory with register to either | 000100dw \| mod reg r/m | 3/10 | 3/10* | |
| Immediate to register/memory | 100000sw \| mod 010 r/m \| data \| data if s w=01 | 4/16 | 4/16* | |
| Immediate to accumulator | 0001010w \| data \| data if w=1 | 3/4 | 3/4 | 8/16-bit |
| **INC = Increment:** | | | | |
| Register/memory | 1111111w \| mod 000 r/m | 3/15 | 3/15* | |
| Register | 01000 reg | 3 | 3 | |
| **SUB = Subtract:** | | | | |
| Reg/memory and register to either | 001010dw \| mod reg r/m | 3/10 | 3/10* | |
| Immediate from register/memory | 100000sw \| mod 101 r/m \| data \| data if s w=01 | 4/16 | 4/16* | |
| Immediate from accumulator | 0010110w \| data \| data if w=1 | 3/4 | 3/4 | 8/16-bit |
| **SBB = Subtract with borrow:** | | | | |
| Reg/memory and register to either | 000110dw \| mod reg r/m | 3/10 | 3/10* | |
| Immediate from register/memory | 100000sw \| mod 011 r/m \| data \| data if s w=01 | 4/16 | 4/16* | |
| Immediate from accumulator | 0001110w \| data \| data if w=1 | 3/4 | 3/4* | 8/16-bit |
| **DEC = Decrement** | | | | |
| Register/memory | 1111111w \| mod 001 r/m | 3/15 | 3/15* | |
| Register | 01001 reg | 3 | 3 | |
| **CMP = Compare:** | | | | |
| Register/memory with register | 0011101w \| mod reg r/m | 3/10 | 3/10* | |
| Register with register/memory | 0011100w \| mod reg r/m | 3/10 | 3/10* | |
| Immediate with register/memory | 100000sw \| mod 111 r/m \| data \| data if s w=01 | 3/10 | 3/10* | |
| Immediate with accumulator | 0011110w \| data \| data if w=1 | 3/4 | 3/4 | 8/16-bit |
| **NEG** = Change sign register/memory | 1111011w \| mod 011 r/m | 3/10 | 3/10* | |
| **AAA** = ASCII adjust for add | 00110111 | 8 | 8 | |
| **DAA** = Decimal adjust for add | 00100111 | 4 | 4 | |
| **AAS** = ASCII adjust for subtract | 00111111 | 7 | 7 | |
| **DAS** = Decimal adjust for subtract | 00101111 | 4 | 4 | |
| **MUL** = Multiply (unsigned): | 1111011w \| mod 100 r/m | | | |
| Register-Byte | | 26–28 | 26–28 | |
| Register-Word | | 35–37 | 35–37 | |
| Memory-Byte | | 32–34 | 32–34 | |
| Memory-Word | | 41–43 | 41–43* | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | 80C186EB Clock Cycles | 80C188EB Clock Cycles | Comments |
|---|---|---|---|---|
| **ARITHMETIC** (Continued) | | | | |
| **IMUL** = Integer multiply (signed): | 1 1 1 1 0 1 1 w \| mod 1 0 1 r/m | | | |
| Register-Byte | | 25–28 | 25–28 | |
| Register-Word | | 34–37 | 34–37 | |
| Memory-Byte | | 31–34 | 31–34 | |
| Memory-Word | | 40–43 | 40–43* | |
| **IMUL** = Integer Immediate multiply (signed) | 0 1 1 0 1 0 s 1 \| mod reg r/m \| data \| data if s = 0 | 22–25/ 29–32 | 22–25/ 29–32 | |
| **DIV** = Divide (unsigned): | 1 1 1 1 0 1 1 w \| mod 1 1 0 r/m | | | |
| Register-Byte | | 29 | 29 | |
| Register-Word | | 38 | 38 | |
| Memory-Byte | | 35 | 35 | |
| Memory-Word | | 44 | 44* | |
| **IDIV** = Integer divide (signed): | 1 1 1 1 0 1 1 w \| mod 1 1 1 r/m | | | |
| Register-Byte | | 44–52 | 44–52 | |
| Register-Word | | 53–61 | 53–61 | |
| Memory-Byte | | 50–58 | 50–58 | |
| Memory-Word | | 59–67 | 59–67* | |
| **AAM** = ASCII adjust for multiply | 1 1 0 1 0 1 0 0 \| 0 0 0 0 1 0 1 0 | 19 | 19 | |
| **AAD** = ASCII adjust for divide | 1 1 0 1 0 1 0 1 \| 0 0 0 0 1 0 1 0 | 15 | 15 | |
| **CBW** = Convert byte to word | 1 0 0 1 1 0 0 0 | 2 | 2 | |
| **CWD** = Convert word to double word | 1 0 0 1 1 0 0 1 | 4 | 4 | |
| **LOGIC** | | | | |
| **Shift/Rotate Instructions:** | | | | |
| Register/Memory by 1 | 1 1 0 1 0 0 0 w \| mod TTT r/m | 2/15 | 2/15 | |
| Register/Memory by CL | 1 1 0 1 0 0 1 w \| mod TTT r/m | 5+n/17+n | 5+n/17+n | |
| Register/Memory by Count | 1 1 0 0 0 0 0 w \| mod TTT r/m \| count | 5+n/17+n | 5+n/17+n | |
| | **TTT Instruction**<br>0 0 0 ROL<br>0 0 1 ROR<br>0 1 0 RCL<br>0 1 1 RCR<br>1 0 0 SHL/SAL<br>1 0 1 SHR<br>1 1 1 SAR | | | |
| **AND** = **And:** | | | | |
| Reg/memory and register to either | 0 0 1 0 0 0 d w \| mod reg r/m | 3/10 | 3/10* | |
| Immediate to register/memory | 1 0 0 0 0 0 0 w \| mod 1 0 0 r/m \| data \| data if w = 1 | 4/16 | 4/16* | |
| Immediate to accumulator | 0 0 1 0 0 1 0 w \| data \| data if w = 1 | 3/4 | 3/4* | 8/16-bit |
| **TEST** = **And function to flags, no result:** | | | | |
| Register/memory and register | 1 0 0 0 0 1 0 w \| mod reg r/m | 3/10 | 3/10* | |
| Immediate data and register/memory | 1 1 1 1 0 1 1 w \| mod 0 0 0 r/m \| data \| data if w = 1 | 4/10 | 4/10* | |
| Immediate data and accumulator | 1 0 1 0 1 0 0 w \| data \| data if w = 1 | 3/4 | 3/4 | 8/16-bit |
| **OR** = **Or:** | | | | |
| Reg/memory and register to either | 0 0 0 0 1 0 d w \| mod reg r/m | 3/10 | 3/10* | |
| Immediate to register/memory | 1 0 0 0 0 0 0 w \| mod 0 0 1 r/m \| data \| data if w = 1 | 4/16 | 4/16* | |
| Immediate to accumulator | 0 0 0 0 1 1 0 w \| data \| data if w = 1 | 3/4 | 3/4* | 8/16-bit |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | 80C186EB Clock Cycles | 80C188EB Clock Cycles | Comments |
|---|---|---|---|---|
| **LOGIC** (Continued) | | | | |
| **XOR** = **Exclusive or:** | | | | |
| Reg/memory and register to either | 0 0 1 1 0 0 d w \| mod reg r/m | 3/10 | 3/10* | |
| Immediate to register/memory | 1 0 0 0 0 0 0 w \| mod 1 1 0 r/m \| data \| data if w = 1 | 4/16 | 4/16* | |
| Immediate to accumulator | 0 0 1 1 0 1 0 w \| data \| data if w = 1 | 3/4 | 3/4 | 8/16-bit |
| **NOT** = Invert register/memory | 1 1 1 1 0 1 1 w \| mod 0 1 0 r/m | 3/10 | 3/10* | |
| **STRING MANIPULATION** | | | | |
| **MOVS** = Move byte/word | 1 0 1 0 0 1 0 w | 14 | 14* | |
| **CMPS** = Compare byte/word | 1 0 1 0 0 1 1 w | 22 | 22* | |
| **SCAS** = Scan byte/word | 1 0 1 0 1 1 1 w | 15 | 15* | |
| **LODS** = Load byte/wd to AL/AX | 1 0 1 0 1 1 0 w | 12 | 12* | |
| **STOS** = Store byte/wd from AL/AX | 1 0 1 0 1 0 1 w | 10 | 10* | |
| **INS** = Input byte/wd from DX port | 0 1 1 0 1 1 0 w | 14 | 14 | |
| **OUTS** = Output byte/wd to DX port | 0 1 1 0 1 1 1 w | 14 | 14 | |
| Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ) | | | | |
| **MOVS** = Move string | 1 1 1 1 0 0 1 0 \| 1 0 1 0 0 1 0 w | 8+8n | 8+8n* | |
| **CMPS** = Compare string | 1 1 1 1 0 0 1 z \| 1 0 1 0 0 1 1 w | 5+22n | 5+22n* | |
| **SCAS** = Scan string | 1 1 1 1 0 0 1 z \| 1 0 1 0 1 1 1 w | 5+15n | 5+15n* | |
| **LODS** = Load string | 1 1 1 1 0 0 1 0 \| 1 0 1 0 1 1 0 w | 6+11n | 6+11n* | |
| **STOS** = Store string | 1 1 1 1 0 0 1 0 \| 1 0 1 0 1 0 1 w | 6+9n | 6+9n* | |
| **INS** = Input string | 1 1 1 1 0 0 1 0 \| 0 1 1 0 1 1 0 w | 8+8n | 8+8n* | |
| **OUTS** = Output string | 1 1 1 1 0 0 1 0 \| 0 1 1 0 1 1 1 w | 8+8n | 8+8n* | |
| **CONTROL TRANSFER** | | | | |
| **CALL** = **Call:** | | | | |
| Direct within segment | 1 1 1 0 1 0 0 0 \| disp-low \| disp-high | 15 | 19 | |
| Register/memory indirect within segment | 1 1 1 1 1 1 1 1 \| mod 0 1 0 r/m | 13/19 | 17/27 | |
| Direct intersegment | 1 0 0 1 1 0 1 0 \| segment offset \| segment selector | 23 | 31 | |
| Indirect intersegment | 1 1 1 1 1 1 1 1 \| mod 0 1 1 r/m (mod ≠ 11) | 38 | 54 | |
| **JMP** = **Unconditional jump:** | | | | |
| Short/long | 1 1 1 0 1 0 1 1 \| disp-low | 14 | 14 | |
| Direct within segment | 1 1 1 0 1 0 0 1 \| disp-low \| disp-high | 14 | 14 | |
| Register/memory indirect within segment | 1 1 1 1 1 1 1 1 \| mod 1 0 0 r/m | 11/17 | 11/21 | |
| Direct intersegment | 1 1 1 0 1 0 1 0 \| segment offset \| segment selector | 14 | 14 | |
| Indirect intersegment | 1 1 1 1 1 1 1 1 \| mod 1 0 1 r/m (mod ≠ 11) | 26 | 34 | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | 80C186EB Clock Cycles | 80C188EB Clock Cycles | Comments |
|---|---|---|---|---|
| **CONTROL TRANSFER** (Continued) | | | | |
| **RET** = **Return from CALL:** | | | | |
| Within segment | 11000011 | 16 | 20 | |
| Within seg adding immed to SP | 11000010 data-low data-high | 18 | 22 | |
| Intersegment | 11001011 | 22 | 30 | |
| Intersegment adding immediate to SP | 11001010 data-low data-high | 25 | 33 | |
| **JE/JZ** = Jump on equal/zero | 01110100 disp | 4/13 | 4/13 | JMP not taken/JMP taken |
| **JL/JNGE** = Jump on less/not greater or equal | 01111100 disp | 4/13 | 4/13 | |
| **JLE/JNG** = Jump on less or equal/not greater | 01111110 disp | 4/13 | 4/13 | |
| **JB/JNAE** = Jump on below/not above or equal | 01110010 disp | 4/13 | 4/13 | |
| **JBE/JNA** = Jump on below or equal/not above | 01110110 disp | 4/13 | 4/13 | |
| **JP/JPE** = Jump on parity/parity even | 01111010 disp | 4/13 | 4/13 | |
| **JO** = Jump on overflow | 01110 000 disp | 4/13 | 4/13 | |
| **JS** = Jump on sign | 01111000 disp | 4/13 | 4/13 | |
| **JNE/JNZ** = Jump on not equal/not zero | 01110101 disp | 4/13 | 4/13 | |
| **JNL/JGE** = Jump on not less/greater or equal | 01111101 disp | 4/13 | 4/13 | |
| **JNLE/JG** = Jump on not less or equal/greater | 01111111 disp | 4/13 | 4/13 | |
| **JNB/JAE** = Jump on not below/above or equal | 01110011 disp | 4/13 | 4/13 | |
| **JNBE/JA** = Jump on not below or equal/above | 01110111 disp | 4/13 | 4/13 | |
| **JNP/JPO** = Jump on not par/par odd | 01111011 disp | 4/13 | 4/13 | |
| **JNO** = Jump on not overflow | 01110001 disp | 4/13 | 4/13 | |
| **JNS** = Jump on not sign | 01111001 disp | 4/13 | 4/13 | |
| **JCXZ** = Jump on CX zero | 11100011 disp | 5/15 | 5/15 | |
| **LOOP** = Loop CX times | 11100010 disp | 6/16 | 6/16 | LOOP not taken/LOOP taken |
| **LOOPZ/LOOPE** = Loop while zero/equal | 11100001 disp | 6/16 | 6/16 | |
| **LOOPNZ/LOOPNE** = Loop while not zero/equal | 11100000 disp | 6/16 | 6/16 | |
| **ENTER** = Enter Procedure | 11001000 data-low data-high L | | | |
| L = 0 | | 15 | 19 | |
| L = 1 | | 25 | 29 | |
| L > 1 | | 22+16(n−1) | 26+20(n−1) | |
| **LEAVE** = Leave Procedure | 11001001 | 8 | 8 | |
| **INT** = **Interrupt:** | | | | |
| Type specified | 11001101 type | 47 | 47 | |
| Type 3 | 11001100 | 45 | 45 | if INT. taken/ if INT. not taken |
| **INTO** = Interrupt on overflow | 11001110 | 48/4 | 48/4 | |
| **IRET** = Interrupt return | 11001111 | 28 | 28 | |
| **BOUND** = Detect value out of range | 01100010 mod reg r/m | 33–35 | 33–35 | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | 80C186EB Clock Cycles | 80C188EB Clock Cycles | Comments |
|---|---|---|---|---|
| **PROCESSOR CONTROL** | | | | |
| **CLC** = Clear carry | 11111000 | 2 | 2 | |
| **CMC** = Complement carry | 11110101 | 2 | 2 | |
| **STC** = Set carry | 11111001 | 2 | 2 | |
| **CLD** = Clear direction | 11111100 | 2 | 2 | |
| **STD** = Set direction | 11111101 | 2 | 2 | |
| **CLI** = Clear interrupt | 11111010 | 2 | 2 | |
| **STI** = Set interrupt | 11111011 | 2 | 2 | |
| **HLT** = Halt | 11110100 | 2 | 2 | |
| **WAIT** = Wait | 10011011 | 6 | 6 | if $\overline{TEST}$ = 0 |
| **LOCK** = Bus lock prefix | 11110000 | 2 | 2 | |
| **NOP** = No Operation | 10010000 | 3 | 3 | |
| | (TTT LLL are opcode to processor extension) | | | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

## FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

**Segment Override Prefix**

| 0 | 0 | 1 | reg | 1 | 1 | 0 |
|---|---|---|---|---|---|---|

reg is assigned according to the following:

| reg | Segment Register |
|---|---|
| 00 | ES |
| 01 | CS |
| 10 | SS |
| 11 | DS |

REG is assigned according to the following table:

| 16-Bit (w = 1) | 8-Bit (w = 0) |
|---|---|
| 000 AX | 000 AL |
| 001 CX | 001 CL |
| 010 DX | 010 DL |
| 011 BX | 011 BL |
| 100 SP | 100 AH |
| 101 BP | 101 CH |
| 110 SI | 110 DH |
| 111 DI | 111 BH |

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

## ERRATA

An 80C186EB/80L186EB with a STEPID value of 0001H has the following known errata. A device with a STEPID of 0001H can be visually identified by the **presence** of an **"A"** alpha character next to the FPO number. The FPO number location is shown in Figures 4, 5 and 6.

1. A19/$\overline{\text{ONCE}}$ is not latched by the rising edge of $\overline{\text{RESIN}}$. A19/$\overline{\text{ONCE}}$ must remain active (LOW) at all times to remain in the ONCE Mode. Removing A19/$\overline{\text{ONCE}}$ after $\overline{\text{RESIN}}$ is high will return all output pins to a driving state, however, the 80C186EB will remain in a reset state.
2. During interrupt acknowledge (INTA) bus cycles, the bus controller will ignore the state of the READY pin if the previous bus cycle ignored the state of the READY pin. This errata can only occur if the Chip-Select Unit is being used. All active chip-selects must be programmed to use READY (RDY bit must be programmed to a 1) if wait-states are required for INTA bus cycles.
3. CLKOUT will transition off the **rising** edge of CLKIN rather than the falling edge of CLKIN. This does not affect any bus timings other than $T_{CD}$.
4. $\overline{\text{RESIN}}$ has a hysterisis of only 130 mV. It is recommended that $\overline{\text{RESIN}}$ be driven by a Schmitt triggered device to avoid processor lockup during reset using an RC circuit.
5. SINT1 will only go active for one clock period when a receive or transmit interrupt is pending (i.e., it does not remain active until the S1STS register is read). If SINT1 is to be connected to any of the processor interrupt lines (INT0–INT4), then it must be latched by user logic.

An 80C186EB/80L186EB with a STEPID value of 0001H or 0002H has the following known errata. A device with a STEPID of 0002H can be visually identified by noting the presence of a ''B'', ''C'', ''D'', or ''E'' alpha character next to the FPO number. The FPO number location is shown in Figures 4, 5 and 6.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the $\overline{\text{INTA1}}$ line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

## REVISION HISTORY

This data sheet replaces the following data sheets:

| | |
|---|---|
| 270803-004 | 80C186EB |
| 270885-003 | 80C188EB |
| 270921-003 | 80L186EB |
| 270920-003 | 80L188EB |
| 272311-001 | SB80C188EB/SB80L188EB |
| 272312-001 | SB80C186EB/SB80L186EB |

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А