# 16-bit or 24-bit, 2/4/8-channel ADCs with PGIA

## Features

- Low Input Current (100 pA), Chopper-stabilized Instrumentation Amplifier
- Scalable Input Span (Bipolar/Unipolar)
  - 2.5V VREF: 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, 5 V
  - External: 10 V, 100 V
- Wide $V_{REF}$ Input Range (+1 to +5 V)
- Fourth Order Delta-Sigma A/D Converter
- Easy to Use Three-wire Serial Interface Port
  - Programmable/Auto Channel Sequencer with Conversion Data FIFO
  - Accessible Calibration Registers per Channel
  - Compatible with SPI™ and Microwire™
- System and Self Calibration
- Eight Selectable Word Rates
  - Up to 617 Sps (XIN = 200 kHz)
  - Single Conversion Settling
  - 50/60 Hz ±3 Hz Simultaneous Rejection
- Single +5 V Power Supply Operation
  - Charge Pump Drive for Negative Supply
  - +3 to +5 V Digital Supply Operation
- Low Power Consumption: 6.0 mW

## General Description

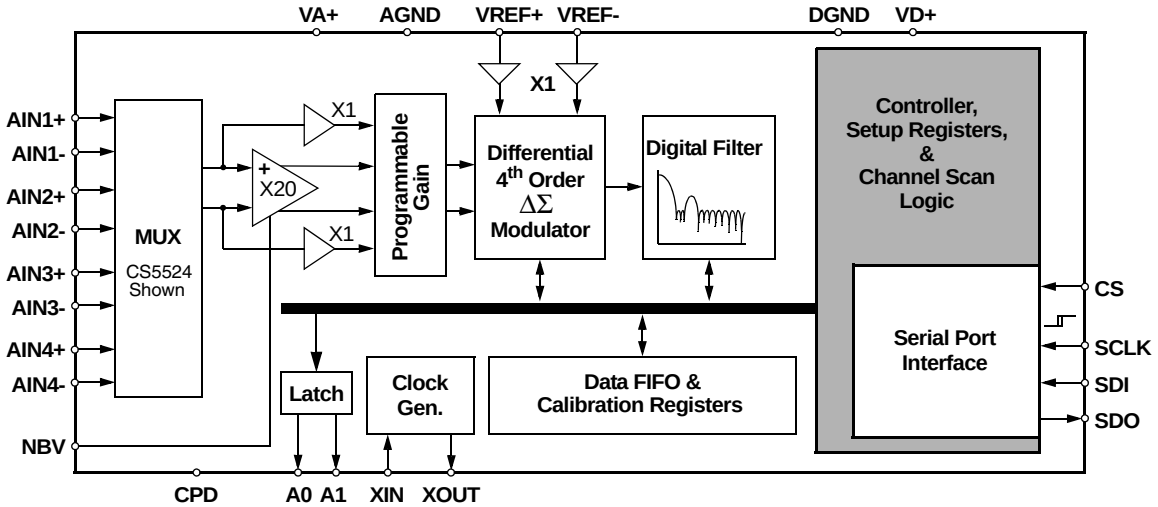
The CS5521/22/23/24/28 are highly integrated ΔΣ analog-to-digital converters (ADCs) which use charge-balance techniques to achieve 16-bit (CS5521/23) and 24-bit (CS5522/24/28) performance. The ADCs come as either two-channel (CS5521/22), four-channel (CS5523/24), or eight-channel (CS5528) devices and include a low-input-current, chopper-stabilized instrumentation amplifier. To permit selectable input spans of 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, and 5 V, the ADCs include a PGA (programmable gain amplifier). To accommodate ground-based thermocouple applications, the devices include a charge pump drive which provides a negative bias voltage to the on-chip amplifiers.

These devices also include a fourth-order ΔΣ modulator followed by a digital filter which provides eight selectable output word rates. The digital filters are designed to settle to full accuracy within one conversion cycle and when operated at word rates below 30 Sps, they reject both 50 Hz and 60 Hz interference.

These single-supply products are ideal solutions for measuring isolated and non-isolated, low-level signals in process control applications.

**ORDERING INFORMATION**

See page 53.



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# TABLE OF CONTENTS

## LIST OF FIGURES



## LIST OF TABLES

## CHARACTERISTICS AND SPECIFICATIONS

## ANALOG CHARACTERISTICS ($T_A$ = 25° C; VA+, VD+ = 5 V ±5%; VREF+ = 2.5 V, VREF- = AGND, NBV = -2.1 V, XIN = 32.768 kHz, CFS1-CFS0 = '00', OWR (Output Word Rate) = 15 Sps, Bipolar Mode, Input Range = ±100 mV; See Notes 1 and 2.)

| Parameter | CS5521/23 | | | CS5522/24/28 | | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | |
| ***Accuracy*** | | | | | | | |
| Resolution | - | - | 16 | - | - | 24 | Bits |
| Linearity Error | - | ±0.0015 | ±0.003 | - | ±0.0007 | ±0.0015 | %FS |
| Bipolar Offset (Note 3) | - | ±1 | ±2 | - | ±16 | ±32 | $LSB_N$ |
| Unipolar Offset (Note 3) | - | ±2 | ±4 | - | ±32 | ±64 | $LSB_N$ |
| Offset Drift (Notes 3 and 4) | - | 20 | - | - | 20 | - | nV/°C |
| Bipolar Gain Error | - | ±8 | ±31 | - | ±8 | ±31 | ppm |
| Unipolar Gain Error | - | ±16 | ±62 | - | ±16 | ±62 | ppm |
| Gain Drift (Note 4) | - | 1 | 3 | - | 1 | 3 | ppm/°C |
| ***Power Supplies*** | | | | | | | |
| Power Supply Currents (Normal Mode) | | | | | | | |
| $I_{A+}$ | - | 1.2 | 1.6 | - | 1.5 | 2.1 | mA |
| (Note 5) $I_{D+}$ | - | 110 | 150 | - | 110 | 150 | µA |
| $I_{NBV}$ | - | 400 | 570 | - | 525 | 700 | µA |
| Power Consumption (Note 6) | | | | | | | |
| Normal Mode | - | 7.0 | 10 | - | 10.1 | 14.8 | mW |
| Low Power Mode | N/A | N/A | N/A | - | 5.5 | 7.5 | mW |
| Sleep | - | 500 | - | - | 500 | - | µW |
| Power Supply Rejection | | | | | | | |
| Positive Supplies | - | 120 | - | - | 120 | - | dB |
| dc NBV | - | 110 | - | - | 110 | - | dB |

Notes:
1. Applies after system calibration at any temperature within -40° C ~ +85° C.
2. Specifications guaranteed by design, characterization, and/or test.
3. Specification applies to the device only and does not include any effects by external parasitic thermocouples. $LSB_N$: N is 16 for the CS5521/23 and N is 24 for the CS5522/24/28
4. Drift over specified temperature range after calibration at power-up at 25° C.
5. Measured with Charge Pump Drive off.
6. All outputs unloaded. All input CMOS levels and the CS5521/23 do not have a low power mode.

## ANALOG CHARACTERISTICS (Continued)

| Parameter | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***Analog Input*** | | | | | | |
| Common Mode + Signal on AIN+ or AIN- | | Bipolar/Unipolar Mode | | | | |
| NBV = -1.8 to -2.5 V | | Range = 25 mV, 55 mV, or 100 mV | -0.150 | - | 0.950 | V |
| | | Range = 1 V, 2.5 V, or 5 V | NBV | - | VA+ | V |
| NBV = AGND | | Range = 25 mV, 55 mV, or 100 mV (Note 7) | 1.85 | - | 2.65 | V |
| | | Range = 1 V, 2.5 V, or 5 V | 0.0 | - | VA+ | V |
| CVF Current on AIN+ or AIN- | | (Note 8) | | | | |
| | | Range = 25 mV, 55 mV, or 100 mV | - | 100 | 300 | pA |
| | | Range = 1 V, 2.5 V, or 5 V | - | 10 | - | nA |
| Input Current Drift | | (Note 8) | | | | |
| | | Range = 25 mV, 55 mV, or 100 mV | - | 1 | - | pA/°C |
| Input Leakage for Multiplexer when Off | | | - | 10 | - | pA |
| Common Mode Rejection | dc | | - | 120 | - | dB |
| | 50, 60 Hz | | - | 120 | - | dB |
| Input Capacitance | | | - | 10 | - | pF |
| ***Voltage Reference Input*** | | | | | | |
| Range | (VREF+) - (VREF-) | | 1 | 2.5 | VA+ | V |
| VREF+ | | | (VREF-)+1 | - | VA+ | V |
| VREF- | | | NBV | - | (VREF+)-1 | V |
| CVF Current | | (Note 8) | - | 5.0 | - | nA |
| Common Mode Rejection | dc | | - | 110 | - | dB |
| | 50, 60 Hz | | - | 130 | - | dB |
| Input Capacitance | | | - | 16 | - | pF |
| ***System Calibration Specifications*** | | | | | | |
| Full Scale Calibration Range (VREF = 2.5V) | | Bipolar/Unipolar Mode | | | | |
| | 25 mV | | 10 | - | 32.5 | mV |
| | 55 mV | | 25 | - | 71.5 | mV |
| | 100 mV | | 40 | - | 105 | mV |
| | 1 V | | 0.40 | - | 1.30 | V |
| | 2.5 V | | 1.0 | - | 3.25 | V |
| | 5 V | | 2.0 | - | VA+ | V |
| Offset Calibration Range | | Bipolar/Unipolar Mode | | | | |
| | 25 mV | | - | - | ±12.5 | mV |
| | 55 mV | | - | - | ±27.5 | mV |
| | 100 mV | (Note 9) | - | - | ±50 | mV |
| | 1 V | | - | - | ±0.5 | V |
| | 2.5 V | | - | - | ±1.25 | V |
| | 5 V | | - | - | ±2.50 | V |

Notes:
7. For the CS5528, the 25 mV, 55 mV and 100 mV ranges cannot be used unless NBV is powered at -1.8 to -2.5 V
8. See the section of the data sheet which discusses input models. Chop clock is 256 Hz (XIN/128) for PGIA (programmable gain instrumentation amplifier). XIN = 32.768 kHz.
9. The maximum full scale signal can be limited by saturation of circuitry within the internal signal path.

## TYPICAL RMS NOISE, CS5521/23 (Notes 10 and 11)

| Output Rate (Sps) | -3 dB Filter Frequency | Input Range, (Bipolar/Unipolar Mode) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 25 mV | 55 mV | 100 mV | 1 V | 2.5 V | 5 V |
| 1.88 | 1.64 | 90 nV | 148 nV | 220 nV | 1.8 µV | 3.9 µV | 7.8 µV |
| 3.76 | 3.27 | 122 nV | 182 nV | 310 nV | 2.6 µV | 5.7 µV | 11.3 µV |
| 7.51 | 6.55 | 180 nV | 267 nV | 435 nV | 3.7 µV | 8.5 µV | 18.1 µV |
| 15.0 | 12.7 | 280 nV | 440 nV | 810 nV | 5.7 µV | 14 µV | 28 µV |
| 30.0 | 25.4 | 580 nV | 1.1 µV | 2.1 µV | 18.2 µV | 48 µV | 96 µV |
| 61.6 (Note 12) | 50.4 | 2.6 µV | 4.9 µV | 8.5 µV | 92 µV | 238 µV | 390 µV |
| 84.5 (Note 12) | 70.7 | 11 µV | 27 µV | 43 µV | 458 µV | 1.1 mV | 2.4 mV |
| 101.1 (Note 12) | 84.6 | 41 µV | 72 µV | 130 µV | 1.2 mV | 3.4 mV | 6.7 mV |

Notes: 10. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25° C.

11. To estimate Peak-to-Peak Noise, multiply RMS noise by 6.6 for all ranges and output rates.

12. For input ranges <100 mV and output rates ≥60 Sps, 16.384 kHz chopping frequency is used.

## TYPICAL NOISE FREE RESOLUTION (BITS), CS5521/23 (Note 13)

| Output Rate (Sps) | -3 dB Filter Frequency | Input Range, (Bipolar Mode) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 25 mV | 55 mV | 100 mV | 1 V | 2.5 V | 5 V |
| 1.88 | 1.64 | 16 | 16 | 16 | 16 | 16 | 16 |
| 3.76 | 3.27 | 16 | 16 | 16 | 16 | 16 | 16 |
| 7.51 | 6.55 | 15 | 16 | 16 | 16 | 16 | 16 |
| 15.0 | 12.7 | 15 | 15 | 15 | 16 | 16 | 16 |
| 30.0 | 25.4 | 14 | 14 | 14 | 14 | 14 | 14 |
| 61.6 (Note 12) | 50.4 | 12 | 12 | 12 | 12 | 12 | 12 |
| 84.5 (Note 12) | 70.7 | 9 | 9 | 9 | 9 | 9 | 9 |
| 101.1 (Note 12) | 84.6 | 8 | 8 | 8 | 8 | 8 | 8 |

Notes: 13. For bipolar mode, the number of bits of Noise Free Resolution is LOG((2XInput Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. For unipolar mode, the number of bits of Noise Free Resolution is LOG((Input Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. Also, the CS5521/23's output conversions are 16 bits. Noise free Resolution numbers are based upon VREF = 2.5 V and XIN = 32.768 kHz. The values will be affected directly by changes in VREF, but the effects due to changes in the XIN frequency will be minor.

## TYPICAL RMS NOISE, CS5522/24/28 (Notes 14 and 15)

| Output Rate (Sps) | -3 dB Filter Frequency | Input Range, (Bipolar/Unipolar Mode) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 25 mV | 55 mV | 100 mV | 1 V | 2.5 V | 5 V |
| 1.88 | 1.64 | 90 nV | 95 nV | 140 nV | 1.5 µV | 3 µV | 6 µV |
| 3.76 | 3.27 | 110 nV | 130 nV | 190 nV | 2 µV | 4 µV | 8 µV |
| 7.51 | 6.55 | 170 nV | 200 nV | 275 nV | 2.5 µV | 6 µV | 11.5 µV |
| 15.0 | 12.7 | 250 nV | 330 nV | 580 nV | 4.5 µV | 10 µV | 20 µV |
| 30.0 | 25.4 | 500 nV | 1 µV | 1.5 µV | 16 µV | 45 µV | 85 µV |
| 61.6 (Note 16) | 50.4 | 2 µV | 4 µV | 8 µV | 72 µV | 195 µV | 350 µV |
| 84.5 (Note 16) | 70.7 | 10 µV | 20 µV | 35 µV | 340 µV | 900 µV | 2 mV |
| 101.1 (Note 16) | 84.6 | 30 µV | 60 µV | 105 µV | 1.1 mV | 3 mV | 5.3 mV |

Notes: 14. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25° C.

15. To estimate Peak-to-Peak Noise, multiply RMS noise by 6.6 for all ranges and output rates.

16. For input ranges <100 mV and output rates ≥60 Sps, 16.384 kHz chopping frequency is used.

## TYPICAL NOISE FREE RESOLUTION (BITS), CS5522/24/28 (Note 17)

| Output Rate (Sps) | -3 dB Filter Frequency | Input Range, (Bipolar Mode) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 25 mV | 55 mV | 100 mV | 1 V | 2.5 V | 5 V |
| 1.88 | 1.64 | 16 | 17 | 18 | 18 | 18 | 18 |
| 3.76 | 3.27 | 16 | 17 | 17 | 17 | 18 | 18 |
| 7.51 | 6.55 | 15 | 16 | 17 | 17 | 17 | 17 |
| 15.0 | 12.7 | 15 | 16 | 16 | 16 | 16 | 16 |
| 30.0 | 25.4 | 14 | 14 | 14 | 14 | 14 | 14 |
| 61.6 (Note 16) | 50.4 | 12 | 12 | 12 | 12 | 12 | 12 |
| 84.5 (Note 16) | 70.7 | 10 | 10 | 10 | 10 | 10 | 10 |
| 101.1 (Note 16) | 84.6 | 8 | 8 | 8 | 8 | 8 | 8 |

Notes: 17. For bipolar mode, the number of bits of Noise Free Resolution is LOG((2XInput Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. For unipolar mode, the number of bits of Noise Free Resolution is LOG((Input Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. Also, the CS5522/24/28's output conversions are 24 bits. Noise free Resolution numbers are based upon VREF = 2.5 V and XIN = 32.768 kHz. The values will be affected directly by changes in VREF, but the effects due to changes in the XIN frequency will be minor.

## 5 V DIGITAL CHARACTERISTICS ($T_A$ = 25° C; VA+, VD+ = 5 V ±5%; GND = 0; See Notes 2 and 18.))

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High-level Input Voltage | All Pins Except XIN and SCLK | $V_{IH}$ | 0.6 VD+ | - | - | V |
| | XIN | | (VD+)-0.5 | - | - | V |
| | SCLK | | (VD+) - 0.45 | - | - | V |
| Low-level Input Voltage | All Pins Except XIN and SCLK | $V_{IL}$ | - | - | 0.8 | V |
| | XIN | | - | - | 1.5 | V |
| | SCLK | | - | - | 0.6 | V |
| High-level Output Voltage | | $V_{OH}$ | | | | |
| | All Pins Except CPD and SDO (Note 19) | | (VA+) - 1.0 | - | - | V |
| | CPD, $I_{out}$ = -4.0 mA | | (VD+) - 1.0 | - | - | V |
| | SDO, $I_{out}$ = -5.0 mA | | (VD+) - 1.0 | - | - | V |
| Low-level Output Voltage | | $V_{OL}$ | | | | |
| | All Pins Except CPD and SDO, $I_{out}$ = 1.6 mA | | - | - | 0.4 | V |
| | CPD, $I_{out}$ = 2 mA | | - | - | 0.4 | V |
| | SDO, $I_{out}$ = 5.0 mA | | - | - | 0.4 | V |
| Input Leakage Current | | $I_{in}$ | - | ±1 | ±10 | µA |
| 3-state Leakage Current | | $I_{OZ}$ | - | - | ±10 | µA |
| Digital Output Pin Capacitance | | $C_{out}$ | - | 9 | - | pF |

Notes: 18. All measurements performed under static conditions.

19. $I_{out}$ = -100 µA unless stated otherwise. ($V_{OH}$ = 2.4 V @ $I_{out}$ = -40 µA.)

## 3 V DIGITAL CHARACTERISTICS ($T_A$ = 25° C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10%; GND = 0; See Notes 2 and 18.)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High-level Input Voltage | All Pins Except XIN and SCLK | $V_{IH}$ | 0.6 VD+ | - | - | V |
| | XIN | | (VD+)-0.5 | - | - | V |
| | SCLK | | (VD+) - 0.45 | - | - | V |
| Low-level Input Voltage | All Pins Except XIN and SCLK | $V_{IL}$ | - | - | 0.16 VD+ | V |
| | XIN | | - | - | 0.3 | V |
| | SCLK | | - | - | 0.6 | V |
| High-level Output Voltage | | $V_{OH}$ | | | | |
| | All Pins Except CPD and SDO, $I_{out}$ = -400 µA | | (VA+) - 0.3 | - | - | V |
| | CPD, $I_{out}$ = -4.0 mA | | (VD+) - 1.0 | - | - | V |
| | SDO, $I_{out}$ = -5.0 mA | | (VD+) - 1.0 | - | - | V |
| Low-level Output Voltage | | $V_{OL}$ | | | | |
| | All Pins Except CPD and SDO, $I_{out}$ = 400 µA | | - | - | 0.3 | V |
| | CPD, $I_{out}$ = 2 mA | | - | - | 0.4 | V |
| | SDO, $I_{out}$ = 5.0 mA | | - | - | 0.4 | V |
| Input Leakage Current | | $I_{in}$ | - | ±1 | ±10 | µA |
| 3-state Leakage Current | | $I_{OZ}$ | - | - | ±10 | µA |
| Digital Output Pin Capacitance | | $C_{out}$ | - | 9 | - | pF |

## DYNAMIC CHARACTERISTICS

| Parameter | Symbol | Ratio | Unit |
|---|---|---|---|
| Modulator Sampling Frequency | $f_s$ | XIN/4 | Hz |
| Filter Settling Time to 1/2 LSB (Full-scale Step) | $t_s$ | $1/f_{out}$ | s |

## RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V; See Note 20.)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC Power Supplies | Positive Digital | VD+ | 2.7 | 5.0 | 5.25 | V |
| | Positive Analog | VA+ | 4.75 | 5.0 | 5.25 | V |
| Analog Reference Voltage | (VREF+) - (VREF-) | $VRef_{diff}$ | 1.0 | 2.5 | VA+ | V |
| Negative Bias Voltage | | NBV | -1.8 | -2.1 | -2.5 | V |

Notes: 20. All voltages with respect to ground.

## ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V; See Note 20.)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC Power Supplies | (Note 21) | | | | | |
| | Positive Digital | VD+ | -0.3 | - | +6.0 | V |
| | Positive Analog | VA+ | -0.3 | - | +6.0 | V |
| Negative Bias Voltage | Negative Potential | NBV | +0.3 | -2.1 | -3.0 | V |
| Input Current, Any Pin Except Supplies | (Note 22 and 23) | $I_{IN}$ | - | - | ±10 | mA |
| Output Current | | $I_{OUT}$ | - | - | ±25 | mA |
| Power Dissipation | (Note 24) | PDN | - | - | 500 | mW |
| Analog Input Voltage | VREF pins | $V_{INR}$ | NBV -0.3 | - | (VA+) + 0.3 | V |
| | AIN Pins | $V_{INA}$ | NBV -0.3 | - | (VA+) + 0.3 | V |
| Digital Input Voltage | | $V_{IND}$ | -0.3 | - | (VD+) + 0.3 | V |
| Ambient Operating Temperature | | $T_A$ | -40 | - | 85 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | - | 150 | °C |

Notes: 21. No pin should go more negative than NBV - 0.3 V.

22. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

23. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

24. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

## SWITCHING CHARACTERISTICS ($T_A$ = 25° C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10% or 5 V ±5%; Levels: Logic 0 = 0 V, Logic 1 = VD+; $C_L$ = 50 pF.))

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Master Clock Frequency (Note 25) | XIN | | | | |
| External Clock or Internal Oscillator (CS5522/24/28) | | 30 | 32.768 | 200 | kHz |
| (CS5521/23) | | 30 | 32.768 | 130 | kHz |
| Master Clock Duty Cycle | | 40 | - | 60 | % |
| Rise Times (Note 26) | $t_{rise}$ | | | | |
| Any Digital Input Except SCLK | | - | - | 1.0 | µs |
| SCLK | | - | - | 100 | µs |
| Any Digital Output | | - | 50 | - | ns |
| Fall Times (Note 26) | $t_{fall}$ | | | | |
| Any Digital Input Except SCLK | | - | - | 1.0 | µs |
| SCLK | | - | - | 100 | µs |
| Any Digital Output | | - | 50 | - | ns |
| ***Start-up*** | | | | | |
| Oscillator Start-up Time XTAL = 32.768 kHz (Note 27) | $t_{ost}$ | - | 500 | - | ms |
| ***Serial Port Timing*** | | | | | |
| Serial Clock Frequency | SCLK | 0 | - | 2 | MHz |
| SCLK Falling to $\overline{CS}$ Falling for continuous running SCLK (Note 28) | $t_0$ | 100 | - | - | ns |
| Serial Clock Pulse Width High | $t_1$ | 250 | - | - | ns |
| Pulse Width Low | $t_2$ | 250 | - | - | ns |
| ***SDI Write Timing*** | | | | | |
| $\overline{CS}$ Enable to Valid Latch Clock | $t_3$ | 50 | - | - | ns |
| Data Set-up Time prior to SCLK rising | $t_4$ | 50 | - | - | ns |
| Data Hold Time After SCLK Rising | $t_5$ | 100 | - | - | ns |
| SCLK Falling Prior to $\overline{CS}$ Disable | $t_6$ | 100 | - | - | ns |
| ***SDO Read Timing*** | | | | | |
| $\overline{CS}$ to Data Valid | $t_7$ | - | - | 150 | ns |
| SCLK Falling to New Data Bit | $t_8$ | - | - | 150 | ns |
| $\overline{CS}$ Rising to SDO Hi-Z | $t_9$ | - | - | 150 | ns |

Notes: 25. Device parameters are specified with a 32.768 kHz clock; however, clocks up to 200 kHz (CS5522/24/28) or 130 kHz (CS5521/23) can be used for increased throughput.

26. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

27. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

28. Applicable when SCLK is continuously running.

Specifications are subject to change without notice.

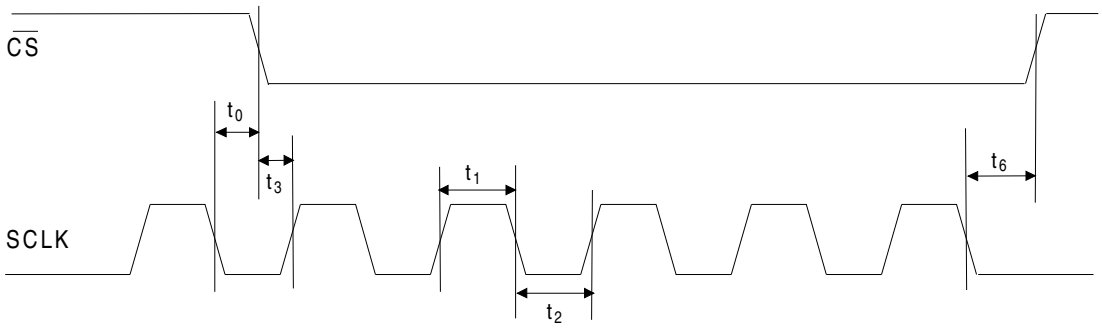



**Figure 1. Continuous Running SCLK Timing (Not to Scale)**

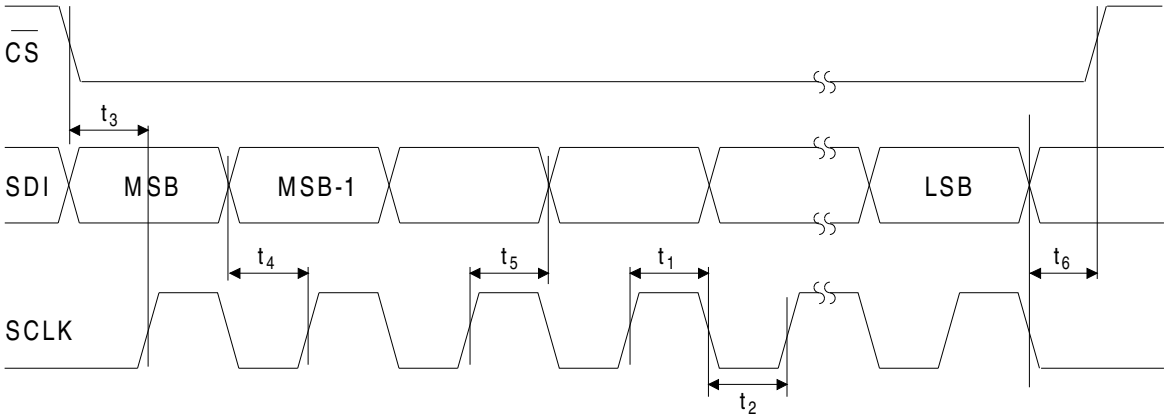



**Figure 2. SDI Write Timing (Not to Scale)**

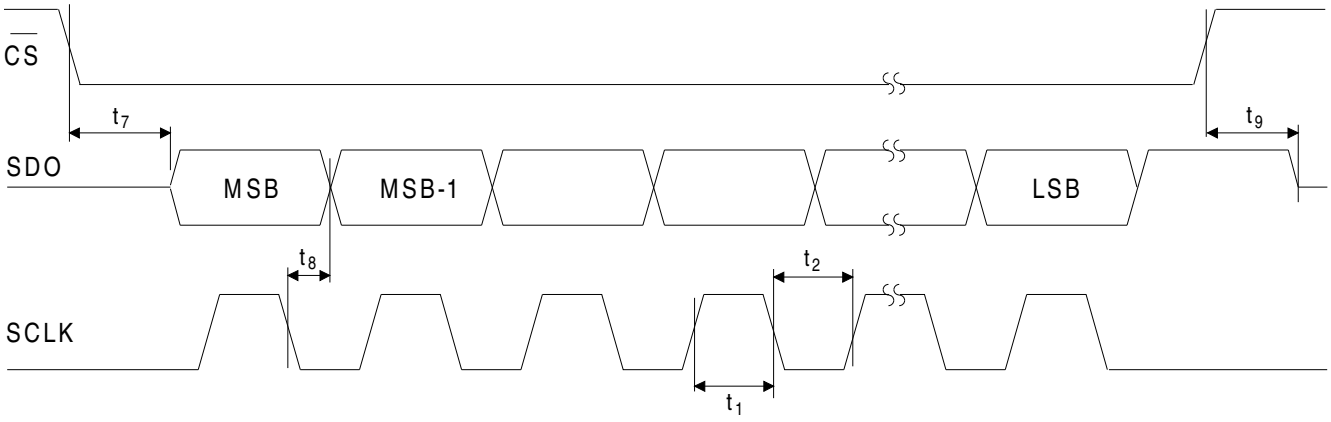



**Figure 3. SDO Read Timing (Not to Scale)**

# 1. GENERAL DESCRIPTION

The CS5521/22/23/24/28 are highly integrated ΔΣ Analog-to-Digital Converters (ADCs) which use charge-balance techniques to achieve 16-bit (CS5521/23) and 24-bit (CS5522/24/28) performance. The ADCs come as either two-channel (CS5521/22), four-channel (CS5523/24), or eight-channel (CS5528) devices, and include a low input current, chopper-stabilized instrumentation amplifier. To permit selectable input spans of 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, and 5 V, the ADCs include a PGA (programmable gain amplifier). To accommodate ground-based thermocouple applications, the devices include a CPD (Charge Pump Drive) which provides a negative bias voltage to the on-chip amplifiers.

These devices also include a fourth order DS modulator followed by a digital filter which provides eight selectable output word rates of 1.88 Sps, 3.76 Sps, 7.51 Sps, 15 Sps, 30 Sps, 61.6 Sps, 84.5 Sps, and 101.1 Sps (XIN = 32.768 kHz). The devices are capable of producing output update rates up to 617 Sps when a 200 kHz clock is used (CS5522/24/28) or up to 401 Sps using a 130 kHz clock (CS5521/23). Further note that the digital filters are designed to settle to full accuracy within one conversion cycle and simultaneously reject both 50 Hz and 60 Hz interference when operated at word rates below 30 Sps (assuming a XIN clock frequency of 32.768 kHz).

To ease communication between the ADCs and a micro-controller, the converters include an easy to use three-wire serial interface which is SPI™ and Microwire™ compatible.

## 1.1 Analog Input

Figure 4 illustrates a block diagram of the analog input signal path inside the CS5521/22/23/24/28. The front end consists of a multiplexer (break before make configuration), a chopper-stabilized instrumentation amplifier with fixed gain of 20X, coarse/fine charge buffers, and a programmable gain section. For the 25 mV, 55 mV, and 100 mV input ranges, the input signals are amplified by the 20X instrumentation amplifier. For the 1 V, 2.5 V, and 5 V input ranges, the instrumentation amplifier is bypassed and the input signals are connected to the Programmable Gain block via coarse/fine charge buffers.

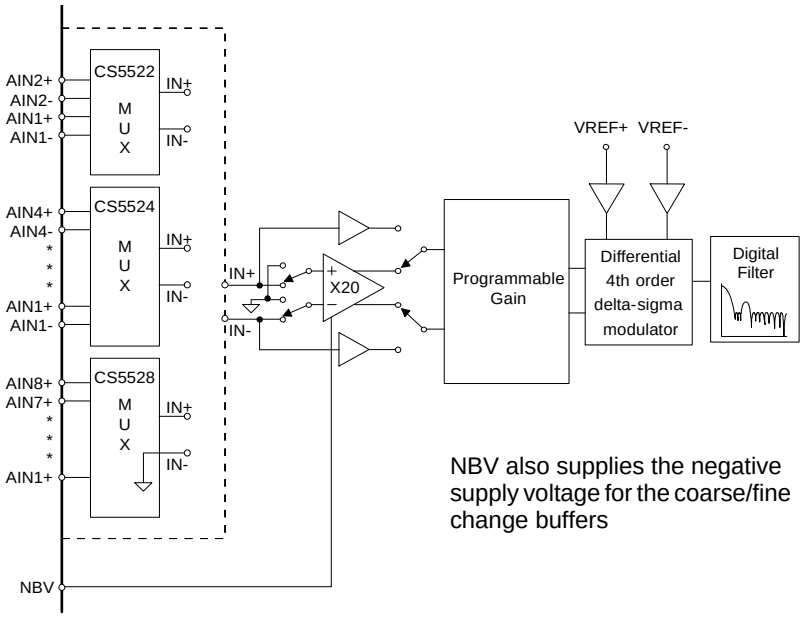



**Figure 4. Multiplexer Configurations**

### 1.1.1 Instrumentation Amplifier

The instrumentation amplifier is chopper stabilized and is activated any time conversions are performed with the low-level input ranges, ≤100 mV. The amplifier is powered from VA+ and from the NBV (Negative Bias Voltage) pin allowing the CS5521/22/23/24/28 to be operated in either of two analog input configurations. The NBV pin can be biased to a negative voltage between -1.8 V and -2.5 V, or tied to AGND (for the CS5528, NBV has to be between -1.8 V and -2.5 V for the ranges below 100 mV when the amplifier is engaged). The common-mode-plus-signal range of the instrumentation amplifier is 1.85 V to 2.65 V with NBV grounded. The common-mode-plus-signal range of the instrumentation amplifier is -0.150 V to 0.950 V with NBV between -1.8 V to -2.5 V. Whether NBV is tied between -1.8 V and -2.5 V or tied to AGND, the (Common Mode + Signal) input on AIN+ and AIN- must stay between NBV and VA+.

Figure 5 illustrates an analog input model for the ADCs when the instrumentation amplifier is engaged. The CVF (sampling) input current for each of the analog input pins depends on the CFS1 and CFS0 (Chop Frequency Select) bits in the configuration register (see *Configuration Register* for details). Note that the CVF current is lowest with the CFS bits in their default states (cleared to logic 0s). Further note that the CVF current into the instrumentation amplifier is less than 300 pA over -40°C to +85°C. Note that Figure 5 is for input current modeling only. For physical input capacitance see 'Input Capacitance' specification under *ANALOG CHARACTERISTICS*. Also refer to Applications Note AN30 - *"Switched-Capacitor A/D Converter Input Structures"* for more details on input models and input sampling currents.

***Note:*** *Residual noise appears in the converter's baseband for output word rates greater than 61.6 Sps if the CFS bits are logic 0 (chop clock = 256 Hz). For word rates of 30 Sps and lower, 256 Sps chopping is recommended, and for 61.6 Sps, 84.5 Sps and 101.1 Sps word rate settings, 4096 Hz chopping is recommended.*

### 1.1.2 Coarse/Fine Charge Buffers

The unity gain buffers are activated any time conversions are performed with the high-level inputs ranges, 1 V, 2.5 V, and 5 V. The unity gain buffers are designed to accommodate rail-to-rail input signals. The common-mode-plus-signal range for the unity gain buffer amplifier is NBV to VA+.

Typical CVF (sampling) current for the unity gain buffer amplifiers is about 10 nA (XIN = 32.768 kHz, see Figure 6).

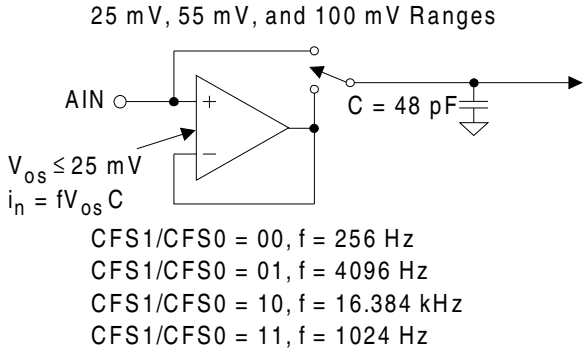



**Figure 5. Input Models for AIN+ and AIN- pins, ≤100 mV Input Ranges**

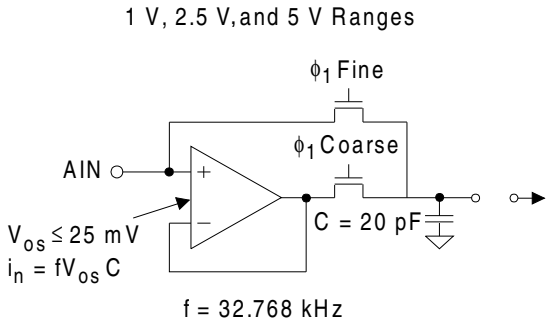



**Figure 6. Input Models for AIN+ and AIN- pins, >100 mV input ranges**

### *1.1.3 Analog Input Span Considerations*

The CS5521/22/23/24/28 is designed to measure full-scale ranges of 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, and 5 V. Other full scale values can be accommodated by performing a system calibration within the limits specified. See the *Calibration* section for more details. Another way to change the full scale range is to increase or to decrease the voltage reference to a voltage other than 2.5 . See the *Voltage Reference* section for more details.

Three factors set the operating limits for the input span. They include: instrumentation amplifier saturation, modulator 1's density, and a lower reference voltage. When the 25 mV, 55 mV, or 100 mV range is selected, the input signal (including the common-mode voltage and the amplifier offset voltage) must not cause the 20X amplifier to saturate in either its input stage or output stage. To prevent saturation, the absolute voltages on AIN+ and AIN- must stay within the limits specified (refer to the *Analog Input* section). Additionally, the differential output voltage of the amplifier must not exceed 2.8 V. The equation

$$ABS(VIN + VOS) \times 20 = 2.8\ V$$

defines the differential output limit, where

$$VIN = (AIN+) - (AIN-)$$

is the differential input voltage and VOS is the absolute maximum offset voltage for the instrumentation amplifier (VOS will not exceed 40 mV). If the differential output voltage from the amplifier exceeds 2.8 V, the amplifier may saturate, which will cause a measurement error.

The input voltage into the modulator must not cause the modulator to exceed a low of 20 percent or a high of 80 percent 1's density. The nominal full-scale input span of the modulator (from 30 percent to 70 percent 1's density) is determined by the VREF voltage divided by the Gain Factor. See Table 1 to determine if the CS5521/22/23/24/28 is being used properly. For example, in the 55 mV range, to determine the nominal input voltage to the modulator, divide VREF (2.5 V) by the Gain Factor (2.2727).

When a smaller voltage reference is used, the resulting code widths are smaller causing the converter output codes to exhibit more changing codes for a fixed amount of noise. Table 1 is based upon a VREF = 2.5 V. For other values of VREF, the values in Table 1 must be scaled accordingly.

### *1.1.4 Measuring Voltages Higher than 5 V*

Some systems require the measurement of voltages greater than 5 V. The input current of the instru-

| Input Range(1) | Max. Differential Output 20X Amplifier | VREF | Gain Factor | Δ-Σ Nominal(1) Differential Input | Δ-Σ(1) Max. Input |
|---|---|---|---|---|---|
| ± 25 mV | 2.8 V (2) | 2.5V | 5 | ± 0.5 V | ± 0.75 V |
| ± 55 mV | 2.8 V (2) | 2.5V | 2.272727... | ± 1.1 V | ± 1.65 V |
| ± 100 mV | 2.8 V (2) | 2.5V | 1.25 | ± 2.0 V | ± 3.0 V |
| ± 1.0 V | - | 2.5V | 2.5 | ± 1.0 V | ± 1.5 V |
| ± 2.5 V | - | 2.5V | 1.0 | ± 2.5 V | ± 5.0 V |
| ± 5.0 V | - | 2.5V | 0.5 | ± 5.0 V | 0V, VA+ |

**Table 1. Relationship between Full Scale Input, Gain Factors, and Internal Analog Signal Limitations**

Note: 1. The converter's actual input range, the delta-sigma's nominal full-scale input, and the delta-sigma's maximum full-scale input all scale directly with the value of the voltage reference. The values in the table assume a 2.5 V VREF voltage.
2. The 2.8 V limit at the output of the 20X amplifier is the differential output voltage.

mentation amplifier with a gain range setting of 100 mV or less, is typically 100 pA. This is low enough to permit large external resistors to divide down a large external signal without significant loading. Figure 7 illustrates an example circuit. Refer to Application Note 158 for more details on high-voltage (>5 V) measurement.

### *1.1.5 Voltage Reference*

The CS5521/22/23/24/28 devices are specified for operation with a 2.5 V reference voltage between the VREF+ and VREF- pins of the device. For a single-ended reference voltage, such as the LT1019-2.5, the reference voltage is input into the VREF+ pin of the converter and the VREF- pin is grounded.

The differential voltage between the VREF+ and VREF- can be any voltage from 1.0 V up to VA+, however, the VREF+ cannot go above VA+ and the VREF- pin can not go below NBV.

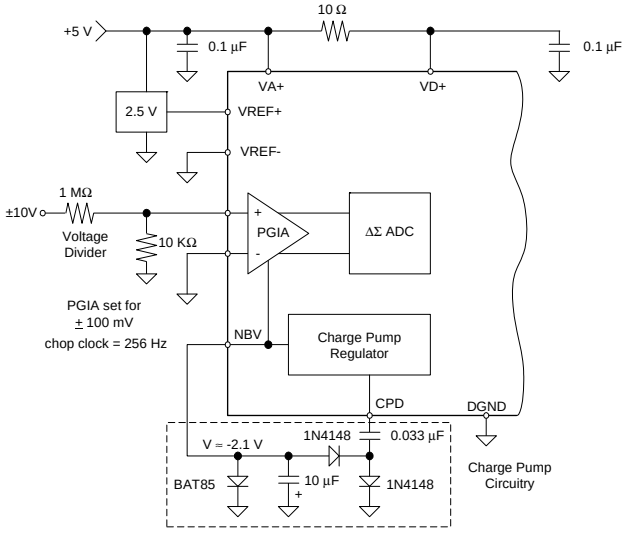



**Figure 7. Input Ranges Greater than 5 V**

Figure 8 illustrates the input models for the VREF pins. The dynamic input current for each of the pins can be determined from the models shown.

## 1.2 Overview of ADC Register Structure and Operating Modes

The CS5521/22/23/24/28 ADCs have an on-chip controller, which includes a number of user-accessible registers. The registers are used to hold offset and gain calibration results, configure the chip's operating modes, hold conversion instructions, and to store conversion data words. Figure 9 depicts a block diagram of the on-chip controller's internal registers for the CS5523/24.

Each of the converters has 24-bit registers to function as offset and gain calibration registers for each channel. The converters with two channels have two offset and two gain calibration registers, the converters with four channels have four offset and four gain calibration registers, and the eight channel converter has eight offset and eight gain calibration registers. These registers hold calibration results. The contents of these registers can be read or written by the user. This allows calibration data to be off-loaded into an external EEPROM. The user can also manipulate the contents of these registers to modify the offset or the gain slope of the converter.

The converters include a 24-bit configuration register of which 17 of the bits are used for setting options such as the conversion mode, operating power options, setting the chop clock rate of the instru-

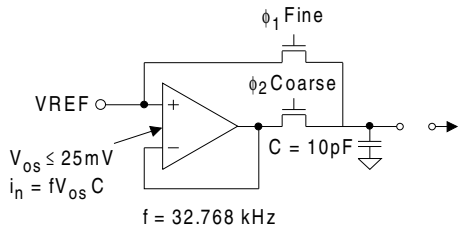



**Figure 8. Input Model for VREF+ and VREF- Pins**

mentation amplifier, and providing a number of flags which indicate converter operation.

A group of registers, called Channel Set-up Registers, are also included in the converters. These registers are used to hold pre-loaded conversion instructions. Each channel set-up register is 24 bits wide and holds two 12-bit conversion instructions (Setups). Upon power-up, these registers can be initialized by the user's microcontroller with conversion instructions. The user can then use bits in the configuration register to choose a conversion mode.

Several conversion modes are possible. Using the single conversion mode, an 8-bit command word can be written into the serial port. The command includes pointer bits which 'point' to a 12-bit command in one of the Channel Setup Registers which is to be executed. The 12-bit commands can be setup to perform a conversion on any of the input channels of the converter. More than one of the 12-bit Setups can be used for the same analog input channel. This allows the user to convert on the same signal with either a different conversion speed, a different gain range, or any of the other options available in the Setup Register. The user can set up the registers to perform conversions using different conversion options on each of the input channels.

The ADCs also include multiple-channel conversion capability. User bits in the configuration register of the ADCs can be configured to sequence through the 12-bit command Setups, performing a conversion according to the content of each 12-bit Setup. This channel scanning capability can be configured to run continuously, or to scan through a specified number of Setup Registers and stop until commanded to continue. In the multiple-channel scanning modes, the conversion data words are loaded into an on-chip data FIFO. The converter issues a flag on the SDO pin when a scan cycle is completed so the user can read the FIFO. More details are given in the following pages.

Instructions are provided on how to initialize the converter, perform offset and gain calibrations, and to configure the converter for the various conversion modes. Each of the bits of the configuration register and of the Channel Setup Registers is described. A list of examples follows the description section. Table 2 can be used to decode all valid commands (the first 8 bits into the serial port).

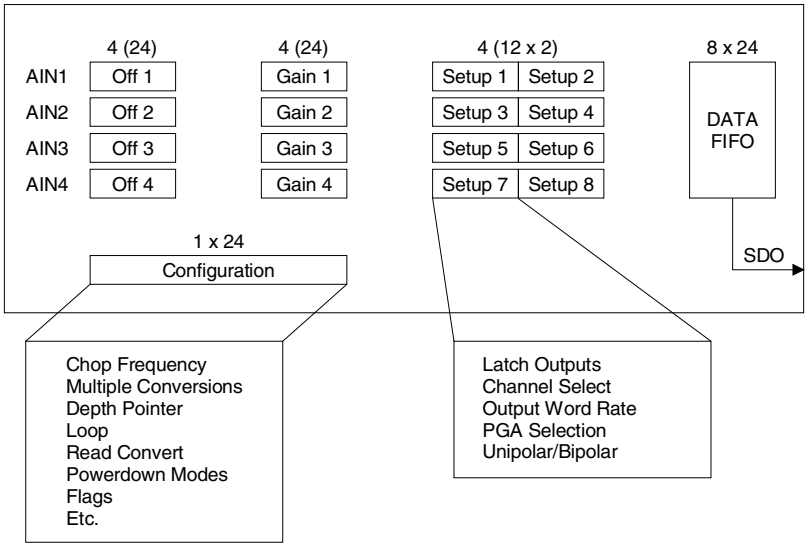



**Figure 9. CS5523/24 Register Diagram**

### *1.2.1 System Initialization*

After power is first applied to the CS5521/22/2324/28 devices, the user should wait for the oscillator to start before attempting to communicate with the converter. If a 32.768 kHz crystal is used, this may be 500 milliseconds.

The initialization sequence should be as follows: Initialize the serial port by sending the port initialization sequence of 15 bytes of all 1's followed by one byte with the following bit contents '1111 110'. This sequence places the chip in the command mode where it waits for a valid command to be written. The first command should be to perform a system reset. This is accomplished by writing a logic 1 to the RS (Reset System) bit in the configuration register. After a reset the RV bit is set until the configuration register is read. The user must then write a logic 0 to the RS bit to take the part out of reset mode. Any other bits written to the configuration register at this time will be lost. The configuration register must be written again once RS= 0 to set any other bits to their desired settings.

After a reset, the on-chip registers are initialized to the following states:

| | |
|---|---|
| configuration register: | 000040(H) |
| offset registers: | 000000(H) |
| gain registers: | 400000(H) |
| channel setup registers: | 000000(H) |

### *1.2.2 Command Register Quick Reference*

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| CB | CS2 | CS1 | CS0 | R/$\overline{W}$ | RSB2 | RSB1 | RSB0 |

| BIT | NAME | VALUE | FUNCTION |
|---|---|---|---|
| D7 | Command Bit, CB | 0<br>1 | Must be logic 0 for these commands.<br>See table below. |
| D6-D4 | Channel Select Bits, CSB2-CSB0 | 000<br>.<br>.<br>111 | CS2-CS0 provide the address of one of the eight physical channels. These bits are used to access the calibration registers associated with respective channels.<br>Note: These bits are ignored when reading the data register. |
| D3 | Read/$\overline{Write}$, R/$\overline{W}$ | 0<br>1 | Write to selected register.<br>Read from selected register. |
| D2-D0 | Register Select Bit, RSB2-RSB0 | 000<br>001<br>010<br>011<br>101<br><br><br><br>110<br>111 | Reserved<br>Offset Register<br>Gain Register<br>Configuration Register<br>Channel Set-up Registers<br>- register is 48-bits long for CS5521/22<br>- register is 96-bits long for CS5523/24<br>- register is 192-bits long for CS5528<br>Reserved<br>Reserved |

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| CB | CSRP3 | CSRP2 | CSRP1 | CSRP0 | CC2 | CC1 | CC0 |

| BIT | NAME | VALUE | FUNCTION |
|---|---|---|---|
| D7 | Command Bit, CB | 0<br>1 | See table above.<br>Must be logic 1 for these commands. |
| D6-D3 | Channel Pointer Bits, CSRP3-CSRP0 | 0000<br>.<br>.<br>.<br>1111 | These bits are used as pointers to the Setups.<br>Note: The MC bit, must be logic 0 for these bits to take effect. When MC = 1, these bits are ignored. The LP, MC, and RC bits in the configuration register are ignored during calibration. |
| D2-D0 | Conversion/Calibration Bits, CC2-CC0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | Normal Conversion<br>Self-Offset Calibration<br>Self-Gain Calibration<br>Reserved<br>Reserved<br>System-Offset Calibration<br>System-Gain Calibration<br>Reserved |

**Table 2. Command Register Quick Reference**

### *1.2.3 Command Register Descriptions*

**READ/$\overline{\text{WRITE}}$ INDIVIDUAL OFFSET CALIBRATION REGISTER**

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | CS2 | CS1 | CS0 | R/$\overline{\text{W}}$ | 0 | 0 | 1 |

*Function*: *These commands are used to access each offset register separately. CS1 - CS0 decode the registers accessed.*

*R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)*

0 Write to selected register.

1 Read from selected register.

*CS[2:0] (Channel Select Bits)*

000 Offset Register 1(All devices)

001 Offset Register 2 (All devices)

010 Offset Register 3 (CS5523/24/28 only)

011 Offset Register 4 (CS5523/24/28 only)

100 Offset Register 5 (CS5528 only)

101 Offset Register 6 (CS5528 only)

110 Offset Register 7 (CS5528 only)

111 Offset Register 8 (CS5528 only)

**READ/$\overline{\text{WRITE}}$ INDIVIDUAL GAIN REGISTER**

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | CS2 | CS1 | CS0 | R/$\overline{\text{W}}$ | 0 | 1 | 0 |

*Function*: *These commands are used to access each gain register separately. CS1 - CS0 decode the registers accessed.*

*R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)*

0 Write to selected register.

1 Read from selected register.

*CS[2:0] (Channel Select Bits)*

000 Gain Register 1(All devices)

001 Gain Register 2 (All devices)

010 Gain Register 3 (CS5523/24/28 only)

011 Gain Register 4 (CS5523/24/28 only)

100 Gain Register 5 (CS5528 only)

101 Gain Register 6 (CS5528 only)

110 Gain Register 7 (CS5528 only)

111 Gain Register 8 (CS5528 only)

### READ/$\overline{\text{WRITE}}$ CONFIGURATION REGISTER

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | R/$\overline{W}$ | 0 | 1 | 1 |

*Function:* *These commands are used to read from or write to the configuration register.*

*R/$\overline{W}$ (Read/$\overline{Write}$)*

0 Write to selected register.

1 Read from selected register.

### READ/$\overline{\text{WRITE}}$ CHANNEL-SETUP REGISTER(S)

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | R/$\overline{W}$ | 1 | 0 | 1 |

*Function*: *These commands are used to access the channel-setup registers (CSRs). The number of CSRs accessed is determined by the device being used and the number of CSRs that are being accessed (i.e. the depth bits in the configuration register determine the number of levels accessed). This register is 48-bits long (4 Setups) for the CS5521/22, 96-bits long (8 Setups) for the CS5523/24, and 192-bits (16 Setups) long for the CS5528.*

*R/$\overline{W}$ (Read/$\overline{Write}$)*

0 Write to selected register.

1 Read from selected register.

### PERFORM CONVERSION

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 1 | CSRP3 | CSRP2 | CSRP1 | CSRP0 | 0 | 0 | 0 |

*Function:* *These commands instruct the ADC to perform conversions on the physical input channel pointed to by the pointer bits (CSRP2 - CSRP0) in the channel-setup registers. The particular type of conversion performed is determined by the states of the conversion control bits (the multiple conversion bit, the loop bit, read convert bit, and the depth pointer bits) in the configuration register.*

*CSRP [3:0] (Channel Setup Register Pointer Bits)*

| | |
|---|---|
| 0000 | Setup 1 (All devices) |
| 0001 | Setup 2 (All devices) |
| 0010 | Setup 3 (All devices) |
| 0011 | Setup 4 (All devices) |
| 0100 | Setup 5 (CS5523/24/28) |
| 0101 | Setup 6 (CS5523/24/28) |
| 0110 | Setup 7 (CS5523/24/28) |
| 0111 | Setup 8 (CS5523/24/28) |
| 1000 | Setup 9 (CS5528 only) |
| 1001 | Setup 10 (CS5528 only) |
| 1010 | Setup 11 (CS5528 only) |
| 1011 | Setup 12 (CS5528 only) |
| 1100 | Setup 13 (CS5528 only) |
| 1101 | Setup 14 (CS5528 only) |
| 1110 | Setup 15 (CS5528 only) |
| 1111 | Setup 16 (CS5528 only) |

### PERFORM CALIBRATION

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 1 | CSRP3 | CSRP2 | CSRP1 | CSRP0 | CC2 | CC1 | CC0 |

*Function:* *These commands instruct the ADC to perform a calibration on the physical input channel referenced which is chosen by the command byte pointer bits (CSRP3 - CRSP0).*

*CSRP [3:0] (Channel Setup Register Pointer Bits)*

0000 Setup 1 (All devices)
0001 Setup 2 (All devices)
0010 Setup 3 (All devices)
0011 Setup 4 (All devices)
0100 Setup 5 (CS5523/24/28 only)
0101 Setup 6 (CS5523/24/28 only)
0110 Setup 7 (CS5523/24/28 only)
0111 Setup 8 (CS5523/24/28 only)
1000 Setup 9 (CS5528 only)
1001 Setup 10 (CS5528 only)
1010 Setup 11 (CS5528 only)
1011 Setup 12 (CS5528 only)
1100 Setup 13 (CS5528 only)
1101 Setup 14 (CS5528 only)
1110 Setup 15 (CS5528 only)
1111 Setup 16 (CS5528 only)

*CC [2:0] (Calibration Control Bits)*

000 Reserved
001 Self-Offset Calibration
010 Self-Gain Calibration
011 Reserved
100 Reserved
101 System-Offset Calibration
110 System-Gain Calibration
111 Reserved

**SYNC1**

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

*Function:* *Part of the serial port re-initialization sequence.*

**SYNC0**

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

*Function:* *End of the serial port re-initialization sequence.*

**NULL**

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*Function:* *This command is used to clear a port flag and keep the converter in the continuous conversion mode.*

### *1.2.4 Serial Port Interface*

The CS5521/22/23/24/28's serial interface consists of four control lines: $\overline{CS}$, SCLK, SDI, SDO. Figure 10 illustrates the serial sequence necessary to write to, or read from the serial port's registers.

$\overline{CS}$ (Chip Select) is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied low, the port can function as a three-wire interface.

SDI (Serial Data In) is the data signal used to transfer data to the converters.

SDO (Serial Data Out) is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK (Serial Clock) is the serial bit clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

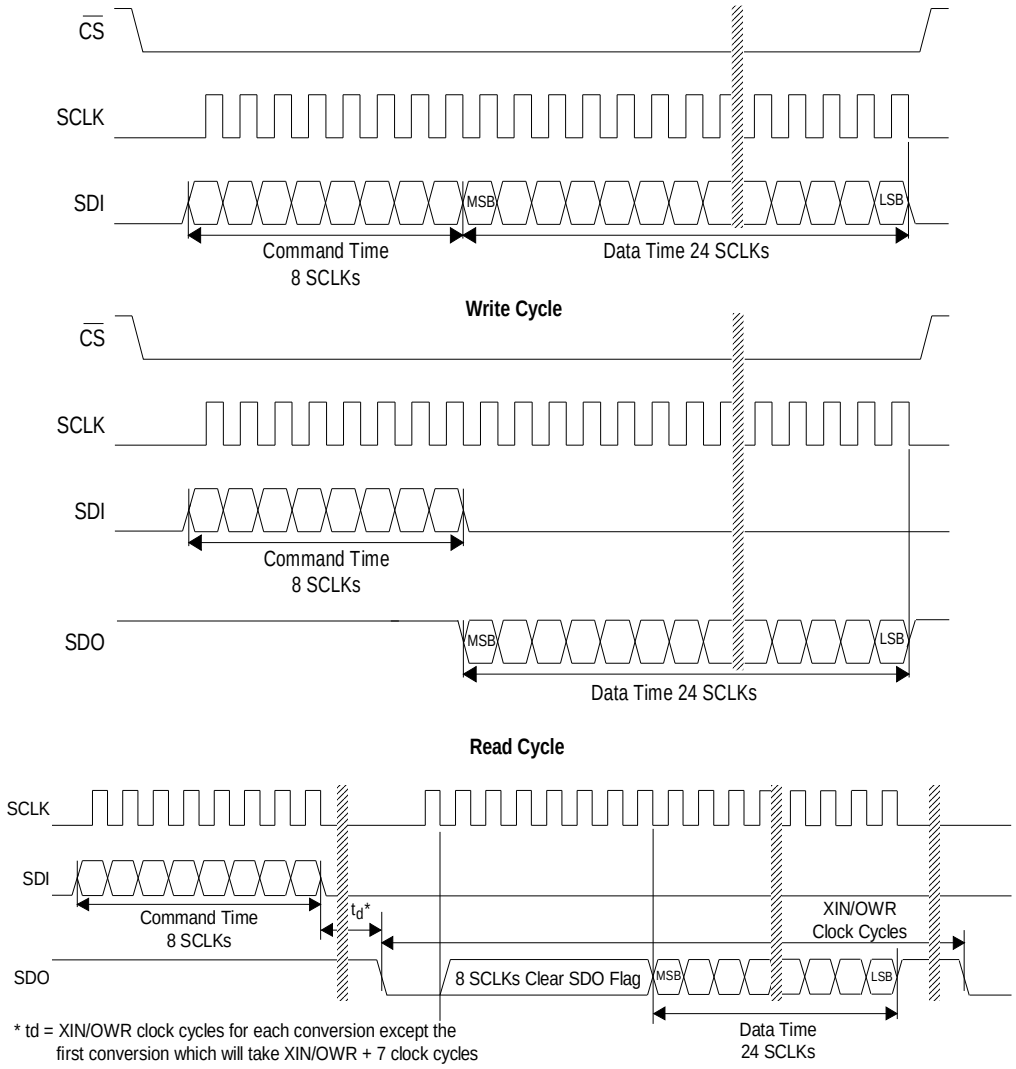



**Figure 10. Command and Data Word Timing**

### *1.2.5 Reading/Writing the Offset, Gain, and Configuration Registers*

The CS5521/22/23/24/28's offset, gain, and configuration registers are accessed individually and can be read from or written to. To write to an offset, a gain, or the configuration register, the user must transmit the appropriate write command which accesses the particular register and then follow that command with 24 bits of data (refer to Figure 10 for details). For example, to write 0x800000 (hexadecimal) to physical channel one's gain register, the user would transmit the command byte 0x02 (hexadecimal) and then follow that command byte with the data 0x800000 (hexadecimal). Similarly, to read physical channel one's gain register, the user must first transmit the command byte 0x0A (hexadecimal) and then read the 24 bits of data. Once an offset, a gain, or the configuration register is written to or read from, the serial port returns to the command mode.

### *1.2.6 Reading/Writing the Channel-Setup Registers*

The CS5521/22 have two 24-bit channel-setup registers (CSRs). The CS5523/24 have four CSRs, and the CS5528 has eight CSRs (refer to Table 3 for more detail on the CSRs). These registers are accessed in conjunction with the depth pointer bits in the configuration register. Each CSR contains two 12-bit Setups which are programmed by the user to contain data conversion or calibration information such as:

1) state of the output latch pins
2) output word rate
3) gain range
4) polarity
5) the address of a physical input channel to be converted.

Once programmed, they are used to determine the mode (e.g. unipolar, 15 Sps, 100 mV range etc.) the ADC will operate in when future conversions or calibrations are performed.

To access the CSRs, the user must first initialize the depth pointer bits in the configuration register as these bits determine the number of CSRs to read from or write to. For example, to write CSR1 (Setup1 and Setup2), the user would first program the configuration register's depth pointer bits with '0001' binary. This notifies the ADC's serial port that only the first CSR is to be accessed. Then, the user would transmit the write command, 0x05 (hexadecimal) and follow that command with 24 bits of data. Similarly, to read CSR1, the user must transmit the command byte 0x0D (hexadecimal) and then read the 24 bits of data. To write more than one CSR, for instance CSR1 and CSR2 (Setup1, Setup2, Setup3, and Setup4), the user would first set the depth pointer bits in the configuration register to '0011' binary. The user would then transmit the write CSR command 0x05 (hexadecimal) and follow that with the information for Setup1, Setup2, Setup 3, and Setup 4 which is 48 bits of information. Note that while reading/writing CSRs, two Setups are accessed in pairs as a single 24-bit CSR register. Even if one of the Setups isn't used, it must be written to or read. Further note that the CSRs are accessed as a closed array – the user can not access CSR2 without accessing CSR1. This requirement means that the depth bits in the configuration register can only be set to one of the following states when the CSRs are being read from or written to: 0001, 0011, 0101, 0111, 1001, 1011, 1101, 1111. Examples detailing the power of the CSRs are provided in the *Performing Conversions and Reading the Data Conversion FIFO* section. Once the CSRs are written to or read from, the serial port returns to the command mode.

**CSR** (Channel-Setup Register)

| | | |
|---|---|---|
| #1 | Setup 1<br>Bits <47:36> | Setup 2<br>Bits <35:24> |
| #2 | Setup 3<br>Bits <23:12> | Setup 4<br>Bits <11:0> |

CS5521/22

**CSR**

| | | |
|---|---|---|
| #1 | Setup 1<br>Bits <95:84> | Setup 2<br>Bits <83:72> |
| #4 | Setup 7<br>Bits <23:12> | Setup 8<br>Bits <11:0> |

CS5523/24

**CSR**

| | | |
|---|---|---|
| #1 | Setup 1<br>Bits <191:180> | Setup 2<br>Bits <179:168> |
| #8 | Setup 15<br>Bits <23:12> | Setup 16<br>Bits <11:0> |

CS5528

| D23(MSB) | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | A0 | CS2 | CS1 | CS0 | WR2 | WR1 | WR0 | G2 | G1 | G0 | U/B |

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | A0 | CS2 | CS1 | CS0 | WR2 | WR1 | WR0 | G2 | G1 | G0 | $\overline{U/B}$ |

| BIT | NAME | VALUE | | FUNCTION |
|---|---|---|---|---|
| D23-D22/<br>D11-D10 | Latch Outputs, A1-A0 | 00 | *R | Latch Output Pins A1-A0 mimic D23/D11-D22/D10 register bits. |
| D21-D19/<br>D9-D7 | Channel Select, CS2-CS0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | R | Select physical channel 1 (All devices)<br>Select physical channel 2(All devices)<br>Select physical channel 3 (CS5523/24/28 only)<br>Select physical channel 4 (CS5523/24/28 only)<br>Select physical channel 5 (CS5528 only)<br>Select physical channel 6 (CS5528 only)<br>Select physical channel 7 (CS5528 only)<br>Select physical channel 8 (CS5528 only) |
| D18-D16/<br>D6-D4 | Word Rate, WR2-WR0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | R | 15.0 Sps (2180 XIN cycles).<br>30.0 Sps (1092 XIN cycles).<br>61.6 Sps (532 XIN cycles).<br>84.5 Sps (388 XIN cycles).<br>101.1 Sps (324 XIN cycles).<br>1.88 Sps (17444 XIN cycles).<br>3.76 Sps (8724 XIN cycles).<br>7.51 Sps (4364 XIN cycles). |
| D15-D13/<br>D3-D1 | Gain Bits, G2-G0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | R | 100 mV (assumes VREF Differential = 2.5 V)<br>55 mV<br>25 mV<br>1.0 V<br>5.0 V<br>2.5 V<br>Not used.<br>Not used. |
| D12/D0 | Unipolar/Bipolar, $U/\overline{B}$ | 0<br>1 | R | Bipolar measurement mode.<br>Unipolar measurement mode. |

* R indicates the bit value after the part is reset

**Table 3. Channel-Setup Registers**

#### *1.2.6.1 Latch Outputs*

The A1-A0 pins mimic the latch output, D23/D11-D22/D10, bits of the channel-setup registers. A1-A0 can be used to control external multiplexers and other logic functions outside the converter. The outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 20 µA to reduce self-heating of the chip. These outputs are powered from VA+, hence their output voltage for a logic 1 will be limited to the VA+ supply voltage.

#### *1.2.6.2 Channel Select Bits*

The channel select, CS1-CS0, bits are used to determine which physical input channel will be used when a conversion is performed with a particular Setup.

#### *1.2.6.3 Output Word Rate Selection*

The word rate, WR2-WR0, bits of the channel-setup registers set the output conversion word rate of the converter when a conversion is performed with a particular Setup. The word rates indicated in Table 3 assume a master clock of 32.768 kHz, and scale linearly when using other master clock frequencies. Upon reset the converter is set to operate with an output word rate of 15.0 Sps.

#### *1.2.6.4 Gain Bits*

The gain bits, G2-G0, of the channel-setup registers set the full-scale differential input range for the ADC when a conversion is performed with a particular Setup. The input ranges in the table assume a 2.5 V reference voltage, and scale linearly when using other reference voltages.

#### *1.2.6.5 Unipolar/Bipolar Bit*

The unipolar/bipolar bit is used to determine the type of conversion, unipolar or bipolar, that will be performed with a particular Setup.

### *1.2.7 Configuration Register*

The configuration register is 24 bits long. The following subsections detail the bits in the configuration register. Table 4 summarizes the configuration register.

#### *1.2.7.1 Chop Frequency Select*

The chop frequency select (CFS1-CFS0) bits are used to set the rate at which the instrumentation amplifier's chop switches modulate the input signal. The 256 Hz rate is desirable as it provides the lowest input CVF (sampling) current, <300 pA over -40 to 85 °C. The higher rates can be used to eliminate modulation/aliasing effects as the frequency of the input signal increases.

#### *1.2.7.2 Conversion/Calibration Control Bits*

The conversion/calibration control bits in the configuration register are used to control the particular type of conversion required for the users applications. In short, the depth pointer (DP3-DP0) bits determine the number of Setups that will be referenced when conversions are performed. The multiple conversion (MC) bit instructs the converter to perform conversions on the number of Setups in the channel-setup registers which are referenced by the depth pointer bits. The converter begins with Setup1 and moves sequentially through the Setups in this mode. The Loop (LP) bit instructs the converter to continuously perform conversions until a Stop command is sent to the converter. The read convert (RC) bit instructs the converter to wait until the conversion data is read before performing the next conversion or set of conversions.

#### *1.2.7.3 Power Consumption Control Bits*

The CS5522/24/28 devices provide three power consumption modes: normal, low power, and sleep. The CS5521/23 provide two power consumption modes: normal, and sleep. The normal (default) mode is entered after a power-on reset. In normal mode, the CS5522/24/28 typically con-

sume 9.0 mW. The CS5521/23 typically consume 6.0 mW. The low-power mode is an alternate mode in the CS5522/24/28 that reduces the consumed power to 5.5 mW. It is entered by setting bit D8 (the low-power mode bit) in the configuration register to logic 1. Slightly degraded noise or linearity performance should be expected in the low-power mode. Note that the XIN clock should not exceed 130 kHz in low-power mode. The final two modes accommodated in all devices are referred to as the power save modes. They power down most of the analog portion of the chip and stop filter convolutions. The power-save modes are entered whenever the PS/$\overline{R}$ bit of the configuration register is set to logic 1. The particular power-save mode entered depends on state of bit D11 (PSS, the Power Save Select bit) in the configuration register. If PSS is logic 0, the converters enters the standby mode reducing the power consumption to 1.2 mW. If the PSS bit (bit D11) is set to logic zero, the PD bit (bit D10) must be set to one. The standby mode leaves the oscillator and the on-chip bias generator running. This allows the converter to quickly return to the normal or low-power mode once the PS/$\overline{R}$ bit is set back to a logic 0. If PSS and PS/$\overline{R}$ in the configuration register are set to logic 1, the sleep mode is entered reducing the consumed power to around 500 µW. Since the sleep mode disables the oscillator, a 500 ms oscillator start-up delay period is required before returning to the normal or low-power mode.

### *1.2.7.4 Charge Pump Disable*

The pump disable (PD) bit permits the user to turn off the charge pump drive thus enabling the user to reduce the radiation of digital interference from the CPD pin when the charge pump is not being used.

### *1.2.7.5 Reset System Control Bits*

The reset system (RS) bit permits the user to perform a system reset. A system reset can be initiated at any time by writing a logic 1 to the RS bit in the configuration register. After a system reset cycle is complete, the reset valid (RV) bit is set indicating that the internal logic was properly reset. The RV remains set until the configuration register is read. Note that the user must write a logic 0 to the RS bit to take the part out of the reset mode. No other bits in the configuration register can be written at this time. A subsequent write to the configuration register is necessary to write to any other bits in this register. Once reset, the on-chip registers are initialized to the following states.

| | |
|---|---|
| configuration register: | 000040(H) |
| offset registers: | 000000(H) |
| gain registers: | 400000(H) |
| channel setup registers: | 000000(H) |

### *1.2.7.6 Data Conversion Error Flags*

The oscillation detect (OD) and overflow (OF) bits in the configuration register are flag bits used to indicate that the ADC performed a conversion on an input signal that was not within the conversion range of the ADC. For convenience, the OD and OF bits are also in the data conversion word of the CS5521/23.

The OF bit is set to logic 1 when the input signal is:

1) more positive than full scale
2) more negative than zero in unipolar mode, or
3) more negative than negative full scale in bipolar mode.

The OF flag is cleared to logic 0 when a conversion occurs which is not out of range.

The OD bit is set to logic 1 any time that an oscillatory condition is detected in the modulator. This does not occur under normal operating conditions, but may occur when the input is extremely overranged. The OD flag will be cleared to logic 0 when the modulator becomes stable.

| D23(MSB) | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| NU | NU | CFS1 | CFS0 | NU | MC | LP | RC | DP3 | DP2 | DP1 | DP0 |

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PSS | PD | PS/$\overline{R}$ | LPM | RS | RV | OD | OF | NU | NU | NU | NU |

| BIT | NAME | VALUE | | FUNCTION |
|---|---|---|---|---|
| D23-D22 | Not Used, NU | 00 | R[1] | Must always be logic 0. |
| D21-D20 | Chop Frequency Select, CFS1-CFS0 | 00<br>01<br>10<br>11 | R | 256 Hz Amplifier chop frequency. (XIN = 32.768 kHz)<br>4,096 Hz Amplifier chop frequency.<br>16,384 Hz Amplifier chop frequency.<br>1,024 Hz Amplifier chop frequency. |
| D19 | Not Used, NU | 0 | R | Must always be logic 0. |
| D18 | Multiple Conversion, MC | 0<br>1 | R | Perform single-Setup conversions. MC bit is ignored during calibrations.<br>Perform multiple-Setup conversions on Setups in the channel-setup register by issuing only one command with MSB = 1. |
| D17 | Loop, LP | 0<br>1 | R | The conversions on the single Setup (MC = 0) or multiple Setups (MC = 1) are performed only once.<br>The conversions on the single Setup (MC = 0) or multiple Setups (MC = 1) are continuously performed. |
| D16 | Read Convert, RC | 0<br>1 | R | Don't wait for user to finish reading data before starting new conversions. The RC bit is used in conjunction with the LP bit when the LP bit is set to logic 1. If LP = 0, the RC bit is ignored. If LP = 1, the ADC waits for user to read data conversion(s) before converting again. The RC bit is ignored during calibrations. Refer to Calibration Protocol for details. |
| D15-D12 | Depth Pointer, DP3-DP0 | 0000<br>.<br>.<br>1111 | R | When writing or reading the CSRs, these bits (DP3-DP0) determine the number of CSR's to be accessed (0000=1). They are also used to determine how many Setups are converted when MC=1 and a command byte with its MSB = 1 is issued. Note that the CS5522 has two CSRS, the CS5524 has four CSRs, and the CS5528 has 8 CSRs. |
| D11 | Power Save Select, PSS | 0[2]<br>1 | R | Standby Mode (Oscillator active, allows quick power-up).<br>Sleep Mode (Oscillator inactive). |
| D10 | Pump Disable, PD | 0<br>1 | R | Charge Pump Enabled.<br>For PD = 1, the CPD pin goes to a Hi-Z output state. |
| D9 | Power Save/$\overline{Run}$, PS/$\overline{R}$ | 0<br>1 | R | Run.<br>Power Save. |
| D8 | Low Power Mode, LPM | 0<br>1 | R | Normal Mode (LPM bit is only for the CS5522/24/28)<br>Reduced Power Mode |
| D7 | Reset System, RS | 0<br>1 | R | Normal Operation.<br>Activate a Reset cycle. To return to Normal Operation write bit to zero. |
| D6 | Reset Valid, RV | 0<br>1 | <br>R | No reset has occurred or bit has been cleared (read only).<br>Bit is set after a Valid Reset has occurred. (Cleared when read.) |
| D5 | Oscillation Detect, OD | 0<br>1 | R | Bit is clear when an oscillation condition has not occurred (read only).<br>Bit is set when an oscillatory condition is detected in the modulator. |
| D4 | Overrange Flag, OF | 0<br>1 | R | Bit is clear when an overrange condition has not occurred (read only).<br>Bit is set when input signal is more positive than the positive full scale, more negative than zero (unipolar mode), or when the input is more negative than the negative full scale (bipolar mode). |
| D3-D0 | Not Used, NU | 0000 | R | Must always be logic 0. |

1.R indicates the bit value after the part is reset.
2.When the chip is placed in standby mode, the PD bit (bit D10) should be set to 1.

**Table 4. Configuration Register**

## 1.3 Calibration

The CS5521/22/23/24/28 offer four different calibration functions including self calibration and system calibration. However, after the devices are reset, the converter is functional and can perform measurements without being calibrated. In this case, the converter will utilize the initialized values of the on-chip registers (Gain = 1.0, Offset = 0.0) to calculate output words for the ±100 mV range. Any initial offset and gain errors in the internal circuitry of the chip will remain.

The gain and offset registers, which are used for both self and system calibration, are used to set the zero and full-scale points of the converter's transfer function. One LSB in the offset register is $2^{-24}$ proportion of the input span when the gain register is set to 1.0 decimal (bipolar span is 2 times the unipolar span). The MSB in the offset register determines if the offset to be trimmed is positive or negative (0 positive, 1 negative). The converter can typically trim ±50 percent of the input span. The gain register spans from 0 to $(4 - 2^{-22})$. The decimal equivalent meaning of the gain register is:

$$D = b_{MSB}2^{1} + (b_0 2^{0} + b_1 2^{-1} + \ldots + b_N 2^{-N}) = b_{MSB}2^{1} + \sum_{i=0}^{N} b_i 2^{-i}$$

where the binary numbers have a value of either zero or one ($b_0$ corresponds to bit MSB-1, N=22). Refer to Table 5 for details.

The offset and gain calibration steps each take one conversion cycle to complete. At the end of the calibration step, SDO falls to indicate that the calibration has finished.

### *1.3.1 Self Calibration*

The CS5521/22/23/24/28 offer both self-offset and self-gain calibrations. For self calibration of offset in the 25 mV, 55 mV, and 100 mv ranges, the converters internally tie the inputs of the instrumentation amplifier together and route them to the AIN- pin as shown in Figure 11 (in the CS5528 they are routed to AGND). For proper self-calibration of

**Offset Register**

| | MSB | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***Register*** | Sign | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-19}$ | $2^{-20}$ | $2^{-21}$ | $2^{-22}$ | $2^{-23}$ | $2^{-24}$ |
| Reset (R) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

One LSB represents $2^{-24}$ proportion of the input span when gain register is set to 1.0 decimal (bipolar span is 2 times unipolar span)
Offset and data word bits align by MSB (bit MSB-4 of offset register changes bit MSB-4 of data)

**Gain Register**

| | MSB | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***Register*** | $2^{1}$ | $2^{0}$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-17}$ | $2^{-18}$ | $2^{-19}$ | $2^{-20}$ | $2^{-21}$ | $2^{-22}$ |
| Reset (R) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The gain register span is from 0 to $(4\text{-}2^{-22})$. After Reset the (MSB-1) bit is 1, all other bits are 0.

**Table 5. Offset and Gain Registers**

offset to occur in the 25 mV, 55 mV, and 100 mV ranges, the AIN- pin must be at the proper common-mode voltage as specified in 'Common Mode +Signal AIN+/-' specification in the *Analog Input* section (if AIN- = 0 V, NBV must be between -1.8 V to -2.5 V). For self calibration of offset in the 1.0 V, 2.5 V, and 5 V ranges, the inputs of the modulator are connected together and then routed to the VREF- pin as shown in Figure 12.

For self calibration of gain, the differential inputs of the modulator are connected to VREF+ and VREF- as shown in Figure 13. For any input range other than the 2.5 V range, the converter's gain error can not be completely calibrated out when using self calibration. This is due to the lack of an accurate full-scale voltage internal to the chips. The 2.5 V range is an exception because the external reference voltage is 2.5 V nominal and is used as the full-scale voltage. In addition, when self calibration of gain is performed in the 25 mV, 55 mV, and 100 mV input ranges, the instrumentation amplifier's gain is not calibrated. These two factors can leave the converters with a gain error of up to ±20% after self calibration of gain. Therefore, a system gain calibration is required to get better accuracy, except for the 2.5 V range.

### *1.3.2 System Calibration*

For the system calibration functions, the user must supply the calibration signals to the converter which represent ground and full scale. When a system offset calibration is performed, a ground-referenced signal must be applied to the converters. See Figures 14 and 15.

As shown in Figures 16 and 17, the user must input a signal representing the positive full-scale point to

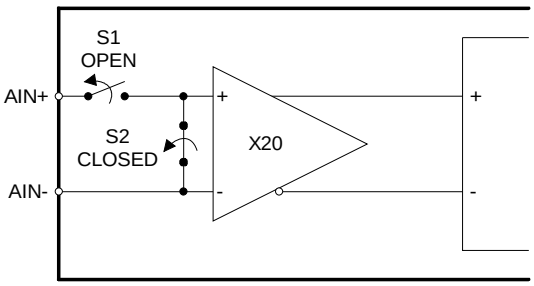



**Figure 11. Self Calibration of Offset (Low Ranges)**

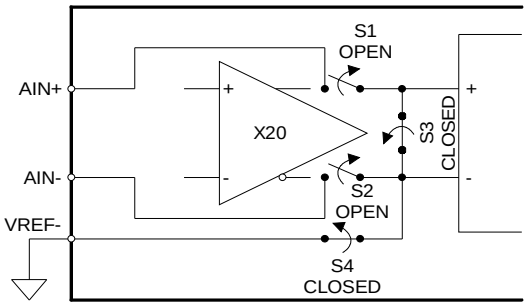



**Figure 12. Self Calibration of Offset (High Ranges)**

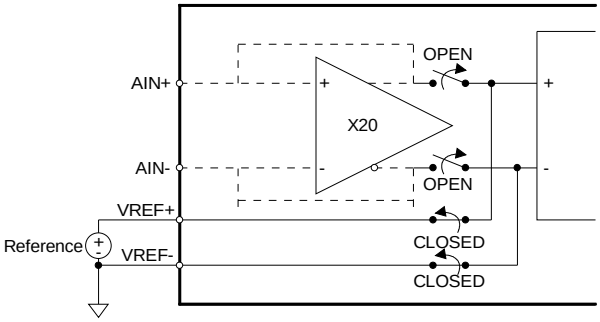



**Figure 13. Self Calibration of Gain (All Ranges)**

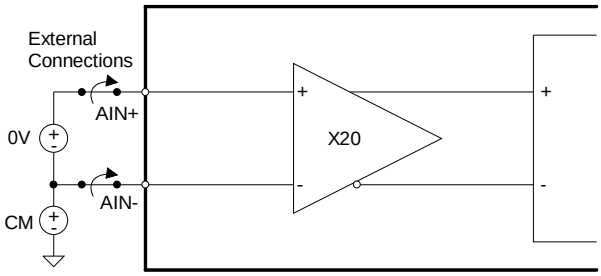



**Figure 14. System Calibration of Offset (Low Ranges)**

perform a system gain calibration. In either case, the calibration signals must be within the specified calibration limits for each specific calibration step (refer to the 'System Calibration Specifications' in *ANALOG CHARACTERISTICS*). If a system gain calibration is performed the following conditions must be met:

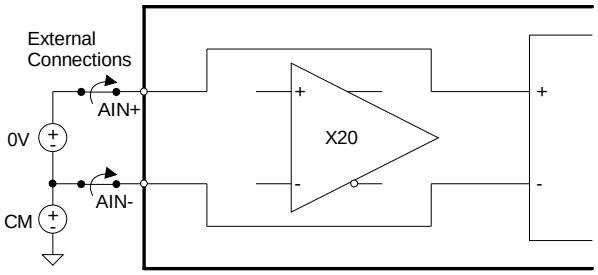



**Figure 15. System Calibration of Offset (High Ranges)**

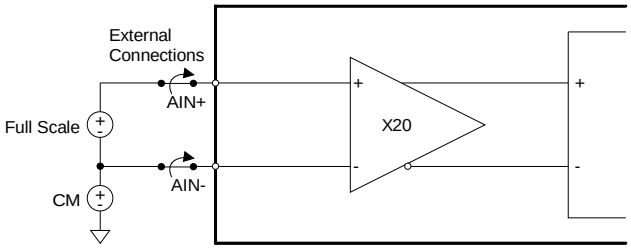



**Figure 16. System Calibration of Gain (Low Ranges)**

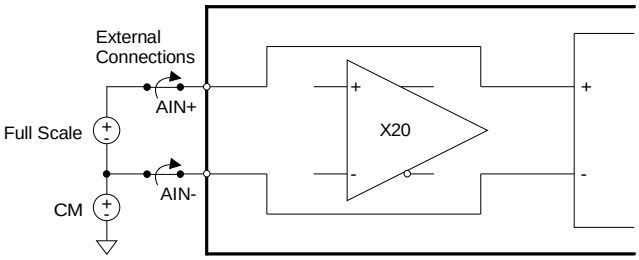



**Figure 17. System Calibration of Gain (High Ranges)**

1) Full-scale input must not saturate the 20X instrumentation amplifier, if the calibration is on an input range where the instrumentation amplifier is involved.

2) The 1's density of the modulator must not be greater than 80 percent (the input to the ΔΣ modulator must not exceed the maximum input which Table 1 specifies).

3) The input must not be so small, relative to the range chosen, that the resulting gain register's content, decoded in decimal, exceeds 3.9999998 (see the discussion of operating limits on input span under the *Analog Input* and *Limitations in Calibration Range* sections). This requires the full-scale input voltage to the modulator to be at least 25 percent of the nominal value.

The converter's input ranges were chosen to guarantee gain calibration accuracy to 1 $LSB_{16}$ or 16 $LSB_{24}$ when system gain calibration is performed. This is useful when a user wants to manually scale the full-scale range of the converter and maintain accuracy. For example, if a gain calibration is performed with a 2.5 V full-scale voltage and a 1.25 V input range is desired, the user can read the contents of the gain register, shift the register contents left by 1 bit, and then write the result back to the gain register. This multiplies the gain by 2.

Assuming a system can provide two known voltages, the following equations allow the user to manually compute the calibration register's values based on two uncalibrated conversions (see note). The offset and gain calibration registers are used to adjust a typical conversion as follows:

$$Rc = (Ru + Co) * Cg / 2^{22}.$$

Calibration can be performed using the following equations:

$$Co = (Rc0/G - Ru0)$$

$$Cg = 2^{22} * G$$

$$\text{where } G = (Rc1 - Rc0)/(Ru1-Ru0).$$

***Note:*** *Uncalibrated conversions imply that the gain and offset registers are at default {gain register = 0x400000 (Hex) and offset register = 0x000000 (Hex)}.*

The variables are defined below.

| | | |
|---|---|---|
| V0 | = | First calibration voltage |
| V1 | = | Second calibration voltage (greater than V0) |
| Ru | = | Result of any uncalibrated conversion |
| Ru0 | = | Result of uncalibrated conversion V0 (24-bit integer or 2's complement) |
| Ru1 | = | Result of uncalibrated conversion of V1 (24-bit integer or 2's complement) |
| Rc | = | Result of any conversion |
| Rc0 | = | Desired calibrated result of converting V0 (24-bit integer or 2's complement) |
| Rc1 | = | Desired calibrated result of converting V1 (24-bit integer or 2's complement) |
| Co | = | Offset calibration register value (24-bit 2's complement) |
| Cg | = | Gain calibration register value (24-bit integer) |

### *1.3.3 Calibration Tips*

Calibration steps are performed at the output word rate selected by the WR2-WR0 bits of the configuration register. Since higher word rates result in conversion words with more peak-to-peak noise, calibration should be performed at lower output word rates. Also, to minimize digital noise near the device, the user should wait for each calibration step to be completed before reading or writing to the serial port.

For maximum accuracy, calibrations should be performed for offset and gain (selected by changing the G2-G0 bits of the desired Setup). Note that only one gain range can be calibrated per physical channel. If factory calibration of the user's system is performed using the system calibration capabilities of the CS5521/22/23/24/28, the offset and gain register contents can be read by the system microcontroller and recorded in EEPROM. These same calibration words can then be uploaded into the offset and gain registers of the converter when power is first applied to the system, or when the gain range is changed.

### *1.3.4 Limitations in Calibration Range*

System calibration can be limited by signal headroom in the analog signal path inside the chip as discussed under the *Analog Input* section of this data sheet. For gain calibration the full-scale input signal can be reduced to the point in which the gain register reaches its upper limit of ($4\text{-}2^{-22}$ decimal) or FFFFFF (hexadecimal). Under nominal conditions, this occurs with a full-scale input signal equal to about 1/4 the nominal full scale. With the converter's intrinsic gain error, this full-scale input signal may be higher or lower. In defining the minimum Full Scale Calibration Range (FSCR) under *ANALOG CHARACTERISTICS*, margin is retained to accommodate the intrinsic gain error. Alternatively the input full-scale signal can be increased to a point in which the modulator reaches its 1's density limit of 80 percent, which under nominal condition occurs when the full-scale input signal is 1.5 times the nominal full scale. With the chip's intrinsic gain error, this full-scale input signal may be higher or lower. In defining the maximum FSCR, margin is again incorporated to accommodate the intrinsic gain error. In addition, for full-scale inputs greater than the nominal full-scale value of the range selected, there is some voltage at which various internal circuits may saturate due to limited amplifier headroom. This is most likely to occur in the 100 mV range.

## 1.4 Performing Conversions and Reading the Data Conversion FIFO

The CS5521/22/23/24/28 offers various modes of performing conversions. The sections that follow detail the differences between the conversion modes. The sections also provide examples illustrating how to use the conversion modes with the channel-setup registers and to acquire conversions for further processing. While reading, note that the CS5521/22 have a FIFO which is four words deep. The CS5523/24 have a FIFO which is eight words deep and the CS5528 has a FIFO which is sixteen

conversion words deep. Further note that the type of conversion(s) performed and the way to access the resulting data from the FIFO is determined by the MC (multiple conversion), the LP (loop), the RC (read convert), and the DP (depth pointer) bits in the configuration register.

### *1.4.1 Conversion Protocol*

The CS552x offer six different conversion modes, which can be categorized into two main types of conversions: one-Setup conversions, which reference only one Setup, and multiple-Setup conversions, which reference any number of Setups. The converter can be instructed to perform single conversions or repeated conversions (with or without wait) in either of these modes, using the MC, LP, and RC bits in the Configuration Register. The MC bit controls whether the part will do one-Setup or multiple-Setup conversions. The LP bit controls whether the part will perform a single or repeated conversion set. When doing repeated conversion sets, the RC bit controls whether or not the converter will wait for the data from the current conversion set to be read before beginning the next conversion set. The sections that follow further detail the various conversion modes.

#### *1.4.1.1 Single, One-Setup Conversion*

(LP = 0 MC = 0 RC = X)

In this conversion mode, the ADC will perform a single conversion, referencing only one Setup, and return to command mode after the data word has been fully read. The 8-bit command word contains the CSRP bits, which instruct the converter which Setup to use when performing the conversion.

To perform a single, one-Setup conversion, the MC and LP bits in the Configuration Register must be set to '0'. Then, the 8-bit command word that references the desired Setup must be sent to the converter. The ADC will then perform a single conversion on the referenced Setup, and SDO will fall to indicate that the conversion is complete. Thirty-two SCLKs are then needed to read the conversion word from the data register. The first 8 SCLKs are used to clear the SDO flag. During the last 24 SCLKs, the data word will be output from the converter on the SDO line. The part returns to command mode immediately after the data word has been read, where it waits for the next command to be issued.

#### *1.4.1.2 Repeated One-Setup Conversions without Wait*

(LP = 1 MC = 0 RC = 0)

In this conversion mode, the ADC will repeatedly perform conversions, referencing only one Setup. The 8-bit command word contains the CSRP bits, which instruct the converter which Setup to use when performing the conversion. Note that in this mode, the part will continually perform conversions, and the user need not read every conversion as it becomes available. Although conversions can be read whenever they are needed, they must be read within one conversion cycle (defined by the referenced Setup), as the data word will be overwritten when new conversion data becomes available. The SDO line rises and falls to indicate the availability of new conversion data. When new data is available, the current conversion data will be lost, or in the case that the user has only read a part of the conversion word, the remainder of the conversion word will be corrupted.

To perform repeated, one-Setup conversions with no wait, the MC bit must be set to '0', the LP bit must be set to '1', and the RC bit must be set to '0' in the Configuration Register. Then, the 8-bit command word that references the desired Setup must be sent to the converter. The ADC will then begin performing conversions on the referenced Setup, and SDO will fall to indicate when a conversion is complete, and data is available. Thirty-two SCLKs are then needed to read the conversion word from the data register. The first 8 SCLKs are used to clear the SDO flag. During the last 24 SCLKs, the data word will be output from the converter on the

SDO line. If, during the first 8 SCLKs, "00000000" is provided on SDI, the converter will remain in this conversion mode, and continue to perform conversions on the selected Setup. To exit this conversion mode, "11111111" must be provided on SDI during the first 8 SCLKs. If the user decides to exit, 24 more SCLKs are required to read the final conversion word from the data register and return to command mode.

#### *1.4.1.3 Repeated One-Setup Conversions with Wait*

(LP = 1 MC = 0 RC = 1)

In this conversion mode, the ADC will repeatedly perform conversions, referencing only one Setup. The 8-bit command word contains the CSRP bits, which instruct the converter which Setup to use when performing the conversion. Note that in this mode, every conversion word must be read. The part will wait for the current conversion word to be read before performing the next conversion.

To perform repeated, one-Setup conversions with wait, the MC bit must be set to '0', the LP bit must be set to '1', and the RC bit must be set to '1' in the Configuration Register. Then, the 8-bit command word that references the desired Setup must be sent to the converter. The ADC will then begin performing conversions on the referenced Setup, and SDO will fall to indicate when a conversion is complete, and data is available. Thirty-two SCLKs are then needed to read the conversion word from the data register. The first 8 SCLKs are used to clear the SDO flag. During the last 24 SCLKs, the data word will be output from the converter on the SDO line. If, during the first 8 SCLKs, "00000000" is provided on SDI, the converter will remain in this conversion mode, and continue to perform conversions on the selected Setup after each data word is read. To exit this conversion mode, "1111 1111" must be provided on SDI during the first 8 SCLKs. If the user decides to exit, 24 more SCLKs are required to read the final conversion word from the data register and return to command mode.

#### *1.4.1.4 Single, Multiple-Setup Conversions*

(LP = 0 MC = 1 RC = X)

In this conversion mode, the ADC will perform single conversions, referencing multiple Setups, and return to command mode after the data for all conversions have been read. The CSRP bits in the command word are ignored in this mode. Instead, the Depth Pointer (DP3-DP0) bits in the Configuration Register are accessed to determine the number of Setups to reference when collecting the data. The number of Setups referenced will be equal to (DP3-DP0) + 1, and will be accessed in order, beginning with Setup1.

To perform single, multiple-Setup conversions, the MC bit must be set to '1', and the LP bit must be set to '0' in the Configuration Register. Then, the 8-bit command word to start a conversion must be sent to the converter. Because the CSRP bits of the command word are ignored in this mode, a "start convert" command referencing any of the available Setups will begin the conversions. The ADC will then perform conversions using the appropriate number of Setups (as dictated by the DP bits in the Configuration Register), beginning with Setup1. The SDO line will fall after the final conversion to indicate that the data is ready. Eight SCLKs, plus 24 SCLKs for each Setup referenced are required to read the conversion words from the data FIFO. The first 8 SCLKs are used to clear the SDO flag. Every 24 bits thereafter consist of the data words of each Setup that was referenced, until all of the data has been read from the part. The data word from Setup1 is output first, followed by the data word from Setup2, and so on for the appropriate number of Setups. The part returns to command mode immediately after the final data word has been read, and waits for the next command to be issued.

#### *1.4.1.5 Repeated Multiple-Setup Conversions without Wait*

(LP = 1 MC = 1 RC = 0)

In this conversion mode, the ADC will repeatedly perform conversions, referencing multiple Setups. The CSRP bits in the command word are ignored in this mode. Instead, the Depth Pointer (DP3-DP0) bits in the Configuration Register are accessed to determine the number of Setups to reference when collecting the data. The number of Setups referenced will be equal to (DP3-DP0) + 1, and will be accessed in order, beginning with Setup1. Note that in this mode, the part will continually perform conversions, looping back to Setup1 when finished with each set, and the user need not read every conversion set as it becomes available. The SDO line rises and falls to indicate the availability of new conversion data sets. When new data is available, the current conversion data set will be lost, or in the case that the user has only read a part of the conversion set, the remainder of the conversion set will be corrupted.

To perform repeated, multiple-Setup conversions with no wait, the MC bit must be set to '1', the LP bit must be set to '1', and the RC bit must be set to '0' in the Configuration Register. Then, the 8-bit command word to start a conversion must be sent to the converter. Because the CSRP bits of the command word are ignored in this mode, a "start convert" command referencing any of the available Setups will begin the conversions. The ADC will then perform conversions using the appropriate number of Setups (as dictated by the DP bits in the Configuration Register), beginning with Setup1. The SDO line will fall after the final conversion to indicate that the data is ready. Eight SCLKs, plus 24 SCLKs for each Setup referenced are required to read the conversion words from the data FIFO. The first 8 SCLKs are used to clear the SDO flag. Every 24 bits thereafter consist of the data words of each Setup that was referenced, until all of the data has been read from the part. If, during the first 8 SCLKs, "00000000" is provided on SDI, the converter will remain in this conversion mode, and continue to perform conversions on the desired number of Setups. To exit this conversion mode, "1111 1111" must be provided on SDI during the first 8 SCLKs. If the user decides to exit, 24 more SCLKs for each referenced Setup are required to read the final conversion data set from the FIFO and return to command mode.

#### *1.4.1.6 Repeated Multiple-Setup Conversions with Wait*

(LP = 1 MC = 1 RC = 1)

In this conversion mode, the ADC will repeatedly perform conversions, referencing multiple Setups. The CSRP bits in the command word are ignored in this mode. Instead, the Depth Pointer (DP3-DP0) bits in the Configuration Register are accessed to determine the number of Setups to reference when collecting the data. The number of Setups referenced will be equal to (DP3-DP0) + 1, and will be accessed in order, beginning with Setup1. Note that in this mode, every conversion data set must be read. The part will wait for the current conversion data set to be read before performing the next set of conversions.

To perform repeated, multiple-Setup conversions with wait, the MC bit must be set to '1', the LP bit must be set to '1', and the RC bit must be set to '1' in the Configuration Register. Then, the 8-bit command word to start a conversion must be sent to the converter. Because the CSRP bits of the command word are ignored in this mode, a "start convert" command referencing any of the available Setups will begin the conversions. The ADC will then perform conversions using the appropriate number of Setups (as dictated by the DP bits in the Configuration Register), beginning with Setup1. The SDO line will fall after the final conversion to indicate that the data is ready. Eight SCLKs, plus 24

SCLKs for each Setup referenced are required to read the conversion words from the data FIFO. The first 8 SCLKs are used to clear the SDO flag. Every 24 bits thereafter consist of the data words of each Setup that was referenced, until all of the data has been read from the part. If, during the first 8 SCLKs, "0000 0000" is provided on SDI, the converter will remain in this conversion mode, and begin performing the next set of conversions. To exit this conversion mode, "1111 1111" must be provided on SDI during the first 8 SCLKs. If the user decides to exit, 24 more SCLKs for each referenced Setup are required to read the final conversion data set from the FIFO and return to command mode.

### *1.4.2 Calibration Protocol*

To perform a calibration, the user must send a command byte with its MSB=1, its pointer bits (CSRP3-CSRP0) set to address the desired Setup to be calibrated, and the appropriate calibration bits (CC2-CC0) set to choose the type of calibration to be performed. Proper calibration assumes that the CSRs have been previously initialized because the information concerning the physical channel, its filter rate, gain range, and polarity, comes from the channel-setup register being addressed by the pointer bits in the command byte.

Once the CSRs are initialized, all future calibrations can be performed with one command byte. Once a calibration cycle is complete, SDO falls and the results are stored in either the gain or offset register for the physical channel being calibrated. Note that if additional calibrations are performed on the same physical channel referenced by a different Setup with different filter rates, gain ranges, or conversion modes, the last calibration results will replace the effects from the previous calibration as only one offset and gain register is available per physical channel. One final note is that only one calibration is performed with each command byte. To calibrate all the channels additional calibration commands are necessary.

### *1.4.3 Example of Using the CSRs to Perform Conversions and Calibrations*

Any time a calibration command is issued (CB=1 and proper CC2-CC0 bits set) or any time a normal conversion command is issued (CB=1, CC2=CC1=CC0=0, MC=0), the bits D6-D3 (or CSRP3 - CSRP0) in the command byte are used as pointers to address one of the Setups in the channel-setup registers (CSRs). Five example situations that a user might encounter when acquiring a conversion or calibrating the converter follow. These examples assume that the user is using a CS5528 (16 Setups) and that its CSRs are programmed with the following physical channel order:
6, 1, 6, 2, 6, 3, 6, 4, 6, 5, 6, 2, 6, 7, 6, 8.

**Example 1:**

The configuration register has the following bits as shown: DP3-DP0 = ‘XXXX’, MC = 0, L = 0, RC = X. The command issued is ‘1111 0000’. These settings instruct the converter to convert the 15th Setup once, as CPB3 - CPB0 = ‘1110’ (which happens to be physical channel 6 in this example). SDO falls after physical channel 6 is converted. To read the conversion results, 32 SCLKs are then required. Once acquired, the serial port returns to the command mode.

**Example 2:**

The configuration register has the following bits as shown: DP3-DP0 = ‘XXXX’, MC = 0, LP = 1, RC = 1. The command byte issued is ‘1001 1000’. These settings instruct the converter to repeatedly convert the fourth Setup as CPB3-CPB0 = ‘0011’ (which happens to be physical channel 2 in this example). SDO falls after physical channel 2 is converted. To read the conversion results 32 SCLKs are required. The first 8 SCLKs are needed to clear the SD0 flag. If ‘0000 0000’ is provided to the SDI pin during the first 8 SCLKs, the conversion is performed again on physical channel 2. The converter will remain in data mode until ‘1111 1111’ is provided during the first 8 SCLKs following the fall of

SD0. After '1111 1111' is provided, 24 additional SCLKs are required to transfer the last 3 bytes of conversion data before the serial port will return to the command mode.

**Example 3:**

The configuration register has the following bits as shown: DP3-DP = '0101', MC = 1, LP = 0, RC = X. The command issued is '1XXX X000'. These settings instruct the converter to perform a single conversion on six Setups once. The order in which the channels are converted is 6, 1, 6, 2, 6, and 3. SDO falls after physical channel 3 is converted. To read the 6 conversion results 8 SCLKs are required to clear the SD0 flag. Then 144 additional SCLKs are required to read the conversion data from the FIFO. Again, the order in which the data is provided is the same as the order in which the channels are converted. After the last 3 bytes of the conversion data corresponding to physical channel 3 is read, the serial port automatically returns to the command mode where it will remain until the next valid command byte is received.

**Example 4:**

The configuration register has the following bits as shown: DP3-DP0 = '1001', MC = 1, LP = 1, RC = 0. The command byte issued is '1XXX X000'. These settings instruct the converter to repeatedly perform multiple-setup conversions using ten Setups. The order in which the channels are converted is: 6, 1, 6, 2, 6, 3, 6, 4, 6, 5. SDO falls after physical channel 5 is converted. To read the 10 conversion results 8 SCLKs with SDI = 0 are required to clear the SD0 flag. Then 240 more SCLKs are required to read the conversion data from the FIFO. The order in which the data is provided is the same as the order in which the channels are converted. The first 3 bytes of data correspond to the first Setup which in this example is physical channel 6; the next 3 bytes of data correspond to the second Setup which in this example is physical channel 1; and, the last 3 bytes of data corresponds to 10th Setup which here is physical channel 5. Since the Setups are converted in the background, while the data is being read, the user must finish reading the conversion data FIFO before it is updated with new conversions. To exit this conversion mode the user must provide '1111 1111' to SDI during the first 8 SCLKs. If a byte of 1's is provided, the serial port returns to the command mode only after the conversion data FIFO is emptied (in this case 10 conversions are performed). Note that in this example physical channel 6 is converted five times. Each conversion could be with the same or different filter rates depending on the setting of Setups 1, 3, 5, 7 and 9. Note that there is only one offset and one gain register per physical channel. Therefore, any physical channel can only be calibrated for the gain range selected during calibration. Specifying a different gain range in the Setup other than the range that was calibrated will result in a gain error.

**Example 5:**

The configuration register has the following bits as shown: DP3-DP0 = 'XXXX', MC = X, LP = X, RC = X. The command issued is '1010 1101'. These settings instruct the converter to perform a system offset calibration of the 6th Setup (which is physical channel 3 in this example). During calibration, the serial port remains in the command mode. Once the calibration is completed, SDO falls. To perform additional calibrations, more commands have to be issued.

***Notes:*** *1)The configuration register must be written before channel-setup registers (CSRs) because the depth information contained in the configuration register defines how many of the CSRs to use.*

*2) The CSRs need to be written regardless of single conversion or multiple single conversion mode.*

*3) When single-Setup conversions (MC = 0) are desired, the channel address is embedded in the command byte. In the multiple-Setup conversion mode (MC = 1), channels are selected in a preprogrammed order based on information contained in the CSRs and the depth bits (DP3-DP0)*

*of the configuration register.*

*4) Once the CSRs are programmed, repeated conversions on up to 16 Setups can be performed by issuing only one command byte.*

*5) The single conversion mode also requires only one command, but whenever another or a different single conversion is wanted, this command or a modified version of it has to be issued again.*

*6) The NULL command is used to keep the serial port in command mode, once it is in command mode.*

## 1.5 Conversion Output Coding

The CS5521/22/23/24/28 devices output 16-bit (CS5521/23) and 24-bit (CS5522/24/28) data conversion words. To read a conversion word, the user must read the conversion data FIFO. The conversion data FIFO is up to 192 bits long and outputs the conversions MSB first. The last byte of the conversion data word (CS5521/23 only) contains data monitoring flags. The channel indicator (CI) bits keep track of which physical channel was converted, and the overrange flag (OF) and the oscillation detect (OD) bits monitor conversions to determine if a valid conversion was performed. Refer to the *Conversion Data FIFO Descriptions* section for more details.

The CS5521/22/23/24/28 output data conversions in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode. Refer to the *Conversion Data FIFO Descriptions* section for more details.

**CS5521/23 16-Bit Output Coding**

| Unipolar Input Voltage | Offset Binary | Bipolar Input Voltage | Two's Complement |
|---|---|---|---|
| >(VFS-1.5 LSB) | FFFF | >(VFS-1.5 LSB) | 7FFF |
| VFS-1.5 LSB | FFFF<br>------<br>FFFE | VFS-1.5 LSB | 7FFF<br>------<br>7FFE |
| VFS/2-0.5 LSB | 8000<br>------<br>7FFF | -0.5 LSB | 0000<br>------<br>FFFF |
| +0.5 LSB | 0001<br>------<br>0000 | -VFS+0.5 LSB | 8001<br>------<br>8000 |
| <(+0.5 LSB) | 0000 | <(-VFS+0.5 LSB) | 8000 |

**CS5522/24/28 24-Bit Output Coding**

| Unipolar Input Voltage | Offset Binary | Bipolar Input Voltage | Two's Complement |
|---|---|---|---|
| >(VFS-1.5 LSB) | FFFFFF | >(VFS-1.5 LSB) | 7FFFFF |
| VFS-1.5 LSB | FFFFFF<br>------<br>FFFFFE | VFS-1.5 LSB | 7FFFFF<br>------<br>7FFFFE |
| VFS/2-0.5 LSB | 800000<br>------<br>7FFFFF | -0.5 LSB | 000000<br>------<br>FFFFFF |
| +0.5 LSB | 000001<br>------<br>000000 | -VFS+0.5 LSB | 800001<br>------<br>800000 |
| <(+0.5 LSB) | 000000 | <(-VFS+0.5 LSB) | 800000 |

Note: VFS in the table equals the voltage between ground and full scale for any of the unipolar gain ranges, or the voltage between ± full scale for any of the bipolar gain ranges. See text about error flags under overrange conditions.

**Table 6. Output Coding for 16-bit CS5521/23 and 24-bit CS5522/24/28**

### *1.5.1 Conversion Data FIFO Descriptions*

**CS5521/23 (EACH 16-BIT CONVERSIONS)**

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 |
| **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 3 | 2 | 1 | LSB | 1 | 1 | 1 | 0 | CI1 | CI0 | OD | OF |

**CS5522/24/28 (EACH 24-BIT CONVERSION LEVELS)**

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
| **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | LSB |

*Conversion Data Bits [23:8 for CS5521/23; 23:0 for CS5522/24/28]*

These bits depict the latest output conversion.

*OD (Oscillation detect Flag Bit)*

0 Bit is clear when oscillatory condition in modulator does not exist (bit is read only).

1 Bit is set any time an oscillatory condition is detected in the modulator. This does not occur under normal operation conditions, but may occur when the input is extremely overranged. The OD flag will be cleared to logic 0 when the modulator becomes stable.

*OF (Over-range Flag Bit)*

0 Bit is clear when over-range condition has not occurred (bit is read only).

1 Bit is set when input signal is more positive than the positive full scale, more negative than zero (unipolar mode) or when the input is more negative than the negative full scale (bipolar mode).

*CI (Channel Indicator Bits) [1:0]*

These bits indicate which physical input channel was converted.

00 Physical Channel 1 (CS5521/23 only)

01 Physical Channel 2 (CS5521/23 only)

10 Physical Channel 3 (CS5523 only)

11 Physical Channel 4 (CS5523 only)

## 1.6 Digital Filter

The CS5521/22/23/24/28 have eight different linear phase digital filters which set the output word rates (OWRs) shown in Table 3. These rates assume that XIN is 32.768 kHz. Each of the filters has a magnitude response similar to that shown in Figure 18. The filters are optimized to settle to full accuracy every conversion and yield better than 80 dB rejection for both 50 and 60 Hz with output word rates at or below 15.0 Sps.

The converter's digital filters scale with XIN. For example with an output word rate of 15 Sps, the filter's corner frequency is typically 12.7 Hz using a 32.768 kHz clock. If XIN is increased to 65.536 kHz the OWR doubles and the filter's corner frequency moves to 25.4 Hz.

## 1.7 Clock Generator

The CS5521/22/23/24/28 include a gate which can be connected with an external crystal to provide the master clock for the chip. The chips are designed to operate using a low-cost 32.768 kHz "tuning fork" type crystal. One lead of the crystal should be connected to XIN and the other to XOUT. Lead lengths should be minimized to reduce stray capacitance. Note that the oscillator circuit will also operate with a 100 kHz "tuning fork" type crystal.

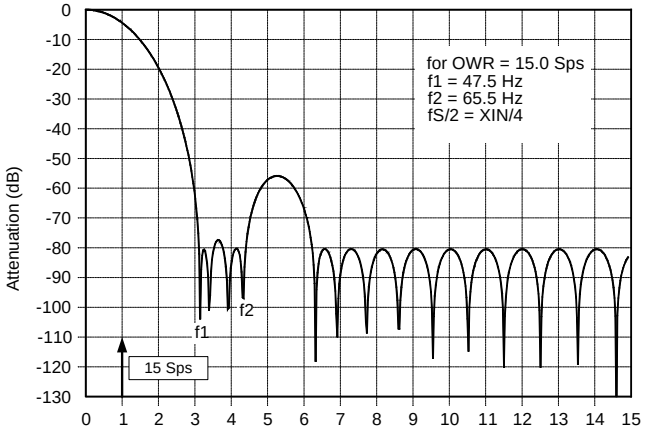



**Figure 18. Filter Response (Normalized to Output Word Rate = 15 Sps)**

The converters will operate with an external (CMOS compatible) clock with frequencies up to 130 kHz (CS5521/23) or 200 kHz (CS5522/24/28). Figures 19 and 20 detail the CS5521/23 and CS5522/24/28's performance (respectively) at increased clock rates.

The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10° C to +60° C). However, applications with the CS5521/22/23/24/28 don't generally require such tight tolerances.

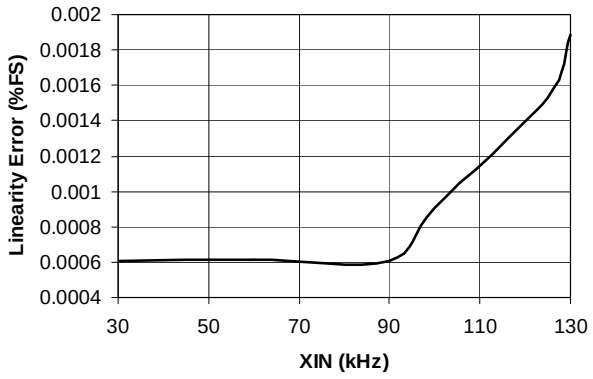



**Figure 19. Typical Linearity Error for CS5521/23**

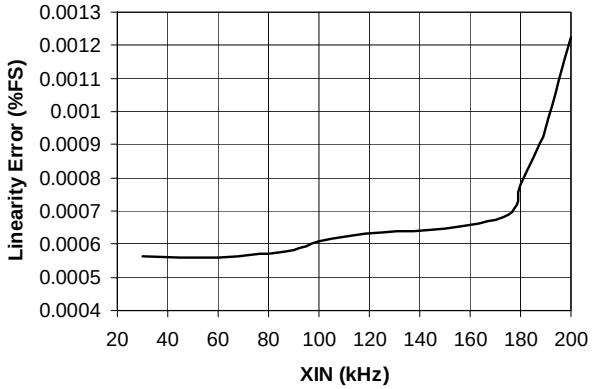



**Figure 20. Typical Linearity Error for CS5522/24/28**

## 1.8 Power Supply Arrangements

The CS5521/22/23/24/28 A/D converters are designed to operate from a single +5 V analog supply and a single +5 V or +3 V digital supply. A -2.1 V supply is usually generated from the charge pump drive to provide power to the instrumentation amplifier's NBV (negative bias voltage) pin. Figure 21 illustrates the CS5522 connected with a +5 V analog supply and with the external components required for the charge pump drive. This enables the CS5522 to measure ground-referenced signals with magnitudes down to ±100 mV.

Figure 22 illustrates the CS5522 connected to measure ground-referenced unipolar signals of a positive polarity using the 1 V, 2.5 V, and 5 V ranges on the converter. For the 25 mV, 55 mV, and 100 mV ranges, the signals being digitized must have a common mode between +1.85 to +2.65 V (NBV = 0 V).

Although CS5521/22/23/24/28 are optimized for the measurement of thermocouple outputs, they are also well suited for the measurement of ratiometric bridge transducer outputs. Figure 23 illustrates the CS5522 connected to measure the output of a ratiometric differential bridge transducer while operating from a single +5 V supply. Bridge outputs may range from 5 mV to 400 mV. See "Digital Gain Scaling" on page 45 section about manipulating the gain register to achieve optimum gain scaling.

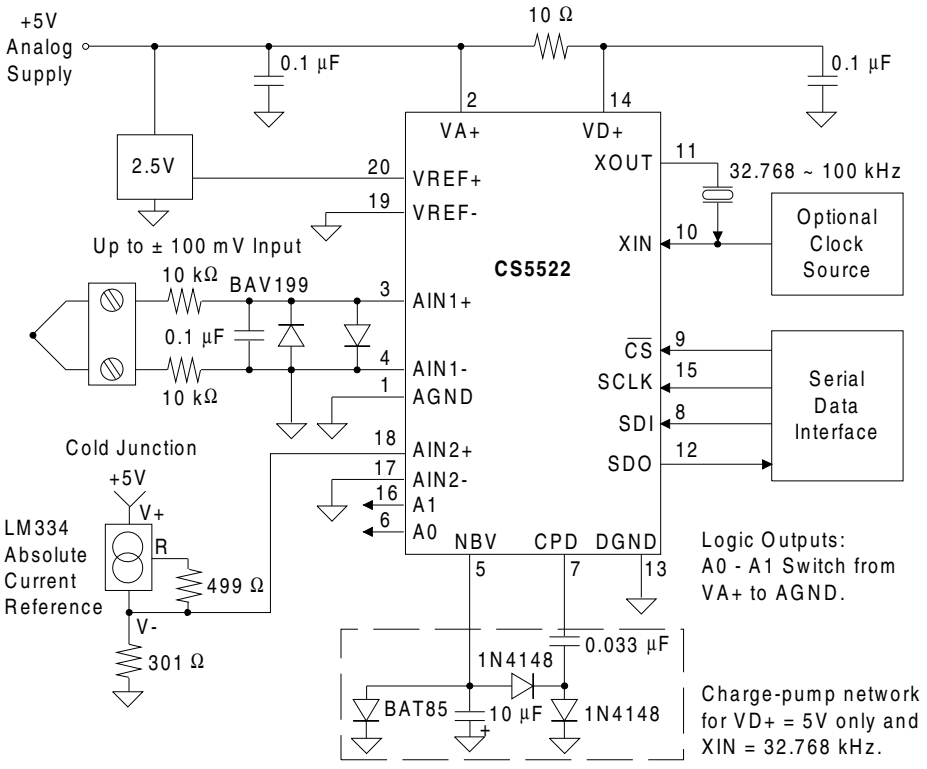



**Figure 21. CS5522 Configured to use on-chip charge pump to supply NBV**

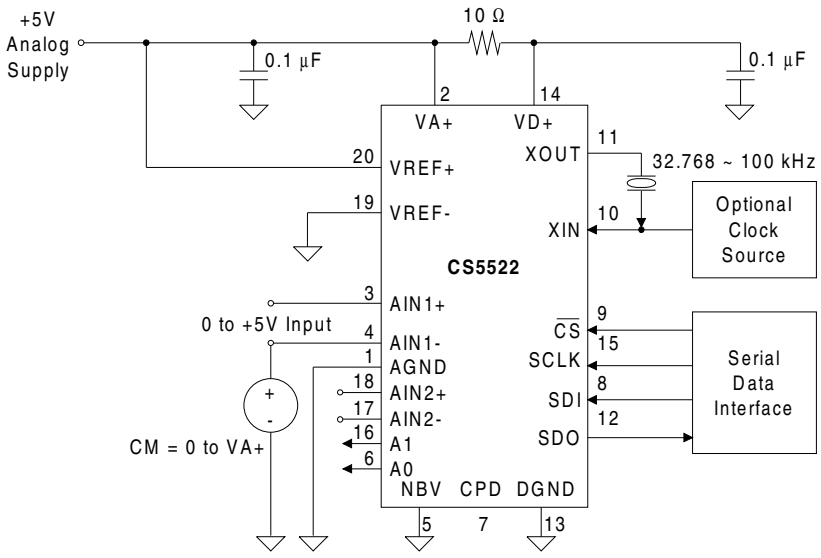



**Figure 22. CS5522 Configured for ground-referenced Unipolar Signals**

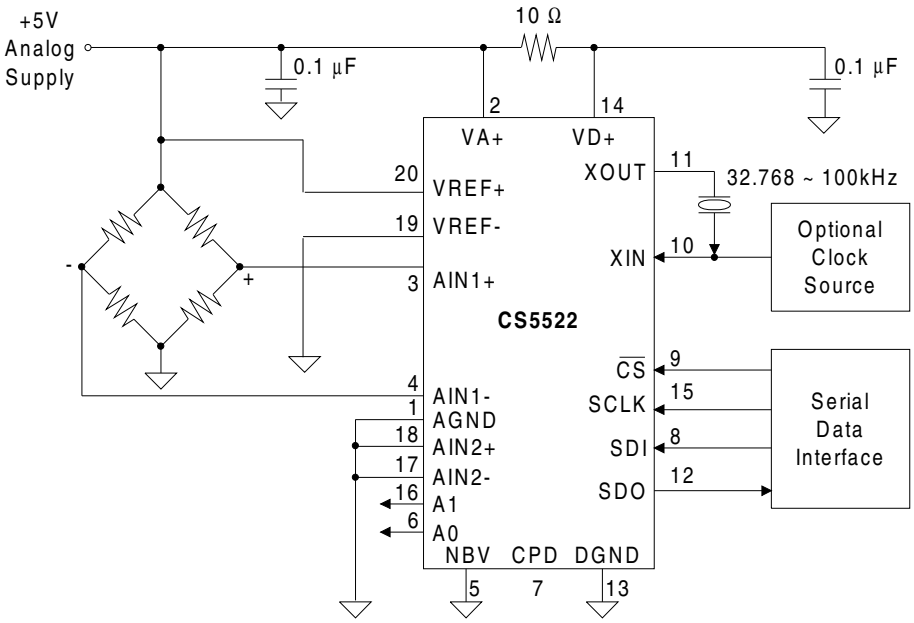



**Figure 23. CS5522 Configured for Single Supply Bridge Measurement**

### *1.8.1 Charge Pump Drive Circuits*

The CPD (Charge Pump Drive) pin of the converter can be used with external components (shown in Figure 21) to develop an appropriate negative bias voltage for the NBV pin. When CPD is used to generate the NBV, the NBV voltage is regulated with an internal regulator loop referenced to VA+. Therefore, any change on VA+ results in a proportional change on NBV. With VA+ = 5 V, NBV's regulation is set proportional to VA+ at approximately -2.1 V.

Figure 24 illustrates a charge pump circuit when the converters are powered from a +3.0 V digital supply. Alternatively, the negative bias supply can be generated from a negative supply voltage or a resistive divider as illustrated in Figure 25.

For ground-based signals with the instrumentation amplifier engaged (when in the 25 mV, 55 mV, or 100 mV ranges), the voltage on the NBV pin should at no time be less negative than -1.8 V or more negative than -2.5 V. To prevent excessive voltage stress to the chip when the instrumentation amplifier isn't engaged (when in the 1 V, 2.5 V, or 5 V ranges) the NBV voltage should not be more negative than -2.5 V.

The components in Figure 21 are the preferred components for the CPD filter. However, smaller capacitors can be used with acceptable results. The 10 µF ensures very low ripple on NBV. Intrinsic safety requirements prohibit the use of electrolytic capacitors. In this case, four 0.47 µF ceramic capacitors in parallel can be used.

***Note:*** *The charge pump is designed to nominally provide 400 µA of current for the instrumentation amplifier when a 0.033 µF pumping capacitor is used (XIN = 32.768 kHz). When a larger pumping capacitor is used, the charge pump can source more current to power external loads. Refer to Applications Note 152 "Using the CS5521/23, CS5522/24/28, and CS5525/26 Charge Pump Drive for External Loads" for more details on using the charge pump with external loads.*

## 1.9 Digital Gain Scaling

The CS5521/22/23/24 and CS5528 all feature a gain register capable of being scaled from 0.6 to 4-$2^{-22}$ in decimal. The specified ranges of the converter are defined with a voltage reference of 2.5 V and the gain register set at approximately 1.0. The gain register can be manipulated to scale the input for ranges other than those specified. For example, when using a 2.5 V voltage reference, and the 25 mV input range setting, the gain register can be changed from 1.000 to 2.000 (shift the entire register contents to the left one position) to achieve an input span of 12.5 mV. Under this condition the full span of the converter codes will appear across a 12.5 mV span. The amount of noise in the con-

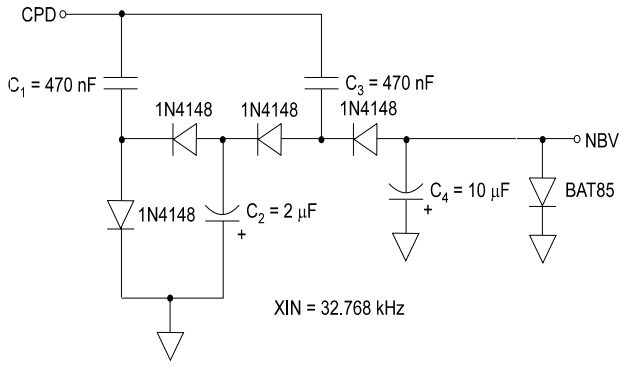



**Figure 24. Charge Pump Drive Circuit for VD+ = 3 V**

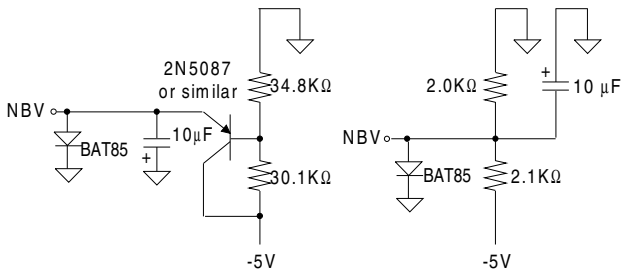



**Figure 25. Alternate NBV Circuits**

verter stays constant but the number of codes affected is doubled because the code size has been reduced by half.

The converter input ranges are specified with a voltage reference of 2.5 V. The device can be operated with the reference tied directly to the +5 V supply. When this is done, the input span of the input ranges is doubled; the 25 mV range actually becomes a 50 mV range. The gain register can be set to 2.0 (shift contents left one bit) and the input range will be scaled back to 25 mV. Since the gain register can actually be as great as $4\text{-}2^{-22}$ decimal, one could scale the input span on the 25 mV range to accept an analog full-scale span of about 6.25 mV. This is useful for ratiometric bridge measurement of low-level differential outputs.

The gain register can also be scaled manually to a value lower than 1.0. It is not recommended to use the devices with the gain register scaled lower than 0.6. This can enable the converter to accept a 40 mV input signal on the 25 mV range when using a voltage reference of 2.5 V. Caution though in scaling the gain register below 1.0 on the 100 mV, 2.5 and 5 volt ranges as the analog signal path into the converter may saturate before the expected full-scale code output is produced by the converter.

Note that digital gain scaling will directly influence the number of digital output codes affected by noise. The effects can be analytically determined by calculating the size of the codes (V/Count) which result from a given gain scaling condition and relating the amount of noise in the converter relative to the determined code size. The evaluation board for the converter is a useful tool to aid the assessment of noise performance with various voltage reference values, input range settings, and gain register settings. The evaluation board supports noise analysis through data capture and noise histogram analysis.

## 1.10 Getting Started

The CS5521/22/23/24/28 have many features. From a software programmer's perspective, what should be done first? To begin, a 32.768 kHz crystal takes approximately 500 ms to start-up. To accommodate for this, it is recommended that a software delay greater than 500 ms precede the processor's ADC initialization code before any registers are accessed in the ADC. This delay time is dependent on the start-up delay of the clock source. If a CMOS clock source with no start-up delay is being used to drive the ADC, then this delay is not necessary.

Once the oscillator is started, the following sequence of instructions should be performed to guarantee the converter begins proper operation:

1) After power is applied, initialize the serial port using the serial port synchronization sequence.
2) Write a '1' to the reset bit (RS) of the configuration register to reset the converter.
3) Read the configuration register to determine if the reset valid bit (RV) is set to '1'. If the RV bit is not set, the configuration register should be read again.
4) When the RV bit has been set to '1', reset the RS bit back to '0' by writing 0x000000 to the configuration register. Note that while the RS bit is set to '1' all other register bits in the ADC will be reset to their default state, and the RS bit must be set to '0' for normal operation of the converters.

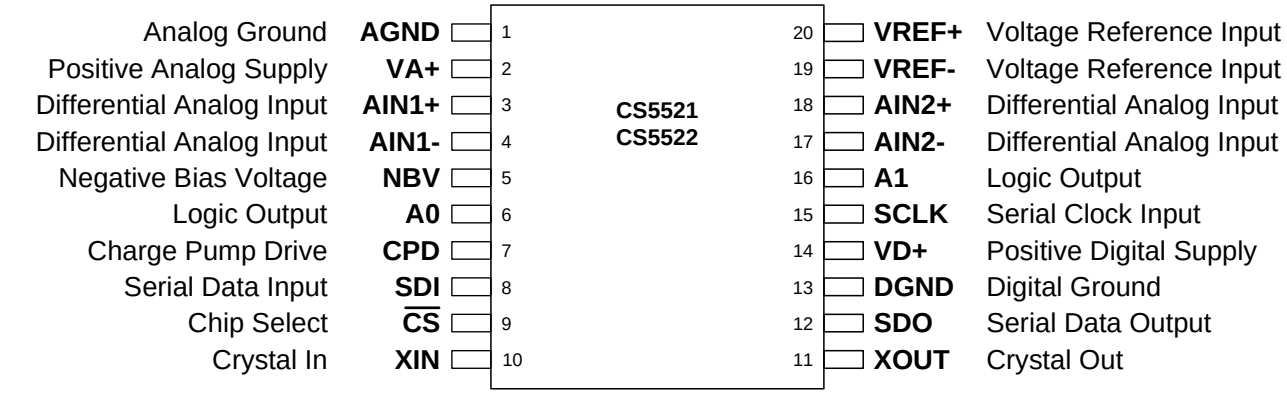
Once the RS bit has been set to '0', the ADC is placed in the command state were it waits for a valid command to execute. The next step is to load the configuration register and then the channel setup registers with conditions that you have decided. If you need to do a factory calibration, perform offset and gain calibrations for each channel that is to be used. Then off-load the offset and gain register contents into EEPROM. These registers can then

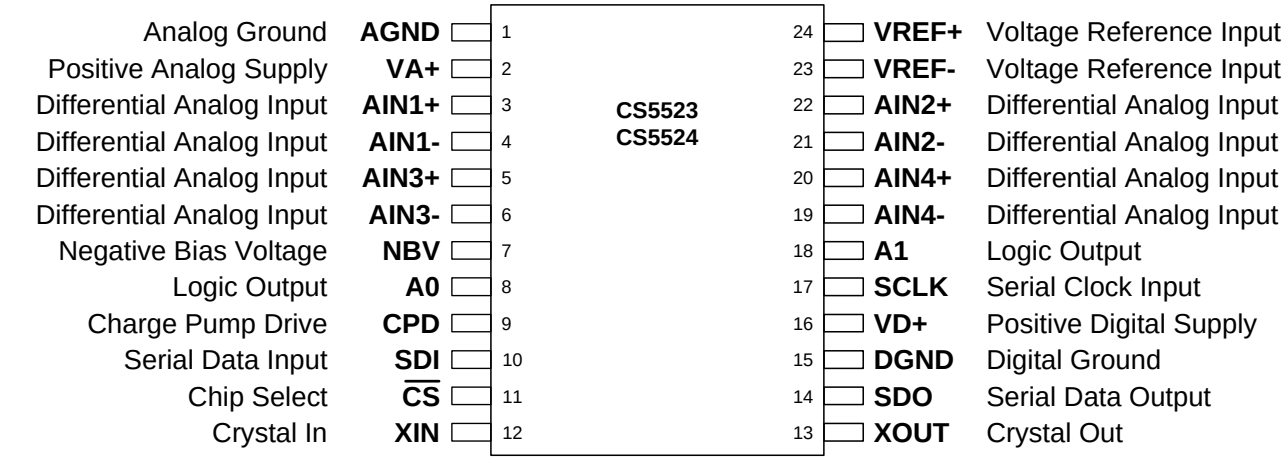
be initialized to these conditions when the instrument is used in normal operation. Once calibration is ready, input the command to start conversions in the mode you have selected via the configuration register bits. Monitor the SDO pin for a flag that the data is ready and read conversion data.

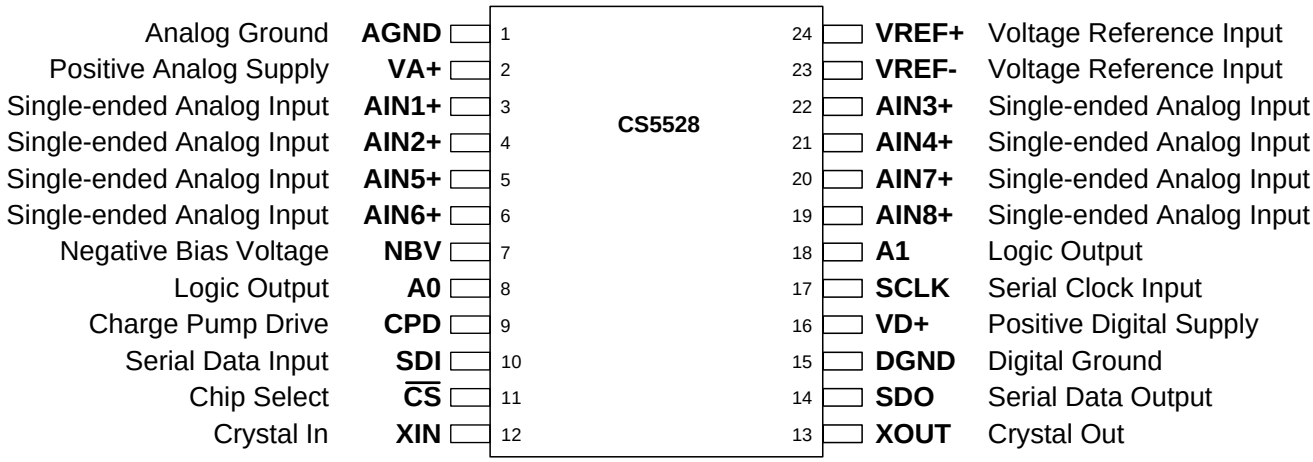
## 1.11 PCB Layout

The CS5521/22/23/24/28 should be placed entirely over an analog ground plane with both the AGND and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip. If separate digital (VD+) and analog (VA+) supplies are used, it is recommended that a diode be placed between them (the cathode of the diode should point to VA+). If the digital supply comes up before the analog supply, the ADC may not start up properly.

## 2. PIN DESCRIPTIONS



## 2.1 Clock Generator

**XIN; XOUT - Crystal In; Crystal Out.**

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device.

## 2.2 Control Pins and Serial Data I/O

**$\overline{\text{CS}}$ - Chip Select.**

When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{\text{CS}}$ should be changed when SCLK = 0.

**SDI - Serial Data Input.**

SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK.

**SDO - Serial Data Output.**

SDO is the serial data output. It will output a high impedance state if $\overline{\text{CS}}$ = 1.

**SCLK - Serial Clock Input.**

A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{\text{CS}}$ is low.

**A0, A1 - Logic Outputs.**

The logic states of A0-A1 mimic the states of the D22/D10-D23/D11 bits of the channel-setup register. Logic Output 0 = AGND, and Logic Output 1 = VA+.

## 2.3 Measurement and Reference Inputs

**AIN1+, AIN1-, AIN2+, AIN2- AIN3+, AIN3-, AIN4+, AIN4- - Differential Analog Input.**

Differential input pins into the CS5522 and CS5524 devices.

**AIN1+, AIN2+, AIN3+, AIN4+, AIN5+, AIN6+, AIN7+, AIN8+ - Single-Ended Analog Input.**

Single-ended input pins into the CS5528.

**VREF+, VREF- - Voltage Reference Input.**

Fully differential inputs which establish the voltage reference for the on-chip modulator.

**NBV - Negative Bias Voltage.**

Input pin to supply the negative supply voltage for the 20X gain instrumentation amplifier and coarse/fine charge buffers. May be tied to AGND if AIN+ and AIN- inputs are centered around +2.5 V; or it may be tied to a negative supply voltage (-2.1 V typical) to allow the amplifier to handle low level signals more negative than ground. When using the CS5528 in either the 25 mV, 55 mV or 100 mV range, the analog inputs are expected to be ground referenced; therefore, NBV must be between -1.8 to -2.5 to ensure proper operation.

**CPD - Charge Pump Drive.**

Square wave output used to provide energy for the charge pump.

## 2.4 Power Supply Connections

**VA+ - Positive Analog Power.**

Positive analog supply voltage. Nominally +5 V.

**VD+ - Positive Digital Power.**

Positive digital supply voltage. Nominally +3.0 V or +5 V.

**AGND - Analog Ground.**

Analog Ground.

**DGND - Digital Ground.**

Digital Ground.

## 3. SPECIFICATION DEFINITIONS

**Linearity Error**

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

**Differential Nonlinearity**

The deviation of a code's width from the ideal width. Units in LSBs.

**Full Scale Error**

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

**Unipolar Offset**

The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.). When in unipolar mode ($U/\overline{B}$ bit = 1). Units are in LSBs.

**Bipolar Offset**

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below the voltage on the AIN- pin). When in bipolar mode ($U/\overline{B}$ bit = 0). Units are in LSBs.

## 4. ORDERING INFORMATION

| Model Number | Bits | Channels | Linearity Error (Max) | Package | Temperature Range |
|---|---|---|---|---|---|
| CS5521-ASZ | 16 | 2 | ±0.003% | 20-pin 0.2" Plastic SSOP (Lead Free) | -40°C to +85°C |
| CS5522-ASZ | 24 | | ±0.0015% | | |
| CS5523-ASZ | 16 | 4 | ±0.003% | 24-pin 0.2" Plastic SSOP (Lead Free) | |
| CS5524-ASZ | 24 | | ±0.0015% | | |
| CS5528-ASZ | | 8 | | | |

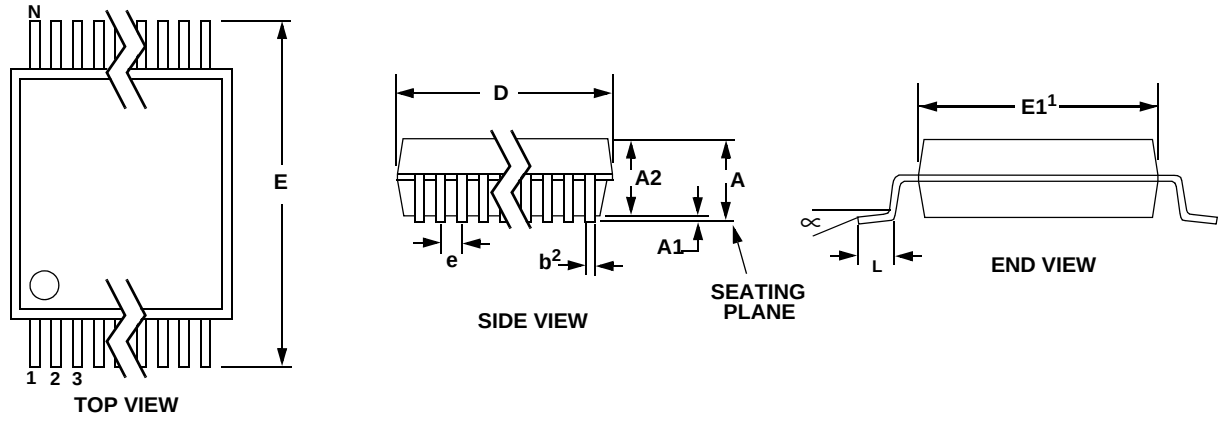
## 5. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

| Model Number | Package | MSL Rating* | Peak Reflow Temp | Max Floor Life |
|---|---|---|---|---|
| CS5521-ASZ | 20-pin 0.2" Plastic SSOP (Lead Free) | 3 | 260 °C | 7 Days |
| CS5522-ASZ | | | | |
| CS5523-ASZ | 24-pin 0.2" Plastic SSOP (Lead Free) | | | |
| CS5524-ASZ | | | | |
| CS5528-ASZ | | | | |

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

## 6. PACKAGE DIMENSION DRAWINGS

### 20L SSOP PACKAGE DRAWING



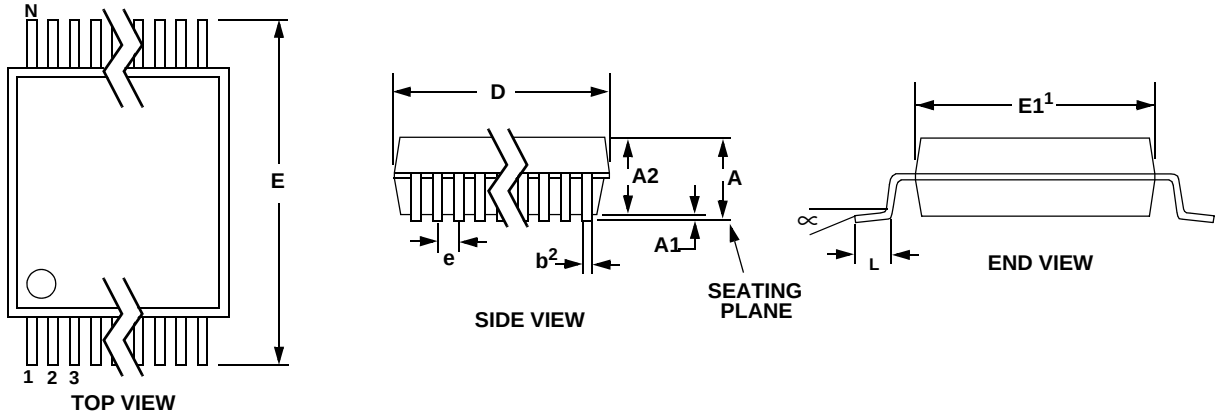

| | INCHES | | | MILLIMETERS | | | NOTE |
|---|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX | |
| A | -- | -- | 0.084 | -- | -- | 2.13 | |
| A1 | 0.002 | 0.006 | 0.010 | 0.05 | 0.13 | 0.25 | |
| A2 | 0.064 | 0.068 | 0.074 | 1.62 | 1.73 | 1.88 | |
| b | 0.009 | -- | 0.015 | 0.22 | -- | 0.38 | 2,3 |
| D | 0.272 | 0.2834 | 0.295 | 6.90 | 7.20 | 7.50 | 1 |
| E | 0.291 | 0.307 | 0.323 | 7.40 | 7.80 | 8.20 | |
| E1 | 0.197 | 0.209 | 0.220 | 5.00 | 5.30 | 5.60 | 1 |
| e | 0.022 | 0.026 | 0.030 | 0.55 | 0.65 | 0.75 | |
| L | 0.025 | 0.03 | 0.041 | 0.63 | 0.75 | 1.03 | |
| ∝ | 0° | 4° | 8° | 0° | 4° | 8° | |

***JEDEC #: MO-150***

Controling Dimension is Millimeters.

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

## 24L SSOP PACKAGE DRAWING




| | INCHES | | | MILLIMETERS | | | NOTE |
|---|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX | |
| A | -- | -- | 0.084 | -- | -- | 2.13 | |
| A1 | 0.002 | 0.006 | 0.010 | 0.05 | 0.13 | 0.25 | |
| A2 | 0.064 | 0.068 | 0.074 | 1.62 | 1.73 | 1.88 | |
| b | 0.009 | -- | 0.015 | 0.22 | -- | 0.38 | 2,3 |
| D | 0.311 | 0.323 | 0.335 | 7.90 | 8.20 | 8.50 | 1 |
| E | 0.291 | 0.307 | 0.323 | 7.40 | 7.80 | 8.20 | |
| E1 | 0.197 | 0.209 | 0.220 | 5.00 | 5.30 | 5.60 | 1 |
| e | 0.022 | 0.026 | 0.030 | 0.55 | 0.65 | 0.75 | |
| L | 0.025 | 0.03 | 0.041 | 0.63 | 0.75 | 1.03 | |
| ∝ | 0° | 4° | 8° | 0° | 4° | 8° | |

***JEDEC #: MO-150***

Controling Dimension is Millimeters.

Notes:
1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

## 7. REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| F8 | JUL 2009 | Leaded (Pb) and PDIP-packaged devices removed from ordering information. |

### Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
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