RF Wideband Gain-Settable Downconverting Mixer 400MHz to 3800MHz

F1792
Datasheet

Description

This document describes the specifications for the F1792 Wideband, Gain-Settable, Zero-Distortion™ Flat-Noise™, RF to IF Downconverting Mixer.

The F1792 offers very low power consumption with excellent linearity. In addition to this the F1792 has four dynamically adjustable gain settings. The F1792 performance is exceptional across an extremely broad range of RF and IF frequencies. All of this makes it ideal for a myriad of applications including:

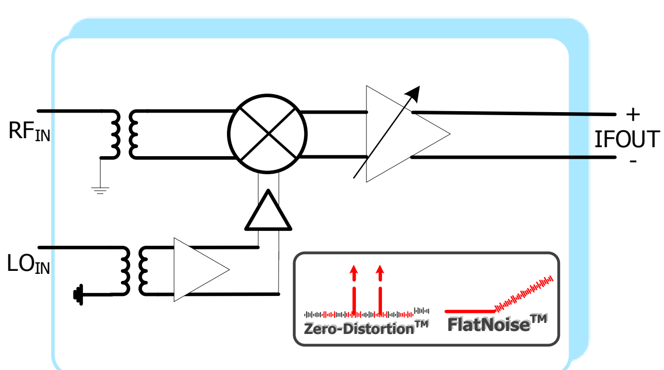
- 2G/3G/4G/5G/Multimode Remote Radio Units
- Point to Point µWave Backhaul systems
- Broadband Repeaters
- Public Safety Infrastructure
- Any radio system operating between 400 MHz and 4000 MHz

Competitive Advantage

F1792 offers maximum performance and flexibility at minimum power consumption. The unique and patented settable-gain feature allows it to be used in a very wide variety of radio card applications, even allowing for dynamic adjustment of gain to maximize performance on the fly. The extremely wide RF and IF bandwidths are achieved using a fixed BOM, all RF matching is internal to the device. The F1792 can function with as little as -6 dBm LO power. It also features a channel shutdown mode for ease of integration into high order TDD systems.

Block Diagram

Figure 1. Functional Block Diagram



Features

- RF range: 400MHz to 3800MHz
- LO range: 400MHz to 3600MHz
- IF Range: 50MHz to 600MHz
- 4 Gain Settings; 11dB, 8dB, 5dB, 2dB
- 2 bit gain step control
- Ideal for Multi-Carrier Systems
- +35dBm OIP3
- Low Noise Figure at any gain setting via IDT's FlatNoise™ technology
- Z = 200 Ω IF balanced, 50 Ω RF, 50 Ω LO single ended
- All internally matched. Single BOM for all RF, LO and IF frequencies
- 4 mm x 4 mm, 24-pin TQFN package
- Independent Path Standby mode
- 75 nsec settling for gain adjustment
- VCC = 3.3V, 462 mW, 373 mW (low power mode)

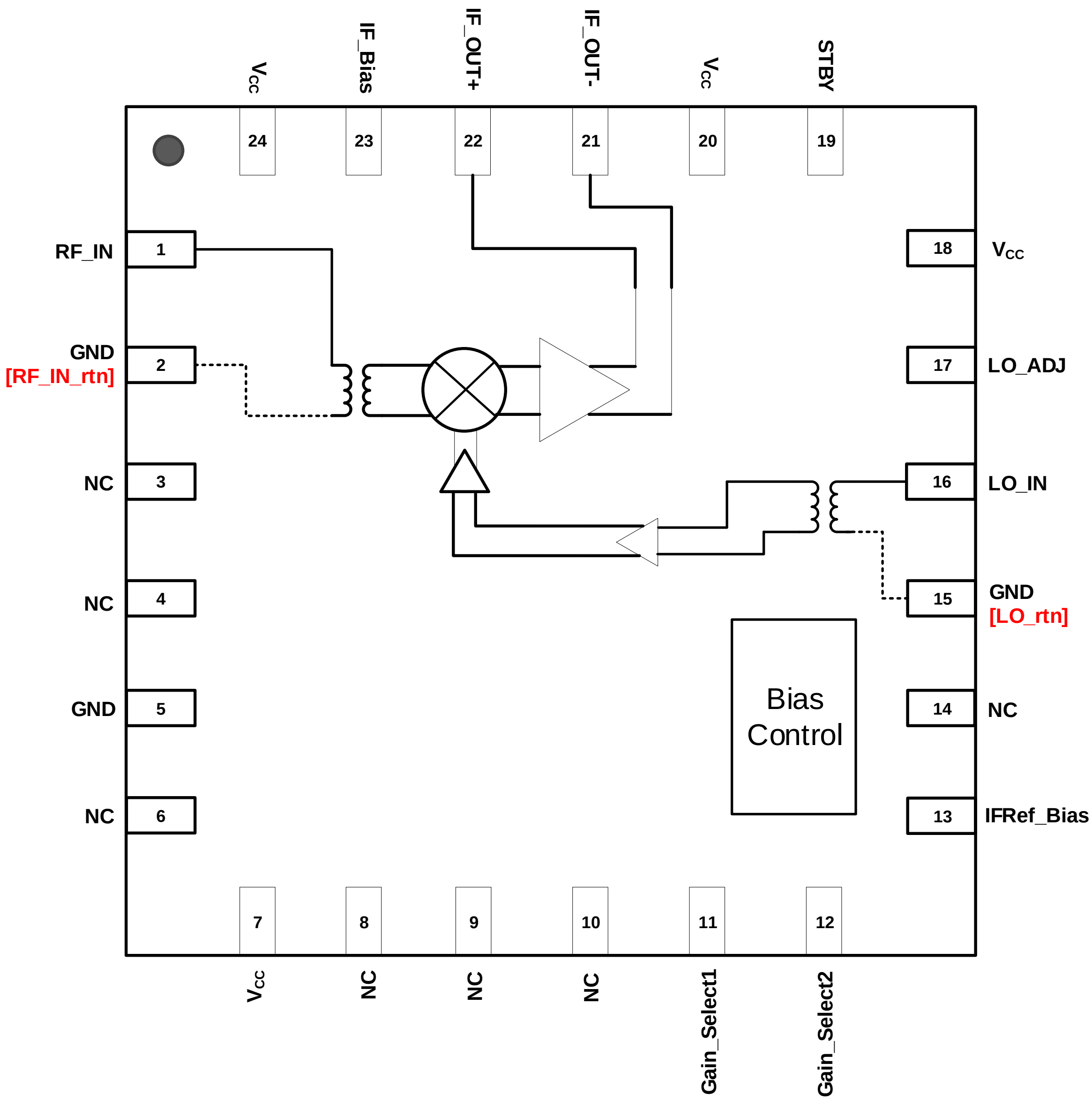
Band Performance Summary

RF Frequency (MHz)	900	1900	2600	3500
Gain (dB, max G11 setting)	11.0	10.8	10.3	9.0
Gain (dB, min G2 setting)	2.5	2.3	1.8	0.5
NF @ max gain (dB)	8.9	8.7	10.0	10.9
IIP3 @ min gain (dBm)	28	27	29	30
OIP3 @ G8 (dBm)	37	34	35	35
IP1dB @ min gain (dBm)	13.6	14.7	14.6	15.8
Pdiss (mW)	442	462	485	520

Pin Assignments

Figure 2. Pin Assignments for 4 x 4 mm 24-pin-TQFN Package – Top View

Red denotes internal connection



Pin Descriptions

Table 1. F1792 Pin Descriptions

Number	Name	Description
1	RF_IN	RF input. Matched to 50 ohms. DO NOT apply DC to this pin.
2	RF_IN_rtn	RF input transformer ground return. Ground this pin.
3, 4, 6, 8, 9, 10, 14	NC	Not connected.
5	GND	Ground this pin.
7, 18, 20, 24	VCC	Power Supply. Bypass to ground with appropriate capacitors as close as possible to pin
11	Gain_Select1	Gain select control pin, includes internal pull-down resistor. See gain select truth table for desired setting
12	Gain_Select2	Gain select control pin, includes internal pull-down resistor. See gain select truth table for desired setting
13	IFRef_Bias	Connect recommended resistor value from this pin to ground to set the IF amplifier reference current
15	LO_IN_rtn	LO input transformer ground return. Ground this pin.
16	LO_IN	Local Oscillator (LO) input. Matched to 50 ohms. DO NOT apply DC to this pin.
17	LO_ADJ	Connect zero ohm resistor to ground here for best performance
19	STBY	Standby Input (Low/Open = Power ON, High = Power OFF). Includes internal pull-down resistor
21, 22	IF_OUT-, IF_OUT+	Mixer Differential IF Output. Connect pull-up inductors from each of these pins to VCC (see the Typical Application Circuit)
23	IF_Bias	Connect the specified resistor from this pin to ground to set the bias for the Main IF amplifier
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Maximum	Units
VCC to GND	V_{CC}		-0.5	+3.6	V
STBY, Gain_Select1, Gain_Select2, RF_IN, LO1_ADJ, LO2_ADJ	V_{CTRL}		-0.5	Vcc+0.5	V
IF_OUT+, IF_OUT-	IF_{OUT}		2.4	Vcc+0.5	V
LO_IN	LO_{IN}		-0.5	+0.5	V
IF_Bias	IF_{BIAS}			50	Ohms
IF_Ref_Bias	IF_{REF}			500	Ohms
RF Input Power	RF_{MAX}	continuous		20	dBm
LO Input Power	LO_{MAX}	continuous		20	dBm
Continuous Power Dissipation	P_{DISS}			1.5	W
Junction temperature	T_J	-	-	150	°C
Storage temperature	T_S	-	-65	150	°C
Lead temperature	T_{LEAD}	(soldering, 10 seconds)		260	°C
ESD – Human Body Model (JEDEC/ESDA JS-001-2012)	-	-	-	Class 2 (2500)	V
ESD – Charged Device Model (JEDEC 22-C101F)	-	-	-	Class C3 (1000)	V

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power supply voltage	V_{CC}	3.15	-	3.45	V
Operating temperature range	T_{CASE}	-40	-	105	°C
RF Frequency Range	F_{RF}	400		3800	MHz
Local Oscillator (LO) Frequency Range	F_{LO}	400		3600	MHz
Intermediate Frequency (IF) Range	F_{IF}	50		600	MHz
Local oscillator power level	P_{LO}	-6		+6	dBm

Electrical Characteristics

Table 4. IDTF1792 Specification (General)

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 900MHz, F_{IF} = 199MHz, F_{LO} = 1099MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Logic Input High[3]	V_{IH}[3]	-	***1.1***[1]			V
Logic Input Low[3]	V_{IL}[3]	Minimum attenuation			***0.65***	V
Logic Current	I_{IH}, I_{IL}	For all control pins	***-5***		***+100***	mA
Supply Current	I_{CH_LB}	Low band LO		134	***154***	mA
Supply Current	I_{CH_MB}	Mid band LO		140	***160***	mA
Supply Current	I_{CH_HB}	High band LO		147	***166***	mA
Supply Current – reduced linearity		FRF = 2.2GHz, FLO = 2GHz OIP3 = +20dBm max gain IFRef_Bias resistor = 3.9Kohm		113	***135***	mA
Shutdown current	I_{SD}			3	***6***	mA
Settling Time	T_{SETT}	Pin = -13 dBm Gate STBY pin Time for IF Signal to settle from 50% STBY to within 90% of final value		340		nsec
		Pin = -13 dBm Gate STBY pin Time for IF Signal to settle from 50% STBY to within 0.1 dB of final value		920		nsec
		Pin = -13 dBm Gate Gain Select pins per Gain Control table Time for IF Signal to settle from 50% Gain Select to within 90% of final value		75		nsec
RFIN Impedance	Z_{RFIN}	Single Ended		50		Ω
LO Port Impedance	Z_{LO}	Single Ended		50		Ω
IF Output Impedance	Z_{IF}	Differential		200		Ω
IF Return Loss	RL_{IF}	Differential 200 ohm with 4:1 Balun		-15		dB
LO Return Loss	RL_{LO}	Single Ended 50 ohm		-15		dB

NOTE 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
NOTE 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic

Table 5. IDTF1792 Specification (Low Band)

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 900MHz, F_{IF} = 199MHz, F_{LO} = 1099MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted. Gain Setting = G_5 (~ 5 dB gain).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Power Gain	G_{11}	Gain setting = G_{11}		11.1		dB
	G_8	Gain setting = G_8		8.3		
	G_5	Gain setting = G_5	***4.05***	5.4	***6.75***[1]	
	G_2	Gain setting = G_2		2.5		
G5 Gain Change over temp	$G5_{TempDrift}$	Tcase -40C / +105C referenced to +25C		-0.7 / +0.7		dB
Gain Slope	$Gain_{SLOPE}$	IF center 200MHz 100MHz BW		+0.006		dB/MHz
Noise Figure	NF_{G11}	Gain setting = G_{11}		8.9		dB
	NF_{G8}	Gain setting = G_8		9.4		
	NF_{G5}[4, 5]	Gain setting = G_5		10.1	11.7[2]	
	NF_{G2}	Gain setting = G_2		10.7		
Input IP3	$IIP3_{G11}$	Gain setting = G_{11} 800 kHz tone separation		24		dBm
	$IIP3_{G8}$	Gain setting = G_8 800 kHz tone separation		29		
	$IIP3_{G5}$[4]	Gain setting = G_5 800 kHz tone separation	26	28		
	$IIP3_{G2}$	Gain setting = G_2 800 kHz tone separation		28		
G3 IIP3 change over temp	$IIP3_{G3TempDrift}$	Tcase -40C / +105C referenced to +25C		-2.6/+0.6		dB
Output IP3	$OIP3_{G11}$	Gain setting = G_{11} 800 kHz tone separation		35		dBm
	$OIP3_{G8}$	Gain setting = G_8 800 kHz tone separation		37		

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NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic
NOTE 4: Specification limits over voltage and temperature
NOTE 5: Max limit at Tcase = +105C

Table 6. IDTF1792 Specification (Low Band) Continued

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 900MHz, F_{IF} = 199MHz, F_{LO} = 1099MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted. Gain Setting = G_5 (~ 5 dB gain).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output IP3	$OIP3_{G5}$	Gain setting = G_5 800 kHz tone separation		32		dBm
		Gain setting = G_5 Tc = +105°C LO power = -3dBm Vcc = 3.15V	33	34		
	$OIP3_{G2}$	Gain setting = G_2 800 kHz tone separation		30		
Input P1dB	$IP1dB_{G11}$	Gain setting = G_{11} IF_B Pout versus IF_A w/ RF_A input		7.0		dB
	$IP1dB_{G8}$	Gain setting = G_8		9.2		
	$IP1dB_{G5}$ [4]	Gain setting = G_5	10.4	11.8		
	$IP1dB_{G2}$	Gain setting = G_2		13.6		
Maximum saturated output power	P_{sat}	P_{in} up to +20dBm		17		dBm
LO to IF leakage	ISO_{LI}		47	48		dBm
2LO to IF leakage	ISO_{LI2}			-38	-35	dBm
3LO to IF leakage	ISO_{LI3}			-25		dBm
4LO to IF leakage	ISO_{LI4}			-49		dBm
RF to IF leakage	ISO_{RI}	RF output power compared to measured IF output power		-25	-23	dBc
LO to RF leakage	ISO_{LR}			-52		dBm
RF Return Loss	RL_{RF}	Single Ended 50 ohm		-12		dB

NOTE 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
NOTE 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic
NOTE 4: Specification limits over voltage and temperature
NOTE 5: Max limit at Tcase = +105C

Table 7. IDTF1792 Specification (Mid Band)

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 1900MHz, F_{IF} = 199MHz, F_{LO} = 1701MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted. Gain Setting = G_5 (~ 5 dB gain).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Power Gain	G_{11}	Gain setting = G_{11}		10.8		dB
	G_8	Gain setting = G_8		8.1		
	G_5	Gain setting = G_5	***3.75***	5.1	***6.45***[1]	
	G_2	Gain setting = G_2		2.3		
G5 Gain Change over temp	$G5_{TempDrift}$	Tcase -40C / +105C referenced to +25C		-0.6 / +0.7		dB
Gain Slope	$Gain_{SLOPE}$	IF center 200MHz 100MHz BW		+0.006		dB/MHz
Noise Figure	NF_{G11}	Gain setting = G_{11}		8.7		dB
	NF_{G8}	Gain setting = G_8		9.1		
	NF_{G5} [4, 5]	Gain setting = G_5		9.8	11.4[2]	
	NF_{G2}	Gain setting = G_2		10.7		
Blocking Noise Figure	NF_{BLK}	Gain setting = G_{11} +100MHz offset blocker Pin = +4 dBm		17		dB
Input IP3	$IIP3_{G11}$	Gain setting = G_{11} 800 kHz tone separation		23		dBm
	$IIP3_{G8}$	Gain setting = G_8 800 kHz tone separation		25		
	$IIP3_{G5}$ [4]	Gain setting = G_5 800 kHz tone separation	25	26		
	$IIP3_{G2}$	Gain setting = G_2 800 kHz tone separation		27		
G3 IIP3 change over temp	$IIP3_{G3TempDrift}$	Tcase -40C / +105C referenced to +25C		-0.2/+5		dB
Output IP3	$OIP3_{G11}$	Gain setting = G_{11} 800 kHz tone separation		33.6		dBm
	$OIP3_{G8}$	Gain setting = G_8 800 kHz tone separation		33.6		

NOTE 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
NOTE 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic
NOTE 4: Specification limits over voltage and temperature
NOTE 5: Max limit at Tcase = +105C

Table 8. IDTF1792 Specification (Mid Band) Continued

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 1900MHz, F_{IF} = 199MHz, F_{LO} = 1701MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted. Gain Setting = G_5 (~ 5 dB gain).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
	$OIP3_{G5}$	Gain setting = G_5 800 kHz tone separation	***29***	31.0		
		Gain setting = G_5 Tc = +105°C LO power = -3dBm Vcc = 3.15V	28.8	29.5		
	$OIP3_{G2}$	Gain setting = G_2 800 kHz tone separation		29.0		
Input P1dB	$IP1dB_{G11}$	Gain setting = G_{11}	***6.0***	7.7		dB
	$IP1dB_{G8}$	Gain setting = G_8		10.1		
	$IP1dB_{G5}$ [4]	Gain setting = G_5	11.3	12.7		
	$IP1dB_{G2}$	Gain setting = G_2		14.7		
Maximum saturated output power	P_{sat}	P_{in} up to +20dBm		17		dBm
LO to IF leakage	ISO_{LI}			-31	***-22***	dBm
2LO to IF leakage	ISO_{LI2}			-20		dBm
3LO to IF leakage	ISO_{LI3}			-59		dBm
4LO to IF leakage	ISO_{LI4}			-44		dBm
RF to IF leakage	ISO_{RI}	RF output power compared to measured IF output power		-25	***-20***	dBc
LO to RF leakage	ISO_{LR}			-46		dBm
RF Return Loss	RL_{RF}	Single Ended 50 ohm		-13		dB

NOTE 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
NOTE 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic
NOTE 4: Specification limits over voltage and temperature
NOTE 5: Max limit at Tcase = +105C

Table 9. IDTF1792 Specification (High Band)

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 2600MHz, F_{IF} = 199MHz, F_{LO} = 2401MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted. Gain Setting = G_5 (~ 5 dB gain).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Power Gain	G_{11}	Gain setting = G_{11}		10.3		dB
	G_8	Gain setting = G_8		7.5		
	G_5	Gain setting = G_5	***3.25***	4.6	***5.95***[1]	
		Gain setting = G_5 F_{IF} = 469MHz F_{LO} = 2130MHz	***2.4***	4.0	***5.6***	
	G_2	Gain setting = G_2		1.8		
G5 Gain Change over temp	$G5_{TempDrift}$	Tcase -40C / +105C referenced to +25C		-0.7 / +0.7		dB
Gain Slope	$Gain_{SLOPE1}$	IF center 200MHz 100MHz BW		+0.006		dB/MHz
	$Gain_{SLOPE2}$	IF center 370MHz 200MHz BW		+0.008		dB/MHz
Noise Figure	NF_{G11}	Gain setting = G_{11}		10.0		dB
	NF_{G8}	Gain setting = G_8		10.4		
	NF_{G5} [4, 5]	Gain setting = G_5		11.1	13[2]	
		Gain setting = G_5 F_{IF}= 469MHz F_{LO} = 2130MHz		11.8		
	NF_{G2}	Gain setting = G_2		11.9		
Input IP3	$IIP3_{G11}$	Gain setting = G_{11} 800 kHz tone separation		24		dBm
	$IIP3_{G8}$	Gain setting = G_8 800 kHz tone separation		28		
	$IIP3_{G5}$ [4]	Gain setting = G_5 800 kHz tone separation	25	28		
	$IIP3_{G2}$	Gain setting = G_2 800 kHz tone separation		29		
G3 IIP3 change over temp	$IIP3_{G3TempDrift}$	Tcase -40C / +105C referenced to +25C		-0.8/+1.8		dB

NOTE 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
NOTE 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic
NOTE 4: Specification limits over voltage and temperature
NOTE 5: Max limit at Tcase = +105C

Table 10. IDTF1792 Specification (High Band) Continued (-1-)

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 2600MHz, F_{IF} = 199MHz, F_{LO} = 2401MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted. Gain Setting = G_5 (~ 5 dB gain).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output IP3	OIP3$_{G11}$	Gain setting = G_{11} 800 kHz tone separation		34.7		dBm
	OIP3$_{G8}$	Gain setting = G_8 800 kHz tone separation		35.4		
	OIP3$_{G5}$	Gain setting = G_5 800 kHz tone separation		32.5		dBm
		Gain setting = G_5 Tc = +105°C LO power = -3dBm Vcc = 3.15V	28.4	29.3		
		Gain setting = G_5 F_{IF} = 469MHz F_{LO} = 2130MHz		31.0		
	OIP3$_{G2}$	Gain setting = G_2 800 kHz tone separation		30.5		
Input P1dB	IP1dB$_{G11}$	Gain setting = G_{11}		8.3		dBm
	IP1dB$_{G8}$	Gain setting = G_8		10.8		
	IP1dB$_{G5}$ [4]	Gain setting = G_5	11.8	13.2		
		Gain setting = G_5 F_{IF} = 469MHz F_{LO} = 2130MHz		13.1		
	IP1dB$_{G2}$	Gain setting = G_2		14.6		
Maximum saturated output power	P_{sat}	P_{in} up to +20dBm		17		dBm
LO to IF leakage	ISO_{LI}			-40	-38	dBm
2LO to IF leakage	ISO_{LI2}			-44		dBm

NOTE 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
NOTE 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic
NOTE 4: Specification limits over voltage and temperature
NOTE 5: Max limit at Tcase = +105C

Table 11. IDTF1792 Specification (High Band) Continued (-2-)

Typical Application Circuit, V_{CC} = +3.3V, T_C = +25°C, F_{RF} = 2600MHz, F_{IF} = 199MHz, F_{LO} = 2401MHz, P_{LO} = 0 dBm, P_{IN} = -10dBm per tone for all gain settings unless otherwise stated, STBY = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted. Gain Setting = G_5 (~ 5 dB gain).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
3LO to IF leakage	ISO_{LI3}			-68		dBm
4LO to IF leakage	ISO_{LI4}			-71		dBm
RF to IF leakage	ISO_{RI}	RF output power compared to measured IF output power		-51	-30	dBc
LO to RF leakage	ISO_{LR}			-51		dBm
RF Return Loss	RL_{RF}	Single Ended 50 ohm		-17		dB

NOTE 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
NOTE 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
NOTE 3: JEDEC 3.3V and JEDEC 1.8V logic
NOTE 4: Specification limits over voltage and temperature
NOTE 5: Max limit at Tcase = +105C

Thermal Characteristics

Table 12. Package Thermal and Moisture Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Theta JA. Junction to ambient.	45[a]	°C/W
θ_{JC}	Theta JC. Junction to case.	2.1	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)	MSL 1	-

Typical Performance Characteristics

TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted, the following apply to the Typ Ops Graphs

- High Side Injection for RF frequencies below 1.2 GHz
- Low Side Injection for RF frequencies from 1.3 to 2.7 GHz
- 199MHz IF
- 800KHz Tone Spacing
- All measurements fully de-embedded for trace, connector, transformer losses
- Pin = -10dBm for Gain
- Pout = 0 dBm/Tone for IP3
- LO level = 0 dBm, VCC = 3.30 V
- Listed Temperatures are Case Temperature (TC = Case Temperature)
- Where noted, TA or TAMB = Ambient Temperature]

NxM (dBc, Gset=5 dB, LO=1700 MHz, IF=200 MHz, RFfund=0 dBm at 1900 MHz, RFspur(MHz)=(N*LO(MHz)+IF(MHz))/M)											
		N (LO)									
		1	2	3	4	5	6	7	8	9	10
M (RF)	1	0.0	37.7	22.0	64.3	39.4	73.3	52.4			
	2	54.3	69.5	53.7	64.2	50.4	57.0	61.3	71.8	62.1	88.7
	3	61.8	73.1	56.0	78.6	60	79.1	69.2	83.8	82.2	96.4
	4	68.0	88.8	94.4	91.5	97.2	96.7	87.7	94.1	87.1	98.7
	5	>99	>99	81.1	95.7	94.9	97.8	94.9	>99	86.6	97.3
	6	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	7	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	8	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	9	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	10	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99

NxM (dBc, Gset=5 dB, LO=1700 MHz, IF=200 MHz, RFfund=0 dBm at 1500 MHz, RFspur(MHz)=(N*LO(MHz)+IF(MHz))/M)											
		N (LO)									
		1	2	3	4	5	6	7	8	9	10
M (RF)	1	0.0	42.1	19.0	61.0	36.5	77.2	50.1			
	2	49.0	72.4	57.0	60.0	53.9	57.1	63.1	68.0	62.5	85.7
	3	69.8	78.6	51.5	75.9	62.1	75.3	66.0	84.5	76.2	91.4
	4	72.9	86.3	98.3	91.1	97.5	>99	88.2	95.8	93.2	>99
	5	>99	>99	85.2	96.9	86.7	>99	93.2	98.2	88.6	98.3
	6	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	7	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	8	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	9	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99
	10	>99	>99	>99	>99	>99	>99	>99	>99	>99	>99

TOCs (-1-) Fixed IF = 199 MHz – IIP3, OIP3, and Gain

Figure 3. IIP3 vs. Temperature and Gain Setting

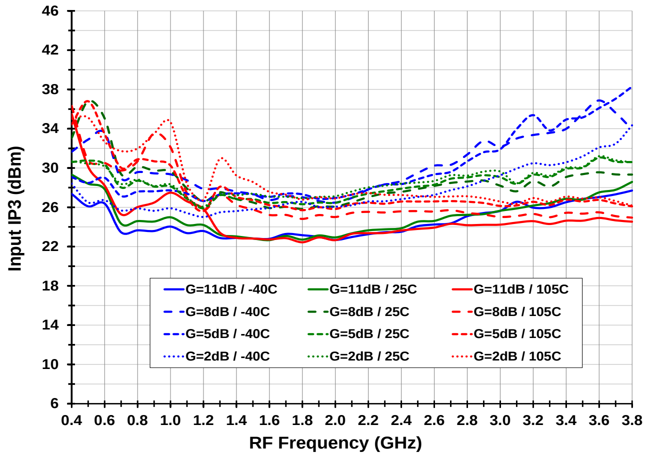


Figure 4. OIP3 vs. Temperature and Gain Setting

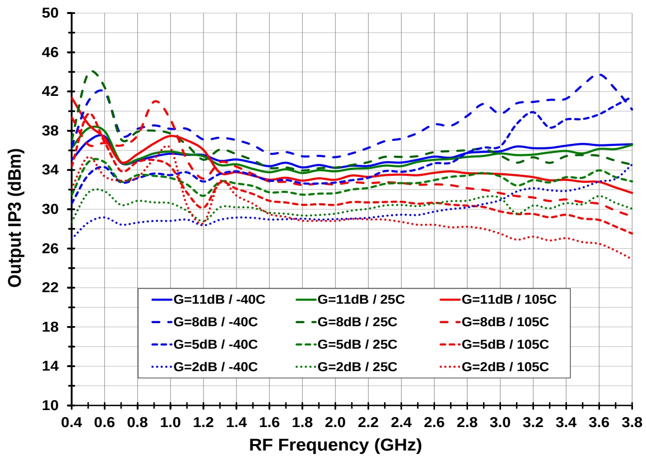


Figure 5. Gain vs. Temperature and Gain Setting

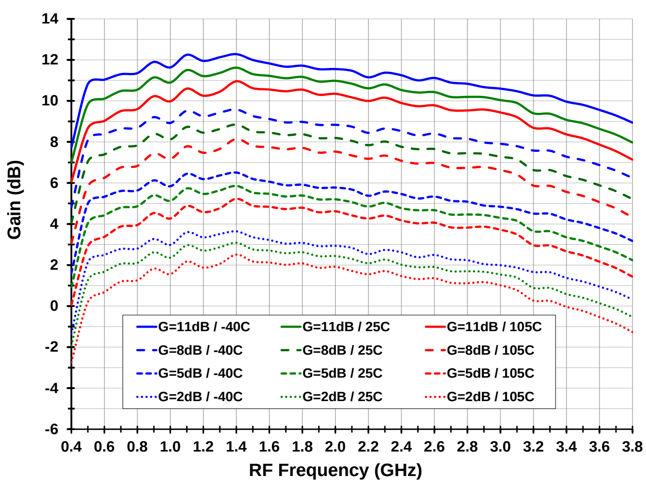


Figure 6. IIP3 vs. LO Power and Gain Setting (Vcc = 3.15, Tcase = 105C)

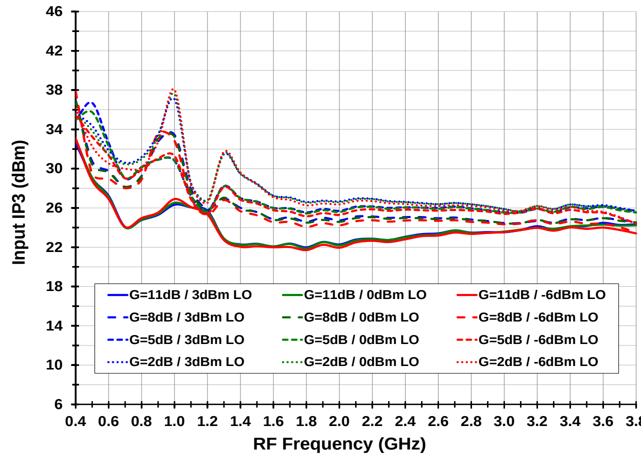


Figure 7. OIP3 vs. LO Power and Gain Setting (Vcc = 3.15, Tcase = 105C)

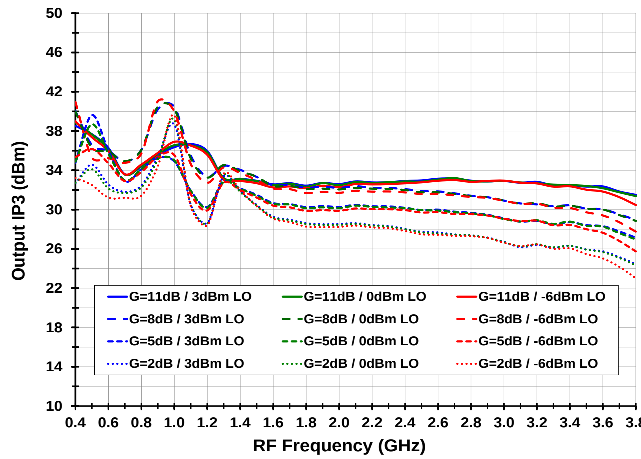
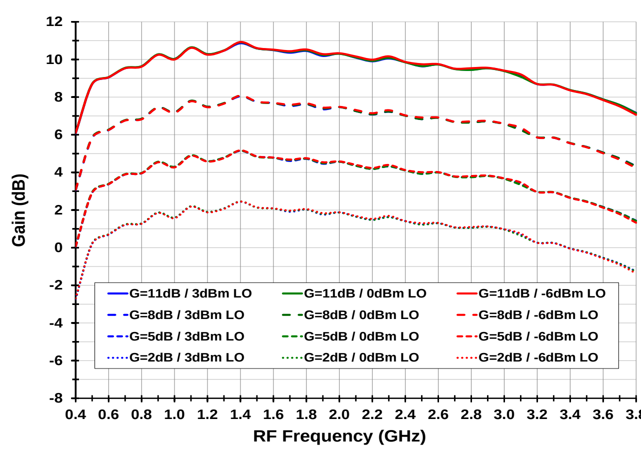


Figure 8. Gain vs. LO Power and Gain Setting (Vcc = 3.15, Tcase = 105C)



TOCs (-2-) Fixed IF = 199 MHz – P1dB

Figure 9. Input P1dB vs. Temperature and Gain Setting

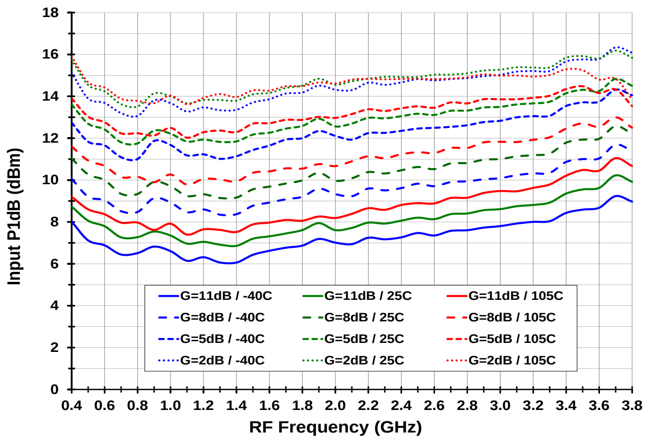
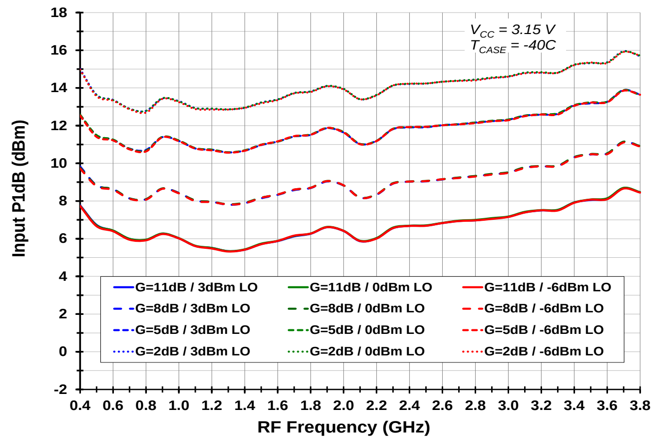


Figure 10. Input P1dB vs. LO Level and Gain Setting (Vcc = 3.15, Tcase = -40C)



TOCs (-3-) Fixed IF=199 MHz – Power Consumption, LO to IF Leakage, and RF to IF

Figure 11. Power Consumption vs. Temperature and Gain Setting

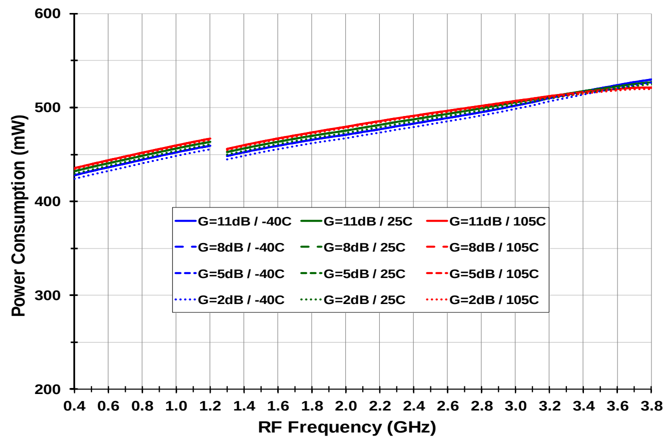


Figure 14. LO to IF Leakage vs. Temperature and Gain Setting

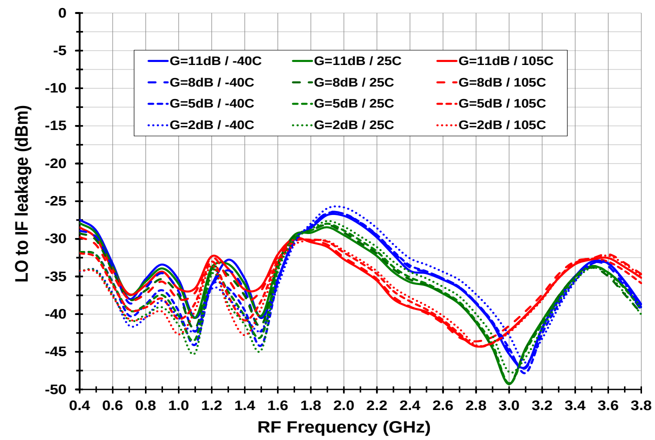


Figure 12. Power Consumption vs. Temperature and Gain Setting (Vcc = 3.15, Tcase = 105C)

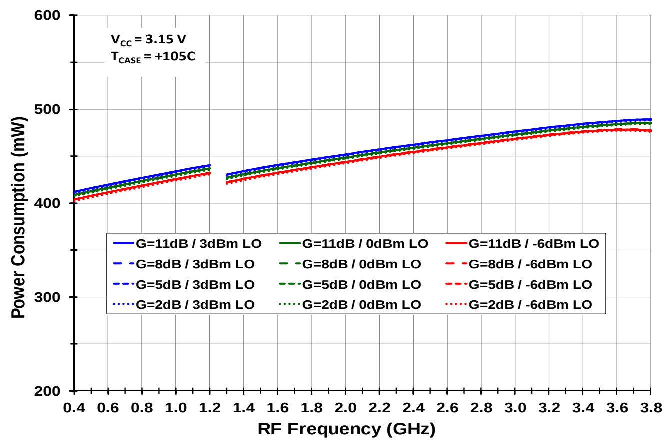


Figure 15. RF to IF Leakage vs. Temperature and Gain Setting

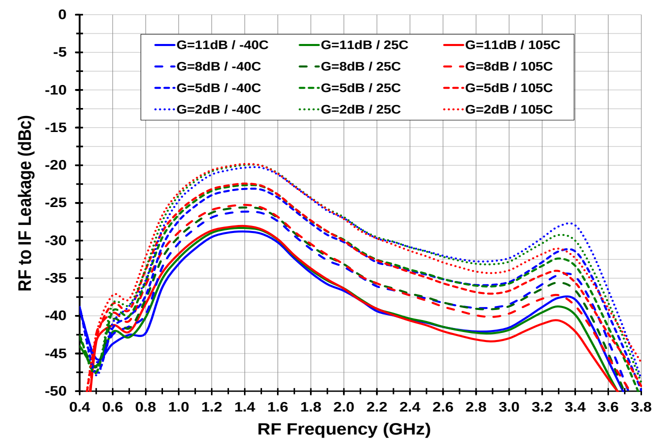
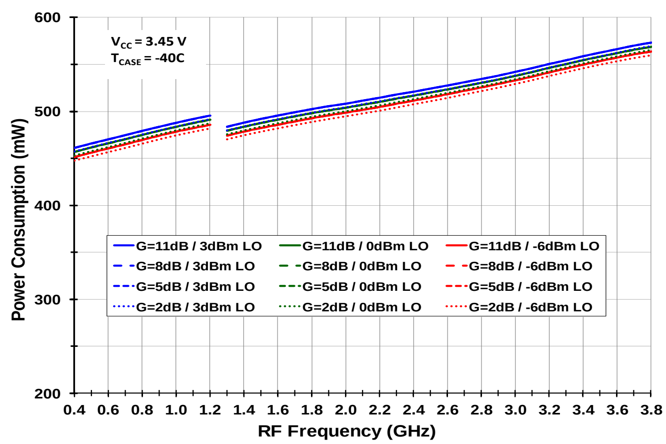


Figure 13. Power Consumption vs. Temperature and Gain Setting (Vcc = 3.45, Tcase = -40C)



TOCs (-4-) Fixed IF=199 MHz – Output IP2, Noise Figure

Figure 16. Output IP2 vs. Temperature and Gain Setting

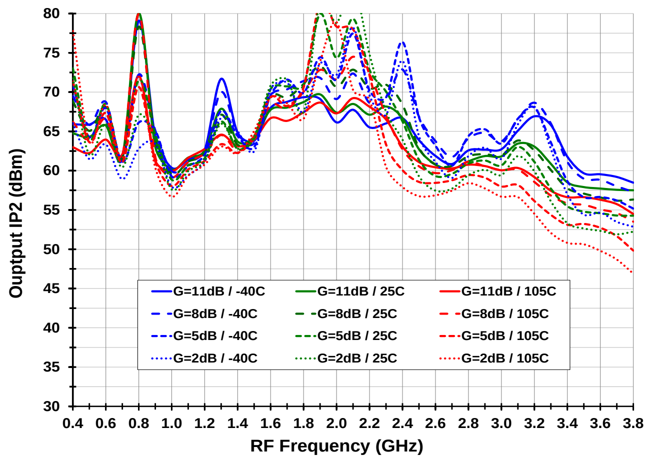


Figure 18. Output IP2 vs. Temperature and Gain Setting (Vcc = 3.15, Tcase = 105C)

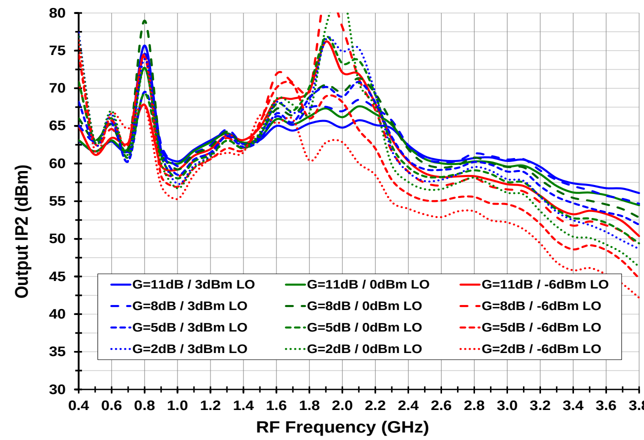


Figure 17. Noise Figure vs. Temperature and Gain Setting

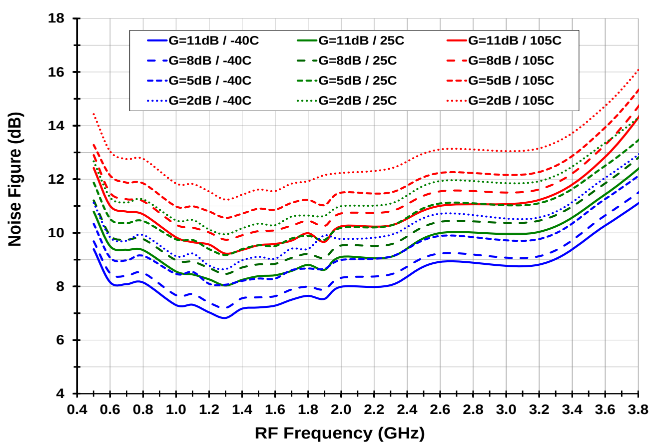
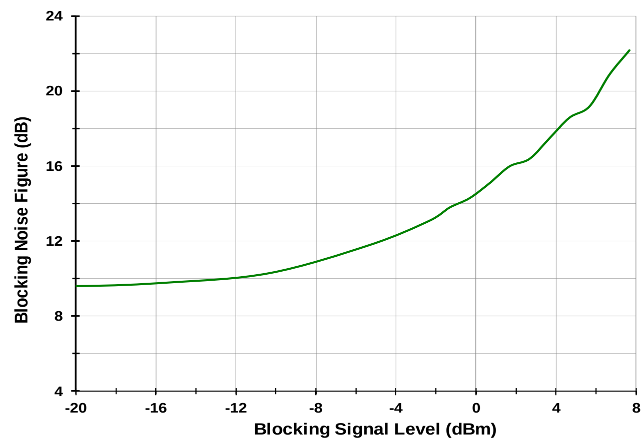


Figure 19. Blocking Noise Figure (Max Gain, LO=1700MHz, RF=1899MHz, Blocker=1999MHz, 25C ambient)



TOCs (-5-) Fixed LO = 1.1 GHz, 1.7 GHz, 2.25 GHz, 3.13 GHz – Input IP3

Figure 20. Input IP3 vs. Temperature and Gain Setting (LO=1.1 Ghz)

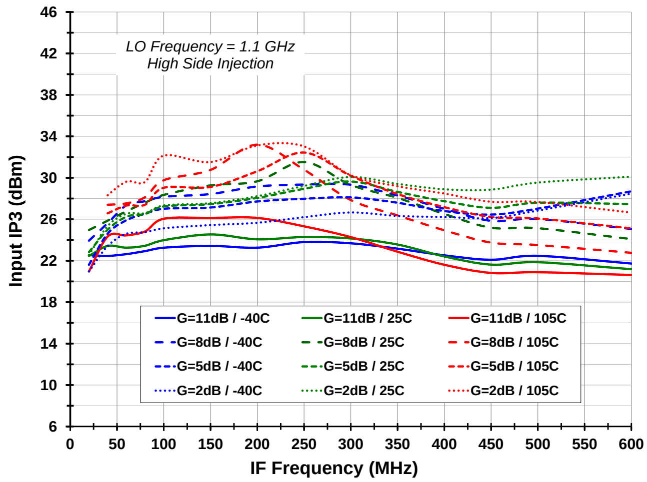


Figure 22. Input IP3 vs. Temperature and Gain Setting (LO=2.25 Ghz)

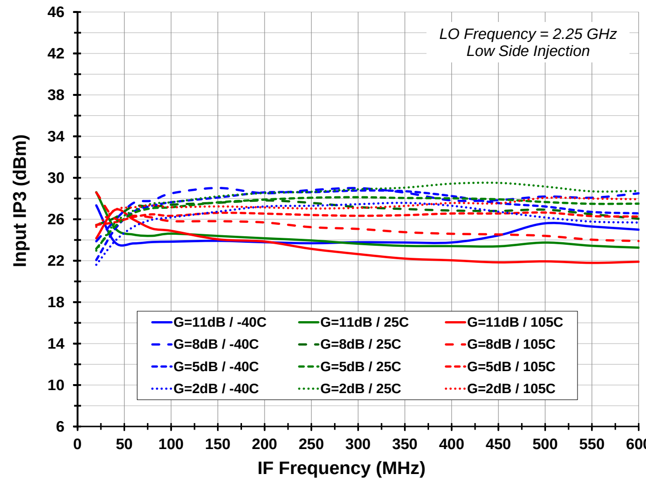


Figure 21. Input IP3 vs. Temperature and Gain Setting (LO=1.7 Ghz)

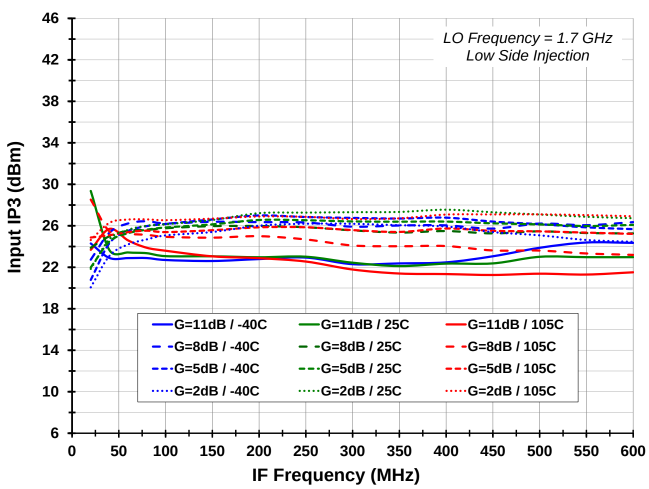
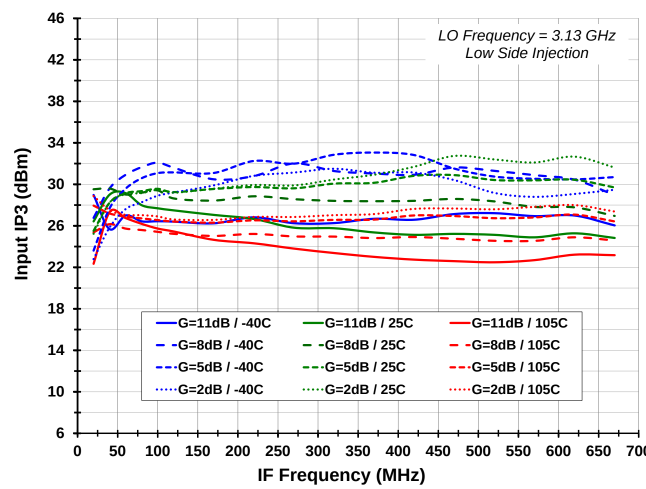


Figure 23. Input IP3 vs. Temperature and Gain Setting (LO=3.13 Ghz)



TOCs (-6-) Fixed LO = 1.1 GHz, 1.7 GHz, 2.25 GHz, 3.13 GHz – Output IP3

Figure 24. Output IP3 vs. Temperature and Gain Setting (LO=1.1 Ghz)

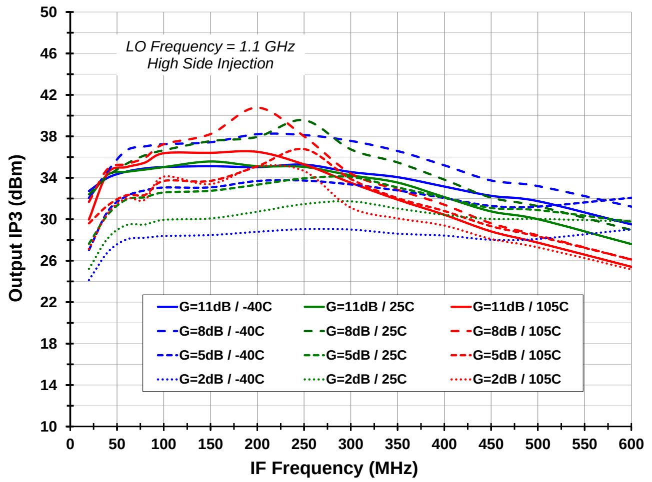


Figure 26. Output IP3 vs. Temperature and Gain Setting (LO=2.25 Ghz)

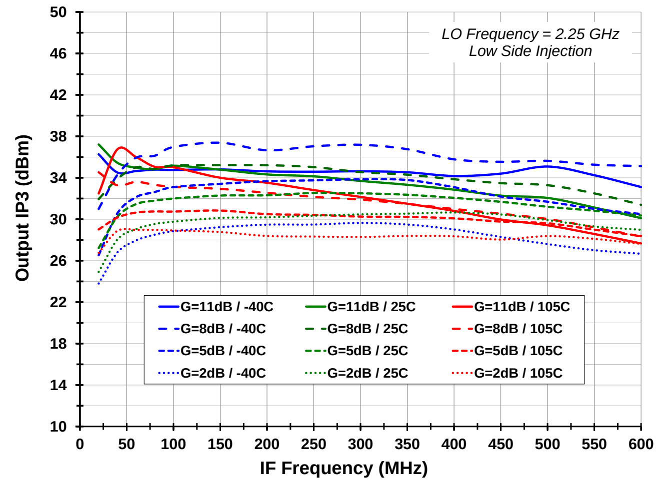


Figure 25. Output IP3 vs. Temperature and Gain Setting (LO=1.7 Ghz)

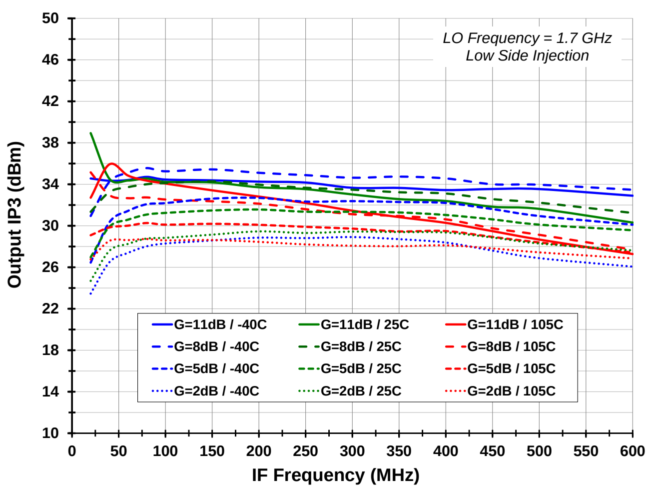
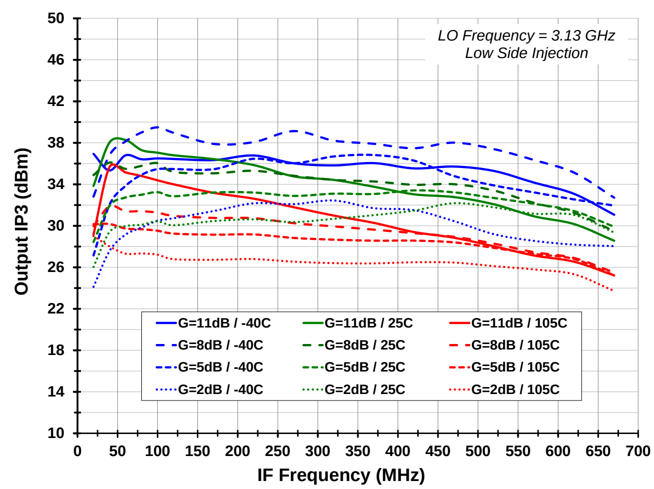


Figure 27. Output IP3 vs. Temperature and Gain Setting (LO=3.13 Ghz)



TOCs (-7-) Fixed LO = 1.1 GHz, 1.7 GHz, 2.25 GHz, 3.13 GHz – Gain

Figure 28. Gain vs. Temperature and Gain Setting (LO=1.1 Ghz)

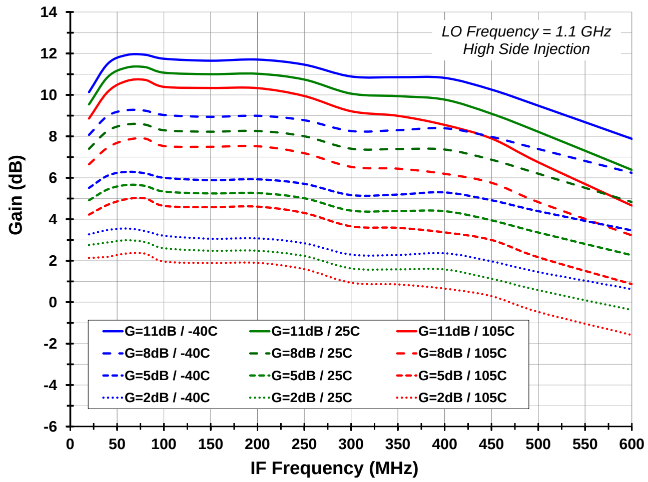


Figure 30. Gain vs. Temperature and Gain Setting (LO=2.25 Ghz)

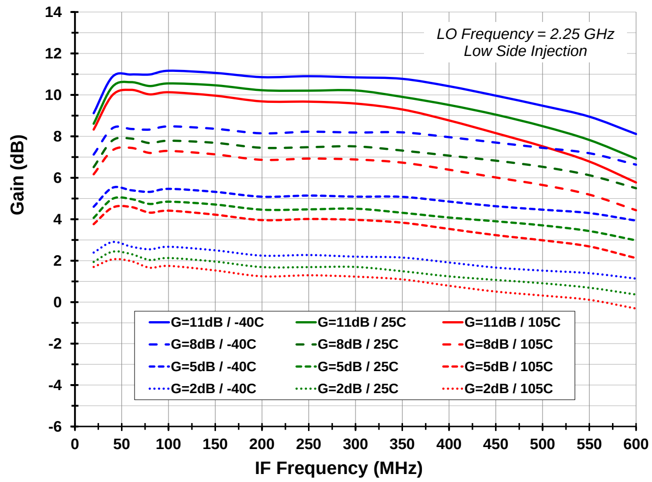


Figure 29. Gain vs. Temperature and Gain Setting (LO=1.7 Ghz)

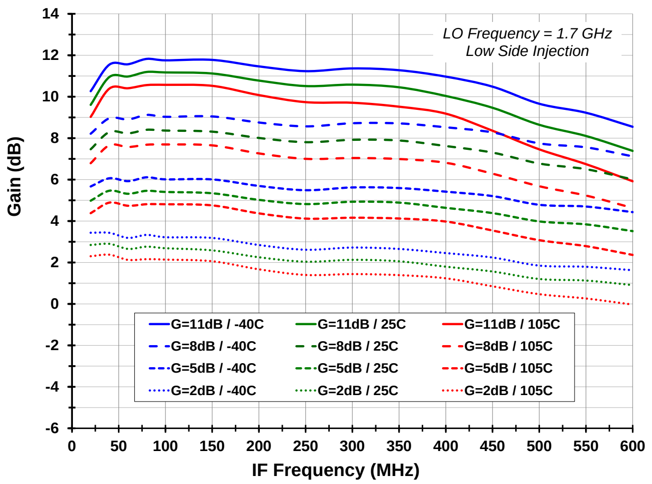
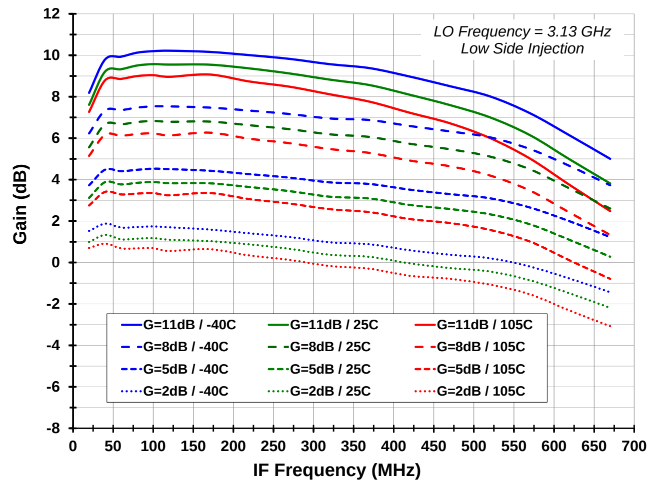


Figure 31. Gain vs. Temperature and Gain Setting (LO=3.13 Ghz)



TOCs (-8-) Fixed LO = 1.1 GHz, 1.7 GHz, 2.25 GHz, 3.13 GHz – Input P1dB

Figure 32. Input P1dB vs. Temperature and Gain Setting (LO=1.1 Ghz)

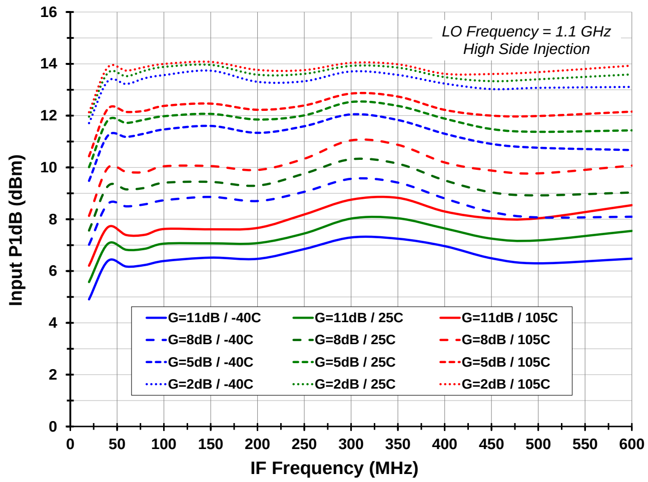


Figure 34. Input P1dB vs. Temperature and Gain Setting (LO=2.25 Ghz)

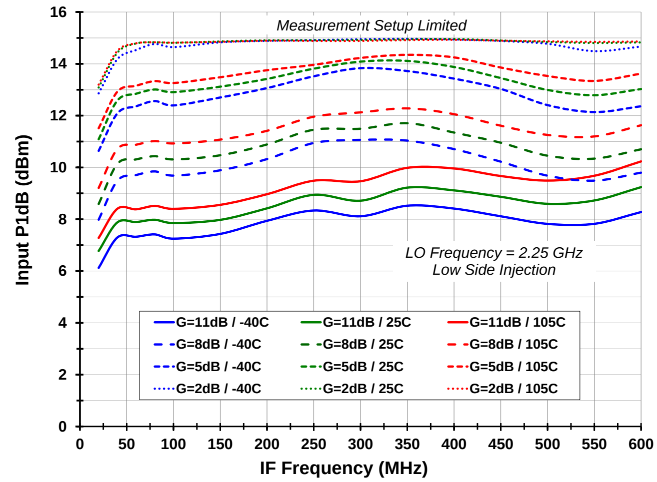


Figure 33. Input P1dB vs. Temperature and Gain Setting (LO=1.7 Ghz)

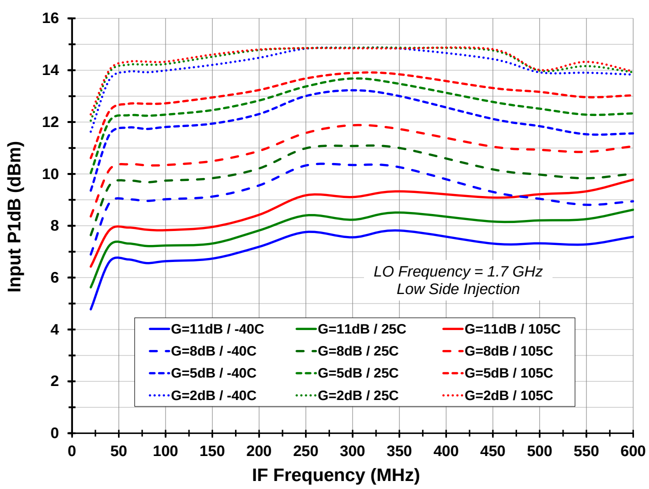
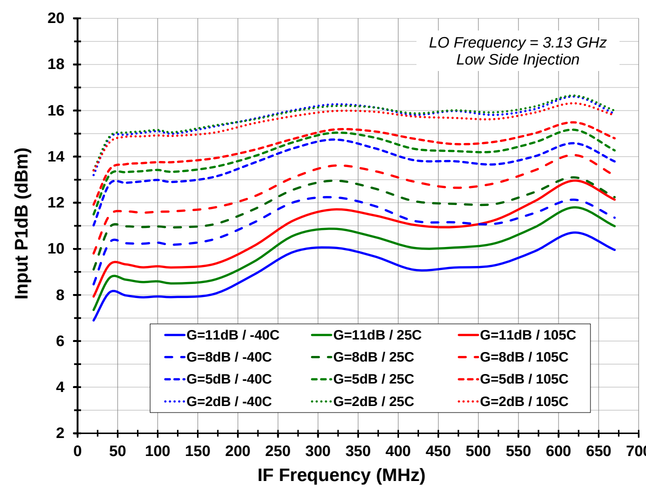


Figure 35. Input P1dB vs. Temperature and Gain Setting (LO=3.13 Ghz)



TOCs (-9-) Fixed LO=1.1GHz, 1.7GHz, 2.25GHz, 3.13GHz – Output IP2

Figure 36. Output IP2 vs. Temperature and Gain Setting (LO=1.1 Ghz)

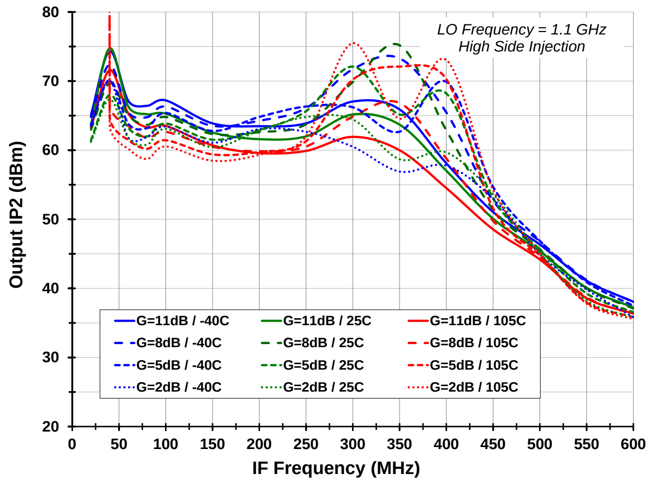


Figure 37. Output IP2 vs. Temperature and Gain Setting (LO=1.7 Ghz)

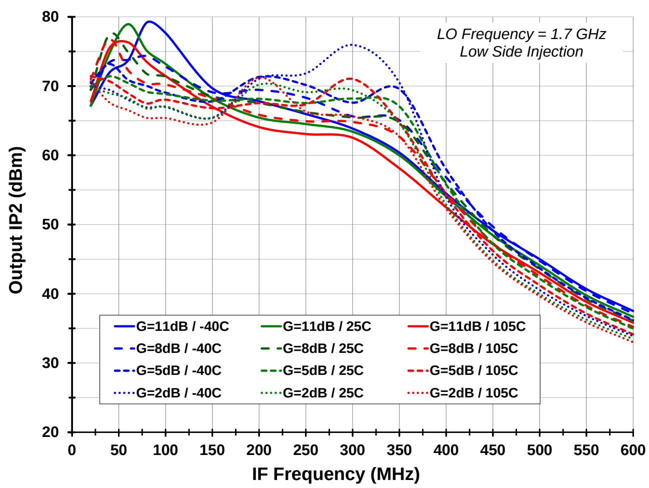


Figure 38. Output IP2 vs. Temperature and Gain Setting (LO=2.25 Ghz)

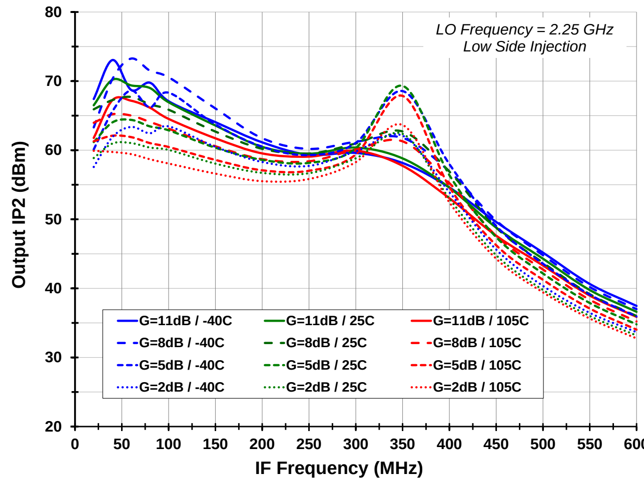
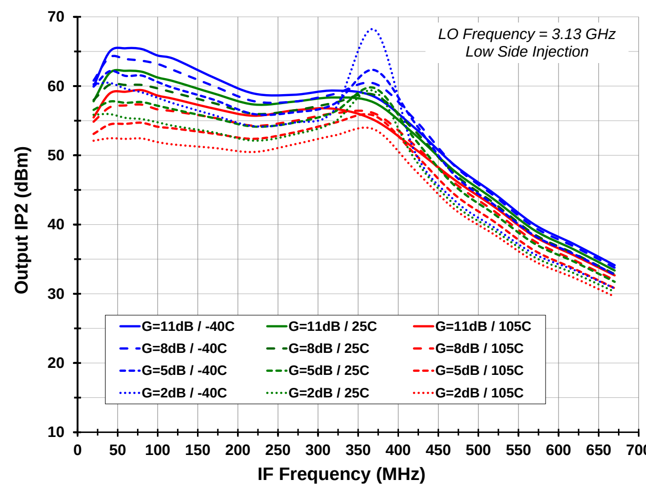


Figure 39. Output IP2 vs. Temperature and Gain Setting (LO=3.13 Ghz)



TOCs (-10-) Return Losses, Evaluation Kit Losses, STBY Settling Time

Figure 40. IF Port Return Loss vs. Gain Setting

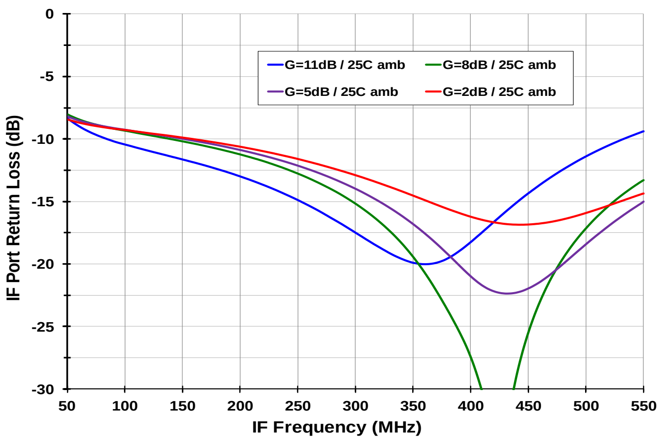


Figure 41. RF Port Return Loss vs. LO Frequency

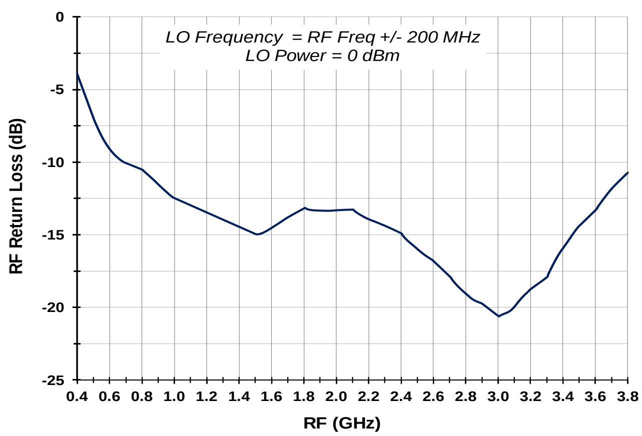


Figure 42. LO Port Return Loss vs. LO Power Level

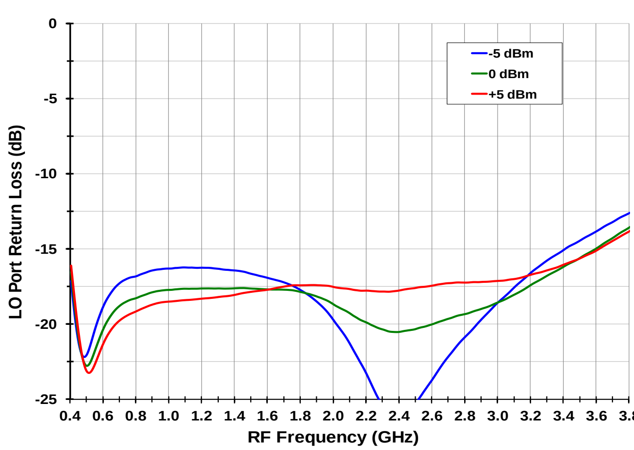


Figure 43. Evaluation Kit IF Transformer Loss vs. Temperature

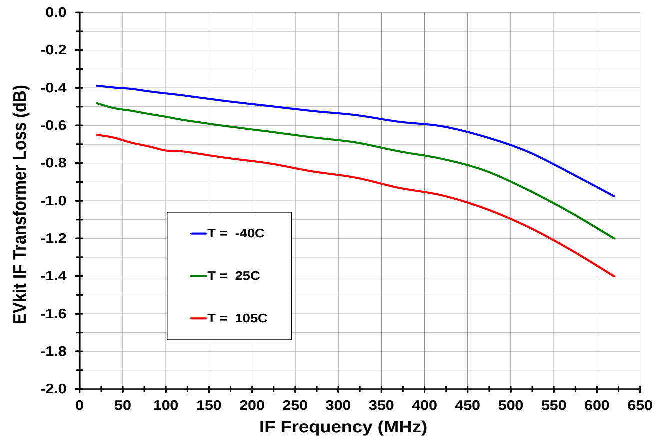


Figure 44. Evaluation Kit RF Trace Loss vs. Temperature

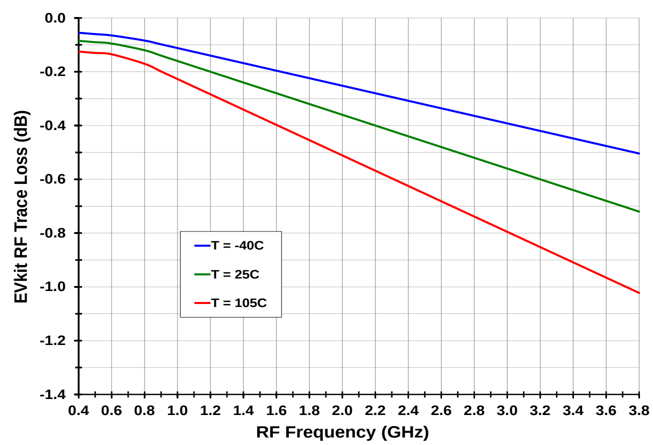
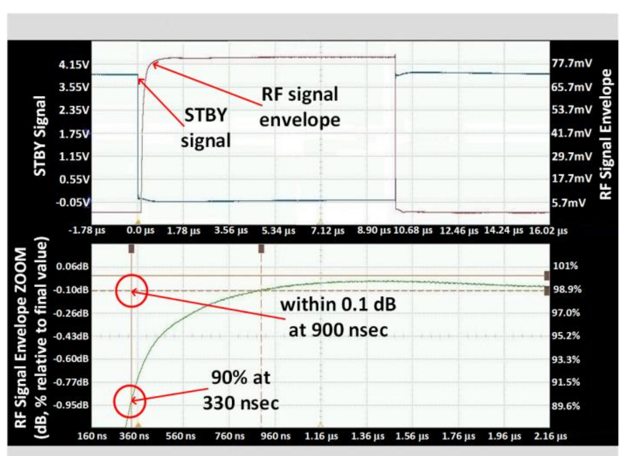


Figure 45. STBY Settling Time



TOCs (-11-) Gain Settling Time

Figure 46. Gain Settling Time for 11 dB to 8 dB Gain Setting

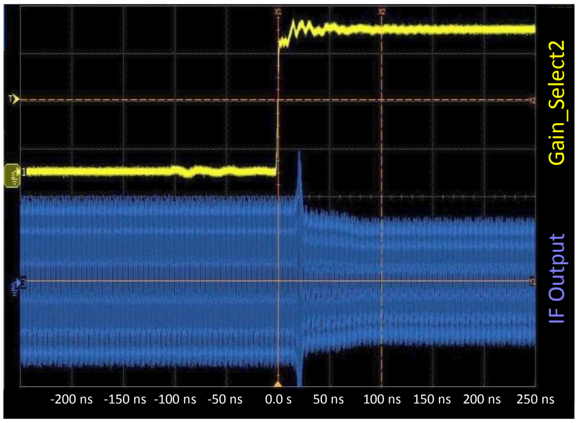


Figure 47. Gain Settling Time for 8 dB to 11 dB Gain Setting

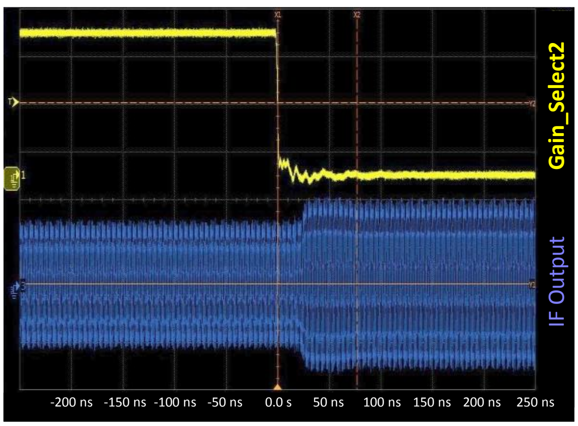


Figure 48. Gain Settling Time for 8 dB to 5 dB Gain Setting

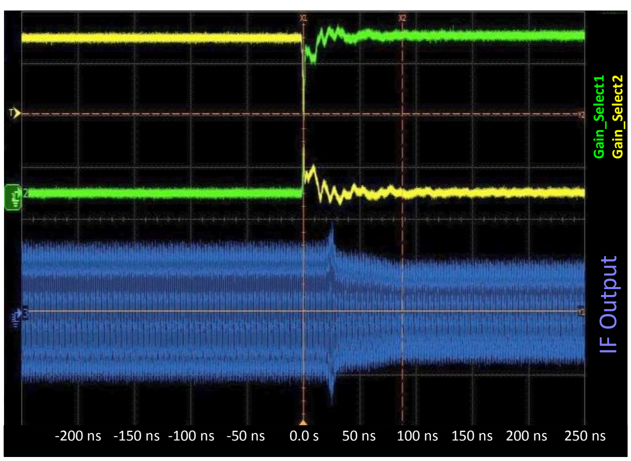


Figure 49. Gain Settling Time for 5 dB to 8 dB Gain Setting

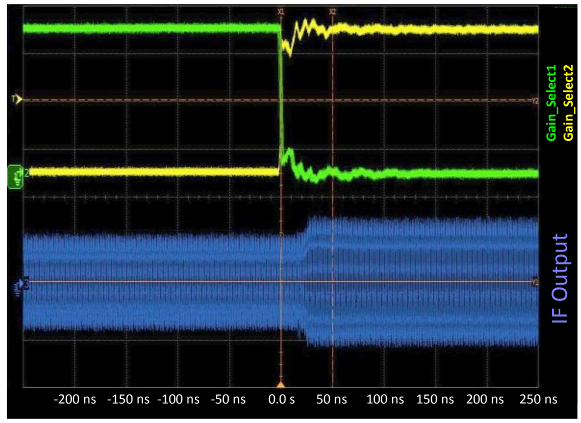


Figure 50. Gain Settling Time for 5 dB to 2 dB Gain Setting

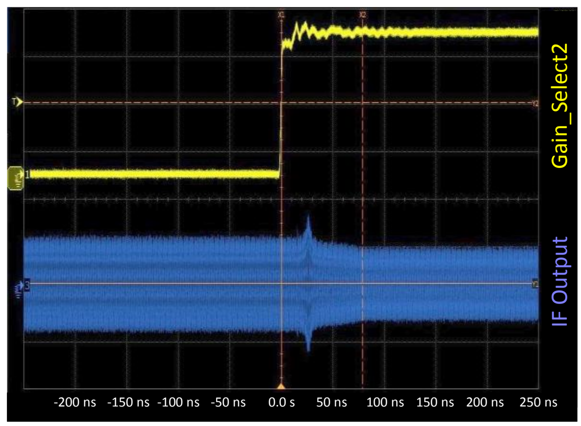
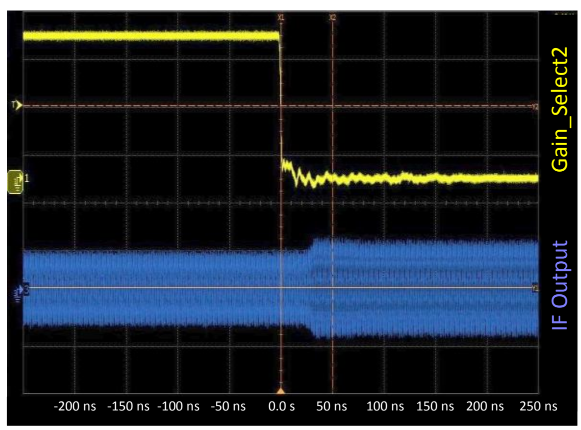
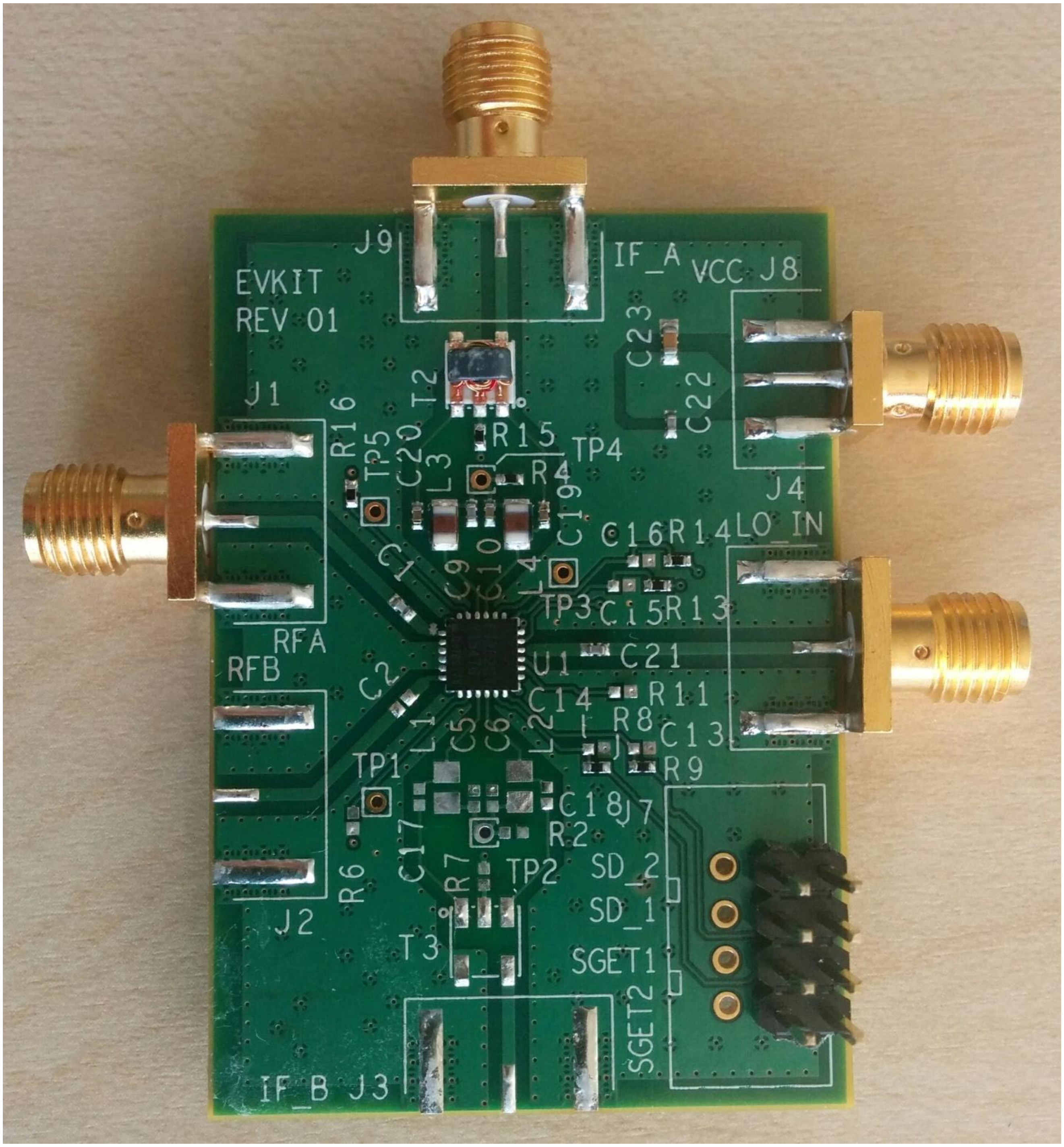


Figure 51. Gain Settling Time for 2 dB to 5 dB Gain Setting

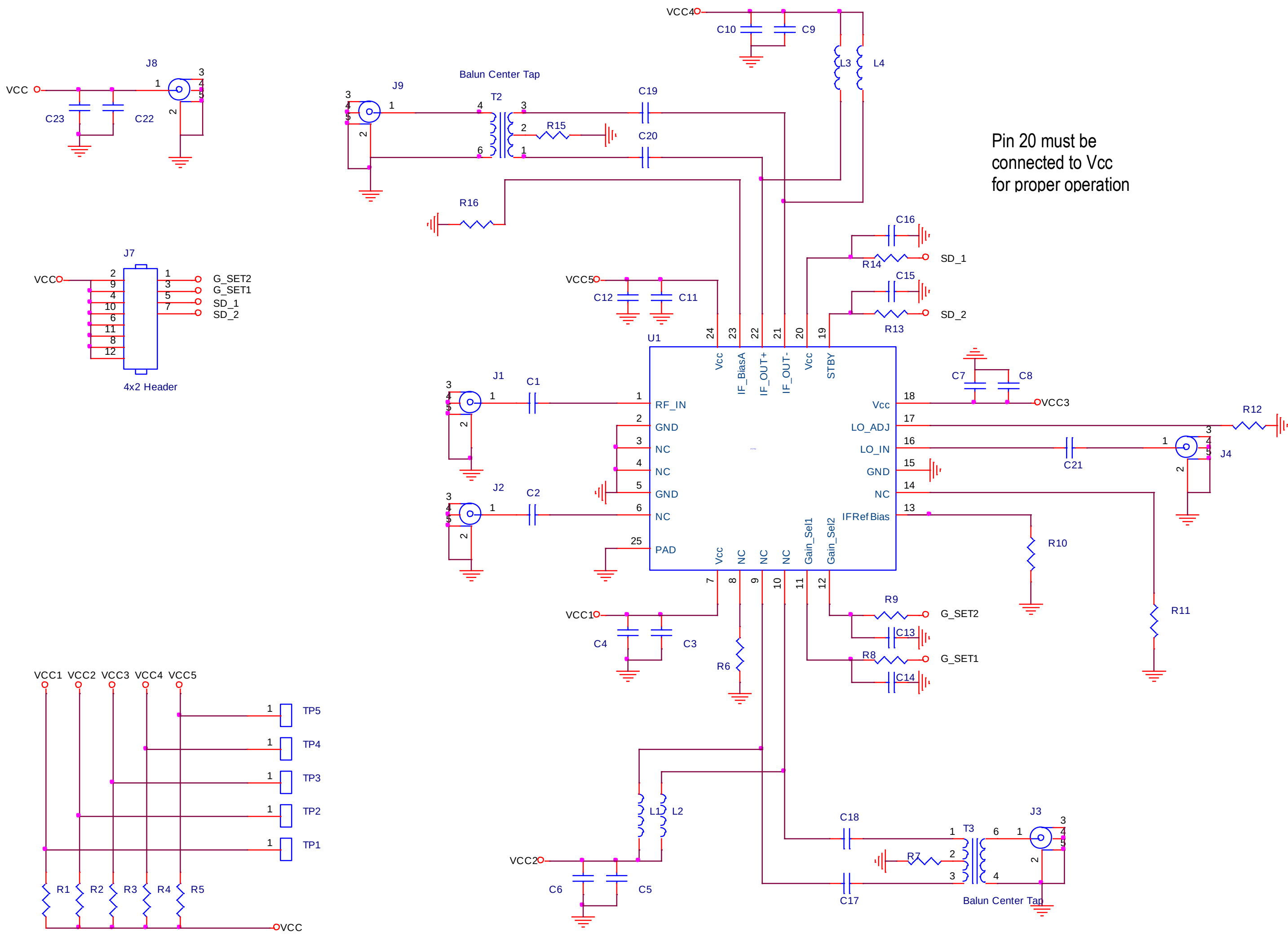


Applications Information

EvKit Picture



EvKit / Applications Circuit



EvKit BOM

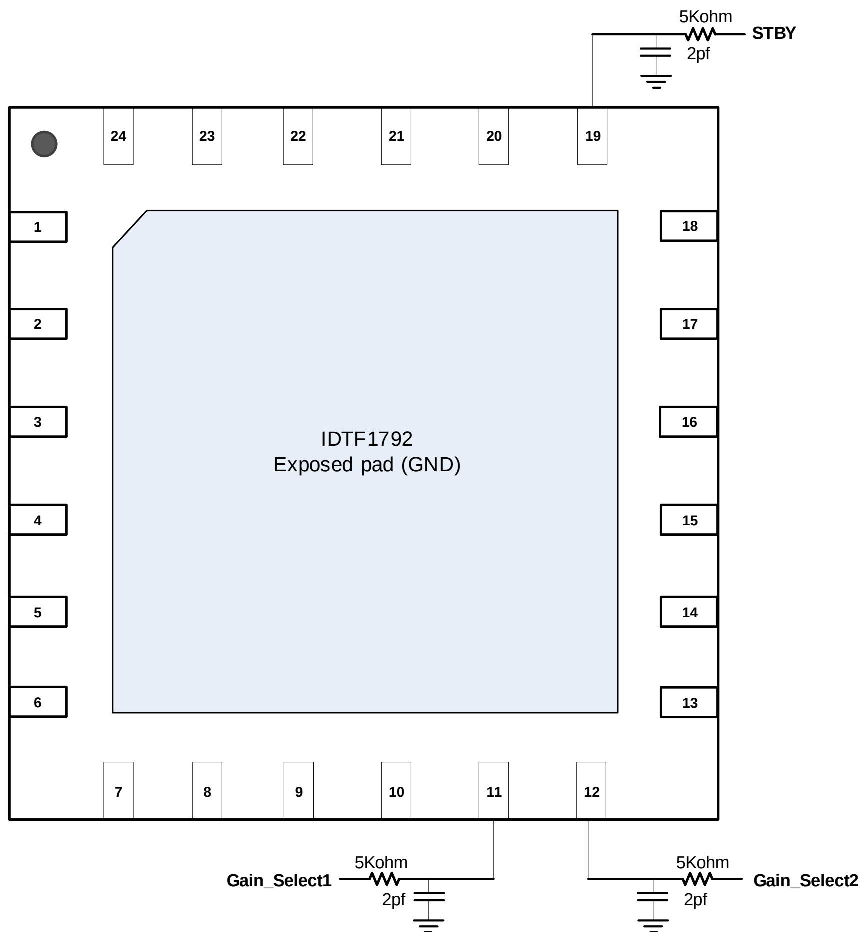
Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C3, C7, C9, C11, C22	6	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C4, C8, C10, C12, C19, C20, C23	10	10,000pF ±10%, 50V, X7R Ceramic Capacitor (0603)	GRM188R71H103KA01D	Murata
C21	1	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C1,	2	39pF ±5%. 5V, C0G Ceramic Capacitor (0402)	GRM1555C1H390J	Murata
R1, R3-R5, R8, R9, R12, R13, R14, R15	13	0 Ohm, 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
R16	2	390 Ohm ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3900X	Panasonic
R10	1	1.74 kOhm ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1741X	Panasonic
L3, L4	4	390nH ±5%, 0.29 A, Ceramic Chip Inductor (0805)	0805CS-391XJL	Coilcraft
T2	2	4:1 Center Tap Balun	TC4-6TG2+	Mini-Circuits
J7	1	CONN HEADER VERT DBL 4POS GOLD	67997-108HLF	FCI
J1, J4, J9	3	Edge Launch SMA Connector (Big)	142-0701-851	Emerson Johnson
J8	1	Edge Launch SMA Connector (Small)	142-0711-821	Emerson Johnson
U1	1	RF Dual Wideband Gain-Settable Downconverting Mixer 4x4 TQFN24	F1192NLGI	IDT
	1	Printed Circuit Board	F1192 EVKIT REV 01	IDT

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., provisions for an R-C circuit at the input of each control pin is recommended. This applies to pins 11, 12, and 19 as shown below.



Gain Select

F1192 provides a gain select feature requiring 2 pins for logic control. The following table summarizes the required pin logic to achieve the desired gain setting. Internal pull down resistors are included requiring no control to set both channels to maximum gain.

Desired Power Gain (dB)	Gain Select1 (Pin 11) #	Gain Select2 (Pin 12)
11	0	0
8	0	1
5	1	0
2	1	1

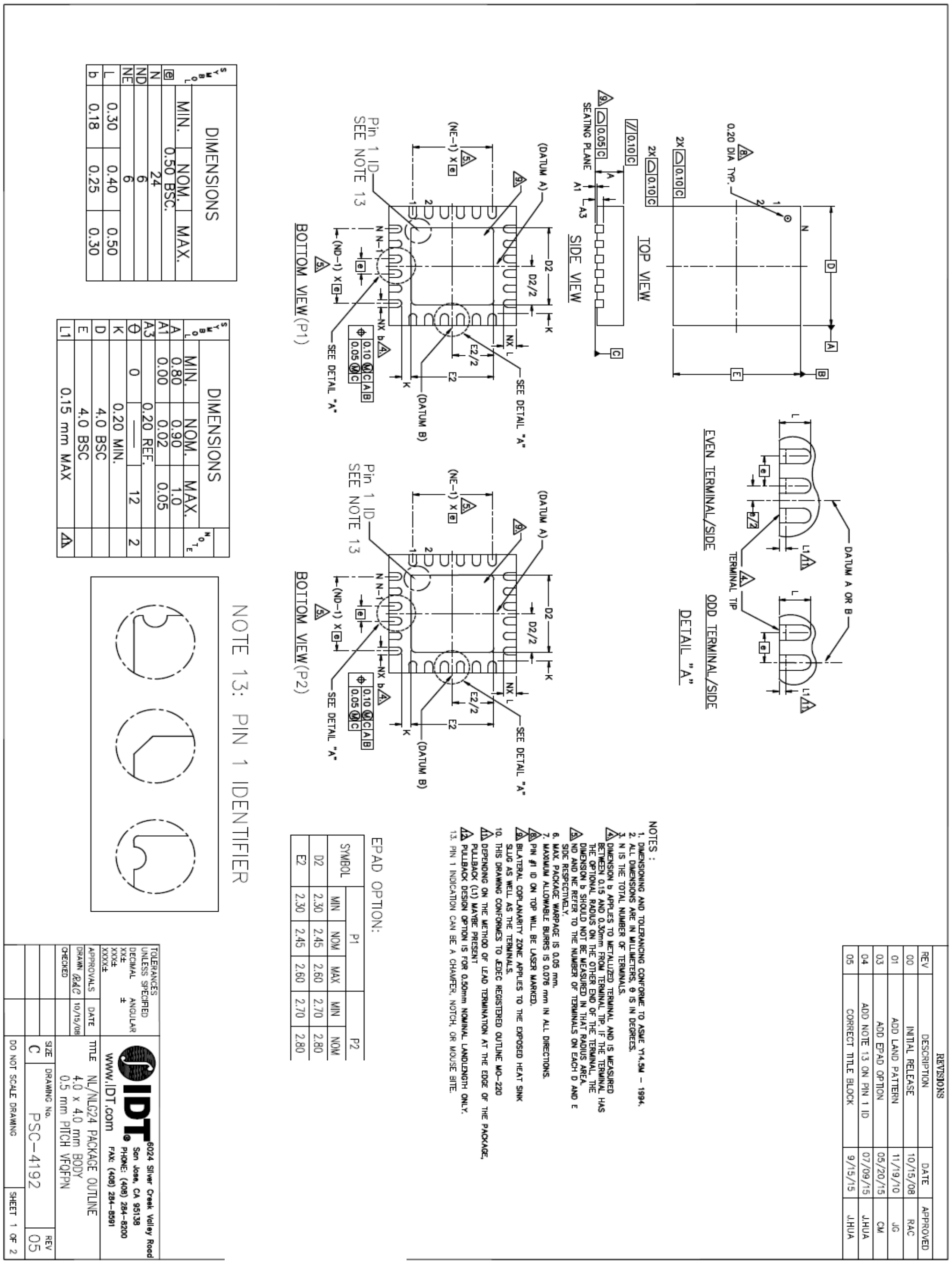
Default Start-up

Upon start-up, the device gain will be whatever the gain select pins are set for as defined in the table above.

Package Drawings

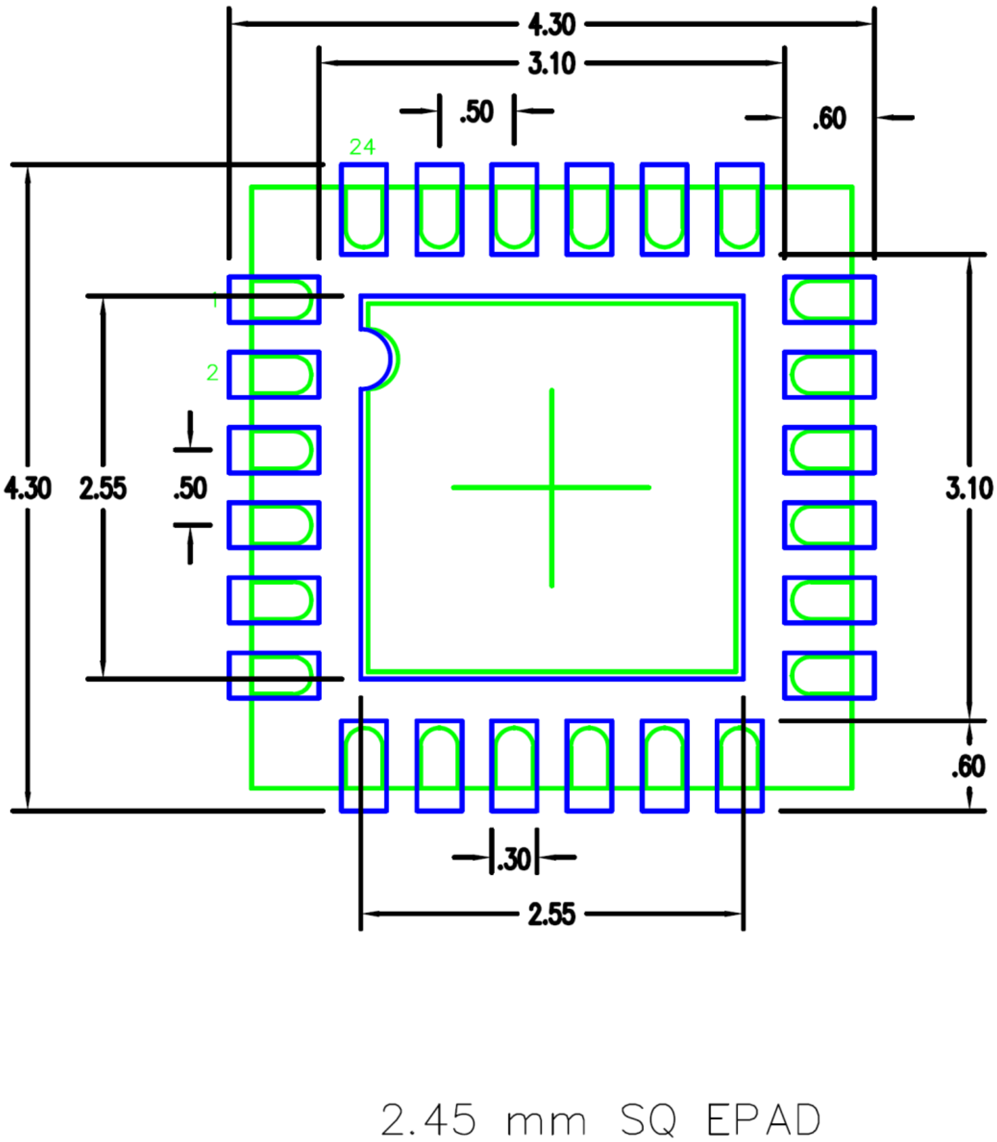
(4mm x 4mm 24-pin TQFN) with EPAD Option P1

Figure 52. Package Outline Drawing



Recommended Land Pattern

Figure 53. Recommended Land Pattern

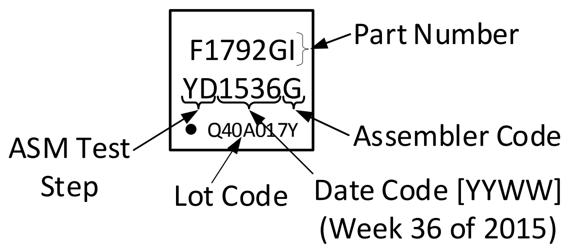


NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F1792NLGI	4 x 4 x 0.9 mm-QFN	MSL1	Tray	-40° to +85°C
F1792NLGI8	4 x 4 x 0.9 mm-QFN	MSL1	Tape and Reel	-40° to +85°C

Marking Diagram



Revision History

Revision Date	Description of Change
April 5, 2016	First release (Rev O) of the F1792 datasheet.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А