



PSMN3R0-60ES

N-channel 60 V 3.0 mΩ standard level MOSFET in I2PAK.

3 June 2014

Product data sheet

1. General description

Standard level N-channel MOSFET in a I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

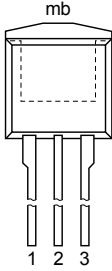
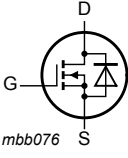
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	-	60	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2	[1]	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	306	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 ; Fig. 12		-	2.4	3	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 80\text{ A}$; $V_{DS} = 12\text{ V}$; Fig. 13 ; Fig. 14		-	28	-	nC

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 I2PAK (SOT226)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R0-60ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R0-60ES	PSMN3R0-60ES

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	60	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	306	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	83.4	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	824	A
T_{stg}	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	824	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 60\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped		-	800	mJ

[1] Continuous current is limited by package.

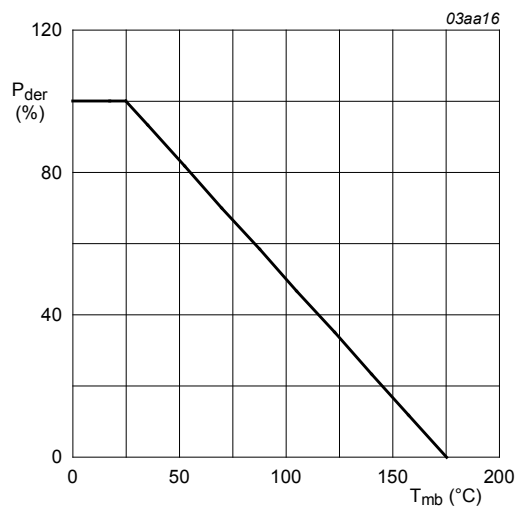


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

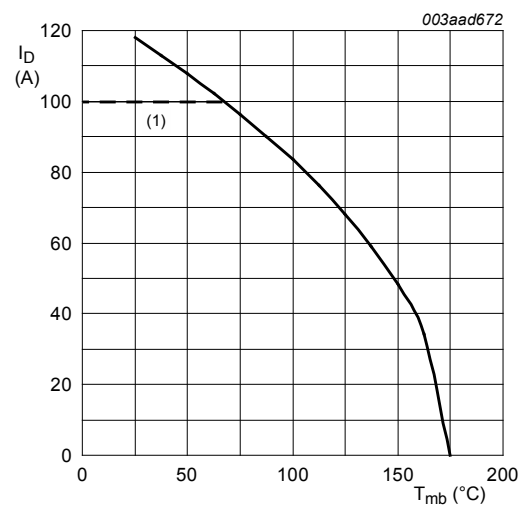


Fig. 2. Continuous drain current as a function of mounting base temperature.

$V_{GS} \geq 10\text{ V}$; (1) Capped at 100 A due to package

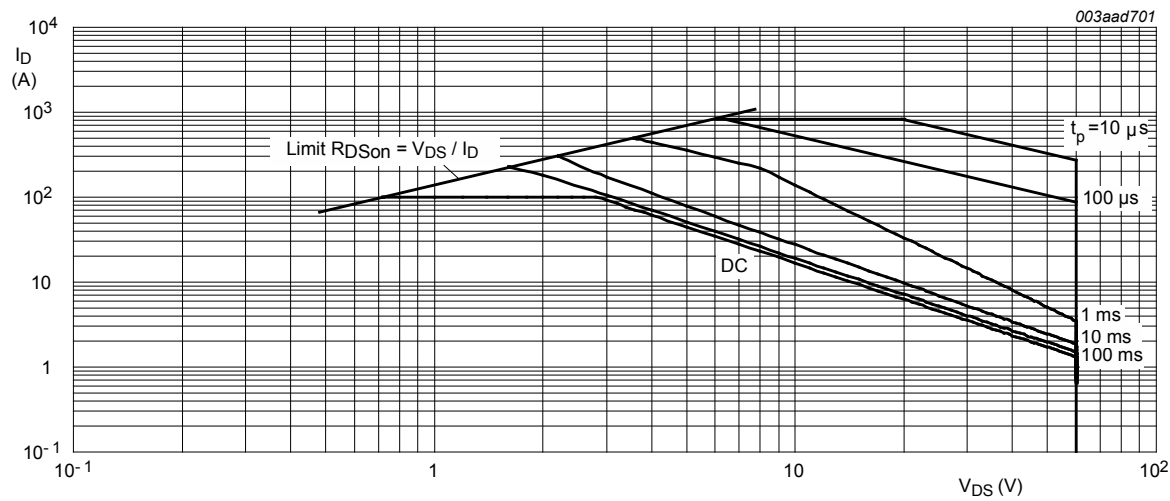


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25\text{ }^{\circ}\text{C}$; I_{DM} is a single pulse; Capped at 100 A due to package

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.3	0.49	K/W

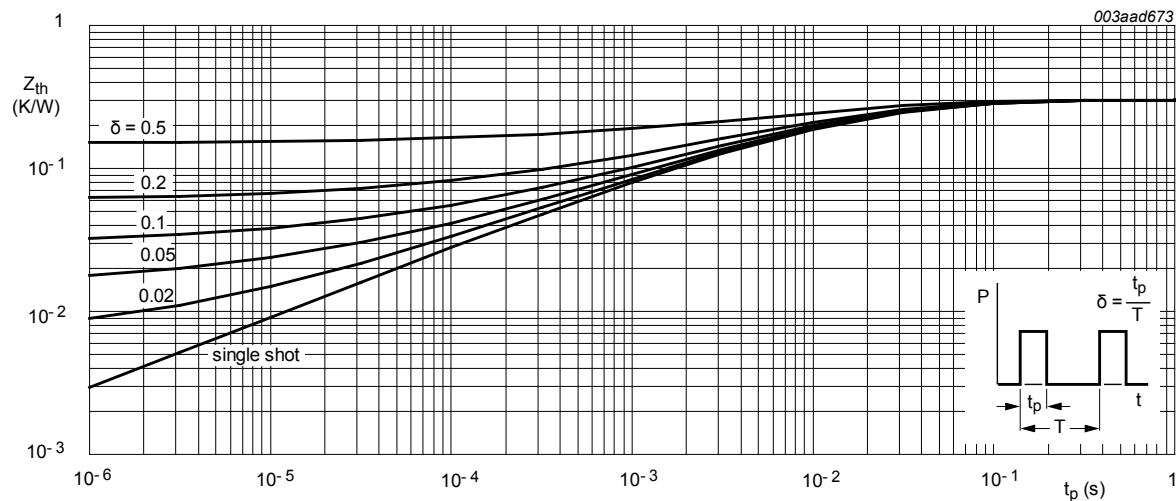


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -55 ^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = 25 ^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 25 ^\circ C$; Fig. 8 ; Fig. 9	2	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 175 ^\circ C$; Fig. 9	1	-	-	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_J = -55 ^\circ C$; Fig. 9	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_J = 25 ^\circ C$	-	0.05	10	μA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_J = 175 ^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_J = 175 ^\circ C$; Fig. 10	-	-	7.2	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_J = 25 ^\circ C$; Fig. 11 ; Fig. 12	-	2.4	3	mΩ
R_G	gate resistance	$f = 1 MHz$	0.55	1.1	2.2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 80 A; V_{DS} = 12 V; V_{GS} = 10 V$; Fig. 13 ; Fig. 14	-	130	-	nC
Q_{GS}	gate-source charge	$I_D = 80 A; V_{DS} = 12 V; V_{GS} = 10 V$; Fig. 14 ; Fig. 13	-	43	-	nC
Q_{GD}	gate-drain charge	$I_D = 80 A; V_{DS} = 12 V; V_{GS} = 10 V$; Fig. 13 ; Fig. 14	-	28	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz$; $T_J = 25 ^\circ C$; Fig. 15 ; Fig. 16	-	8079	-	pF
C_{oss}	output capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz$; $T_J = 25 ^\circ C$; Fig. 15	-	971	-	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz$; $T_J = 25 ^\circ C$; Fig. 15 ; Fig. 16	-	492	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; R_L = 0.5 \Omega; V_{GS} = 10 V$; $R_{G(ext)} = 1.5 \Omega$	-	31	-	ns
t_r	rise time		-	26	-	ns
$t_{d(off)}$	turn-off delay time		-	77	-	ns
t_f	fall time		-	22	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 17	-	0.88	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	54	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$	-	97	-	nC

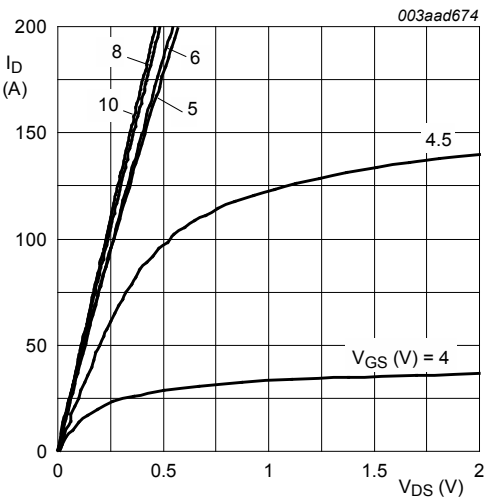


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ °C}$

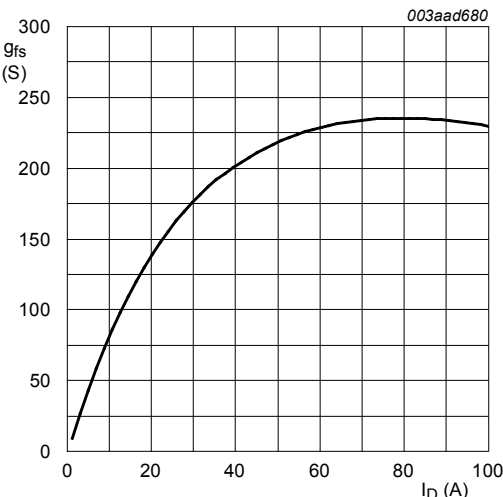


Fig. 6. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ °C}$; $V_{DS} = 30\text{ V}$

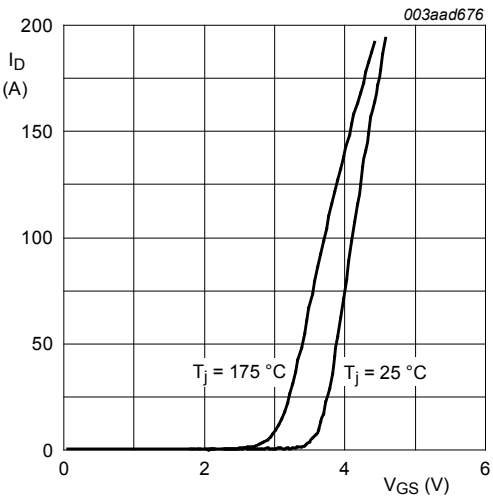


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

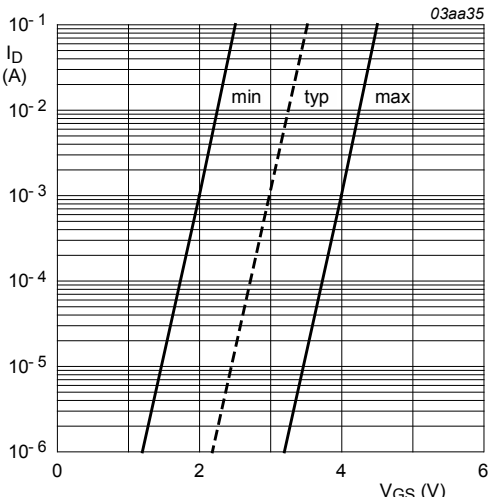


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ °C}$; $V_{DS} = 5\text{ V}$

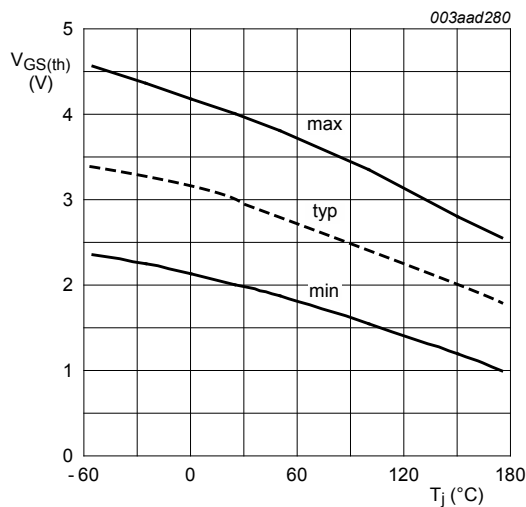


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

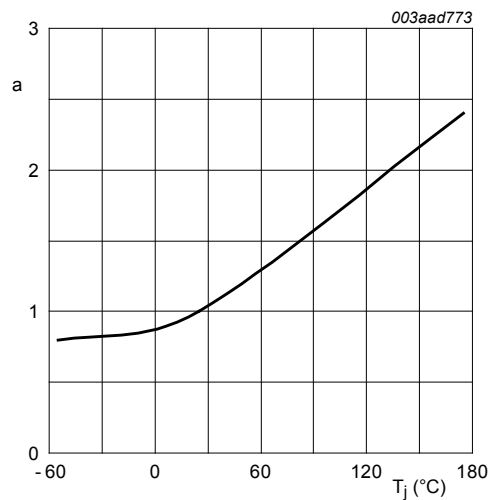


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

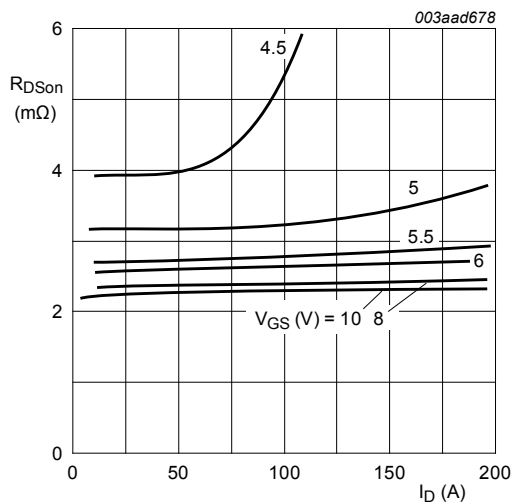


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

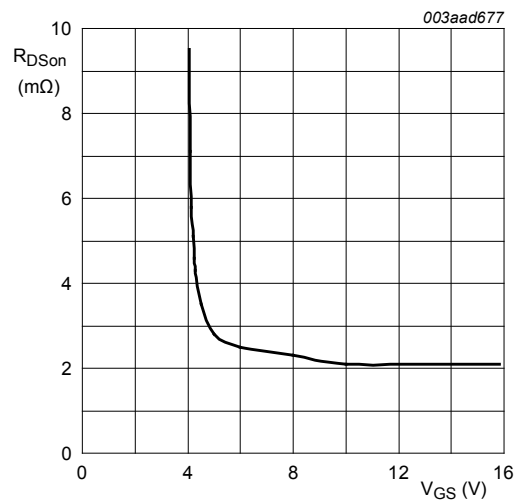


Fig. 12. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^\circ\text{C}; I_D = 25 \text{ A}$$

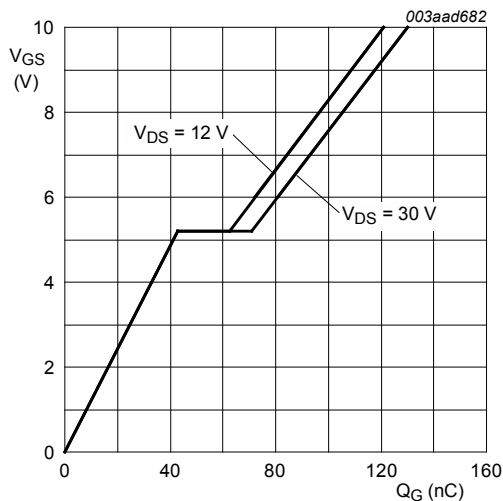


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^{\circ}\text{C}$; $I_D = 25\text{ A}$

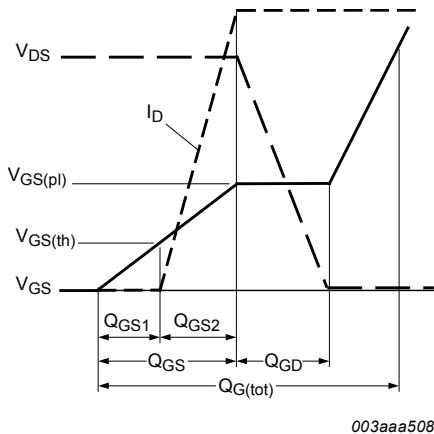


Fig. 14. Gate charge waveform definitions

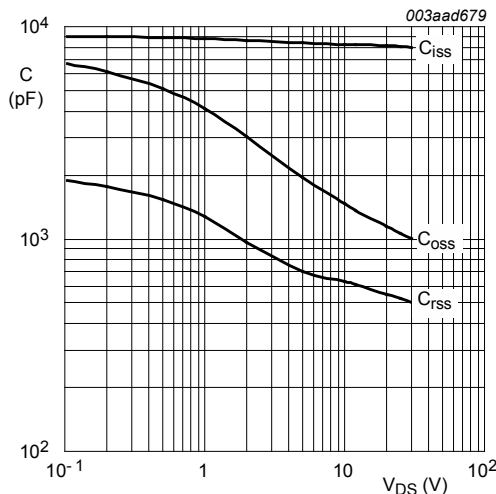


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

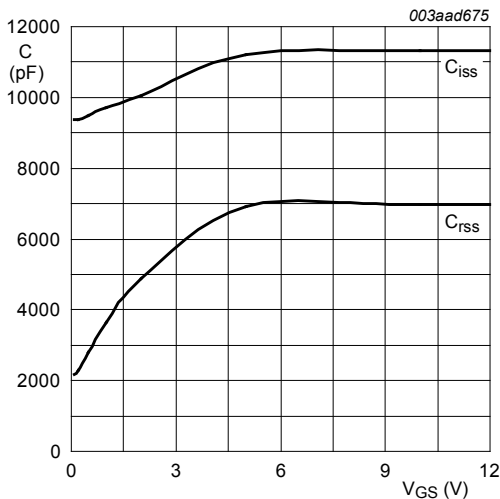


Fig. 16. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$

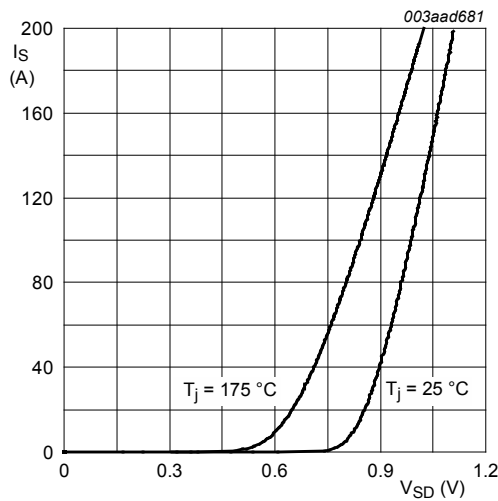


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

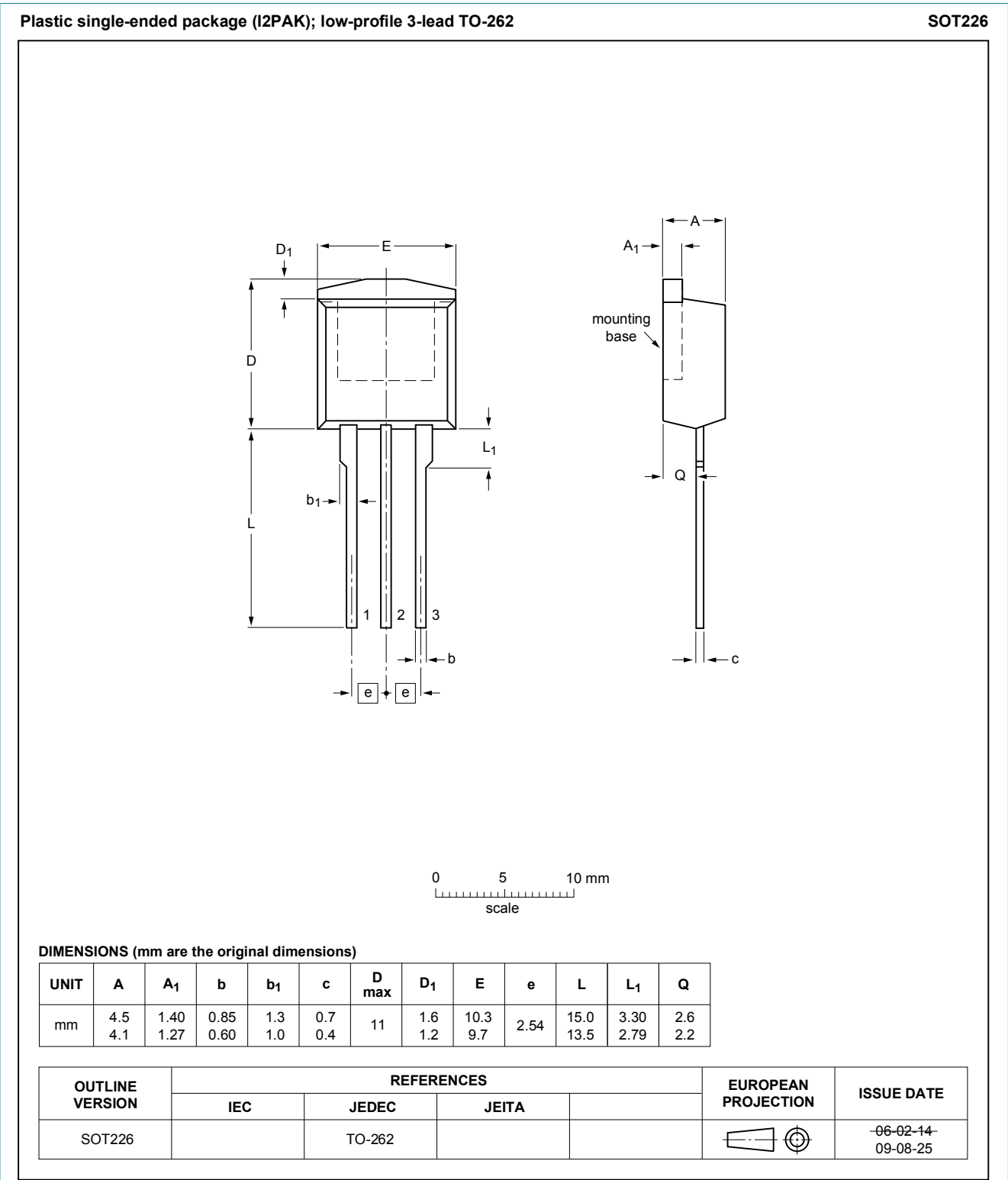


Fig. 18. Package outline I2PAK (SOT226)

12. Legal information

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