



## SY89311U

2.5V/3.3V/5V 1:2 DIFFERENTIAL  
PECL/LVPECL/ECL FANOUT BUFFER

Precision Edge®

### General Description

The SY89311U is a precision, high-speed 1:2 differential fanout buffer. Having within-device skews and output transition times significantly improved over the EL11V, the SY89311U is ideally suited for those applications which require the ultimate in AC performance in a small package.

The differential inputs of the SY89311U employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open, the Q outputs will be LOW.

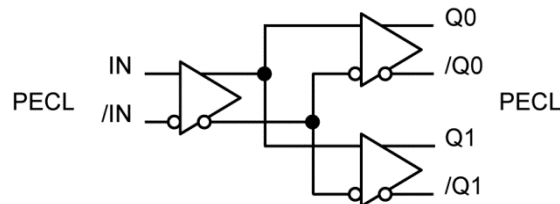
The differential inputs can accept 10/100K ECL/PECL signals (external termination required) and the outputs are 100K ECL/PECL compatible.

Datasheets and support documentation are available on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

### Features

- 2.5V, 3.3V and 5V power supply
- Guaranteed AC parameters over temperature:
  - $f_{MAX} > 3.0\text{GHz}$
  - $< 20\text{ps}$  output-to-output skew
  - $< 200\text{ps}$   $t_r / t_f$
  - $< 300\text{ps}$  propagation delay
  - $51\text{fs}_{(RMS)}$  phase jitter (typical)
- 100K compatible I/O
- Wide temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Available in ultra-small 8-pin MLF® (2mm x 2mm) package

### Block Diagram



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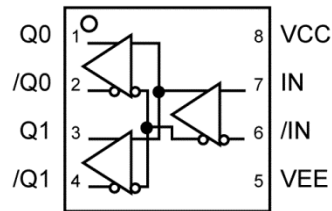
## Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89311UMITR	MLF-8	Industrial	311	Sn-Pb
SY89311UMGT <sup>(1)</sup>	MLF-8	Industrial	311 with Pb-Free bar-line indicator	Pb-Free NiPdAu

### Note:

1. Other voltages are available. Contact Micrel for details.

## Pin Configuration



8-Pin MLF<sup>®</sup>  
Ultra-Small Outline (2mm x 2mm)

## Pin Description

Pin Number	Pin Name	Type	Pin Function
1, 2, 3, 4	Q0, /Q0, Q1, /Q1	100K Output	Differential PECL/ECL Outputs: Default to LOW if IN inputs are left open. Q1, /Q1 See "Output Interface Applications" section for recommendations on terminations. Unused output pairs may be left floating without any impact on skew or jitter.
5	VEE, Exposed Pad	Negative Power Supply	Negative Power Supply: VEE and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
6	/IN	100K Input	Differential PECL/ECL Input: Internal 75k $\Omega$ pull-up and pull-down resistors. If left floating, pin defaults to VCC/2. When not used, this input can be left open. See "Input Interface Applications" section for single-ended inputs.
7	IN	100K Input	Differential PECL/ECL Input: Internal 75k $\Omega$ pull-down resistor. If left open, pin defaults LOW. Q output will be LOW. Accepts differential 10K and 100K ECL/PECL. See "Input Interface Applications" section for single-ended inputs.
2	5	Positive Power Supply	Positive Power Supply: Bypass with 0.1 $\mu$ F//0.01 $\mu$ F low ESR capacitors

**Absolute Maximum Ratings** (Error! Reference source not found.)

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +6.0V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5 to  $V_{CC}$   
 LVPECL Output Current ( $I_{OUT}$ )  
     Continuous..... 50mA  
     Surge ..... 100mA  
 Input Current  
     Source or sink current on IN, /IN .....  $\pm 50$ mA  
 Lead Temperature (soldering, 20 sec.) ..... +260°C  
 Storage Temperature ( $T_S$ ) ..... -65°C to +150°C

**Operating Ratings** (Error! Reference source not found.)

Supply Voltage  $|V_{CC}-V_{EE}|$  ..... +2.375V to +2.625V  
     ..... +3.0V to +3.6V  
     ..... +4.5V to +5.5V  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance, **Note 3**  
 MLF™ ( $\theta_{JA}$ )  
     Still-Air ..... 93°C/W  
     500lfpm ..... 87°C/W  
 MLF™ ( $\theta_{JB}$ )  
     Junction-to-Board ..... 60°C/W

**DC Electrical Characteristics** (3)

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{CC}$	Power Supply Voltage	LVPECL	2.375	2.5	2.625	V
		LVPECL	3.0	3.3	3.6	V
		PECL	4.5	5.0	5.5	V
		ECL	-5.5	-5.0	-4.5	V
		LVECL	-3.6	-3.3	-3.0	V
		LVECL	-2.625	-2.5	-2.375	V
$I_{EE}$	Power Supply Current	Max. $V_{CC}$ , no load		30	44	mA
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{IH}$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	IN	0.5			$\mu\text{A}$
		/IN	-150			$\mu\text{A}$
$C_{IN}$	Input Capacitance			1.0		pF

**(100K) ECL/LVECL DC Electrical Characteristics**

$V_{CC} = +2.5\text{V} \pm 5\%$  or  $+3.3\text{V} \pm 10\%$  or  $+5.0\text{V} \pm 10\%$  and  $V_{EE} = 0\text{V}$ ;  $V_{CC} = 0\text{V}$  and  $V_{EE} = -2.5\text{V} \pm 5\%$  or  $-3.3\text{V} \pm 10\%$  or  $-5.0\text{V} \pm 10\%$ ;  
 $R_L = 50\Omega$  to  $V_{CC}-2\text{V}$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{OH}$	Output HIGH Voltage		$V_{CC}-1.145$		$V_{CC}-0.895$	V
$V_{OL}$	Output LOW Voltage		$V_{CC}-1.945$		$V_{CC}-1.695$	V
$V_{IH}$	Input HIGH Voltage		$V_{CC}-1.225$		$V_{CC}-0.88$	V
$V_{IL}$	Input LOW Voltage		$V_{CC}-1.945$		$V_{CC}-1.625$	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range	<b>Note 6</b>	$V_{EE}+1.2$		$V_{CC}$	V
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{IH}$			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (IN)	$V_{IN} = V_{IL}$	0.5			$\mu\text{A}$
	Input LOW Current (/IN)	$V_{IN} = V_{IL}$	-150			$\mu\text{A}$

**Notes:**

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package Thermal Resistance values assume exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
- This circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- $V_{IHCMR}$  (min) varies 1:1 with  $V_{EE}$ , (max) varies 1:1 with  $V_{CC}$ .

## AC Electrical Characteristics<sup>(7)</sup>

$V_{CC} = +2.5V \pm 5\%$  or  $+3.3V \pm 10\%$  or  $+5.0V \pm 10\%$  and  $V_{EE} = 0V$ ;  $V_{CC} = 0V$  and  $V_{EE} = -2.5V \pm 5\%$  or  $-3.3V \pm 10\%$  or  $-5.0V \pm 10\%$ ;  
 $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted.

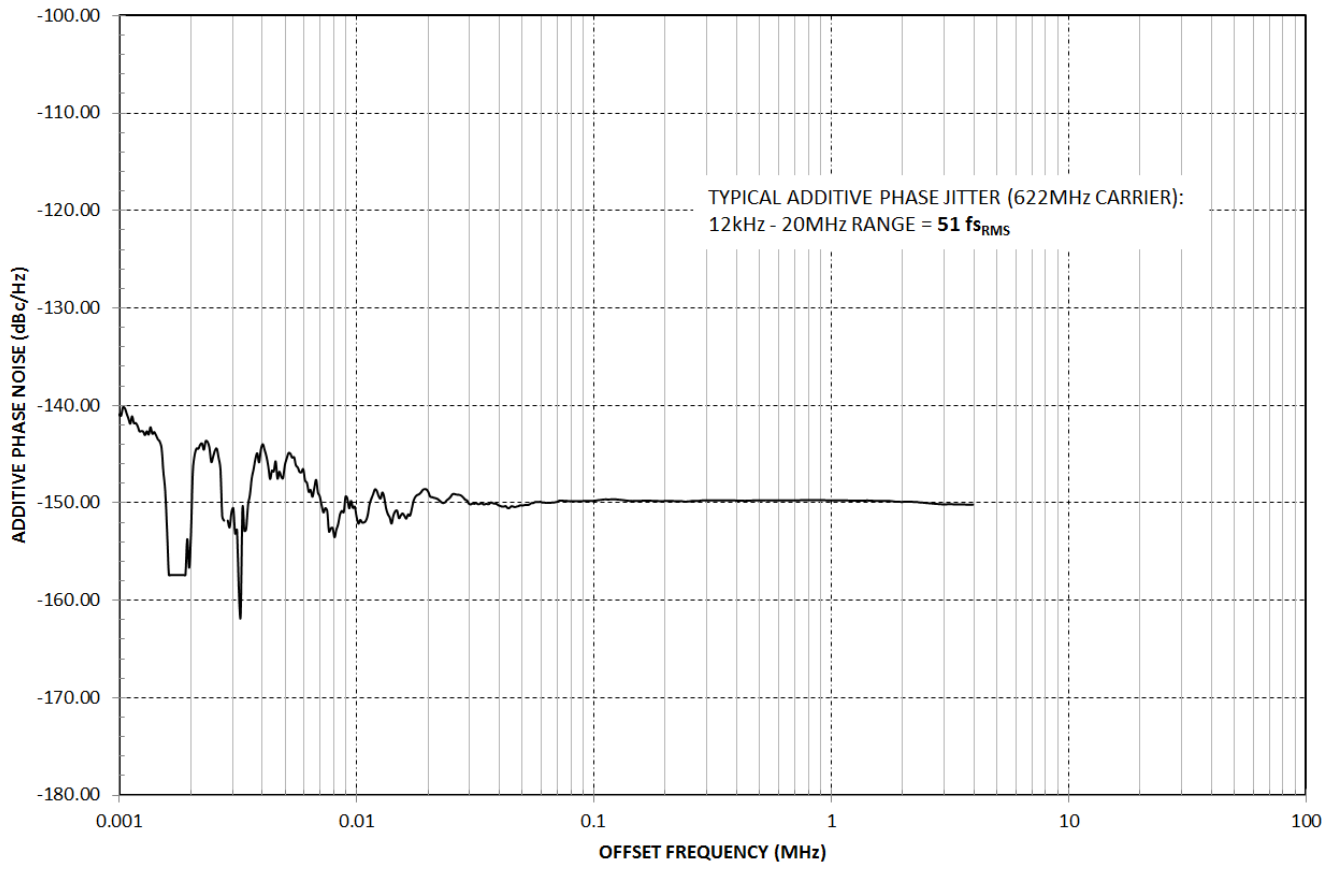
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{MAX}$	Maximum Toggle Frequency		3			GHz
$t_{pd}$	Propagation Delay (Differential) IN to Q, /Q	$V_{CC} = 3.3V/5V$	140	220	300	ps
		$V_{CC} = 2.5V$	170	240	360	ps
$t_{SKEW}$	Within-Device Skew Q, /Q	Note 8		5	20	ps
	Part-to-Part Skew	$V_{CC} = 3.3V/5V$ , Note 8 $V_{CC} = 2.5V$ , Note 8			150 120	ps ps
$t_{JITTER}$	Cycle-to-Cycle Jitter (rms)				1	ps <sub>(rms)</sub>
	Additive Phase Jitter	622MHz over 12kHz-20MHz		51		fs <sub>(rms)</sub>
$V_{DIFF}$	Input Swing	Note 9	150	800	1200	mV
$t_r, t_f$	Output Rise/Fall Time (20% to 80%)		70	120	200	ps

### Notes:

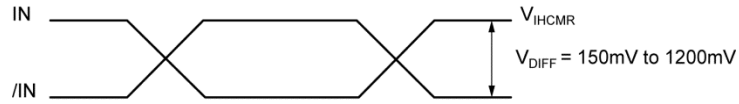
7. Measured with 750mV input signal, 50% duty cycle.  $V_{DIFF\_OUT}$  is  $\geq 400mV$ .
8. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
9. See "Input Waveform".

### Additive Phase Noise Plot

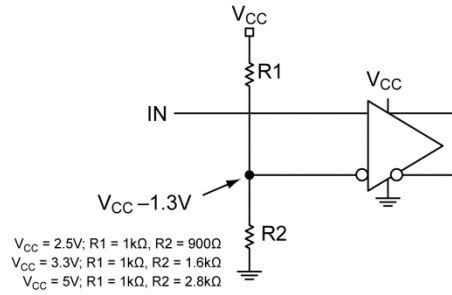
$V_{CC} = +3.3V$ ,  $GND = 0$ ,  $R_L = 50\Omega$  to  $V_{CC}-2V$ ,  $T_A = 25^\circ C$



## Input Waveform

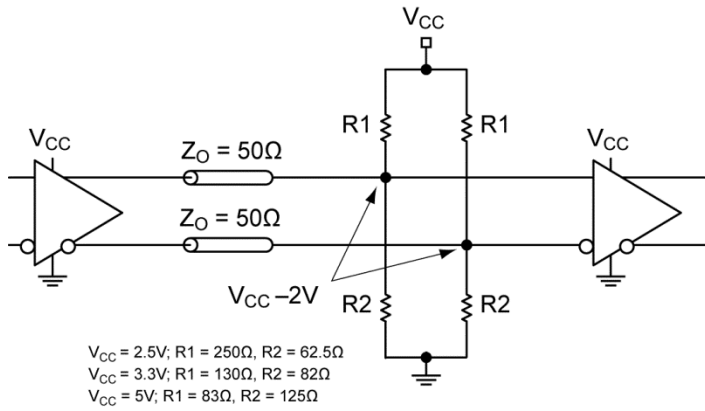


## Input Interface Applications

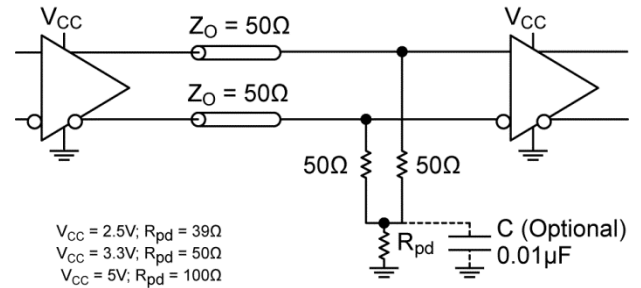


**Figure 1. Single-Ended Input (Terminating unused Input)**

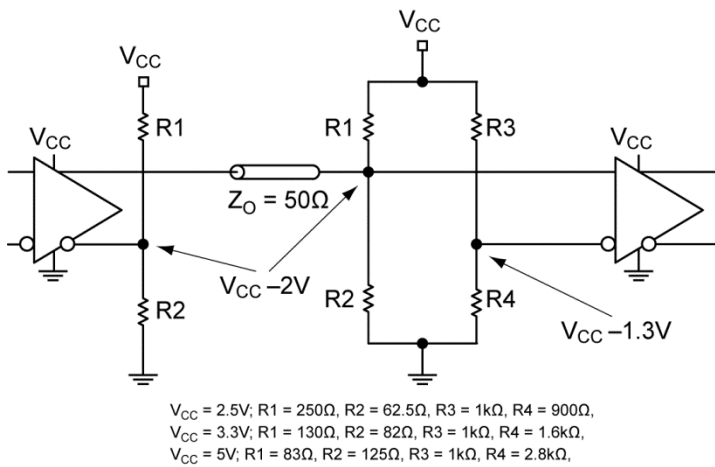
## LVPECL Output Interface Applications



**Figure 2. Parallel Thevenin-Equivalent Termination**

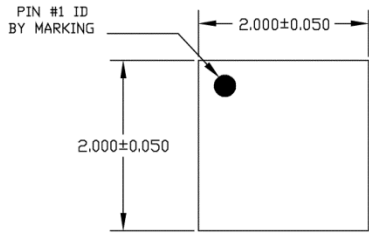


**Figure 3. Three Resistor "Y Termination"**

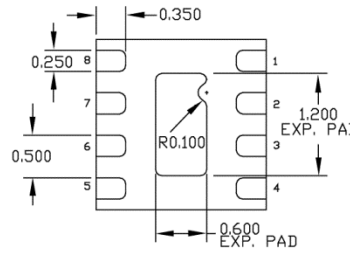


**Figure 4. Termination Unused I/O**

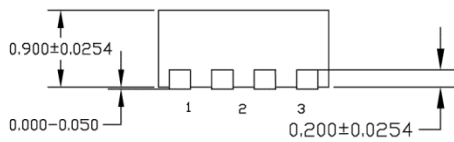
# Package Information<sup>(10)</sup>



TOP VIEW

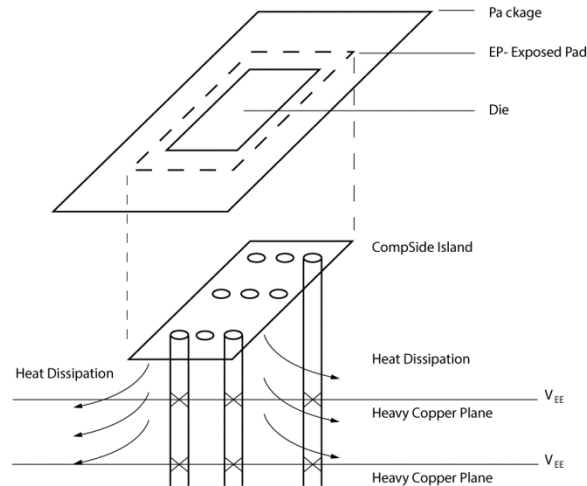


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF<sup>®</sup> Package

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

### 8-Lead MLF (MLF-8)

**Note:**

10. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).



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## Revision History

Date	Change Description/Edits by:	Rev.
8/4/10	Added new paragraph to disclaimer in boiler plate. Per Colin Sturt. M.Galvan	14
1/16/13	Complete rework	15

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