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January 2015

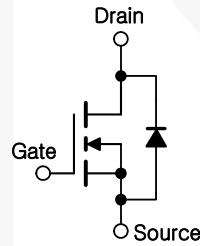
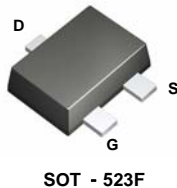


2N7002T — N-Channel Enhancement Mode Field Effect Transistor

# 2N7002T N-Channel Enhancement Mode Field Effect Transistor

## Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Lead Free/RoHS Compliant



## Ordering Information

Part Number	Top Mark	Package	Packing Method
2N7002T	AA	SOT-523F 3L	Tape and Reel

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \leq 1.0 \text{ M}\Omega$ )	60	V
$V_{GSS}$	Gate-Source Voltage	Continuous	$\pm 20$
		Pulsed	$\pm 40$
$I_D$	Drain Current	Continuous	115
		Continuous at $100^\circ\text{C}$	73
		Pulsed	800
$T_J$	Junction Temperature	150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to +150	$^\circ\text{C}$

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$P_D$	Total Device Dissipation	200	mW
	Derate Above $T_A = 25^\circ\text{C}$	1.6	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>(1)</sup>	625	$^\circ\text{C}/\text{W}$

### Note:

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.

## Electrical Characteristics

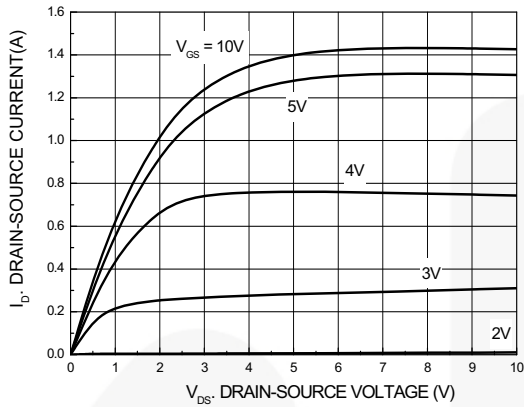
Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics<sup>(2)</sup></b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\ \mu\text{A}$	60	78		V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$		0.001	1.0	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		7	500	
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$		0.2	$\pm 10$	nA
<b>On Characteristics<sup>(2)</sup></b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.00	1.76	2.00	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 5\text{ V}, I_D = 0.05\text{ A}$		1.6	7.5	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$			2.0	
		$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}, T_J = 125^\circ\text{C}$		2.53	13.5	
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 7.5\text{ V}$	0.50	1.43		A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 0.2\text{ A}$	80.0	356.5		mS
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		37.8	50	pF
$C_{oss}$	Output Capacitance			12.4	25	pF
$C_{rss}$	Reverse Transfer Capacitance			6.5	7	pF
<b>Switching Characteristics</b>						
$t_{D(ON)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 0.2\text{ A}, V_{GEN} = 10\text{ V}, R_L = 150\ \Omega, R_{GEN} = 25\ \Omega$		5.85	20	ns
$t_{D(OFF)}$	Turn-Off Delay Time			12.5	20	ns

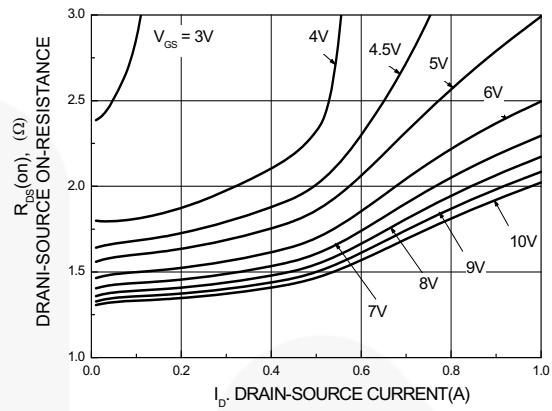
### Note:

2. Short duration test pulse used to minimize self-heating effect.

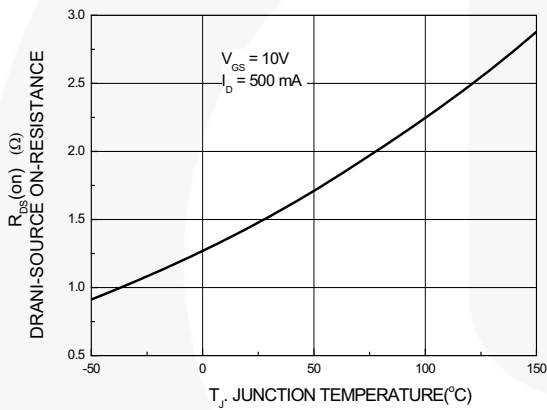
## Typical Performance Characteristics



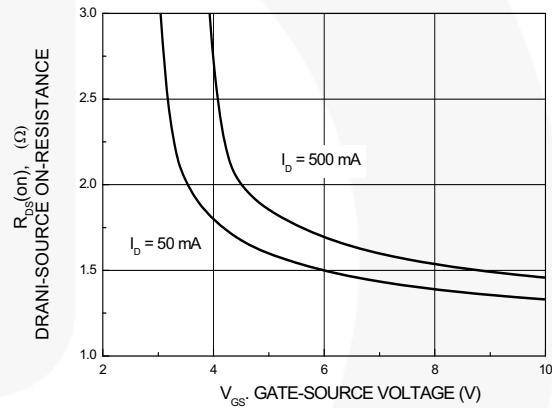
**Figure 1. On-Region Characteristics**



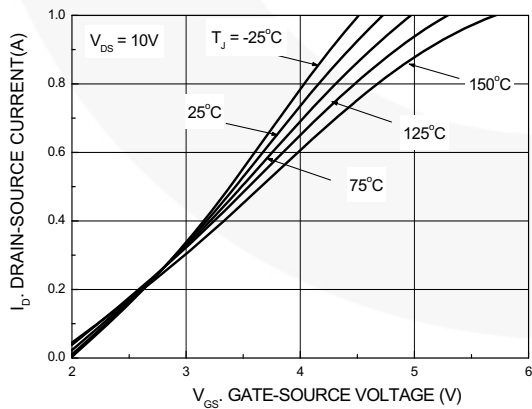
**Figure 2. On-Resistance Variation with Gate Voltage and Drain Current**



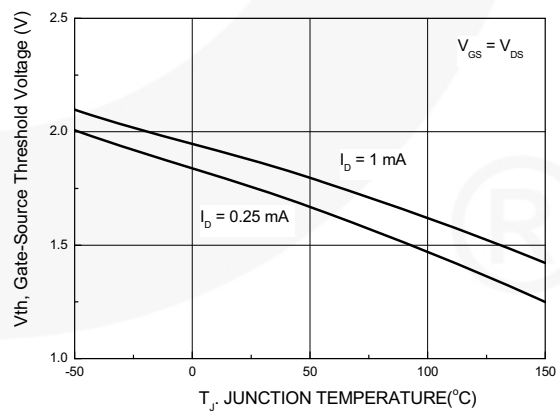
**Figure 3. On-Resistance Variation with Temperature**



**Figure 4. On-Resistance Variation with Gate-Source Voltage**



**Figure 5. Transfer Characteristics**



**Figure 6. Gate Threshold Variation with Temperature**

Typical Performance Characteristics (Continued)

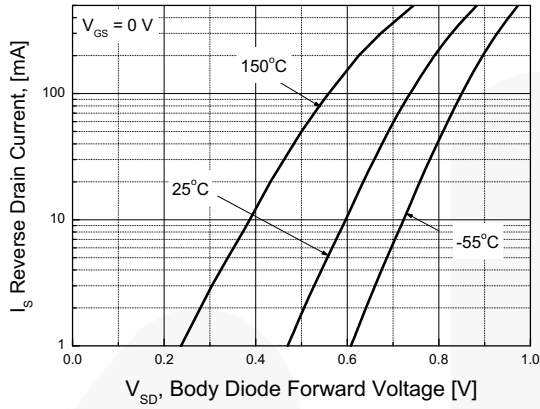


Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature

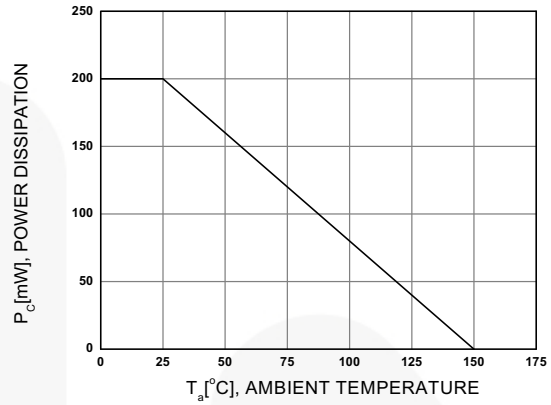
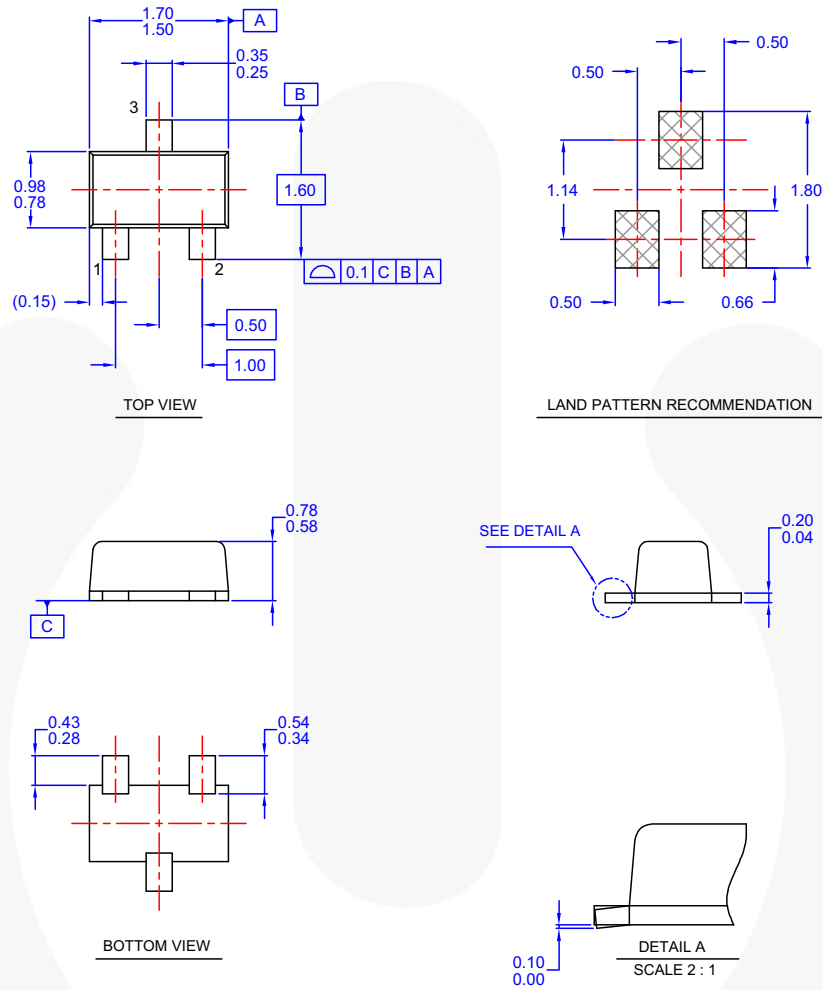


Figure 8. Power Derating

## Physical Dimensions



**NOTES:**

- A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.






MAD03ArevA

**Figure 9. 3-LEAD, SC89, EIAJ-SC89, 0.88MM WIDE, SOT523F**



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