



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

1. General Discription

THCV215/216-8LANE Evaluation Kits are designed to evaluate THCV215 and THCV216 for transmission of video data. Each has four THCV215's or four THCV216's.

This kits can transmit video data of "Full-HD / 240 Hz / 30 bit" and "4Kx2K / 60 Hz / 30 bit".

The supply voltage range are "3.0V to 3.6V" or "5.0V to 12.0V".

2. Block Diagram

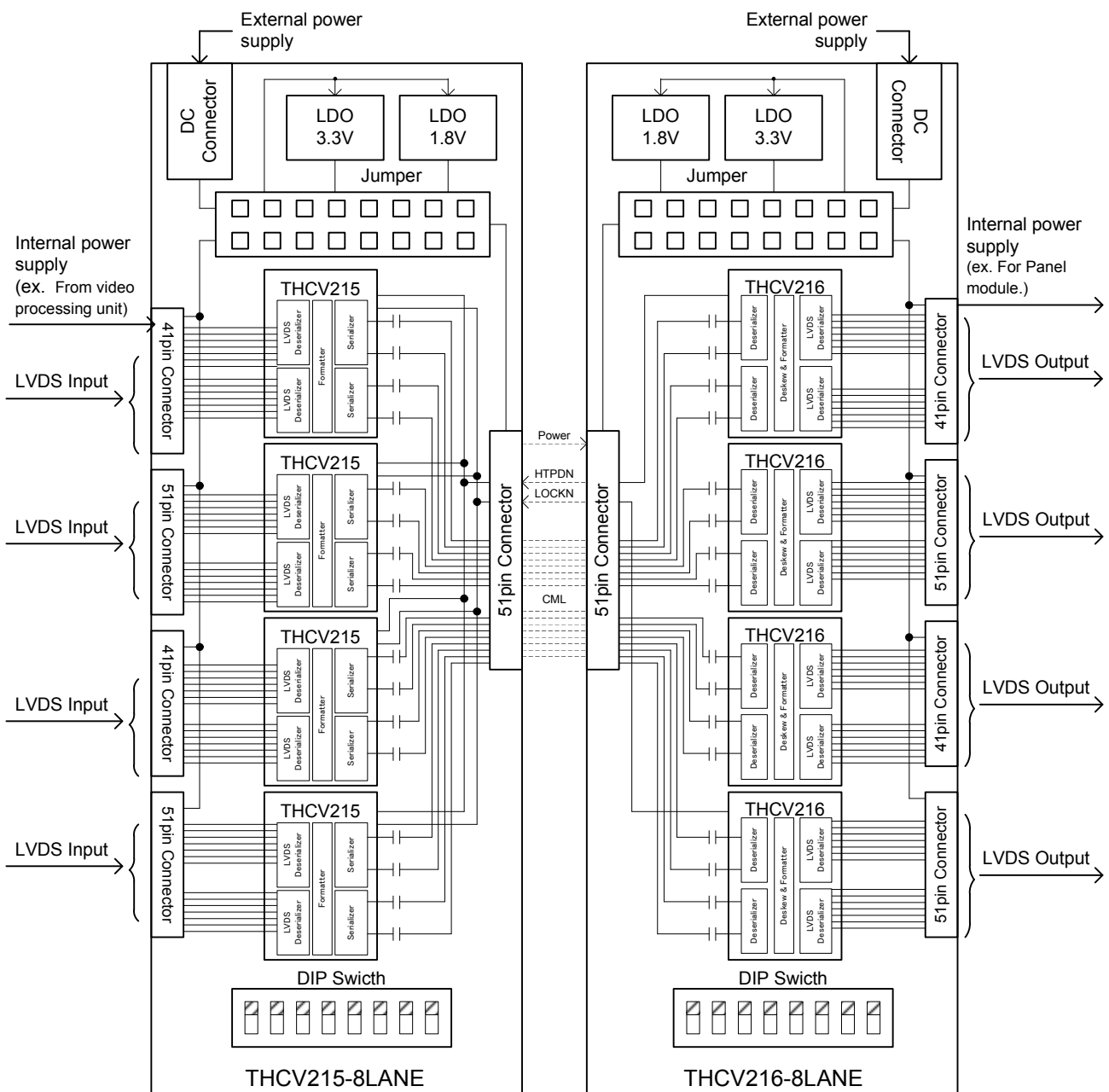


Figure 2-1. Block Diagram



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

3. Connector

This chapter shows the connector to connect the THCV215 and THCV216.

Table 3-1. Pin assignments of LVDS connector (41 pin)

THCV215 CN101 & CN301		Descriptions	THCV216 CN102 & CN104	
Pin No.	Symbol		Symbol	Pin No.
1	Vcc	Supply voltage from video processing unit, And for Panel module (Internal Supply)	Vcc	41
2				40
3				39
4				38
5				37
6	NC	Non Connected	NC	36
7	GND	Ground	GND	35
8				34
9				33
10	TLA0-	LVDS data input/output	RLA0-	32
11	TLA0+		RLA0+	31
12	TLB0-		RLB0-	30
13	TLB0+		RLB0+	29
14	TLC0-		RLC0-	28
15	TLC0+	RLC0+	27	
16	GND	Ground	GND	26
17	TLCLK0-	LVDS clock input/output	RLCLK0-	25
18	TLCLK0+		RLCLK0+	24
19	GND	Ground	GND	23
20	TLD0-	LVDS data input/output	RLD0-	22
21	TLD0+		RLD0+	21
22	TLE0-		RLE0-	20
23	TLE0+		RLE0+	19
24	GND	Ground	GND	18
25	TLA1-	LVDS data input/output	RLA1-	17
26	TLA1+		RLA1+	16
27	TLB1-		RLB1-	15
28	TLB1+		RLB1+	14
29	TLC1-		RLC1-	13
30	TLC1+	RLC1+	12	
31	GND	Ground	GND	11
32	TLCLK1-	LVDS clock input/output	RLCLK1-	10
33	TLCLK1+		RLCLK1+	9
34	GND	Ground	GND	8
35	TLD1-	LVDS data input/output	RLD1-	7
36	TLD1+		RLD1+	6
37	TLE1-		RLE1-	5
38	TLE1+		RLE1+	4
39	GND	Ground	GND	3
40	NC	Non Connected	NC	2
41				1

Table 3-2. Pin assignments of LVDS connector (51 pin)

THCV215 CN201 & CN401		Descriptions	THCV216 CN103 & CN105	
Pin No.	Symbol		Symbol	Pin No.
1	Vcc	Supply voltage from video processing unit, And for Panel module (Internal Supply)	Vcc	51
2				50
3				49
4				48
5				47
6	NC	Non Connected	NC	46
7	GND	Ground	GND	45
8				44
9				43
10	TLA0-	LVDS data input/output	RLA0-	42
11	TLA0+		RLA0+	41
12	TLB0-		RLB0-	40
13	TLB0+		RLB0+	39
14	TLC0-		RLC0-	38
15	TLC0+	RLC0+	37	
16	GND	Ground	GND	36
17	TLCLK0-	LVDS clock input/output	RLCLK0-	35
18	TLCLK0+		RLCLK0+	34
19	GND	Ground	GND	33
20	TLD0-	LVDS data input/output	RLD0-	32
21	TLD0+		RLD0+	31
22	TLE0-		RLE0-	30
23	TLE0+		RLE0+	29
24	GND	Ground	GND	28
25	TLA1-	LVDS data input/output	RLA1-	27
26	TLA1+		RLA1+	26
27	TLB1-		RLB1-	25
28	TLB1+		RLB1+	24
29	TLC1-		RLC1-	23
30	TLC1+	RLC1+	22	
31	GND	Ground	GND	21
32	TLCLK1-	LVDS clock input/output	RLCLK1-	20
33	TLCLK1+		RLCLK1+	19
34	GND	Ground	GND	18
35	TLD1-	LVDS data input/output	RLD1-	17
36	TLD1+		RLD1+	16
37	TLE1-		RLE1-	15
38	TLE1+		RLE1+	14
39	GND	Ground	GND	13
40	NC	Non Connected	NC	12
41				11
42				10
43				9
44				8
45				7
46				6
47				5
48				4
49				3
50				2
51	1			



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

3. Connector and Cable (Continued)

Table 3-3. Pin assignments of CML connector (51 pin)

THCV215_CN501		Descriptions	THCV216_CN101	
Pin No.	Symbol		Symbol	Pin No.
51	Vcc	Supply voltage from THC215 to THC216	Vcc	1
50				2
49				3
48				4
47				5
46				6
45				7
44				8
43				9
42				10
41	GND	Ground	GND	11
40				12
39				13
38				14
37				15
36	HTPDN	Hot plug detect	HTPDN	16
35	LOCKN	Lock detect	LOCKN	17
34	GND	Ground	GND	18
33	Tx0n	V-by-One® HS Channel 0 (CML)	Rx0n	19
32	Tx0p		Rx0p	20
31	GND	Ground	GND	21
30	GND		GND	22
29	Tx1n	V-by-One® HS Channel 1 (CML)	Rx1n	23
28	Tx1p		Rx1p	24
27	GND	Ground	GND	25
26	GND		GND	26
25	Tx2n	V-by-One® HS Channel 2 (CML)	Rx2n	27
24	Tx2p		Rx2p	28
23	GND	Ground	GND	29
22	GND		GND	30
21	Tx3n	V-by-One® HS Channel 3 (CML)	Rx3n	31
20	Tx3p		Rx3p	32
19	GND	Ground	GND	33
18	GND		GND	34
17	Tx4n	V-by-One® HS Channel 4 (CML)	Rx4n	35
16	Tx4p		Rx4p	36
15	GND	Ground	GND	37
14	GND		GND	38
13	Tx5n	V-by-One® HS Channel 5 (CML)	Rx5n	39
12	Tx5p		Rx5p	40
11	GND	Ground	GND	41
10	GND		GND	42
9	Tx6n	V-by-One® HS Channel 6 (CML)	Rx6n	43
8	Tx6p		Rx6p	44
7	GND	Ground	GND	45
6	GND		GND	46
5	Tx7n	V-by-One® HS Channel 7 (CML)	Rx7n	47
4	Tx7p		Rx7p	48
3	GND	Ground	GND	49
2	NC		Non Connected	NC
1		51		



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

4. Power supply setting

This chapter shows the power supply setting with the jumper.

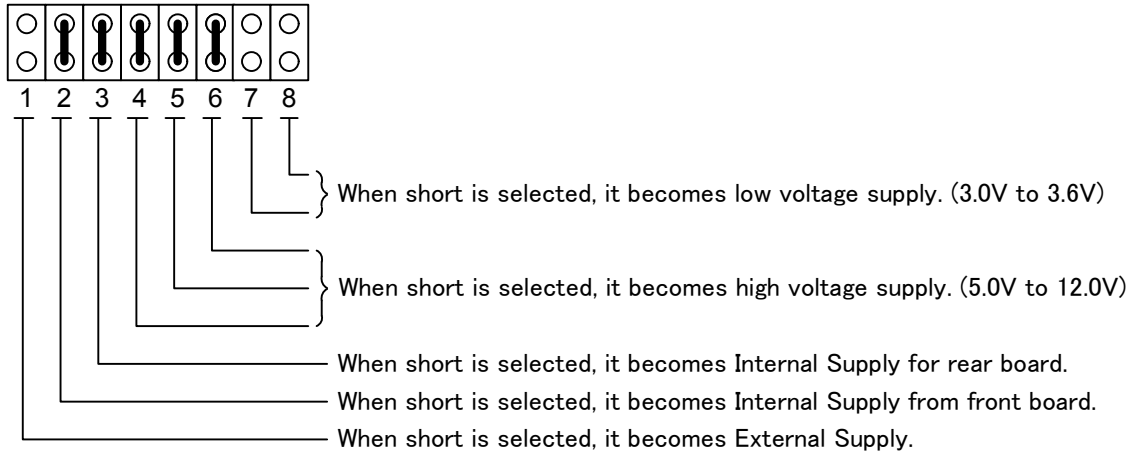


Figure 4. power supply setting with the jumper

Example4-1 : Internal Supply 5.0 V to 12.0V (Default Setting)

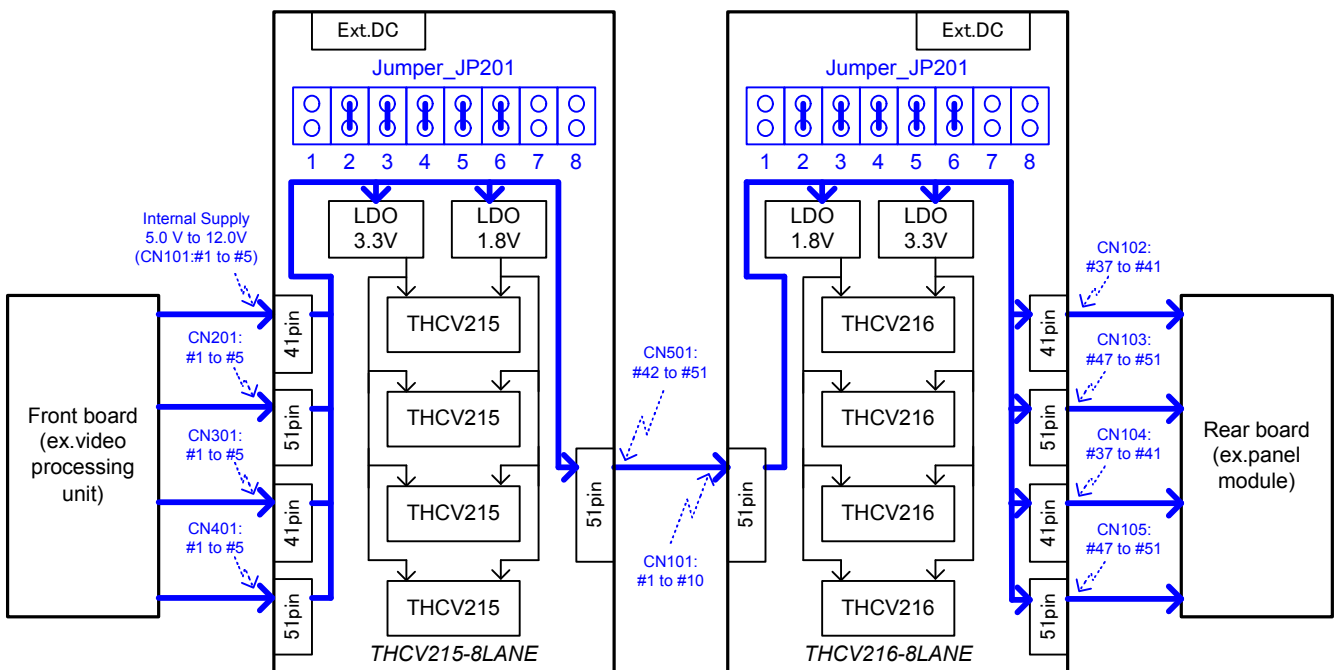


Figure 4-1. Internal Supply 5.0V to 12.0V



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

4. Power supply setting (Continued)

Example4-2 : External Supply 5.0V to 12.0V

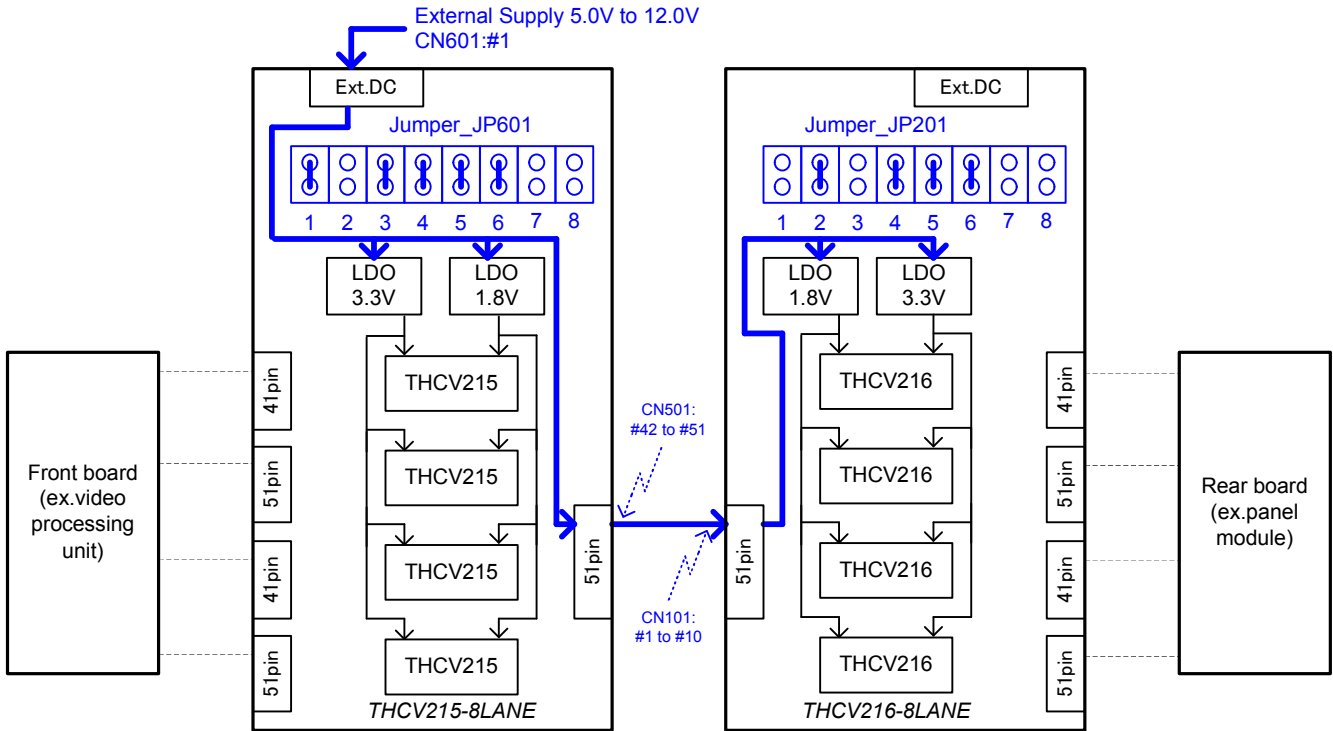


Figure 4-2. External Supply 5.0V to 12.0V

Example4-3 : External Supply 3.0V to 3.6V

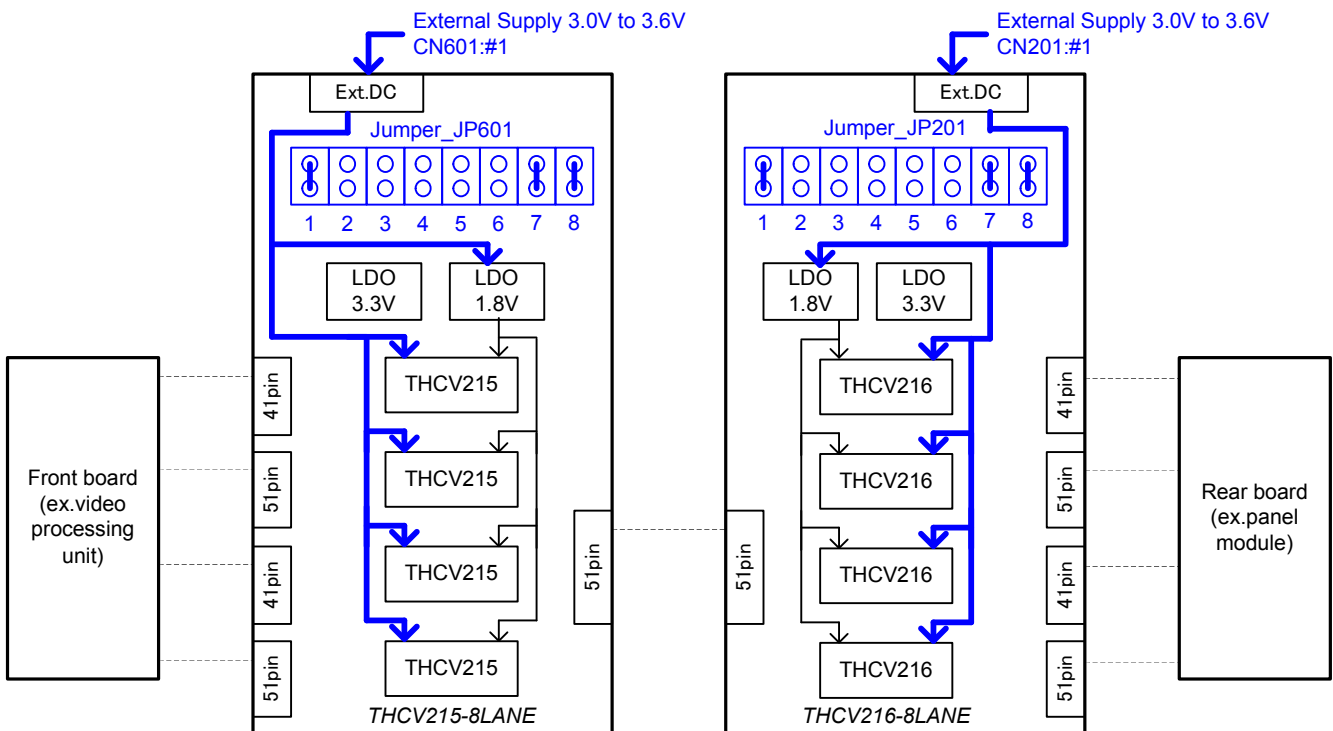


Figure 4-3. External Supply 3.0V to 3.6V



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

5. Function setting

This chapter shows the DIP switches of the control settings.

Table 5-1. DIP switches on the THCV215-8LANE Board

SW#	Symbol	Default Setting	Function															
1	SDSEL	High (8 lane)	Selects the Lanes. Low : Not available High : 8 lane															
2	COL0	Low	Selects the color depth. <table border="1"> <thead> <tr> <th>COL0</th> <th>COL1</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>Low</td> <td>6 bit mode</td> </tr> <tr> <td>High</td> <td>Low</td> <td>8 bit mode</td> </tr> <tr> <td>Low</td> <td>High</td> <td>10 bit mode</td> </tr> <tr> <td>High</td> <td>High</td> <td>Not available</td> </tr> </tbody> </table>	COL0	COL1	Function	Low	Low	6 bit mode	High	Low	8 bit mode	Low	High	10 bit mode	High	High	Not available
COL0	COL1	Function																
Low	Low	6 bit mode																
High	Low	8 bit mode																
Low	High	10 bit mode																
High	High	Not available																
3	COL1	High																
4	PDN	High (Normal)	Selects the power down. Low : Power down (CML output High Fix, other Hi-Z) High : Normal operation															
5	DRV1	Low	Selects the drive strength. Must be set to DRV1=Low and to DRV0=High															
6	DRV0	High																
7	PRE1	Low (0%)	Selects the pre-emphasis level. Low : 0% High : 100%															
8	RES1	Low (Normal)	Selects the Field BET Mode. * Low : Normal operation (default) High : Field BET Mode enable															

* Please see the datasheet for details. (THCV215-THCV216_Rev.x.xx_E.pdf)

Table 5-2. DIP switches on the THCV216-8LANE Board

SW#	Symbol	Default Setting	Function															
1	SDSEL	High (8 lane)	Selects the Lanes. Low : Not available High : 8 lane															
2	COL1	High	Selects the color depth. <table border="1"> <thead> <tr> <th>COL1</th> <th>COL0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>Low</td> <td>6 bit mode</td> </tr> <tr> <td>Low</td> <td>High</td> <td>8 bit mode</td> </tr> <tr> <td>High</td> <td>Low</td> <td>10 bit mode</td> </tr> <tr> <td>High</td> <td>High</td> <td>Not available</td> </tr> </tbody> </table>	COL1	COL0	Function	Low	Low	6 bit mode	Low	High	8 bit mode	High	Low	10 bit mode	High	High	Not available
COL1	COL0	Function																
Low	Low	6 bit mode																
Low	High	8 bit mode																
High	Low	10 bit mode																
High	High	Not available																
3	COL0	Low																
4	PDN	High (Normal)	Selects the power down. Low : Power down High : Normal operation															
5	RES3	Low (Normal)	Selects the Field BET Mode. * Low : Normal operation (default) High : Field BET Mode enable															
6	NC	Low	Not connected															
7	NC	Low																
8	RS	Low (Normal)	Direction of RS pin depends on RES3. Selects the LVDS swing range when RES3=Low High : Normal swing (350 mV typ.) Low : Reduced swing (200mV typ.) Field BET output when RES3=High *															

* Please see the datasheet for details. (THCV215-216_Rev.x.xx_E.pdf)



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

6. Other functional Descriptions

This chapter shows other function.

6-1. About LED on the board.

Board	Power On detect.	Lock detect.
THCV215-8LANE	D601	D701
THCV216-8LANE	D201	-

6-2. THCV215 Link Ready function (RDY)

This is a CMOS output for indicating the link status. If link is ready RDY = High.

6-3. THCV216 Field BET mode settings.

Please detach Jumper (JP101 to JP104) for Field BET mode.



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

7. Schematic

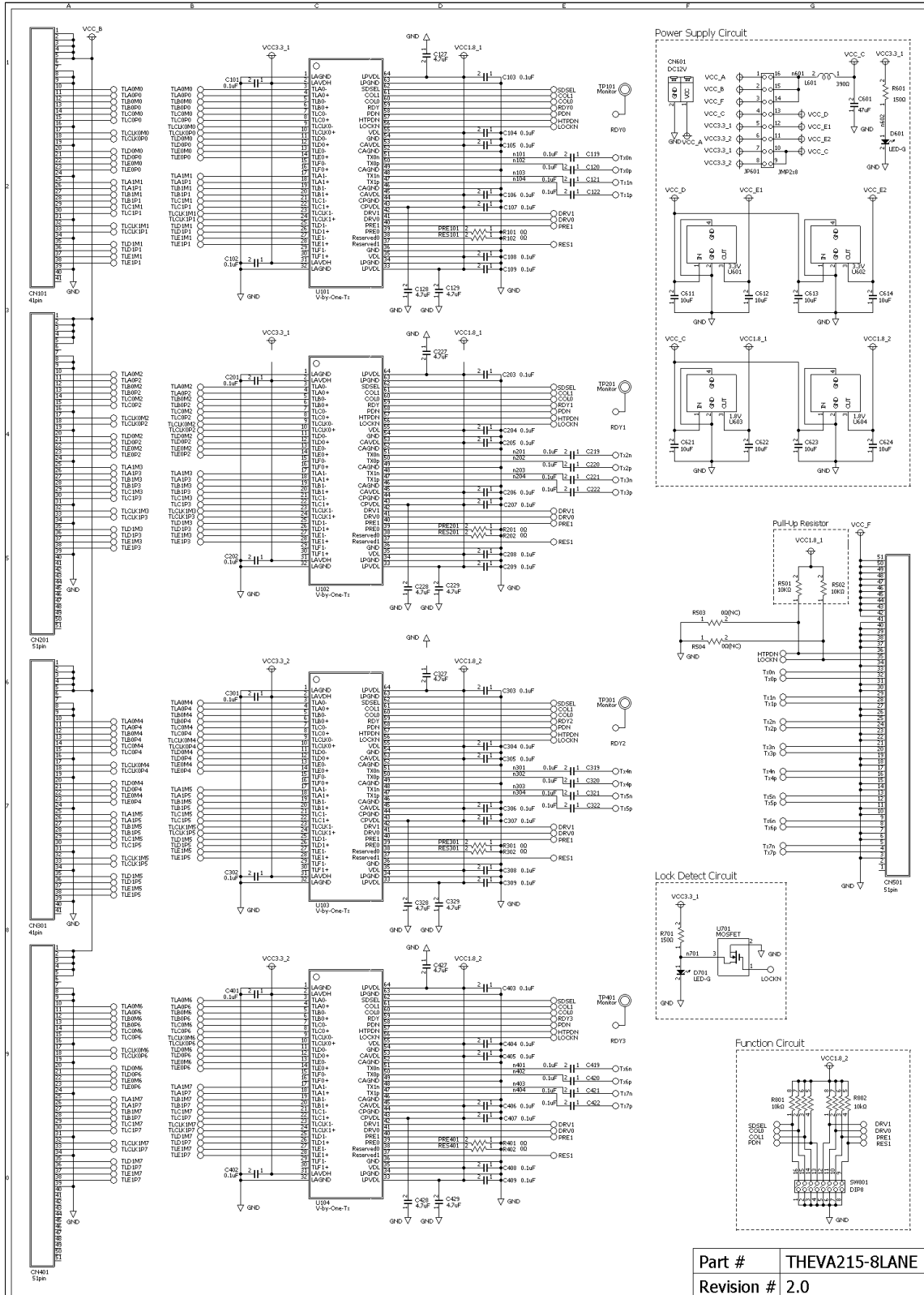


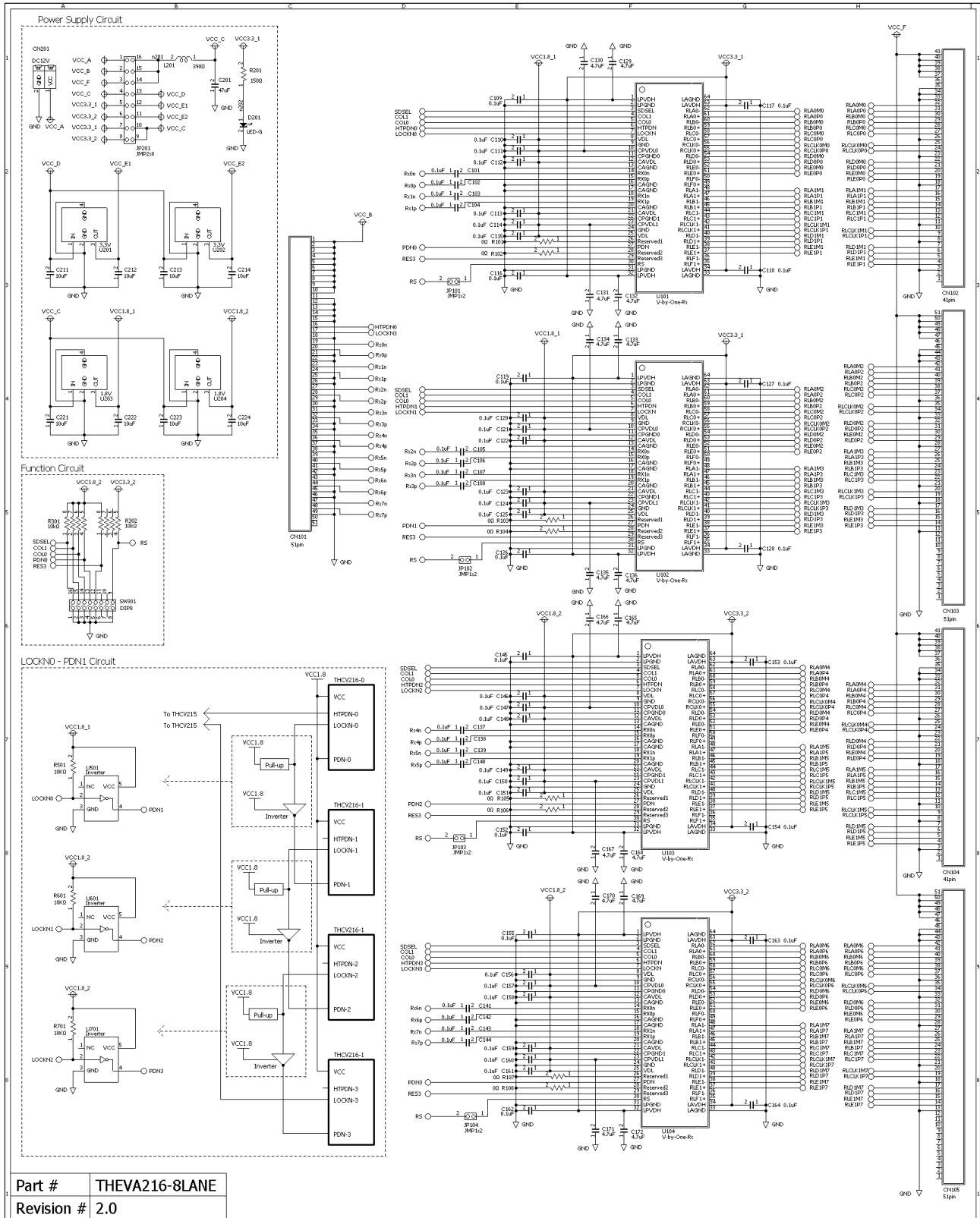
Figure 7-1. THCV215-8LANE schematic



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

7. Schematic



Part # THEVA216-8LANE
Revision # 2.0

Figure 7-2. THCV216-8LANE schematic



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

9. Layout

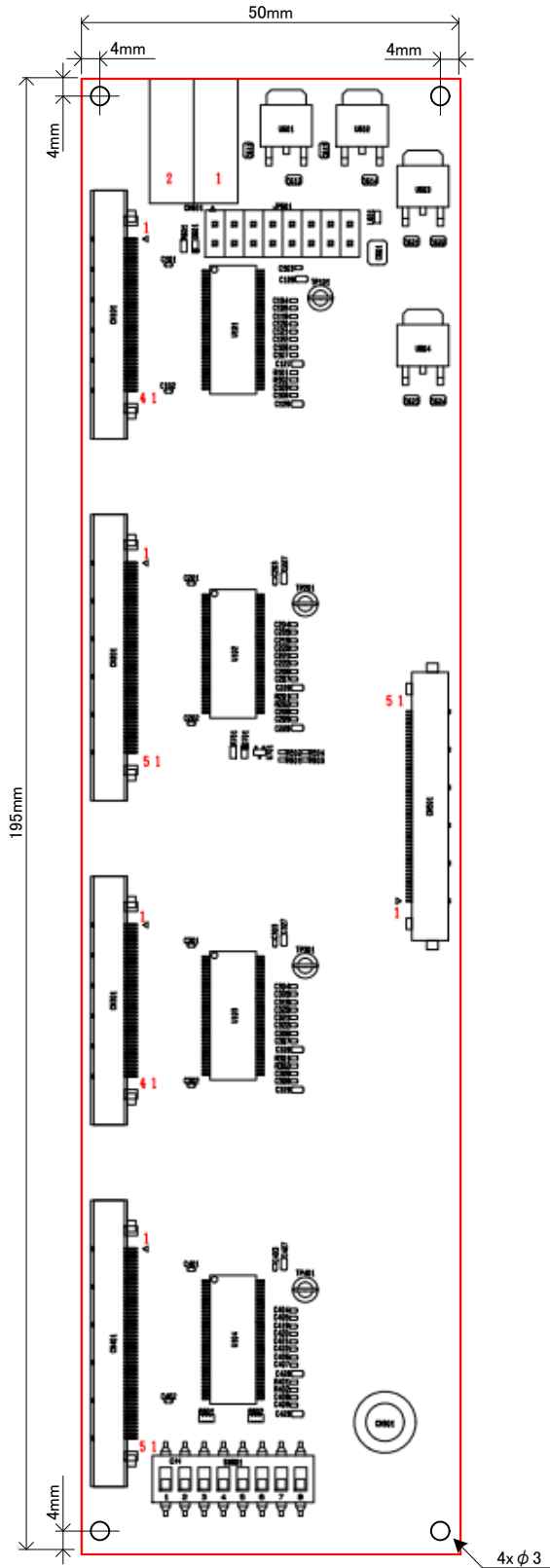


Figure 9-1. Component Placement Guide of THCV215-8LANE

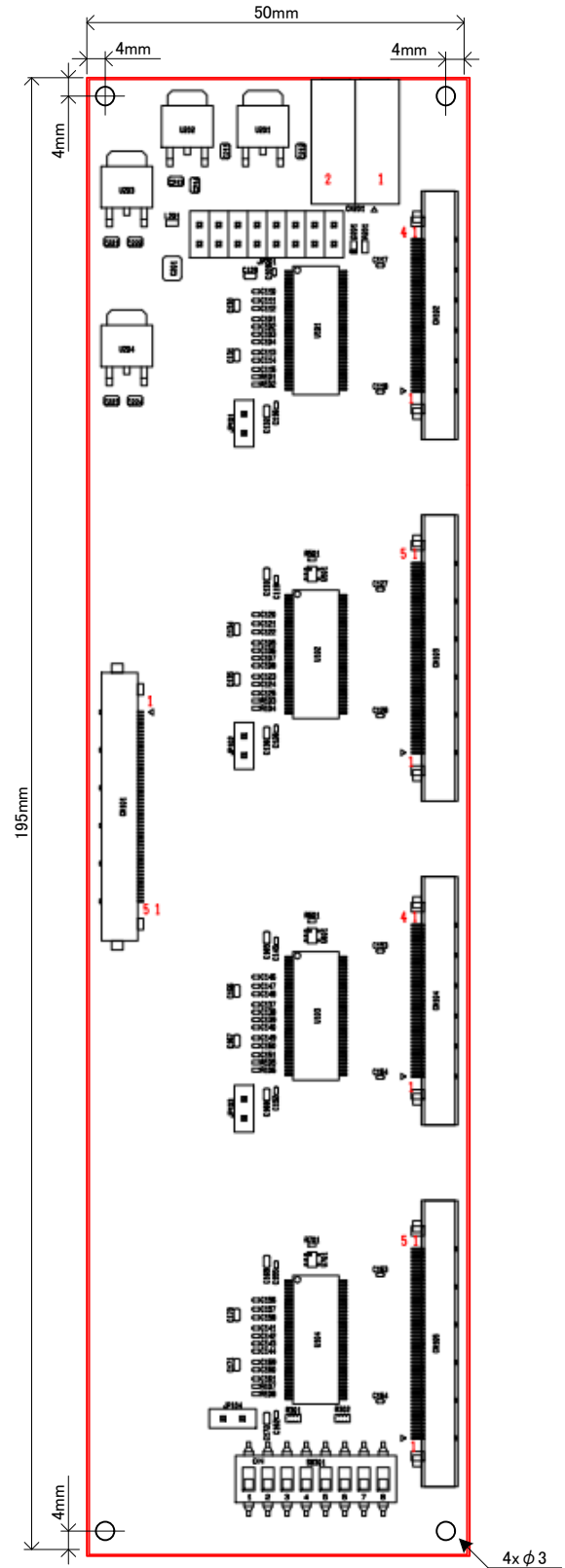


Figure 9-2. Component Placement Guide of THCV216-8LANE



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

10. Cable

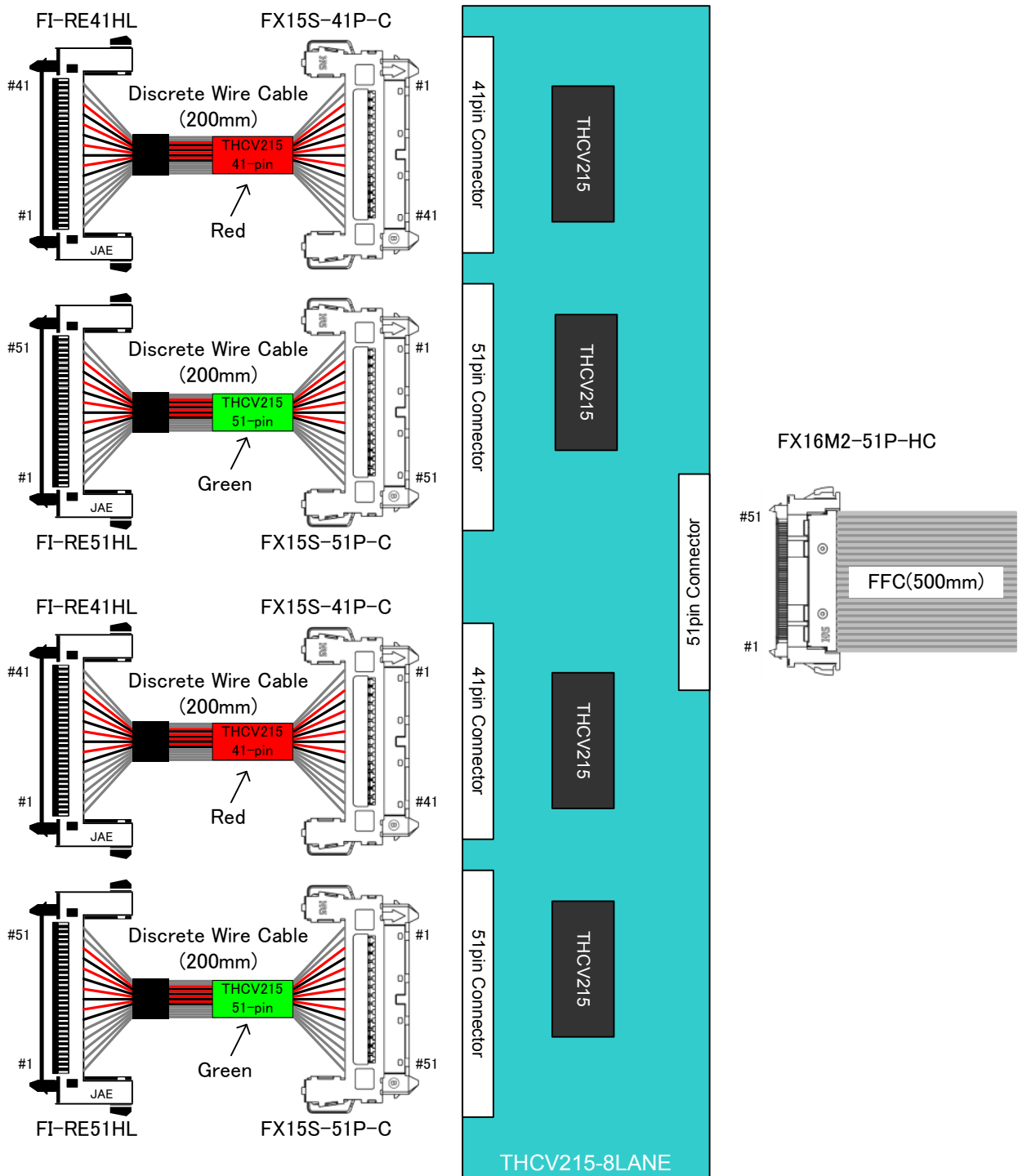


Figure 10-1. Cable of THCv215-8LANE



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

10. Cable

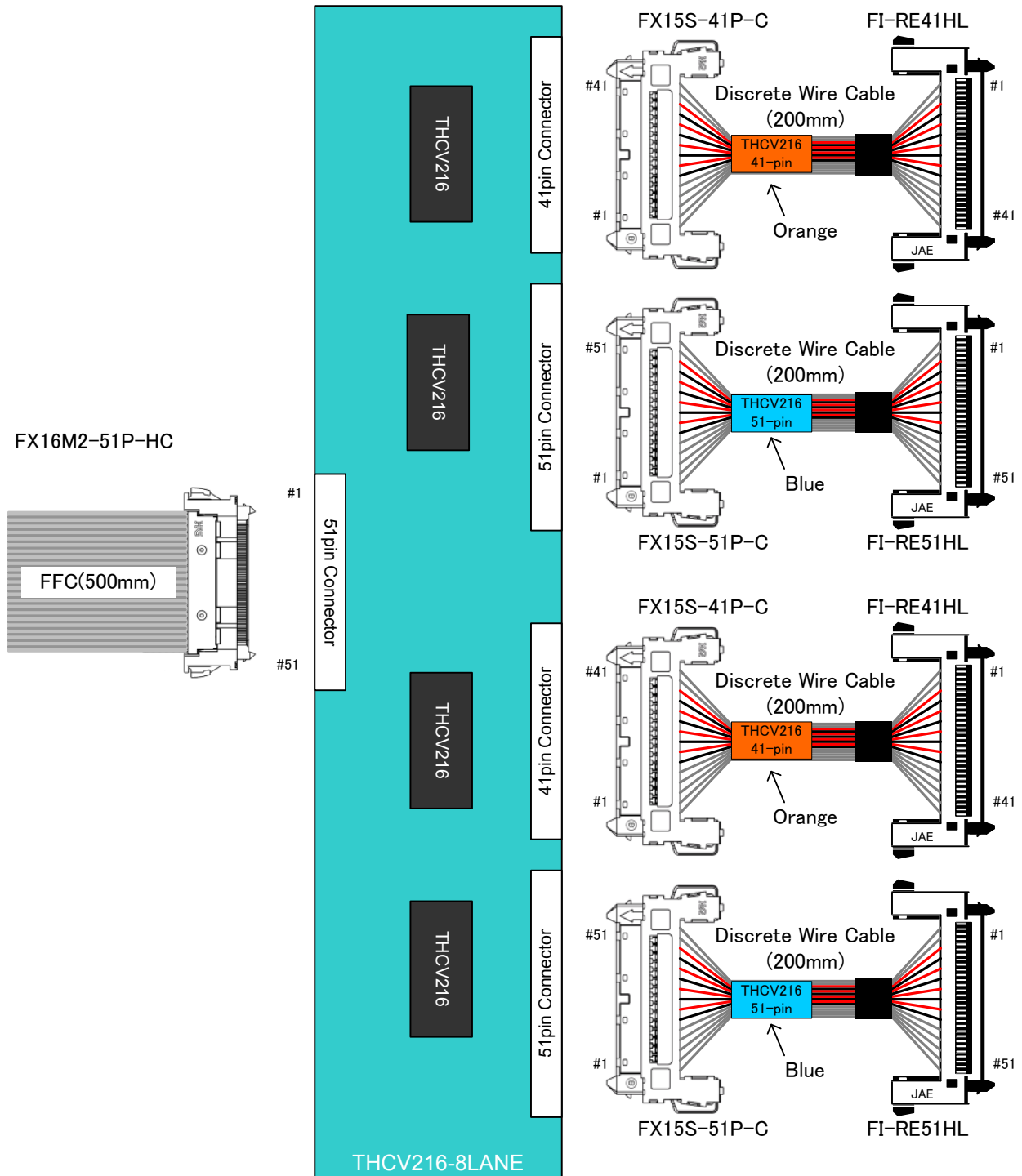


Figure 10-2. Cable of THCV216-8LANE



THCV215/216-8LANE Evaluation Kits

SerDes transmitter and receiver evaluation board

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