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# 1 Electrical data

## 1.1 Maximum ratings

**Table 1. Absolute maximum ratings ( $T_{CASE} = 25^{\circ}C$ )**

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source voltage	65	V
$V_{DGR}$	Drain-Gate voltage ( $R_{GS} = 1\text{ M}\Omega$ )	65	V
$V_{GS}$	Gate-Source voltage	+ 20	V
$I_D$	Drain current	4	A
$P_{DISS}$	Power dissipation (@ $T_c = 70^{\circ}C$ )	74	W
$T_j$	Max. operating junction temperature	200	$^{\circ}C$
$T_{STG}$	Storage temperature	-65 to + 200	$^{\circ}C$

## 1.2 Thermal data

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction - case thermal resistance	1.75	$^{\circ}C/W$

## 2 Electrical characteristics

$$T_{CASE} = +25\text{ }^{\circ}\text{C}$$

### 2.1 Static

**Table 3. Static (per section)**

Symbol	Test conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	$I_{DS} = 10\text{ mA}$	65			V
$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$			1	$\mu\text{A}$
$V_{GS(Q)}$	$V_{DS} = 28\text{ V}$	$I_D = 50\text{ mA}$	2.0		5.0	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$		1.3		V
$G_{FS}$	$V_{DS} = 10\text{ V}$	$I_D = 3\text{ A}$		1.8		mho
$C_{ISS}^{(1)}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		58		pF
$C_{OSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		34		pF
$C_{RSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		2.7		pF

1. Includes Internal Input Moscap.

### 2.2 Dynamic

**Table 4. Dynamic**

Symbol	Test conditions		Min	Typ	Max	Unit
$P_{OUT}$	$V_{DD} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $f = 945\text{ MHz}$	30			W
$G_{PS}$	$V_{DD} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $P_{OUT} = 30\text{ W}$ $f = 945\text{ MHz}$	13	15		dB
$h_D$	$V_{DD} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $P_{OUT} = 30\text{ W}$ $f = 945\text{ MHz}$	50	60		%
Load mismatch	$V_{DD} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $P_{OUT} = 28\text{ W}$ $f = 945\text{ MHz}$ All phase angles	10:1			VSWR

### 3 Typical performance (CW)

Figure 2. Output power vs input power

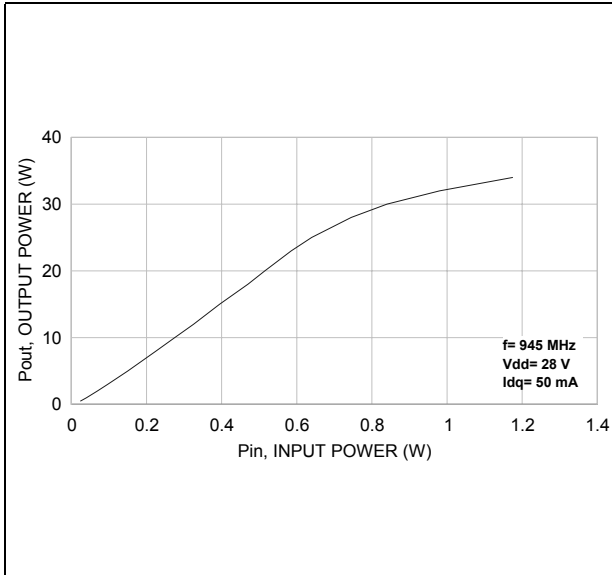


Figure 3. Power gain and efficiency vs output power

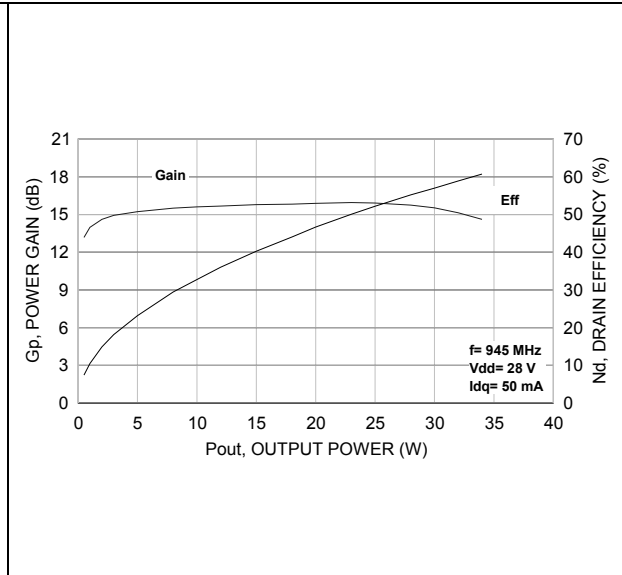


Figure 4. Output power vs gate source voltage

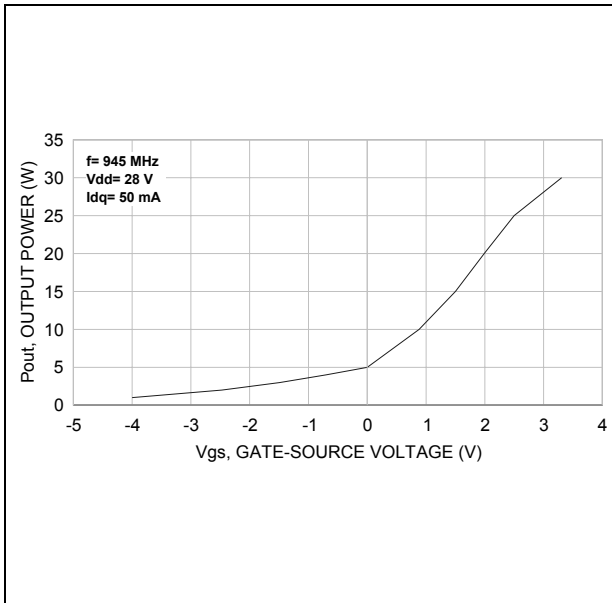
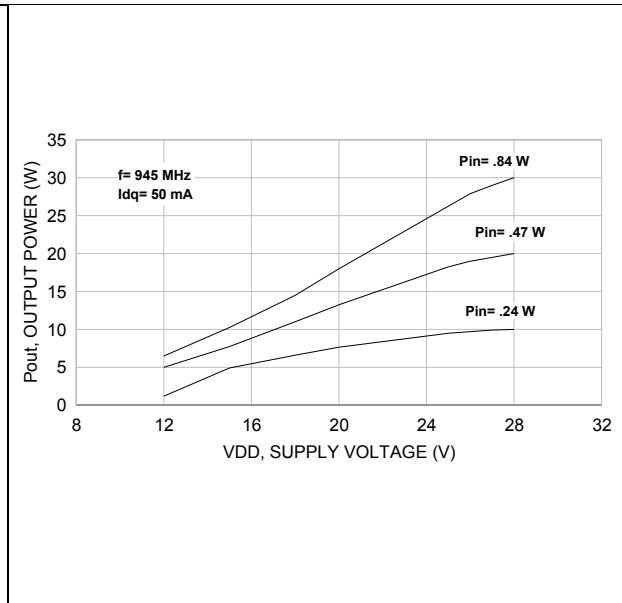
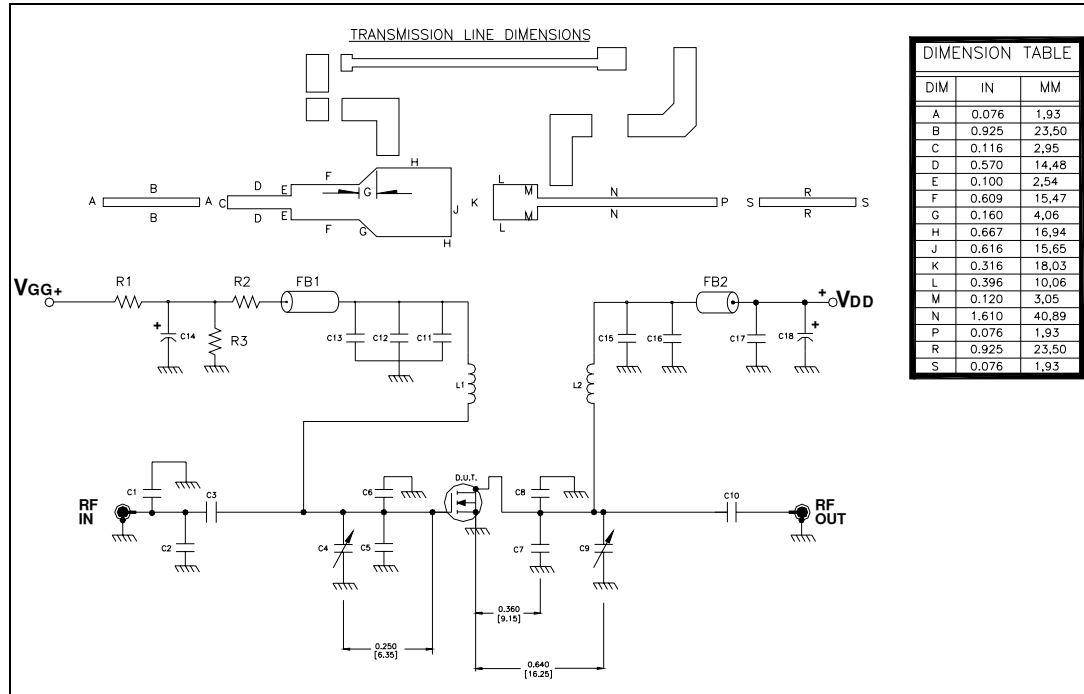


Figure 5. Output power vs supply voltage



# 4 Test circuit

Figure 6. Test circuit schematic



- 1 Dimensions at component symbols are reference for component placement.
- 2 Gap between ground & transmission line = 0.056 [1.42] +0.002 [0.05] -0.000 [0.00] typ.
- 3 Dimensions of input and output component from edge of transmission lines.

**Table 5. Test circuit component part list**

Component	Description
C19	200 $\mu$ F / 63V ALLUMINIUM ELECTROLYTIC RADIAL LEAD CAPACITOR
C18, C14	0.1 $\mu$ F / 500V SURFACE MOUNT CERAMIC CHIP CAPACITOR
C17	100 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C16, C12, C11,C1	47 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C15	10 $\mu$ F / 50V ALUMINIUM ELECTROLYTIC RADIAL LEAD CAPACITOR
C13	100 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C9, C2	0.8-8.0 pF GIGA TRIM VARIABLE CAPACITOR
C8	6.2 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C7, C6, C5 ,C4	10 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C3	3 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
R3	120 0-IM, 2W SURFACE MOUNT CERAMIC CHIP CAPACITOR
R2	4.7 M OHM 1W SURFACE MOUNT CERAMIC CHIP CAPACITOR
R1	18 K OHM, 1W SURFACE MOUNT CERAMIC CHIP CAPACITOR
FB2, FB1	SHIELD BEAD SURFACE MOUNT EMI
L2, L1	INDUCTOR, 5 TURNS AIR WOUND #22AWG, ID=0.059[1.49], NYLON COATED MAGNET WIRE
PCB	WOVEN FIBERGLASS REINFORCED PTFE 0.080" THK, $\epsilon_r=2.55$ , 2 Oz EDCu BOTH SIDE

# 5 Text circuit layout

Figure 7. Test fixture

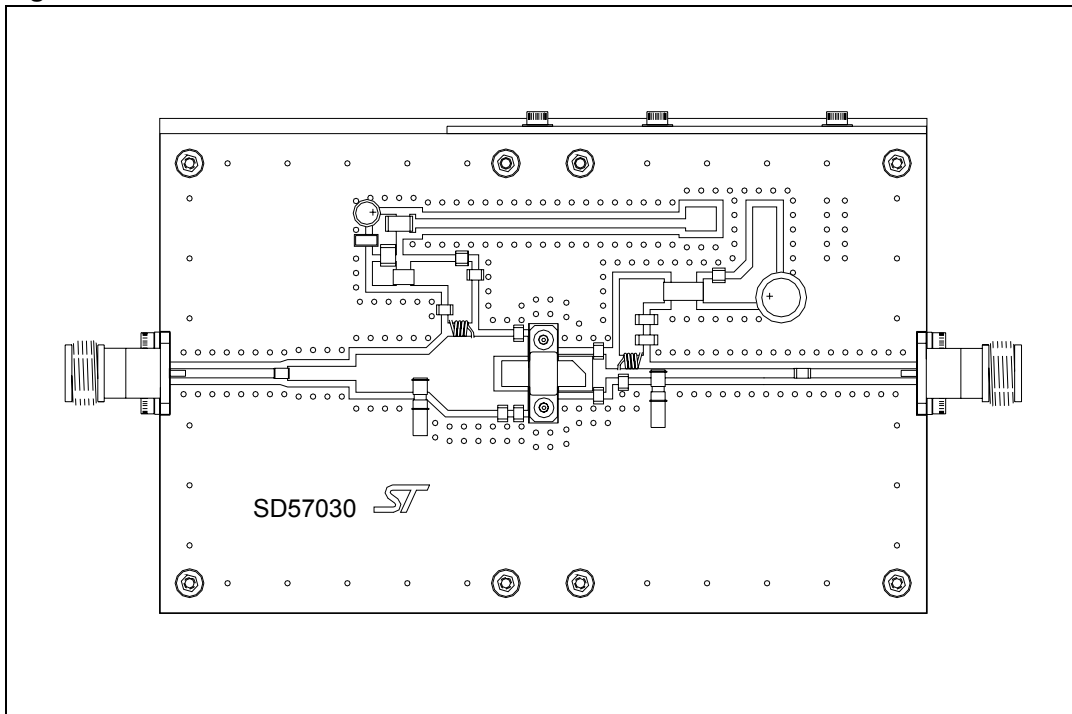
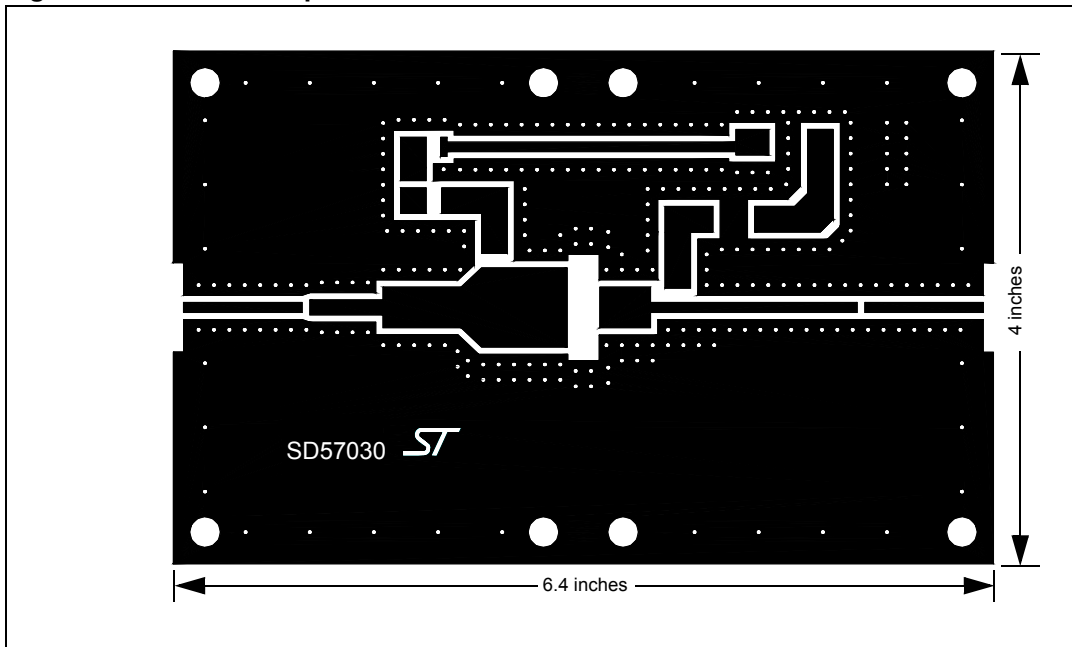


Figure 8. Test circuit photomaster



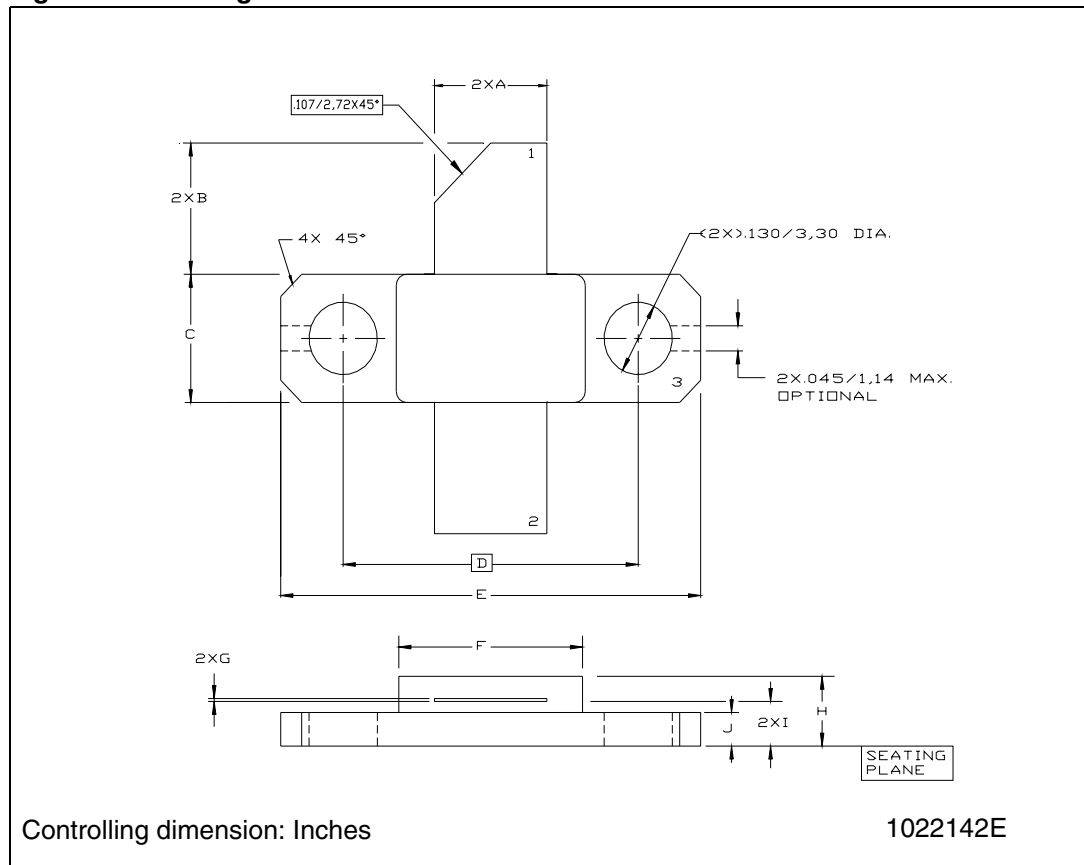


## 6 Package mechanical data

Table 6. M243 (.230 x .360 2L N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.21		5.72	0.205		0.225
B	5.46		6.48	0.215		0.255
C	5.59		6.10	0.220		0.240
D		14.27			0.562	
E	20.07		20.57	0.790		0.810
F	8.89		9.40	0.350		0.370
G	0.10		0.15	0.004		0.006
H	3.18		4.45	0.125		0.175
I	1.83		2.24	0.072		0.088
J	1.27		1.78	0.050		0.070

Figure 9. Package dimensions



## 7 Revision history

**Table 7. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
24-Mar-2003	5	First Issue.
11-Jul-2007	6	Document reformatted, added lead free info
24-Aug-2007	7	Cover page title updated

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