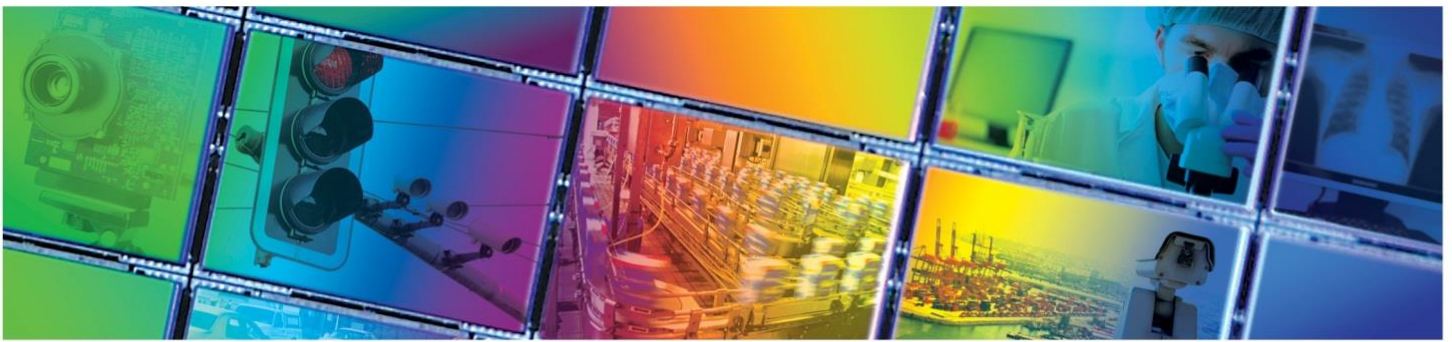


ON Semiconductor[®]



KAI-1003 IMAGE SENSOR

1024 (H) X 1024 (V) INTERLINE CCD IMAGE SENSOR



JUNE 11, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0025



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Summary Specification

KAI-1003 Image Sensor

DESCRIPTION

The KAI-1003 Image Sensor is a high-performance megapixel monochrome image sensor designed for a wide range of medical imaging and machine vision applications.

The 12.8 μm square pixels with microlenses provide high sensitivity and the large capacity results in large dynamic range. The two output, split horizontal register and several binning modes allow a 15 to 60 frame per second (fps) video rate for the progressively scanned images.

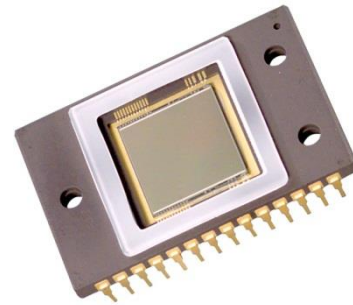
The vertical overflow drain structure provides antiblooming protection, and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

FEATURES

- Megapixel Progressive Scan Interline CCD
- 1024 (H) x 1024 (V) Imaging Pixels
- 12.8 μm Square Pixels
- 13.1 mm Square Imaging Area
- Microlenses for Increased Sensitivity
- Large capacity (170 ke)
- Split Horizontal Register for 1 or 2 Outputs
- Binning to 1 x 2 or 2 x 2

APPLICATIONS

- Machine Vision
- Medical
- Scientific



Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	1056 (H) x 1032 (V)
Number of Effective Pixels	1028 (H) x 1028 (V)
Number of Active Pixels	1024 (H) x 1024 (V)
Pixel Size	12.8 μm (H) x 12.8 μm (V)
Active Image Size	13.1 mm (H) x 13.1 mm (V) 18.5 mm (diagonal)
Aspect Ratio	1:1
Number of Outputs	1 or 2
Charge Capacity	170,000 electrons
Output Sensitivity	7.5 $\mu\text{V}/\text{e}^-$
Quantum Efficiency (500nm)	45%
Read Noise (f= 20MHz)	40 electrons rms
Dark Current	< 0.5 nA/cm ²
Dynamic Range	72 dB
Blooming Suppression	> 100X
Smear	-80 dB
Maximum Pixel Clock Speed	20 MHz
Maximum Frame Rates	15 fps (single output) 30 fps (dual output) 60 fps (dual output 2x2 bin)
Package	28 pin CerDIP
Cover Glass	AR Coated, 2 sides

Parameters above are specified at T = 40 °C unless otherwise noted.



Ordering Information

Catalog Number	Product Name	Description	Marking Code
2H4831	KAI- 1003-AAA-CR-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	KAI-1003 S/N
2H4828	KAI- 1003-AAA-CR-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Grade 2	
2H4440	KAI- 1003-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	KAI-1003M S/N
2H4544	KAI- 1003-ABA-CD-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	
4H0062	KEK-4H0062-KAI-1003/1004-12-20	Evaluation Board (Complete Kit)	n/a

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

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Device Description

ARCHITECTURE

The KAI-1003 is a high-performance, interline charge-coupled device (CCD) designed for a wide range of medical imaging and machine vision applications. The device is built using an advanced two-phase, double-polysilicon, NMOS CCD technology. The p+npn- photodiodes eliminate image lag while providing antiblooming protection and electronic shutter capability. The 12.8 μm square pixels with microlenses provide high sensitivity and large dynamic range. The two output, split horizontal register and several binning modes enable a 15 to 60 frame per second (fps) video rate with this megapixel progressive scan imager.

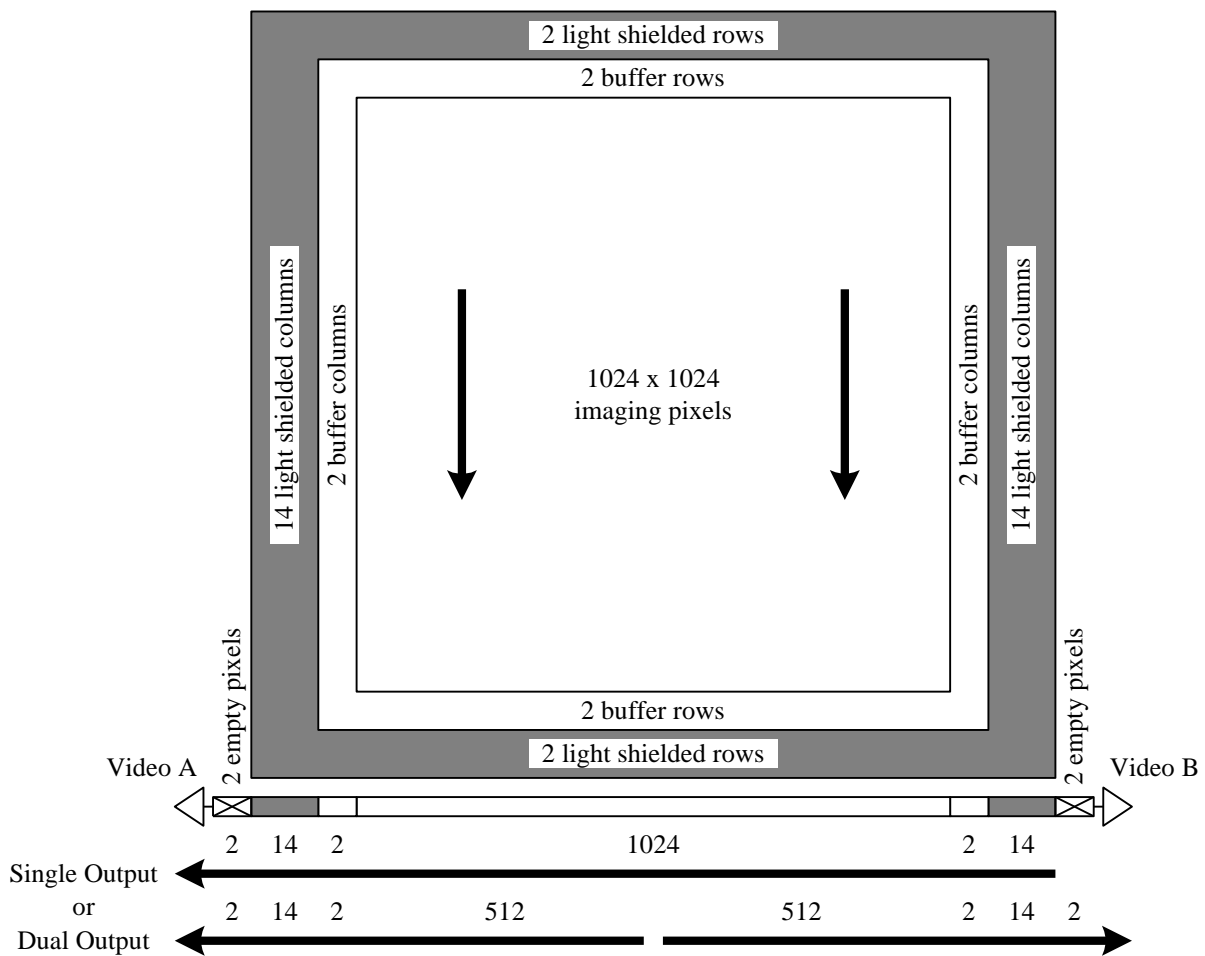


Figure 1: KAI-1003 Sensor Architecture



IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photodiode. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and integration time and nonlinearly dependent on wavelength. When the photodiode’s charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming. The integration time can be decreased below the frame time by using an electronic shutter, which is a voltage pulse applied to the substrate to empty the photodiodes.

CHARGE TRANSPORT

The integrated charge from each photodiode is transported to the output by a three-step process. The charge is first transferred from the photodiodes to the vertical shift registers by applying a large positive voltage to one of the vertical CCD phases. This transfer occurs simultaneously for all photodiodes. The charge is then transported from the vertical CCD registers to the horizontal CCD line by line in parallel. Finally, the horizontal CCD register transports each line of charge pixel by pixel serially to one or both of the output structures.

The single horizontal CCD register is split into two halves to allow a variety of line readout modes, as shown in Figure 1 and Figure 2. The A output half of the register is a true two-phase design, which results in unidirectional transport using phases H1A and H2A. The B output half of the register is a pseudo two-phase design, which allows bi-directional transport using phases H1B, H2B, H1C and H2C. Dual output is achieved with all of the first phases identical and all the second phases identical. If the clocks of H1A and H2A phases are shifted by one half cycle, the output remains dual with the outputs alternating, so that only one analog-to-digital converter is necessary. Finally, single output of the entire image from the A output is obtained by complementing the C phases, which reverses transport in the B half of the horizontal CCD.

Binning can be used in a 1x2 and a 2x2 mode. Two successive vertical transfers vertically bin the charge directly onto the horizontal CCD, as shown in Figure 11 and Figure 12. Horizontal binning is accomplished by two successive horizontal transfers onto the H22 gate, which then transfers the charge to the output structure, as shown in Figure 13.

Combinations of output modes, binning and horizontal clock frequency allow the range of frame rates listed in

HORIZONTAL CLOCK							
Frequency		20	20	20	40	20	MHz
Period	actual	50	50	50	25	50	ns
	effective	50	50	100	50	50	ns
Pixel counts	actual	532	532	532	532	1060	
	effective	532	532	266	266	1060	

VERTICAL TO HORIZONTAL TRANSFER (Horizontal Retrace Time)							
Equivalent H-clock counts (m)		80	80	80	160	80	
Duration		4.0	4.0	4.0	4.0	4.0	µs

HORIZONTAL LINE TIME							
Total H-clock counts		612	612	612	692	1140	
Line time		30.6	30.6	30.6	17.3	57.0	µs



VERTICAL CLOCK							
Line counts	actual	1032	1032	1032	1032	1032	
	effective	1032	516	516	516	1032	

PHOTODIODE READ (Vertical Retrace Time)							
Equivalent line counts (n)	4	4	4	7	2		
Duration	122.4	122.4	122.4	121.1	114.0		μs

FRAME RATE							
Total effective line counts	1036	520	520	523	1034		
Frame time	31.7	15.9	15.9	9.0	58.9		ms
Frame rate	31.5	62.8	62.8	110.5	17.0		frames/s

Table 1.

OUTPUT STRUCTURE

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (ϕ_R) is clocked to remove the signal and the FD is reset to the potential applied by the reset drain (RD). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the output pin of the device.



NON-IMAGING PIXELS

In addition to the 1024 (H) by 1024 (V) imaging pixels, there are active buffer, light shielded and empty pixels, as shown in Figure 1. A two-pixel border of active buffer pixels surrounds the imaging area. These buffer pixels respond to illumination but are not tested for defects and non-uniformities. Two light shielded rows lead and follow each frame, and 14 light shielded columns lead and follow each line. The light shielded columns are tested for column defects and can be used for dark reference. Only the center 10 columns by 1028 rows of light shielded region on each side can be used for dark reference due to light leakage into the border of two pixels at the edges. Finally, two empty pixels occur at the beginning of each line, which are empty shift register cycles not associated with any vertical CCD columns. Empty pixels may also occur at the end of the line, depending on the timing.

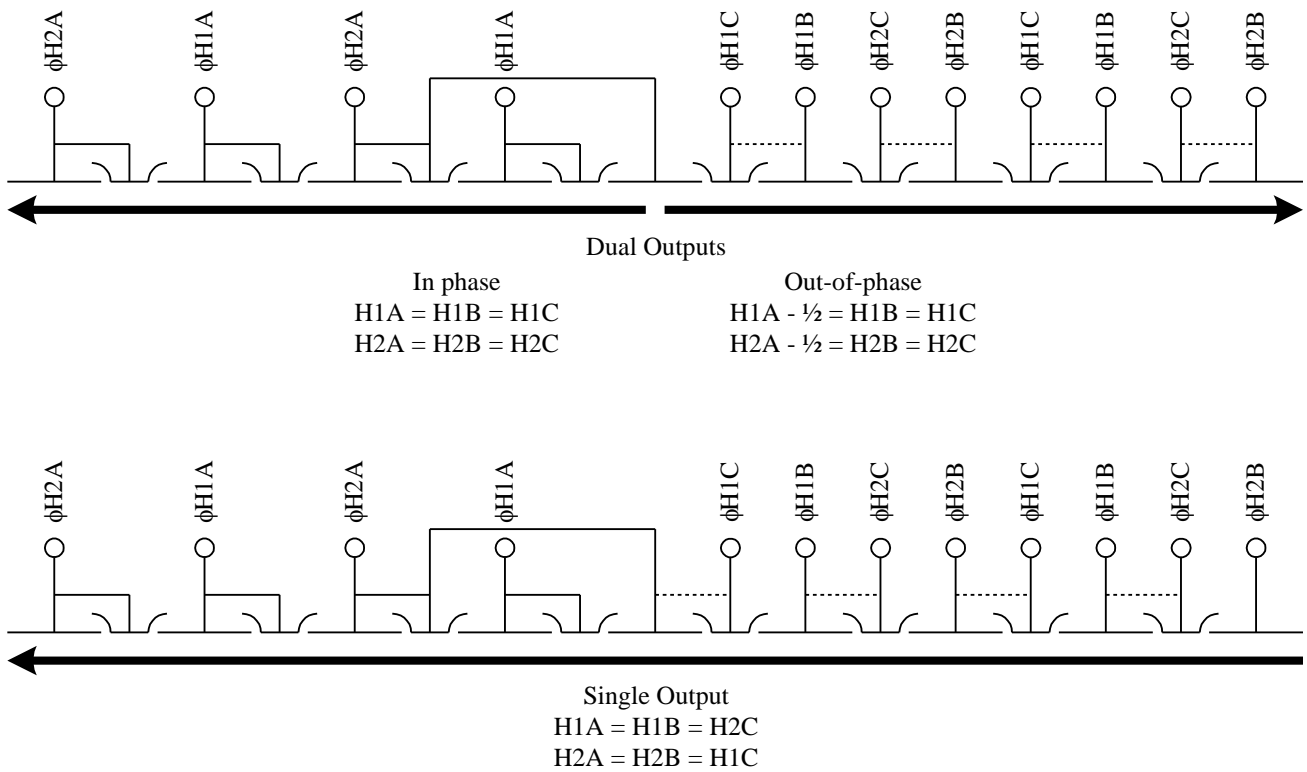


Figure 2: Horizontal CCD Registers



Binning (H x V)	1 x 1	1 x 2	2 x 2	2 x 2	1 x 1	Units
Output	Dual	Dual	Dual	Dual	Single	

HORIZONTAL CLOCK							
Frequency		20	20	20	40	20	MHz
Period	actual	50	50	50	25	50	ns
	effective	50	50	100	50	50	ns
Pixel counts	actual	532	532	532	532	1060	
	effective	532	532	266	266	1060	

VERTICAL TO HORIZONTAL TRANSFER (Horizontal Retrace Time)							
Equivalent H-clock counts (m)		80	80	80	160	80	
Duration		4.0	4.0	4.0	4.0	4.0	µs

HORIZONTAL LINE TIME							
Total H-clock counts		612	612	612	692	1140	
Line time		30.6	30.6	30.6	17.3	57.0	µs

VERTICAL CLOCK							
Line counts	actual	1032	1032	1032	1032	1032	
	effective	1032	516	516	516	1032	

PHOTODIODE READ (Vertical Retrace Time)							
Equivalent line counts (n)		4	4	4	7	2	
Duration		122.4	122.4	122.4	121.1	114.0	µs

FRAME RATE							
Total effective line counts		1036	520	520	523	1034	
Frame time		31.7	15.9	15.9	9.0	58.9	ms
Frame rate		31.5	62.8	62.8	110.5	17.0	frames/s

Table 1: KAI-1003 Calculated Clock Parameters

Notes:

1. Time values have been rounded.
2. The number of counts (n and m) shown here are nominal integers, but in general they do not need be integers. They can be adjusted for frame time, so long as the horizontal and vertical retrace times exceed the minimums specified in AC Timing Requirements.
3. Operation at 40 MHz will have increased readout noise.



PIN DESCRIPTION

Pin	Label
1	$\phi V1$
2	GND
3	SUB
4	VDD
5	VOUTA
6	VLG
7	RDA
8	ϕRA
9	OGA
10	SUB
11	$\phi H1A$
12	$\phi H2A$
13	$\phi H22A$
14	GND

Pin	Label
15	$\phi H22B$
16	$\phi H2B$
17	$\phi H2C$
18	$\phi H1C$
19	$\phi H1B$
20	OGB
21	ϕRB
22	RDB
23	VSS
24	VOUTB
25	VMIN
26	SUB
27	GND
28	$\phi V2$

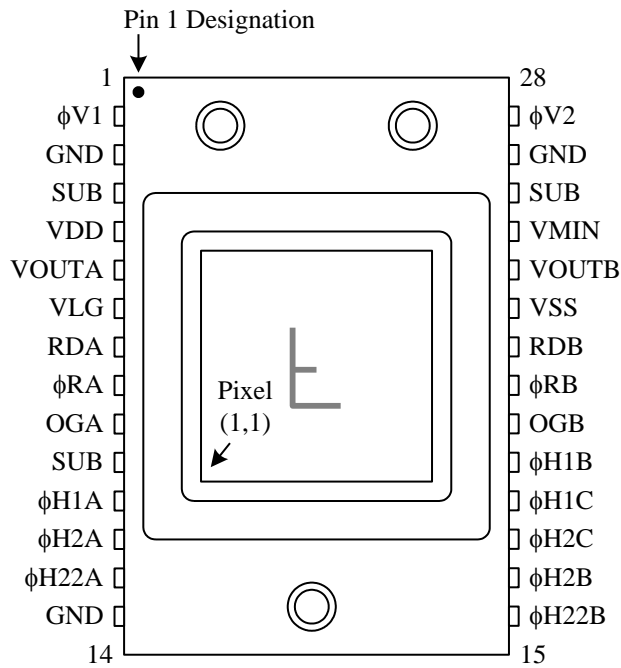


Figure 4: Package Pin Designation Top View



COVER GLASS SPECIFICATION

Item	Specification
Substrate	Schott D263T eco or equivalent
Thickness	0.030" ± 0.002"
Coating	Double-sided anti-reflecting coating on a 0.660" x 0.660" square for a transmission minimum of 98% in the 400 to 700nm wavelength.
Scratch	No scratch greater than 10 microns

Caution: Cover Glass Care and Cleanliness:

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided
3. Improper cleaning of the cover glass may damage these devices. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling and Best Practices*



Operation

ABSOLUTE MAXIMUM RATINGS

Item	Description	Min.	Max.	Units	Notes
Temperature	Operation to Specification	0	40	°C	
	Operation Without Damage	-10	70	°C	
	Storage	-55	80	°C	
Relative Humidity	Operation Without Damage	0	95	%	1
Voltage (Between Pins)	SUB - GND	-0.6	50	V	2, 5
	VRD, VSS, VDD - GND	-0.6	25	V	
	VMIN - GND	-15	0.6	V	
	All Clocks - GND		17	V	
	$\phi V1 - \phi V2$		17	V	3
	$\phi H1 - \phi H2$		17	V	
	$\phi H1, \phi H2 - \phi V2$		17	V	
	$\phi H2 - OG$		17	V	
	VLG, OG - GND		17	V	
Current	Output Bias Current (IDD)	-----	10	mA	4
Capacitance	Output Load Capacitance (CLOAD)	-----	10	pF	4

Notes:

1. Without condensation.
2. Under normal operating conditions, the substrate voltage should be maintained above 8.0 V. The substrate voltage should not remain above 25 V for longer than 100 μ s.
3. Maximum of 20 V for $\phi V1H - \phi V2L$, with 20 μ s maximum duration.
4. Each output.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.



DC OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Output Gate	OG	1.8	2.0	2.2	V	
Reset Drain	VRD	10.0	10.5	11.0	V	
Output Amplifier Return	VSS		0.0		V	1
Output Amplifier Load Gate	VLG	1.4	1.5	1.6	V	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	
Disable ESD Protection	VMIN		-8.5		V	2
Substrate	VSUB	8.0	TBS	18.0	V	3, 4, 5
Ground, P-well	GND		0.0		V	4

Notes:

1. Current sink.
2. Connect a 0.001 μ F capacitor between VMIN and GND. VMIN must be more negative than the low voltage of any of the ϕ H clocks and should be established before the ϕ H voltage is applied.
3. DC value when electronic shutter is not in use. See AC Clock Level Conditions for electronic shutter pulse voltage. The operating value of the substrate voltage, VSUB, will be supplied with each shipment.
4. Ground and substrate biases should be established before other gate and diode potentials are applied.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

AC CLOCK LEVEL CONDITIONS

Description	Level	Symbol	Min.	Nom.	Max.	Units	Notes
Vertical CCD Clocks	High	ϕ V2H	9.5	10.5	11.5	V	1
	Mid	ϕ V1M, ϕ V2M	-0.8	-0.5	0.0	V	1
	Low	ϕ V1L, ϕ V2L	-9.0	-8.5	-8.0	V	1
Horizontal CCD Clocks	High	ϕ H1H, ϕ H2H	4.5	5.0	5.5	V	1
	Low	ϕ H1L, ϕ H2L	-6.5	-6.0	-5.5	V	1
Reset clock	Amplitude	ϕ Rswing		5.0		V	
	Low	V ϕ Rlow	0	TBS	5.0	V	2
Electronic Shutter Pulse	Shutter	VShutter	37	40	45	V	3, 4

Notes:

1. For best results, the CCD clock swings must be greater than or equal to the nominal values.
2. Reset clock low level voltage will be supplied with each shipment.
3. Electronic shutter pulse voltage referenced to GND. See DC Operating Conditions for DC level when electronic shutter is not in use.
4. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.



ELECTRONIC SHUTTER OPERATION

Electronic shuttering is accomplished by pulsing the substrate voltage to empty the photodiodes. See Figure 14 for timing. The pulse must not occur while useful information is being read from a line.

CALCULATED CLOCK CAPACITANCE

Description	Phase	Symbol	Typical	Units	Notes
Vertical CCD Clocks	1 to GND	C ϕ V1	55/37	nF	1
	2 to GND	C ϕ V2	50/32	nF	1
	1 to 2	C ϕ V1 - ϕ V2	4	nF	
Horizontal CCD Clocks	1A	C ϕ H1A	58/21	pF	1,2
	1B	C ϕ H1B	41/13	pF	1,2
	1C	C ϕ H1C	15/10	pF	1,2
	2A	C ϕ H2A	48/22	pF	1,2
	2B	C ϕ H2B	30/11	pF	1,2
	2C	C ϕ H2C	18/13	pF	1,2
HCCD Summing Clock		C ϕ H22A/B	3	pF	
Reset clock - GND		C ϕ RA/B	5	pF	

Notes:

1. Accumulation/depletion capacitances.
2. Capacitance of this gate to GND and all other gates.

AC TIMING REQUIREMENTS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Vertical High Level Duration	T _{VZH}	15		20	μ s	
Vertical Transfer Time	T _V	1.0	2.0/1.0		μ s	1
Vertical Pedestal Delay 1 & 3	T _{VPD1} , T _{VPD3}	40			μ s	
Vertical Pedestal Delay 2	T _{VPD2}	15			μ s	
Horizontal Delay	T _{HD}	1.5/0.5			μ s	1
Reset Duration	T _R		10		ns	2
Horizontal CCD Clock Frequency	f _H		20		MHz	3
Pixel Time	T _H		50		ns	
Line Time	T _L					4
Frame Time	T _F					4
Clamp Delay	T _{CD}				ns	5
Sample Delay	T _{SD}				ns	5
Electronic Shutter Pulse Duration	T _{ES}	5	7.5	10	μ s	
Electronic Shutter Horizontal Delay	T _{ESHD}	1.0			μ s	

Notes:

1. Non-binning/binning times.
2. The rising edge of ϕ R should be coincident with the rising edge of ϕ H22, within ± 5 ns.
3. Horizontal CCD clock frequency can be increased to 40 MHz, with increased readout noise.
4. See Table 1 for nominal line and frame time in each mode.
5. The clamp delay and sample delay should be adjusted for optimum results.



CCD CLOCK WAVEFORM CONDITIONS

Non-binning

Description	Phase	Symbol	twh	twl	tr	tf	Units	Notes
Vertical CCD Clocks	1	$\phi V1M/L$	-----	1.5	0.5	0.5	μs	
	2	$\phi V2M/L$	1.5	-----	0.5	0.5	μs	
	2, High	$\phi V2H$	15	-----	1.0	1.0	μs	
Horizontal CCD Clocks	1	$\phi H1$	20.5	21.5	4.0	4.0	ns	
	2	$\phi H2$	20.5	21.5	4.0	4.0	ns	
	2, Binning	$\phi H22$	20.5	21.5	4.0	4.0	ns	1
Reset clock		ϕR	5	39	3	3	ns	

2 x 2 binning

Description	Phase	Symbol	twh	twl	tr	tf	Units	Notes
Vertical CCD Clocks	1	$\phi V1M/L$	0.5	0.5	0.5	0.5	μs	2
	2	$\phi V2M/L$	0.5	0.5	0.5	0.5	μs	2
	2, High	$\phi V2H$	15	-----	1.0	1.0	μs	
Horizontal CCD Clocks	1	$\phi H1$	20.5	21.5	4.0	4.0	ns	
	2	$\phi H2$	20.5	21.5	4.0	4.0	ns	
	2, Binning	$\phi H22$	46.0	46.0	4.0	4.0	ns	
Reset clock		ϕR	5	89	3	3	ns	

Notes:

1. Typical values measured with clocks connected to image sensor device. The actual values should be optimized for particular board layout.
2. $\phi H22$ may be connected to $\phi H2$ in 1x1 mode.
3. Twh and twl for $\phi V1M/L$ and $\phi V2M/L$ are the time periods during the double pulses.

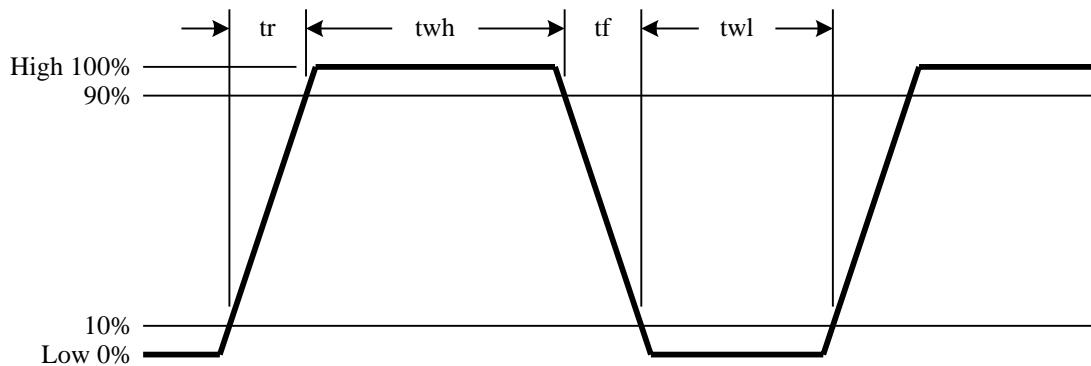


Figure 5: CCD Clock Waveform



Frame Timing - 1 x 1

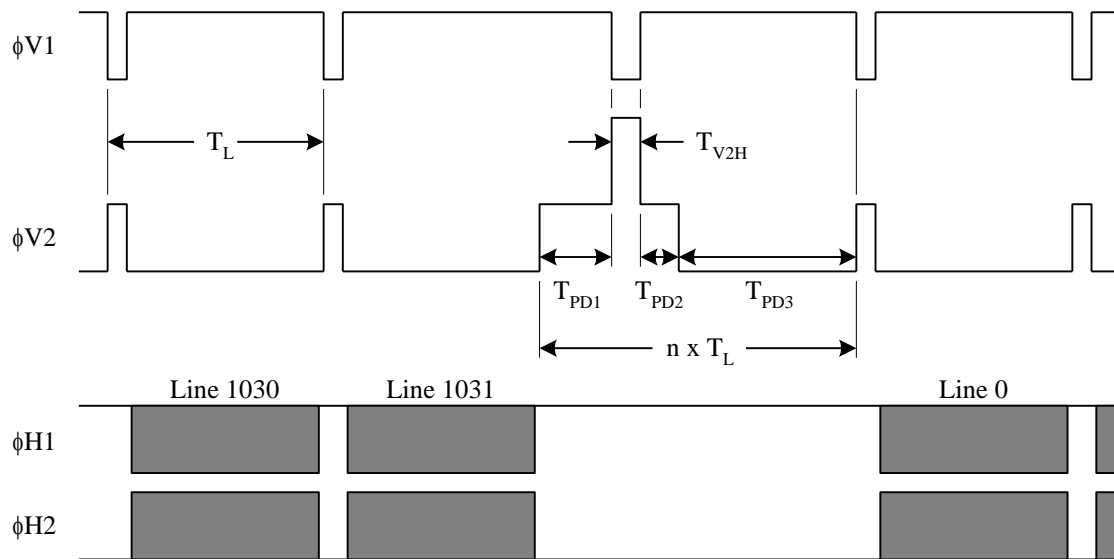
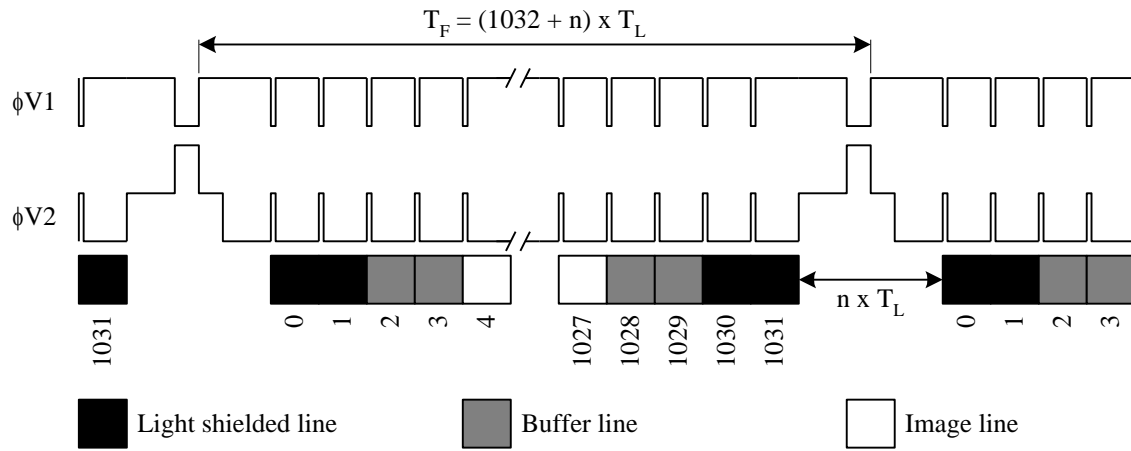


Figure 6: Frame Timing - 1 x 1



Line Timing - 1 x 1 - Dual Output, In-phase

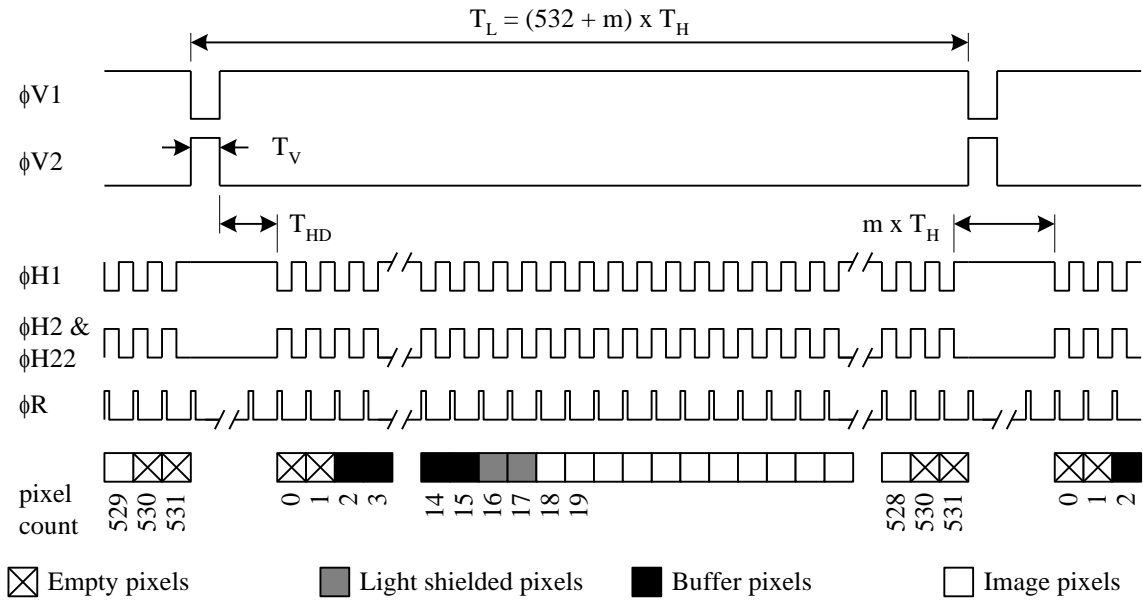


Figure 7: Line Timing - Dual Outputs, In-phase



Line Timing - 1 x 1 - Dual Output, Out-of-phase

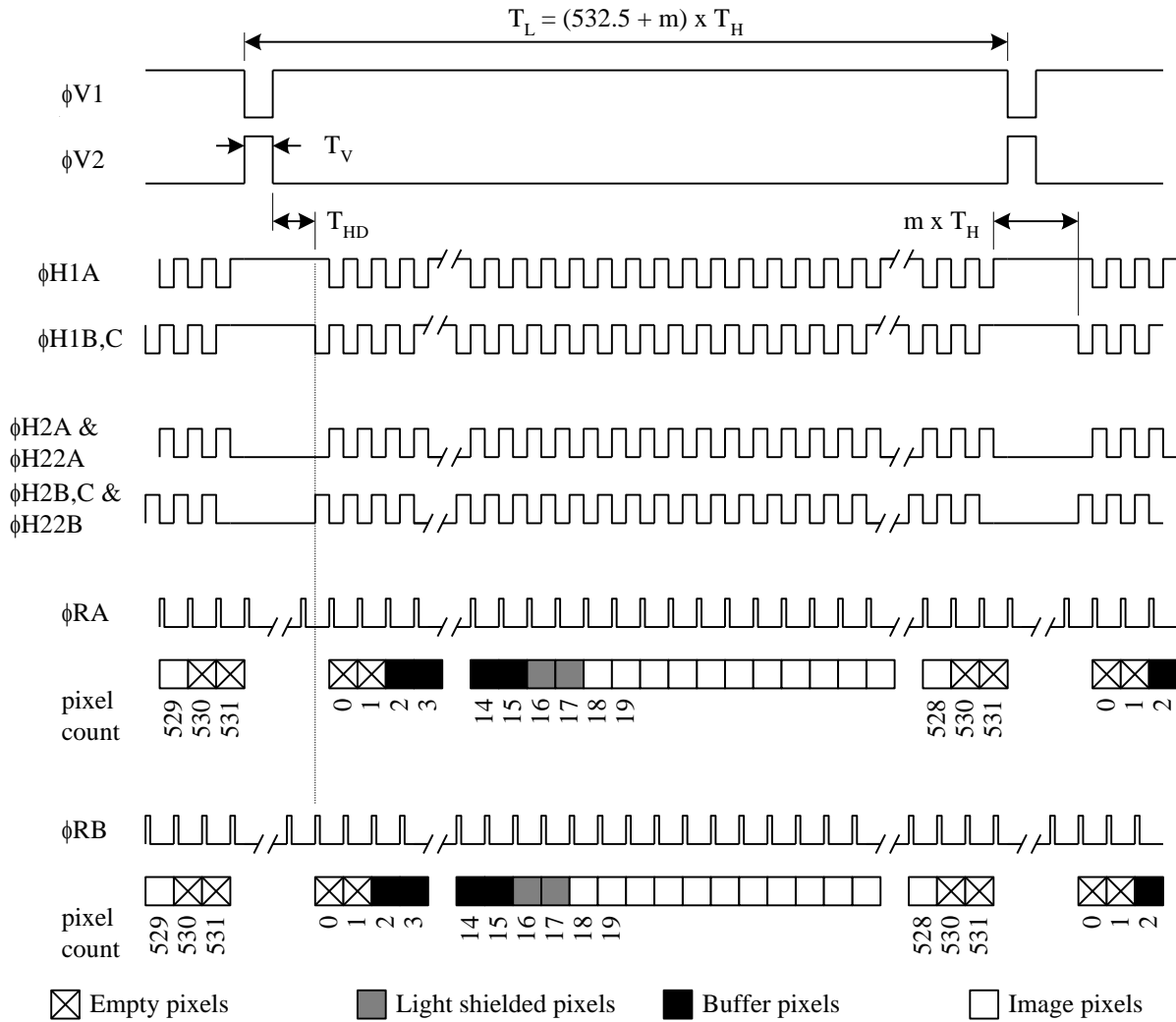


Figure 8: Line Timing - 1 x 1 - Dual Outputs, Out-of-phase



Line Timing - 1 x 1 - Single Output

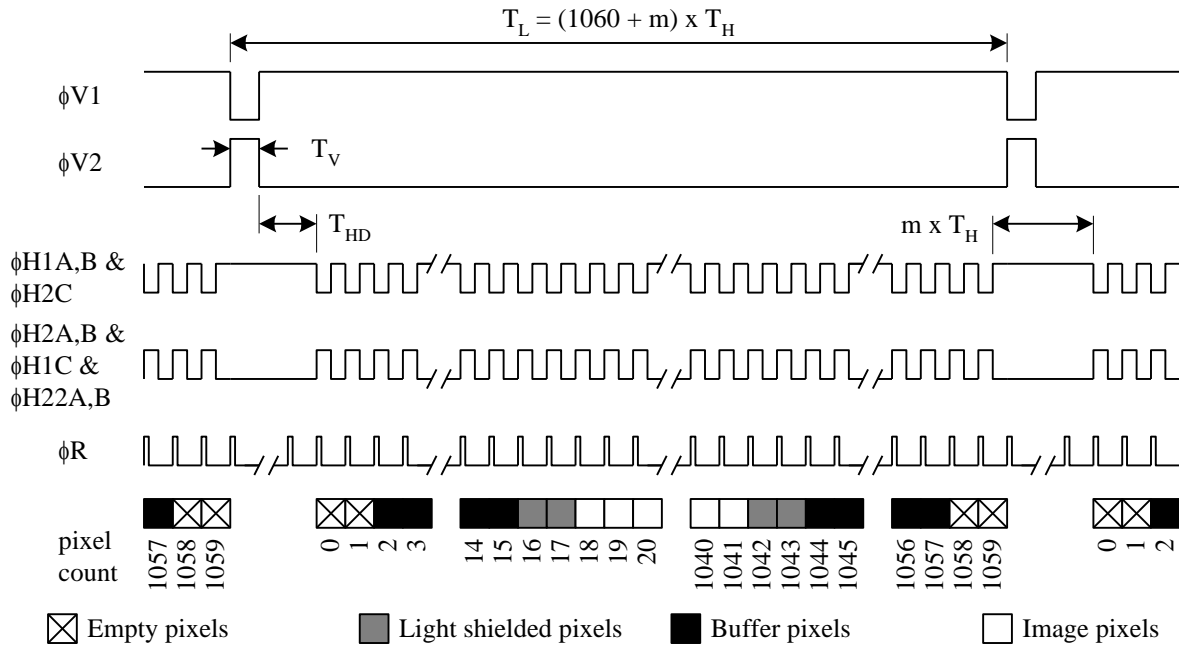


Figure 9: Line Timing - 1 x 1 - Single Output



Pixel Timing - 1 x 1

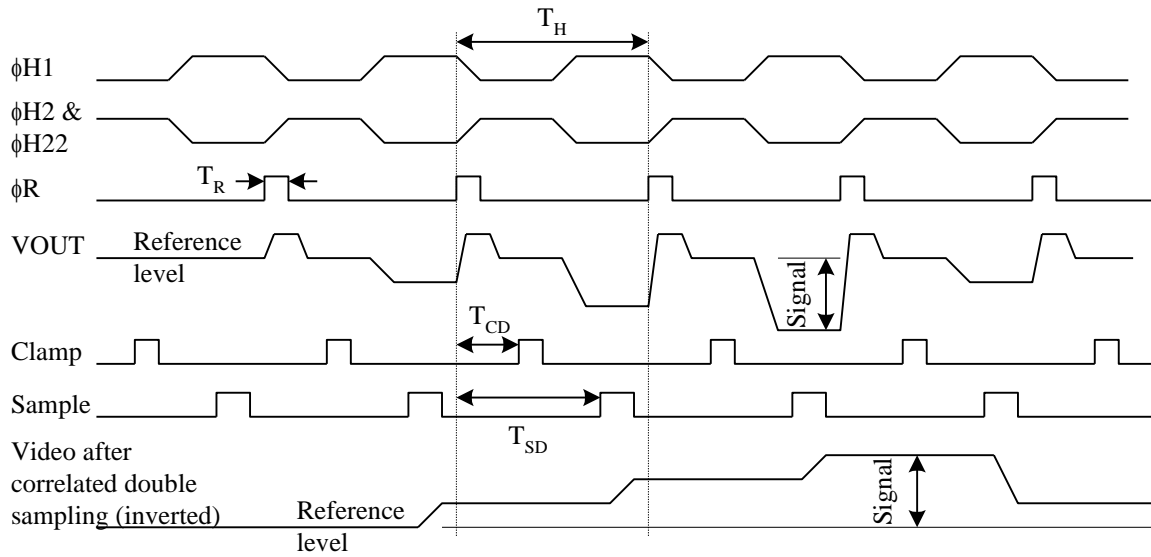


Figure 10: Pixel Timing - 1 x 1



Frame Timing - 2 x 2

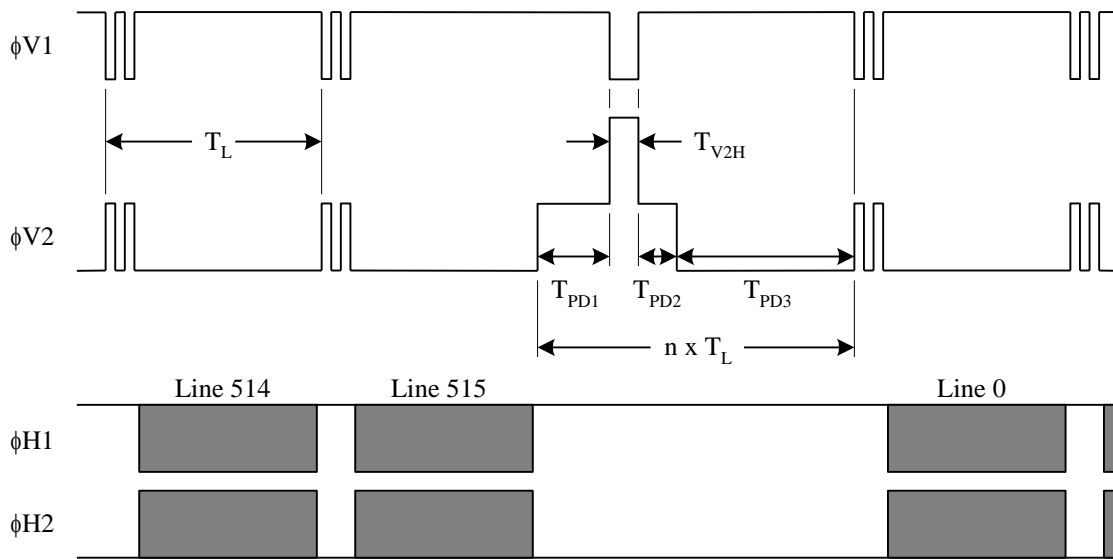
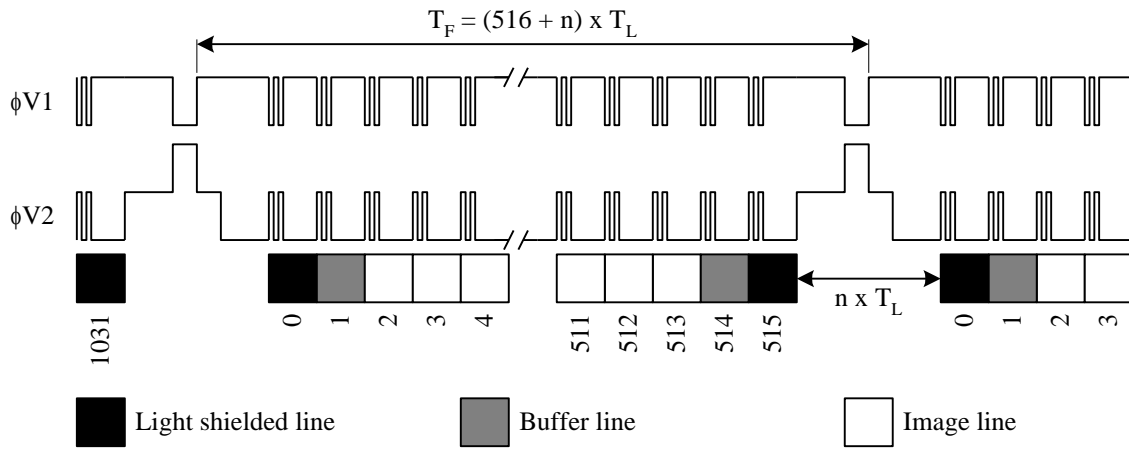


Figure 11: Frame Timing - 2 x 2



Line Timing - 2 x 2

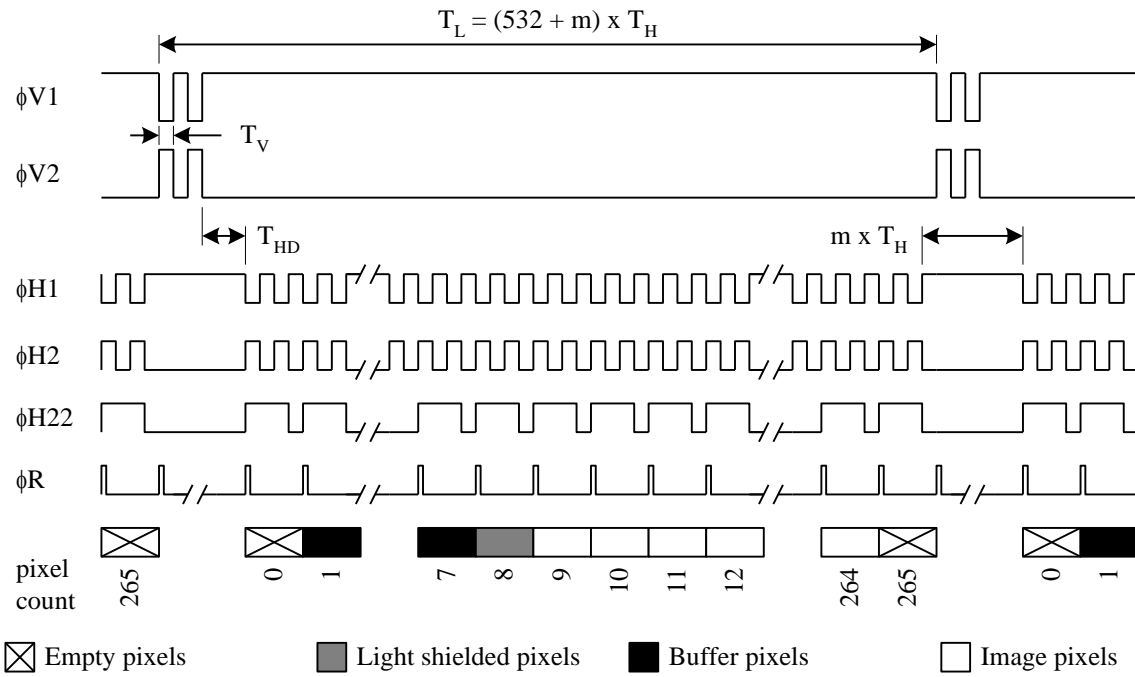


Figure 12: Line Timing - 2 x 2

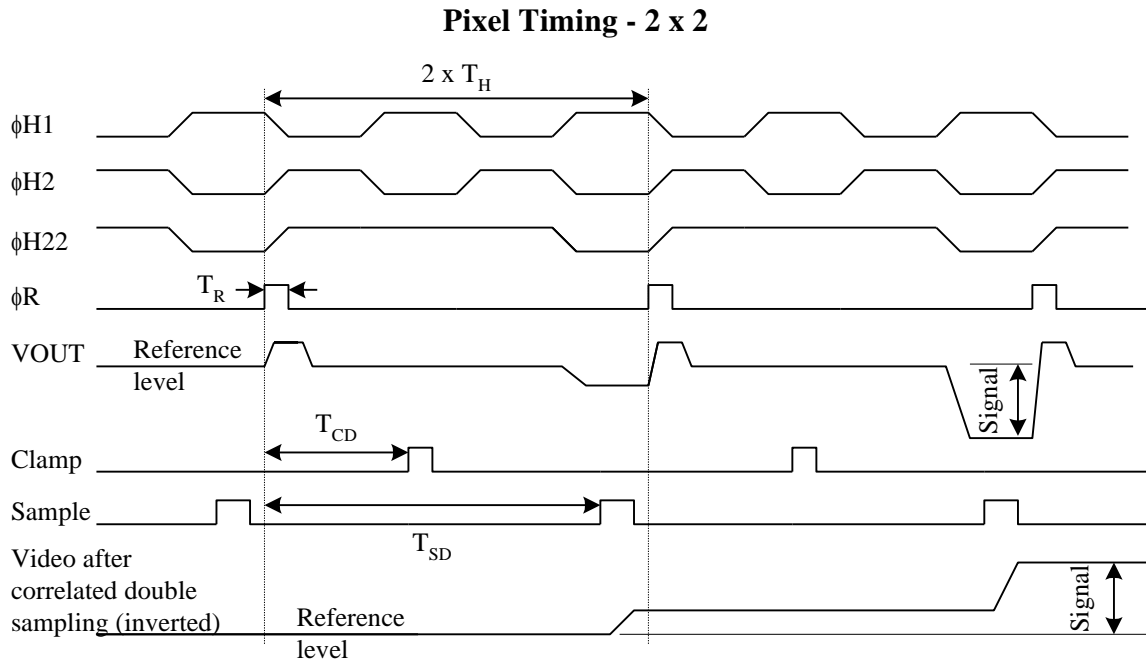
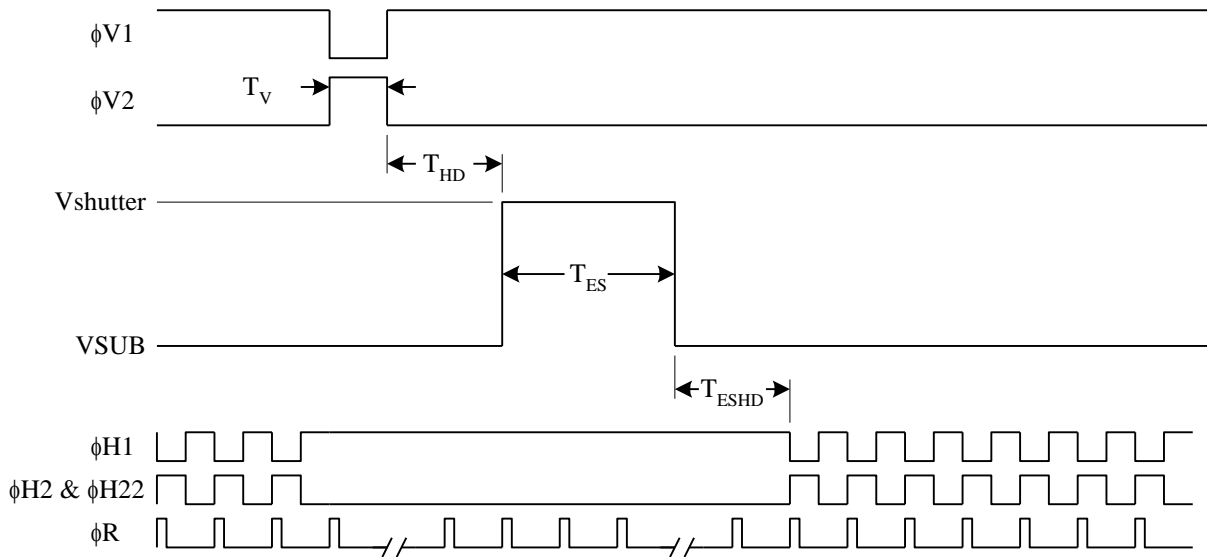


Figure 13: Pixel Timing - 2 x 2



Electronic Shutter Line Timing



Integration Time Definition

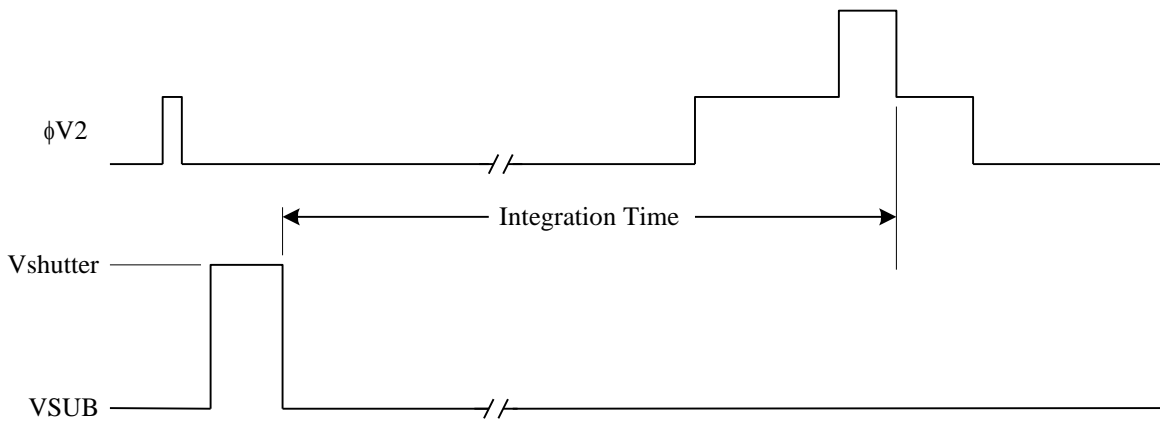


Figure 14: Electronic Shutter Timing



Performance Specifications

All values measured at 40 °C and 30 frames/s (integration time = 33 ms, fH = 20 MHz) for nominal operating parameters unless otherwise noted. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation charge capacity with blooming control	Q_{sat}	170			ke^-	
Output gain		6.5	7.5	8.5	$\mu V/e^-$	
Output voltage at the saturation level	V_{sat}		1.3		V	
Quantum efficiency at 500 nm			32		%	
Quantum efficiency at 540 nm			30		%	
Quantum efficiency at 600 nm			24		%	
CCD readout noise with CDS			40	50	$e^- rms$	
Dark current	I_{dark}		0.25	0.45	nA/cm^2	
Antiblooming factor	X_{ab}	100				1, 2
Vertical smear			0.005	0.01	%	2, 6
Nonuniformity of sensitivity			0.3	0.5	% rms	3, 4
Nonuniformity of dark current			14		$e^- rms$	4
Output signal nonlinearity			1	2	%	5
Gain difference between the two video outputs				10	%	5
Nonuniformity of gain between the two outputs			0.5	1.5	%	5

Notes:

1. The illumination required to bloom the image sensor reported as a multiple of the saturation intensity. Blooming is defined as doubling the vertical height of a spot that is 10% of the vertical CCD height at the saturation intensity.
2. Measured with continuous green light centered at 550 nm, F/4 optics and a spot size that is 10% of the vertical CCD height.
3. Measured at 90% of 150 ke^- output.
4. Measured in the center 50 x 50 pixels.
5. Between 10% and 90% of 150 ke^- output.
6. Measured without electronic shutter operation.



TYPICAL QUANTUM EFFICIENCY

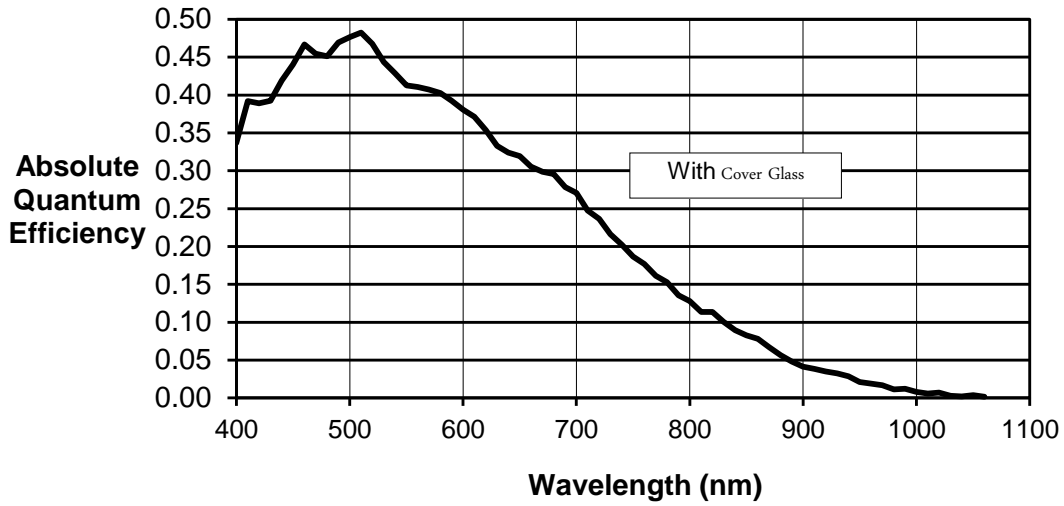


Figure 15: Quantum Efficiency Spectrum

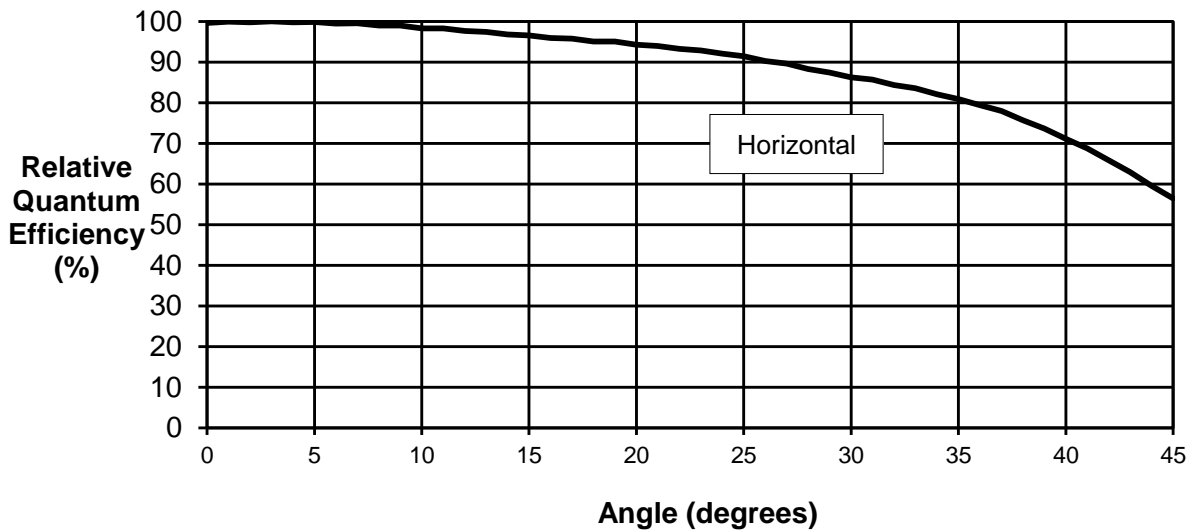


Figure 16: Angular Dependence of Quantum Efficiency

For the curve marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.



Defect Specifications

DEFECT TEST CONDITIONS

Temperature: 40 °C
 Integration time: 33 ms (20 MHz HCCD frequency, no binning, 30 fps frame rate)
 Light source: Continuous green light centered at 550 nm
 Operation: Nominal voltages and timing

DEFECT DEFINITIONS

Name	Maximum Number	Definition
Major Defective Pixel	20	A pixel whose signal deviates by more than 25 mV from the mean value of all active pixels under dark field condition or by more than 8% from the mean value of all active pixels under uniform illumination at 105 ke ⁻ output signal.
Minor Defective Pixel	100	A pixel whose signal deviates by more than 8mV from the mean value of all active pixels under dark field condition.
Cluster Defect	4	A group of 2 to 6 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.
Column Defect	0	A group of more than 6 contiguous major defective pixels along a single column.

DEFECT PROXIMITY

Minimum distance between defective clusters: 2 pixels in all directions without major pixel defects

Minimum distance between defective columns: 3 columns without column defects or cluster defects



Storage and Handling

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

ENVIRONMENTAL EXPOSURE

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight

for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.

2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.



Quality Assurance and Reliability

QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.



Revision Changes

MTD/PS-0601

Revision Number	Description of Changes
4.0	<ul style="list-style-type: none"> Page 3 Figure 1 – Changed caption from “Pixel Architecture” to “Sensor Architecture” Page 8 Figure 4 – Package Pin Designations – Top View Corrected Pixel 1,1 location Page 11 DC Operating Conditions, note 2 – changed μf to μF. Page 23 Performance Specifications – added frequency used to obtain 30 frames per second operation, $f_H = 20 \text{ MHz}$. Page 26 – Updated Quality Assurance and Reliability section. Updated web site, e-mail and phone number information.
4.1	<ul style="list-style-type: none"> Page 9 – Add cover glass cleanliness caution. Page 10 – Added to the maximum absolute rating table ϕR, ϕH1, ϕH2 – VMIN. Page 10 – Update ESD caution. Page 25 – Updated major defective pixel definition. Changed bright field threshold from 15% to 8%.
5.0	<ul style="list-style-type: none"> Page 27 – Updated Part Number Availability Table
6.0	<ul style="list-style-type: none"> Updated format Added Summary Specification page Moved location of Ordering Information page Added Handling section. Moved ESD cautions from Operation page to Handling page Added the note “Refer to Application Note <i>Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions</i>” to the following sections <ul style="list-style-type: none"> DC Operating Conditions AC Clock Level Conditions Handling

PS-0025

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> Initial release with new document number, updated branding and document template Updated <i>Storage and Handling</i> and <i>Quality Assurance and Reliability</i> sections
1.1	<ul style="list-style-type: none"> Updated branding

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