ZARLINK SEMICONDUCTOR

VoiceEdge

Le5712

Dual Subscriber Line Interface Circuit

VE580 Series

APPLICATIONS

- **Ideal for low-cost, high performance line card applications (CO, DLC)**
- **Meets requirements for countries such as: India, China, Korea, Japan, Taiwan, and Australia**
- **Meets requirements for North America DLC applications (TR-57-CORE)**

FEATURES

- **Dual-Channel SLIC device with small footprint**
- **Loop start and Ground start support**
- **+5 V and battery supply required**
- **Optional dual battery operation**
- **–39 to –60 V battery operation**
- **Supplies more than 20 mA into 2000 Ω from –48 V**
- **Programmable current limit**
- **On-chip Thermal Management (TMG) feature in all Active states**
- **Low standby power (24 mW per channel)**
- **Supports 2.0 Vrms metering applications**
- **Control states: Active and Active Metering (Normal and Reverse Polarity), Standby, Tip Open and Disconnect**
- **3.3-V compatible to logic control inputs**
- **Power up in Disconnect state**
- **On-hook transmission in Active states**
- **Per-channel fault detection and indication**
- **Per-channel thermal shutdown**
- **Programmable Off Hook and Ground Start thresholds.**
- **Programmable ring-trip detect threshold**
- **Footprint compatible with Zarlink's Le5711 Dual SLIC**

ORDERING INFORMATION

Device	Package Type[1]	Packing[2]
Le57D121BTC	44-pin eTQFP (Green), –53 dB, Reverse Polarity	Tray
Le57D122BTC	44-pin eTQFP (Green), –63 dB, Reverse Polarity	

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

DESCRIPTION

The innovative Le5712 dual-channel SLIC device is designed for high-density POTS applications requiring a small-footprint, low-power SLIC device. By combining a fully featured line interface of two channels into one SLIC device, the Le5712 device enables the design of a low-cost, high performance, and fully programmable line interface for multiple country applications worldwide, including Ground Start and metering capability. The on-chip Thermal Management (TMG) feature allows for significantly reduced power dissipation on the device. Optional dual battery operation to reduce total power consumption is also available. The device is offered in a thermally efficient, space-saving 44-pin eTQFP package. The 12 x 12 mm footprint allows designers to make a dramatic increase in the density of lines on a board. The Le5712 device is also designed to significantly reduce the number of external components required for line card design.

Zarlink offers a range of compatible SLAC™ devices that perform the codec function in a line card. In particular, the Zarlink Quad and Octal SLAC devices combined with the Le5712 device provides a programmable line circuit that can be configured for varying requirements.

RELATED LITERATURE

- **081110 Thermal Management for the Le5711 and Le5712 SLIC Devices Application Note**
- **080900 Le5711 and Le5712 Comparison Brief Application Note**
- **080753 Le58QL02/021/031 QLSLAC™ Data Sheet**
- **080754 Le58QL061/063 QLSLAC™ Data Sheet**
- **080921 Le58083 Octal SLAC™ Data Sheet**
- **080676 Le5711 Dual SLIC Data Sheet**

BLOCK DIAGRAM

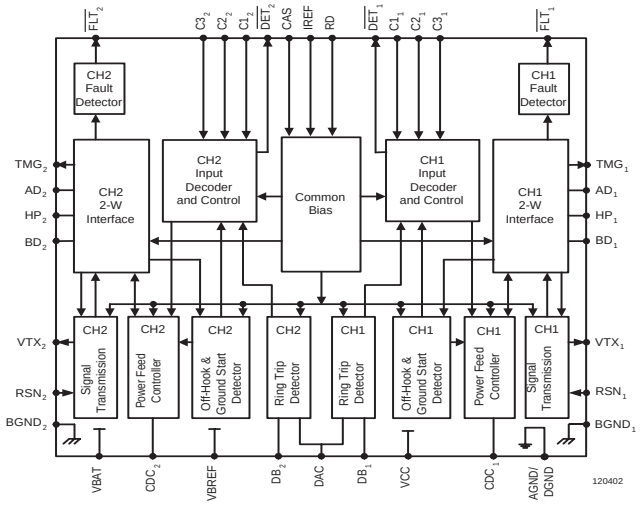

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TABLE OF CONTENTS

PRODUCT DESCRIPTION

The Le5712 device is designed for long loop high-density POTS applications requiring a low power, small footprint SLIC device. The Le5712 device increases line card density by integrating two SLIC devices into a single 44-pin package. This reduction in board space permits a higher density line card, which allows for amortizing common hardware across more channels. The Le5712 device gives line card designers a simple control interface that supports seven states: Active, Active Metering, Reverse Polarity, Reverse Polarity Metering, Standby, Tip Open and Disconnect (Ringing). The low cost and high performance Le5712 device provides the key features for POTS markets requiring loop start, loop start and metering, or ground start. The device includes a thermal management feature for minimizing power dissipation on the SLIC. Alternatively, the device can be operated in a dual battery configuration to reduce overall power consumption.

BLOCK DESCRIPTIONS

Two-Wire Interface

The two-wire interface provides DC current and sends voice and signalling information to a customer premise equipment. The two-wire interface also receives the returning signals from the customer premise equipment.

This block implements the thermal management feature, which allows power that would otherwise be dissipated within the package to be off loaded into an external resistor when the line is Off Hook. R_{TMGi} is connected from TMG_i to the VBAT pin and limits power within the SLIC device (Note: "i" denotes channel number).

The minimum value of R_{TMGi} is given by:

$$R_{TMG} \geq \frac{|BAT_{MAX}| - 6 - I_{LIMITMIN} \cdot (2 \bullet R_F + R_{LMIN} + 40\Omega)}{I_{LIMITMIN} - 3\ mA}$$

where $I_{LIMITMIN}$ is the minimum programmed loop current limit and R_{LMIN} is the minimum loop resistance. The tolerance of R_{TMG} should be taken into account when selecting a value that meets this requirement. For example, if BAT_{MAX} = -56 V, $I_{LOOPMIN}$ = 30 mA and R_{LMIN} = 200 Ω then R_{TMG} = 1.5 kΩ is the minimum recommended value. A value of 1.8 kΩ with 5% accuracy will keep the power in R_{TMG} below 1.0 W, and the total worst case SLIC power dissipation with both channels active below 1.6 W.

The power dissipated in the TMG resistor is given by:

$$P_{RTMG} = \frac{(|BAT| - 5 - I_L \bullet (R_L + 2R_F + 40))^2}{R_{TMG}}$$

where I_L is the loop current, and R_L is the loop resistance.

The maximum power on R_{TMG} is given by:

$$P_{RTMGmax} = \frac{(|BAT|_{max} - 5 - I_{LIMITmin}(R_{Lmin} + 2R_F + 40))^2}{R_{TMGmin}}$$

And the power dissipated per channel in the SLIC device while in the Active states is given by:

$$P_{SLICi} = 0.003|BAT| + (|BAT| - 3 - I_L(R_L + 2R_F + 40))\left(I_L - \frac{I}{R_{TMG}}(|BAT| - 5 - I_L(R_L + 2R_F + 40))\right)$$

The maximum power dissipated per channel in the SLIC device while in the Active states is given by:

$$P_{SLICmaxi} = 0.003|BAT|_{max} + \left(1 + \frac{I_{LIMITmax}}{2}R_{TMGmax}\right)\left(\frac{I_{LIMITmax}}{2} + \frac{1}{R_{TMGmax}}\right)$$

Refer to the *Thermal Management for the Le5711 and Le7512 Dual SLIC Devices Application Note* for further analysis and for dual battery condition.

The AC signal swing supported by the two-wire interface is controlled by the SLIC state. For standard voice transmission, the Active and Reverse Polarity states are used. To support voice plus meter pulses, the Active Metering and Reverse Polarity Metering states are provided which have increased overhead to support 2.0 Vrms metering.

Signal Transmission

The RSN_i input current controls the receive current sent to the two-wire interface. The AC line voltage is sensed by a differential amplifier between the AD_i and HP_i leads. The output of this amplifier is equal to the AC metallic components of the line voltages and is output at VTX_i.

The desired two-wire AC input impedance, Z_{2WIN}, is defined by the fuse resistors, R_F, and an impedance connected from VTX_i to RSN_i, Z_{Ti}. When computing Z_{Ti}, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.

$$Z_{Ti} = \frac{500}{3} \cdot (Z_{2WIN} - 2R_F)$$

To set the desired receive gain (G_{42L}) into a load Z_L from VRX_i, Z_{RXi} is connected from VRX_i to RSN_i, where

$$Z_{RXi} = \frac{Z_L}{G_{42L}} \bullet \frac{500 \bullet Z_T}{Z_T + \frac{500}{3}(Z_L + 2R_F)}$$

The transmission block also contains a longitudinal feedback circuit to shunt longitudinal signals to a DC bias voltage. The longitudinal feedback does not affect metallic signals.

Two application circuits, provided at the end of this data sheet, show how the Le5712 device can connect directly to pins of a QLSLAC codec.

The *POTS Application Circuit (POTS with no metering)*, on page 18 shows an application providing Loop Start and Ground Start capability. The components selected for the transmission network allow a wide range of market transmission requirements to be met when combined with the programmable QLSLAC device. In addition, transmit relative levels of Li = +4 to -4 dBr and receive relative levels of Lo = 0 to -8dBr can be supported using only the digital gain within the QLSLAC device for all markets. This configuration will meet ITU Q.552 and GR57 requirements.

The *Pulse Metering Application Circuit (Pots with metering)*, on page 20 shows a configuration for use in a 12 or 16 kHz pulse metering application with the QLSLAC device. The design allows 2 Vrms into 200 Ω, and supports gain ranges of at least Li = 0 to +4dBr, and Lo = 0 to -8 dBr. This configuration will meet ITU Q.552 requirements over these gain ranges for markets such as India and China.

The relationship between metering source V_M, the feeding resistance, R_M, and the output voltage at tip-ring, V_{TR}, is given in the following equation. The load at tip-ring is R_M. R_F is the protection and other, if any, front-end resistances. Z_T is the impedance between VTX and RSN at metering frequency.

$$V_{TR} = \frac{Z_M}{R_M} \bullet \frac{500}{1 + \frac{500}{3} \bullet \frac{Z_M + 2R_F}{Z_T}} V_M$$

Metering signal at VTX needs to be filtered to prevent from overloading the codec. This has been realized in the applications circuitry in this document.

Power Feed Controller and Common Bias

The power feed controllers have three sections: (1) the common bias circuit, (2) the battery feed circuit, and (3) the reverse polarity circuit which operate in all Active states.

The bias circuit provides a signal which sets the current limit and creates a voltage related to V_{BAT}, filtered by a capacitor connected to the CAS pin, to the battery feed circuit.

The nominal current limit is set by the following equation: $I_{LIMIT} = \frac{470}{R_{REF}}$

A recommended 3 Hz filter pole frequency (f_c) can be implemented from: $C_{CAS} = \frac{1}{RI_{AS} \bullet 2 \bullet \pi \bullet f_c}$

The battery feed circuit regulates the amount of DC current and voltage supplied to the telephone over a wide range of loop resistance. It is designed to operate over a nominal 22 to 33 mA range of programmed current limit. It produces a filtered reference voltage offset from the subscriber line voltage which is applied to the two-wire interface.

In addition, a low pass filter is implemented with a capacitor connected to the CDC_i pin.

In the low power Standby state, an alternative feed is implemented via two current limited on chip 200-Ω resistors. The nominal loop current below current limit in the Standby state is given by: $I_{STANDBY} = \frac{|V_{BAT}| - 4\ V}{600\ \Omega + R_L}$

Input Decoder and Control

The input decoder and control block provides a means for a microprocessor or SLAC device IC to control such system states as Active, Active Metering, Reverse Polarity, Reverse Polarity Metering, Standby, Tip Open and Disconnect (Ringing). The input decoder and control block has TTL-compatible inputs, permitting interfacing to 5 or 3.3 V VCC controllers which set the operating states of the SLIC device. It also provides the loop supervision signal sent back to the controller.

From power up, the device is in disconnect state unless over-written by external control inputs.

Device State Decoding

(For channel i = 1 or 2)

State	$C3_i$	$C2_i$	$C1_i$	Two-Wire state	$\overline{DET}_i$ output
0	0	0	0	Reserved	N/A
1	0	0	1	Active Metering	OHD
2	0	1	0	Tip Open	GSD
3	0	1	1	Reverse Polarity Metering	OHD
4	1	0	0	Disconnect	RTD
5	1	0	1	Active	OHD
6	1	1	0	Standby	OHD
7	1	1	1	Reverse Polarity	OHD

Off-Hook Detector (OHD)

The On-to-Off-hook and Off-to-On-hook detections are based on loop current and are defined as $|I_{AD} - I_{BD}| / 2$. The On-to-Off-hook (OHD) and Off-to-On-hook (OND) thresholds are programmed with the R_D resistor and the threshold applies to all Active and Standby states.

$$I_{OHD} = \frac{935V}{R_D}$$

$$I_{OHD} = I_{OND} + Hysteresis$$

Upon the loss of battery the $\overline{DET}$ pin will be HIGH.

Off-hook detection or $\overline{DET}$ state should be ignored during on-hook metering.

Ground Start Detector (GSD)

This detector is active in the Tip Open state. The threshold, I_{GSD}, is defined by the same equation used for the OHD.

For ground start lines, the device is in the Tip Open state between calls. When a ring ground condition is detected, the device should be switched to the Active state. During this period, the $\overline{DET}$ pin will be active if the ring to ground current is greater than twice the I_{OHD} threshold. The $\overline{DET}$ pin will go active once the ring ground is removed and a loop is applied. It is recommended that a firmware time-out period is applied in case the call attempt is abandoned and $\overline{DET}$ never goes low. The time-out is reset once an active $\overline{DET}$ is seen in the Active state.

Ring-Trip Detector

In the Disconnect state, the ring-trip detector is active. While the DB_i pin is more negative than the DAC pin, the $\overline{DET}$ pin will be High to indicate on hook. When an off hook condition occurs, the DB_i pin becomes more positive than the DAC pin, and the $\overline{DET}$ pin will go Low to indicate off hook during ringing (ring-trip) has been detected. The system implements the Ringing state using external control of a ring relay in combination with the Disconnect SLIC device state, which enables the ring-trip detector.

The *POTS Application Circuit (POTS with no metering)*, on page 18 shows a ring trip bridge configured and components are selected for a typical battery-backed ringing applications such as for the US (TR-57) and China (GF002).

The *Pulse Metering Application Circuit (Pots with metering)*, on page 20 shows a ring trip bridge configured and components are selected for a typical earth-backed ringing applications such as in India (G/LLT and G/MLT).

Fault Detector

The DSLIC device provides a fault detection function in the Active states on each channel. Under a fault condition the detector senses longitudinal voltage at tip and ring and flags a fault by pulling the $\overline{FLT}_i$ pin Low. The $\overline{FLT}_i$ pins are compatible with logic outputs, and may be monitored to clearly identify a fault condition from a loop condition.

In case of low level longitudinal AC induction the $\overline{FLT}_i$ may pulse at twice the frequency of the induction signal.

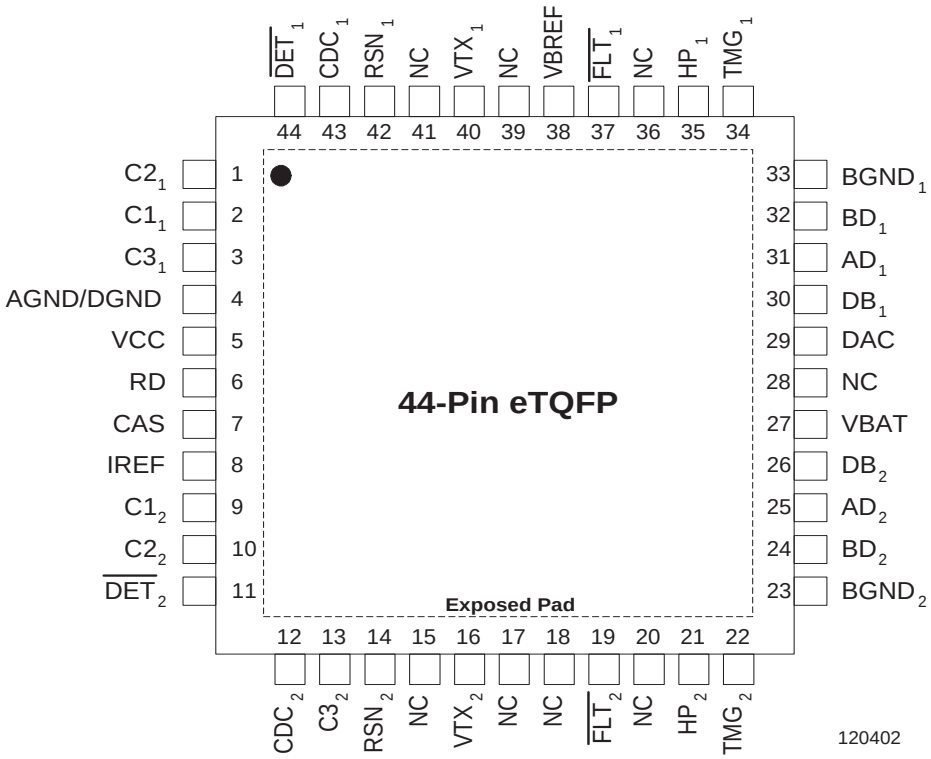
Upon the loss of battery the $\overline{FLT}$ pin will be LOW.

Thermal Shutdown.

Thermal shutdown is provided on a per channel basis to protect the die from excessive temperature. Persistent faults will produce high power dissipation, and may result in the affected channel triggering its thermal shutdown detector (Minimum > 145º C). At this point the power amplifiers are turned off and the device is in a disconnect like state, $\overline{FLT}$ and $\overline{DET}$ will be active. The thermal shutdown detector has approximately 10º C of hysteresis. Thermal shutdown on one channel will not affect the operation of the other channel.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout.The thermal pad at the bottom of the package should be soldered down to printed circuit board. Refer to the *Thermal Management for the Le5711 and Le7512 Dual SLIC Devices Application Note* for details.

CONNECTION DIAGRAM



Note:

1. *Pin 1 is marked for orientation.*
2. *NC = No Connect*
3. *The exposed heat sink pad on the bottom of the eTQFP package should be connected to VBAT pin - the SLIC side of the diode from battery supply. Do not connect it to GND.*

PIN DESCRIPTIONS

Pin Name	Type	Description
AD_1	Output	Output of AD power amplifier of channel 1.
AD_2	Output	Output of AD power amplifier of channel 2.
AGND/DGND	Ground	Analog and digital ground.
BD_1	Output	Output of BD power amplifier of channel 1.
BD_2	Output	Output of BD power amplifier of channel 2.
$BGND_1$	Ground	Battery (power) ground of channel 1
$BGND_2$	Ground	Battery (power) ground of channel 2.
$C1_1/C2_1/C3_1$	Input	State decoder inputs of channel 1.
$C1_2/C2_2/C3_2$	Input	State decoder inputs of channel 2.
CAS	Capacitor	Pin for capacitor to filter reference voltage when operating in anti-saturation region.
CDC_1	Capacitor	DC feed filter capacitor of channel 1.
CDC_2	Capacitor	DC feed filter capacitor of channel 2.
$\overline{FLT}_1$	Output	Channel 1 fault detector output[1].
$\overline{FLT}_2$	Output	Channel 2 fault detector output[1].
DAC	Input	Ring-trip negative of both channels. Negative input to ring-trip comparator.
DB_1	Input	Ring-trip positive of channel 1. Positive input to ring-trip comparator.
DB_2	Input	Ring-trip positive of channel 2. Positive input to ring-trip comparator.
DET_1	Output	Off Hook / Ring-trip detector output of channel1. Logic low indicates that a detector is tripped.
DET_2	Output	Off Hook / Ring-trip detector output of channel 2. Logic low indicates that a detector is tripped.
HP_1	Capacitor	Connect a High-Pass filter capacitor in series with a resistor from HP_1 to BD_1.
HP_2	Capacitor	Connect a High-Pass filter capacitor in series with a resistor from HP_2 to BD_2.
IREF	Resistor	Connection for reference resistor that programs Off Hook Detector threshold and DC feed current limit of both channels.
NC	—	No Connect. This pin is not internally connected.
RD	Resistor	Connection for resistor that programs off hook detector threshold of both channels.
RSN_1	Input	Receive Summing Node of channel 1. In the Active and Reverse Polarity states, the current (both AC and DC) between AD_1 and BD_1 is equal to 500 times the current into this pin. The networks that program receive gain, metering gain and two-wire impedance of Channel 1 connect to this node.
RSN_2	Input	Receive Summing Node of channel 2. In the Active and Reverse Polarity states, the current (both AC and DC) between AD_2 and BD_2 is equal to 500 times the current into this pin. The networks that program receive gain, metering gain and two-wire impedance of Channel 2 connect to this node.
TMG_1	Output	Thermal management of channel 1. External resistor connects from TMG_1 to VBAT to off-load power from the SLIC device.
TMG_2	Output	Thermal management of channel 2. External resistor connects from TMG_2 to VBAT to off-load power from the SLIC device.
VBAT	Battery	Battery supply and connection to substrate. Connect to highest negative supply with a diode on a per line base.
VBREF	Input	This is a Zarlink reserved pin and must always be connected to the VBAT pin.
VCC	Power	+5 V power supply.
VTX_1	Output	Transmit audio signal of channel 1. This output is a scaled version of the A and B metallic voltage. VTX_1 also sources the two-wire input impedance programming network.
VTX_2	Output	Transmit audio signal of channel 2. This output is a scaled version of the A and B metallic voltage. VTX_2 also sources the two-wire input impedance programming network.
EPAD	Battery	The exposed heat sink pad on the bottom of the eTQFP package should be connected to VBAT pin - the SLIC side of the diode from battery supply. This thermal pad should also be soldered down to printed circuit board to achieve the desired package thermal performance.

Note:

1. Consult Zarlink representatives for proper handling when not in use.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability

Storage temperature	–55 to +150° C
V_{CC} with respect to AGND / DGND	–0.4 to +7.0 V
V_{BAT} with respect to AGND / DGND	+0.4 to –63 V
$BGND_1$, $BGND_2$ with respect to AGND / DGND	+3 to –3 V
AD_1, AD_2, BD_1, BD_2 with respect to BGND:	
Continuous	V_{BAT} to + 1 V
10 ms (F = 0.1 Hz)	–70 to +5 V
1 µs (F = 0.1 Hz)	–80 to +8 V
250 ns (F = 0.1 Hz)	–90 to +12 V
Current from AD_1, AD_2, BD_1, BD_2	±150 mA
DB_1, DB_2, and DAC inputs:	
Voltage on ring-trip inputs	V_{BAT} to 0 V
Current into ring-trip inputs	±10 mA
$C1_1$, $C2_1$, $C3_1$, $C1_2$, $C2_2$, $C3_2$	
Input Voltage	–0.4 to V_{CC} + 0.4 V
Maximum power dissipation in 44-pin eTQFP	
T_A = 70° C, continuous	(see note 1)
Thermal Data in 44-pin eTQFP package	
Junction to Ambient, θ_{JA}	(see note 2)
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Notes:

1. *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165° C. Continuous operation above 145° C junction temperature may degrade device reliability. Refer to the Thermal Management for the Le5711 and Le7512 Dual SLIC Devices Application Note for details.*
2. *The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Refer to the Thermal Management for the Le5711 and Le5712 Dual SLIC Devices Application Note for details.*

Package Assembly

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

The operating ranges specified below define those limits between which the device operates and is guaranteed under the noted test conditions. (Refer to *Summary of Test Conditions*, on page 9.)

Environmental Ranges

Zarlink guarantees the performance of this device over commercial (0 to 70° C) and industrial (–40 to 85° C) temperature ranges by conducting electrical characterization, production testing, and periodic sampling over each range. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient Temperature	–40° to 85°C
Ambient Relative Humidity	15% to 85%

Electrical ranges

V_{CC}	4.75 to 5.25 V
VBAT	–39 to –60 V
DB1, DB2, and DAC	V_{BAT} to –2 V
AGND	0 V
$BGND_1$, $BGND_2$ with respect to AGND/DGND	–100 to + 100 mV
Load resistance on VTX_1, VTX_2 to ground	8 kΩ minimum

ELECTRICAL CHARACTERISTICS

Summary of Test Conditions

Unless otherwise noted, the test conditions are defined by the Le5712 device test circuit shown in Figure 7, on page 17 with: VCC=5 V, BAT = -52 V, $R_L = R_{LAC}$ = 600 Ω, R_{REF} = 14.3 kΩ, R_D = 82.5 kΩ.

Supply Currents and Power Dissipation (on-hook)

Operational State	I_{CC} mA (Note 1.)			I_{VBAT} mA (Note 1.)			SLIC Device Power mW			Note
	Min.	Typ	Max	Min.	Typ	Max	Min.	Typ	Max	
Disconnect		3.2	5.5		0.5	0.8		42	62	
Standby		3.2	6.5		0.6	1.0		46	70	
Tip Open		3.1	6.5		0.6	1.0		46	70	
Active		9.0	13		6.0	10.0		353	540	
Reverse Polarity		9.0	13		6.0	10.0		353	540	
Active Metering		9.3	13		6.0	10.0		355	540	
Reverse Polarity Metering		9.3	13		6.0	10.0		355	540	2
One channel Standby One channel Active		6.1	10		3.3	5.5		200	305	

SPECIFICATIONS

Device specifications

Specification	Condition	Min.	Typ	Max	Unit	Note
Line Characteristics						
VAB, Open Circuit	Active	42.75	45.7	48	V	
	Standby	46.75		52		
	Metering states	38	41.5	42.5		
I_L, Long Loops, Active state	R_{LDC}= 2000 Ω, BAT = -48 V	20	20.5		mA	
I_{LIMIT}, Short Loops, Active state	R_{LDC}= 100 Ω to 1100 Ω	30	33	36	mA	3
I_L, Long Loops, Active state	R_{LDC}= 2125 Ω	20	21.1		mA	
I_L, Long Loops, Active state	R_{LDC}= 2125 Ω, BAT = -46.5 V	18	18.5		mA	
I_L, Accuracy, Standby state	$I_L = \left(\frac{\lvert BAT\rvert - 4V}{(R_L + 600)}\right), R_{LDC} \geq 2000\Omega$	$0.9I_L$	I_L	$1.1I_L$	mA	
	Current Limited Region	20	30	45		
I_LLIM, AD and BD to BGND	Active, I_{AD} + I_{BD}		85	120	mA	
I_L, Loop current, Disconnect state	R_L = 0 Ω			100	µA	
I_{AD} leakage, Tip Open state	R_L = 0 Ω			100	µA	
I_{BD} current, Tip Open state	BD to BGND	20	30	45	mA	
V_{AD} Active and Standby states	AD to BAT=7 kΩ, BD to GND=100Ω	-7.5	-5		V	
V_{IREF}, IREF pin output voltage		1.2	1.25	1.3	V	
K1, Incremental RSN current gain		490	500	510	A/A	
Power Supply Rejection Ratio at the Two-Wire Interface (Active states, On or Off Hook)						
V_{CC}	50 Hz to 3.4 kHz V_{RIPPLE} = 100 mVrms	30	40		dB	4
V_{BAT}	V_{RIPPLE} = 100 mVrms 300 Hz to 3.4 kHz	28	50			
	50 Hz to 60 Hz	20				
RI_{AS}, Effective internal resistance	CAS pin to AGND	90	150	210	kΩ	2

Specification	Condition	Min.	Typ	Max	Unit	Note
Longitudinal Capability (See Figure 4, on page 16.)						
Longitudinal to metallic L-T balance 200 Hz to 1.0 kHz, Le57122	Normal polarity 0º C to +70º C	–63	-67		dB	
Longitudinal to metallic L-T balance 3.0 kHz, Le57122	Normal polarity 0º C to +70º C	–60	-64		dB	
Longitudinal to metallic L-T balance 200 Hz to 1.0 kHz, Le57122	Normal polarity -40º C to +85º C	–60	-67		dB	2
Longitudinal to metallic L-T balance 3.0 kHz, Le57122	Normal polarity -40º C to +85º C	–57	-64		dB	2
Longitudinal to metallic L-T balance 200 Hz to 3.0 kHz, Le57121	0º C to +70º C	–53			dB	
Longitudinal to metallic L-T balance 200 Hz to 3.0 kHz, Le57121	-40º C to +85º C	–50				2
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40			dB	
Longitudinal current per pin (AD_i or BD_i)	Active state (off hook)	8.5			mArms	5
Longitudinal impedance at AD_i or BD_i	0 to 100 Hz		18.5		Ω /pin	
RFI Rejection (See Figure 6, on page 16.)						
VTX_1 or VTX_2	f =.01 to 100 MHz HF gen. output = 1.5 Vrms $C_{AXi} = C_{BXi} = 33$ nF $C_{AXi} = C_{BXi} = 2.2$ nF			1 3	mVrms	2
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz (See Figure 5, on page 16)	26			dB	2, 6
Analog output (VTX) impedance			3	25	Ω	2
Analog (VTX) output offset voltage		–50		+50	mV	
Overload level, 2-wire	Active or Reverse Polarity state	2.5			Vpk	7
Overload level, 2-wire	On hook, Active or Reverse Polarity state	1.1				8
Overload level, 2-wire	Metering states	5.5				7
Overload level, 2-wire	On hook, Metering states	5.5				8
THD (Total Harmonic Distortion)	0 dBm		–64	–50	dB	4
	+7 dBm		–55	–40		
	+9 dBm, Metering states		-55	-40		
THD, On hook	0 dBm, $R_{LAC} = 600$ Ω			–36		
THD with metering	$R_L = 300$ Ω			–35		2, 9
Idle Channel Noise	C-Message, $R_L = 600$ Ω		7	12	dBrnC	2
	Psophometric, $R_L = 600$ Ω		-83	-78	dBmp	
Idle Channel Noise with Metering	Psophometric, $R_L = 300$ Ω, Metering states			-46		2, 10
Crosstalk Between Channels						
Crosstalk coupling loss	Averaged over 200 Hz to 3.4 kHz, 0dBm		80		dB	11

Specification	Condition	Min.	Typ	Max	Unit	Note
Insertion Loss (See Figure 2 and Figure 3, on page 15.)						
Gain, 4-to-2-wire	0 dBm, 1 kHz	–0.20	0	+0.20	dB	
Gain K_{TX}, 2-to-4-wire	0 dBm, 1 kHz	–9.74	–9.54	–9.34		
Gain, 4-to-4-wire	0 dBm, 1 kHz	–9.74	–9.54	–9.34		
Gain, 4-to-2-wire	On hook	–0.35		+0.35		
Gain over frequency	300 to 3400 Hz, relative to 1 kHz	–0.15		+0.15		
Gain tracking	+3 to –55 dBm, relative to 0 dBm	–0.15		+0.15		2
Gain tracking, On hook	0 dBm to –37 dBm +3 dBm to 0 dBm	–0.15 –0.35		+0.15 +0.35		
Metering Gain, 4-to-2-wire	V_M = 0.5 vrms, 16 kHz, R_L = 300 Ω	15.1	15.6	16.1	dB	12
Logic Interface						
Inputs ($C1_1$, $C1_2$, $C2_1$, $C2_2$, $C3_1$ and $C3_2$)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current	V_{IH}=2.0V	–110		90	µA	
I_{IL}, Input Low current	V_{IL}=0.8V	–400				
Outputs ($\overline{DET}_1$ and $\overline{DET}_2$)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA	2.4				
Outputs ($\overline{FLT}_1$ and $\overline{FLT}_2$)						
V_{OL}, Output Low voltage	I_{OUT} = 0.06 mA			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.01 mA	2.4				
Ring-Trip Detector Input (Applies to DAC, DB_1 and DB_2.)						
Bias Current		–50	–10	0	nA	2
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	13
Common Mode Voltage Range		V_{BAT} + 1		–2	V	2
Fault Detector (See Figure 1, on page 15.)						
$I_{FAULT} = \|I_{AD} + I_{BD}\|$		8	11.5	20	mA	
Off-Hook and Ground Start Detectors (See Figure 1, on page 15.)						
I_{OHD} On-to-Off hook Detection Threshold	Active and Standby states	9.8	11.5	13.2	mA	
Hysteresis	The difference between On-to-Off hook detection threshold and Off-to-On hook Detection threshold	1.3	2.0	2.7		
I_{GSD}, Ground Start Detect threshold (On-to-Off hook detection threshold)	Tip Open state	11.8	13.5	16.0		
Hysteresis (Ground Start)	The difference between On-to-Off hook detection threshold and Off-to-On hook detection threshold	2.6	4.0	5.4		

Notes:

1. *Total current measured with both channels in the same state, unless otherwise specified.*
2. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
3. *Typical current limit range is designed to be between 22 mA and 33 mA.*
4. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
5. *Minimum current level guaranteed not to cause a false loop detect. The fault detector may activate with longitudinal currents above 2.8 mA rms, and may pulse at twice the frequency of the interfering signal.*
6. *Group delay can be greatly reduced by using a Z_T network such as that shown in* Figure 5, on page 16 *where C_T = 120 pF, R_{TA} = R_{TB} = 50 kΩ. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on line card performance also may be compensated by synthesizing complex impedance with the QLSLAC™ or Octal SLAC™ devices.*
7. *Overload level is defined as THD = 1%,*
8. *Overload level is defined as THD = 1.5%.*
9. *Total Harmonic distortion with metering is specified with a metering signal of 3.0 Vrms at the two-wire output, and a transmit signal of +3 dBm or receive signal of –4 dBm. The transmit or receive signals are single frequency inputs, and the distortion is measured as the highest in band harmonic at the two-wire or the four-wire output relative to the input signal.*
10. *Noise with metering is measured by applying a 3.0 Vrms metering signal (measured at the two-wire output) and measuring the psophometric noise at the two-wire outputs over a 200 ms time interval*
11. *This is test at 1 kHz in production*
12. *In the test set up, Z_T = 100 kΩ, R_M = 16.5 kΩ, and R_F = 0 Ω. The output voltage at tip/ring is expected to be 3 Vrms, into a load of 300 Ω, with 0.5 Vrms source. The typical gain is 15.6 dB.*
13. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*

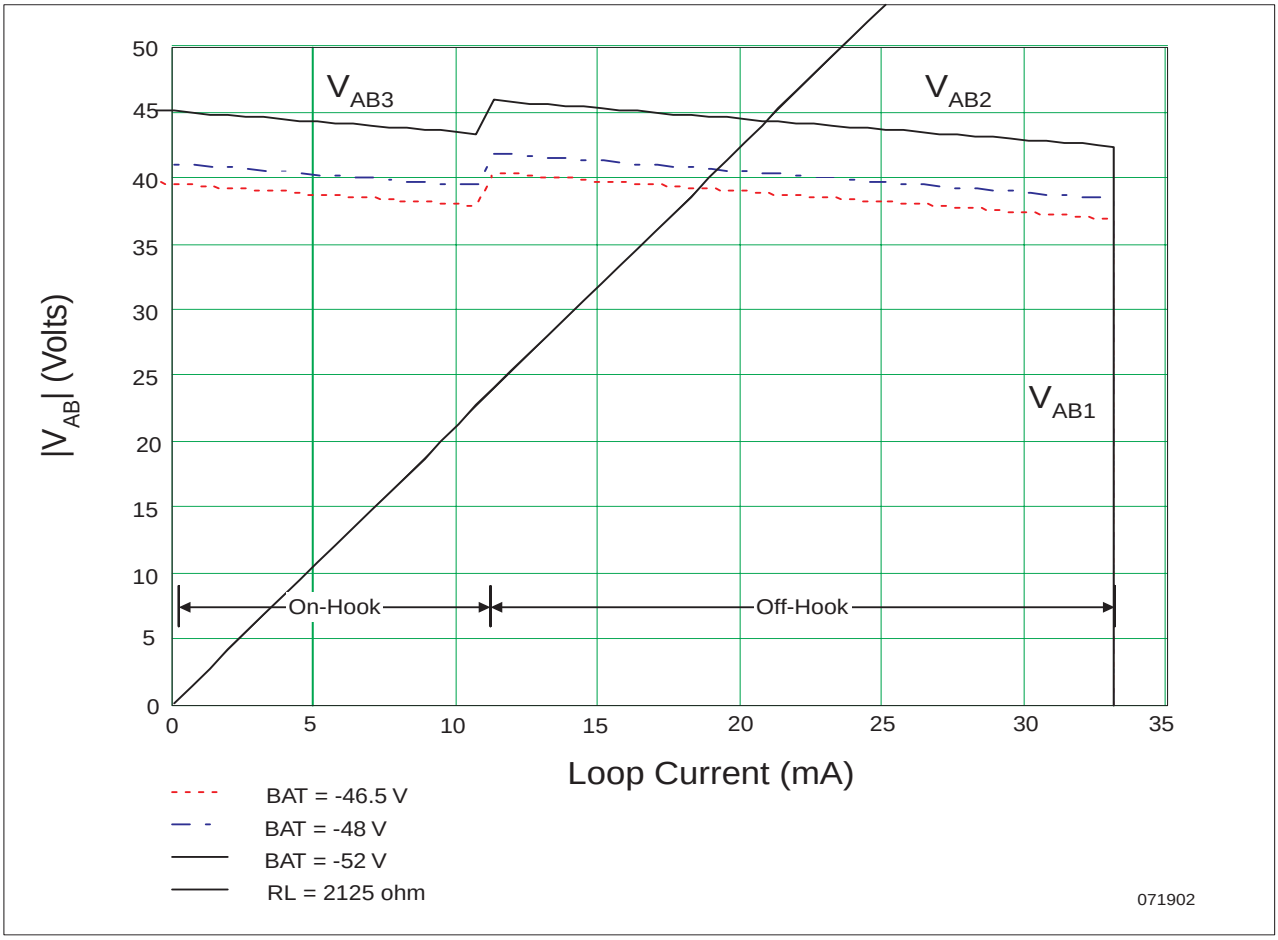
User-Programmable Components Summary

Equation	Description
$Z_{Ti} = \frac{500}{3}(Z_{2WIN} - 2R_F)$	Z_{Ti}* is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_{Ti}, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RXi} = \frac{Z_L}{G_{42L}} \bullet \frac{500 \bullet Z_T}{Z_T + \frac{500}{3} \cdot (Z_L + 2R_F)}$	Z_{RXi}* is connected from VRX to RSN. Z_{Ti} is defined above, and G_{42L} is the desired receive gain.
$R_{REF} = \frac{470 \cdot V}{I_{LIMIT}}$	I_{LIMIT} is the desired loop current limit in the constant-current region.
$C_{CAS} = \frac{1}{RI_{AS} \bullet 2\pi \bullet f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{OHD} = I_{GSD} = \frac{935 \cdot V}{R_D}$	Off Hook Detect (I_{OHD}) and Ground Start Detect (I_{GSD}) thresholds are typically set at 10 to 12 mA.
$I_{STANDBY} = \frac{\lvert V_{BAT}\rvert - 4\ V}{600\ \Omega + R_L}$	Standby loop current (resistive region).
Thermal Management Equations (All Active states for one channel) (Please refer to the *Thermal Management for the Le5711 and Le7512 Dual SLIC Devices* **Application Note for details about dual battery operation.)**	
$R_{TMG} \geq \frac{\lvert BAT_{MAX}\rvert - 6 - I_{LIMITMIN} \cdot (2 \bullet R_F + R_{LMIN} + 40\Omega)}{I_{LIMITMIN} - 3\ mA}$	R_{TMG} is connected from TMG to VBAT and limits power within the SLIC device in Active, Off-Hook states.
$P_{RTMGmax} = \frac{(\lvert BAT\rvert_{max} - 5 - I_{LIMITmin}(R_{Lmin} + 2R_F + 40))^2}{R_{TMGmin}}$	Maximum power dissipated in the TMG resistor, R_{TMG}, during Active, Off-Hook states.
$P_{SLICmaxi} = 0.003\lvert BAT\rvert_{max} + \left(1 + \frac{I_{LIMITmax}}{2} R_{TMGmax}\right)\left(\frac{I_{LIMITmax}}{2} + \frac{1}{R_{TMGmax}}\right)$	Maximum power dissipated per channel in the SLIC device while in Active, Off-Hook states.

** "i" denotes channel number*

DC Feed Characteristics

Load Line (Active) (Typical)



Regions:

1. *Constant current region:*

$$V_{AB1} = I_{LOOP}R_L = \frac{470}{R_{REF}}R_L, \text{ where, } R_L = R_L' + 2R_F$$

In Active and Reverse Polarity states

2. *Battery tracking anti-sat (Off-hook):*

$$V_{AB2} = |BAT| - 7\ V + \frac{47 \cdot k\Omega \cdot V}{R_{REF}} - I_L \cdot 160\ \Omega$$

3. *Battery tracking anti-sat (On-hook):*

$$V_{AB3} = |BAT| - 7\ V + \frac{10 \cdot k\Omega \cdot V}{R_{REF}} - I_L \cdot 160\ \Omega$$

In Active Metering and Reverse Polarity Metering states

4. *Battery tracking anti-sat (Off-hook):*

$$V_{AB2} = |BAT| - 10.7\ V + \frac{47 \cdot k\Omega \cdot V}{R_{REF}} - I_L \cdot 160\ \Omega$$

5. *Battery tracking anti-sat (On-hook):*

$$V_{AB3} = |BAT| - 10.7\ V + \frac{10 \cdot k\Omega \cdot V}{R_{REF}} - I_L \cdot 160\ \Omega$$

Test Circuits

Figure 1. Feed Programming

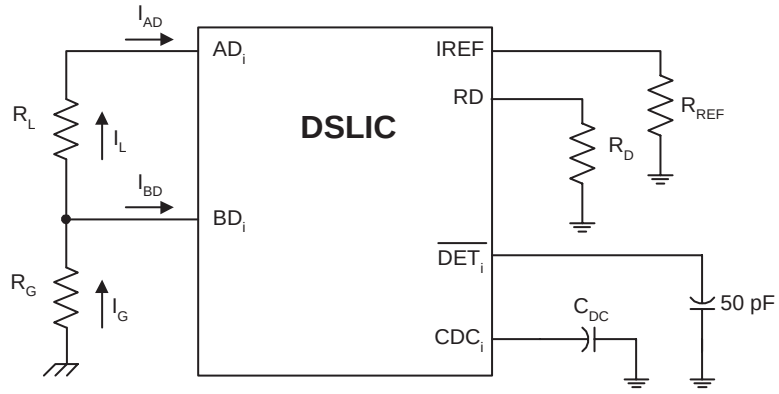


Figure 2. Two-to-Four Wire Insertion Loss

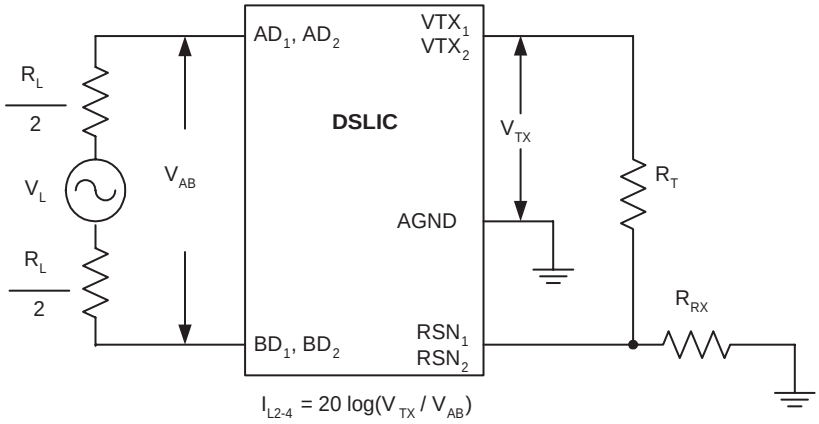


Figure 3. Four-to-Two Wire Insertion Loss and Balance Return Signals

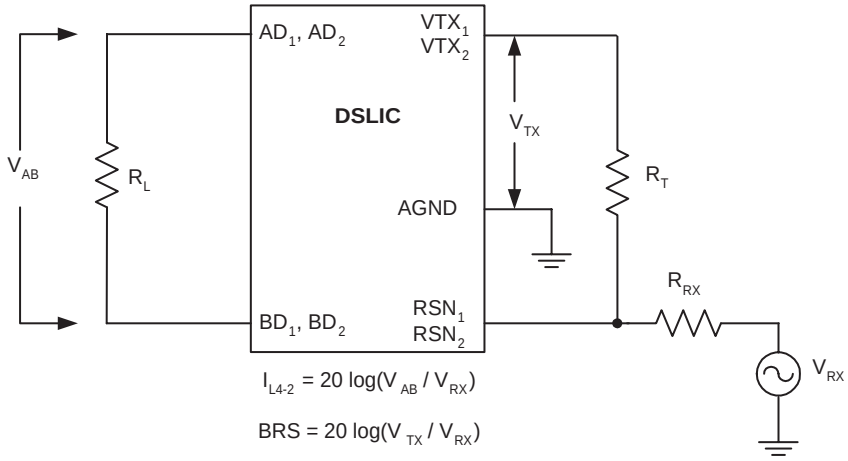


Figure 4. Longitudinal Balance

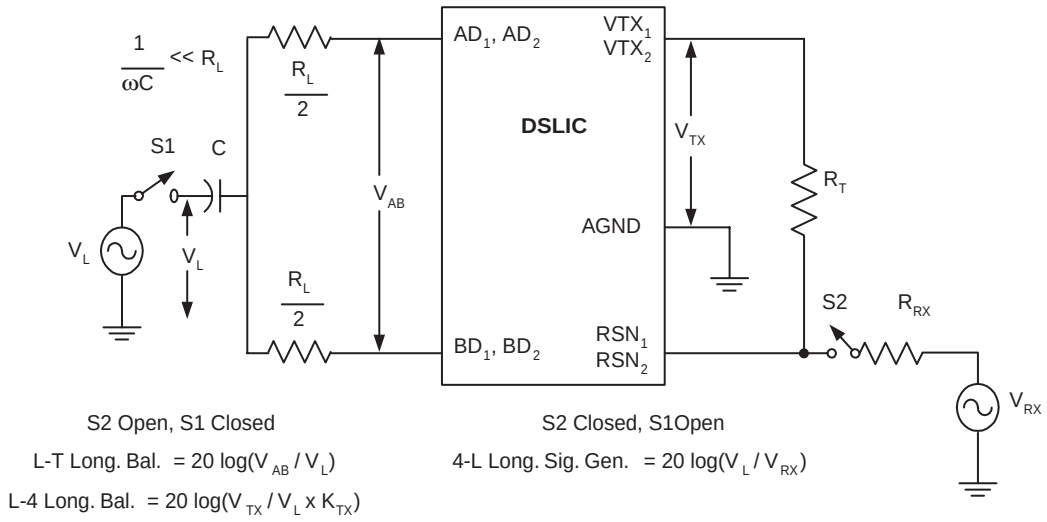


Figure 5. Two-Wire Return Loss Test Circuit

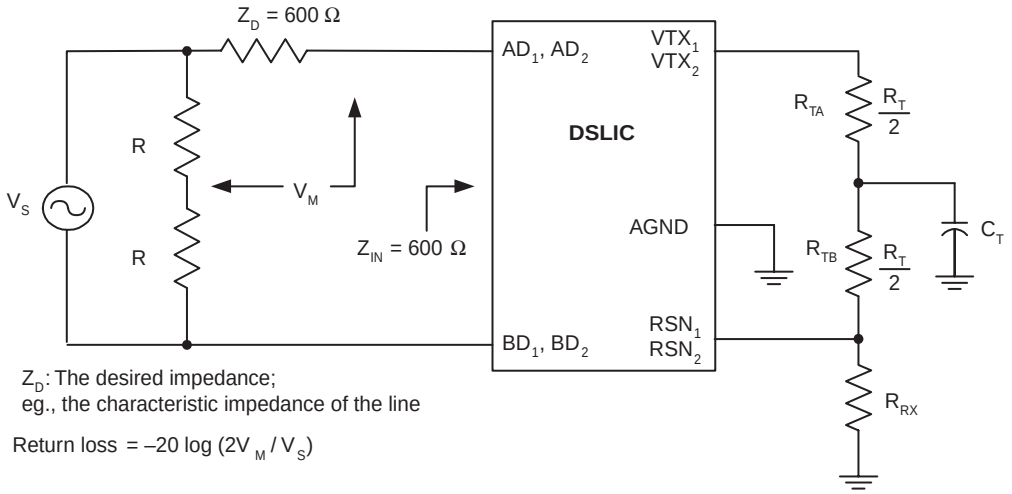


Figure 6. RFI Test Circuit

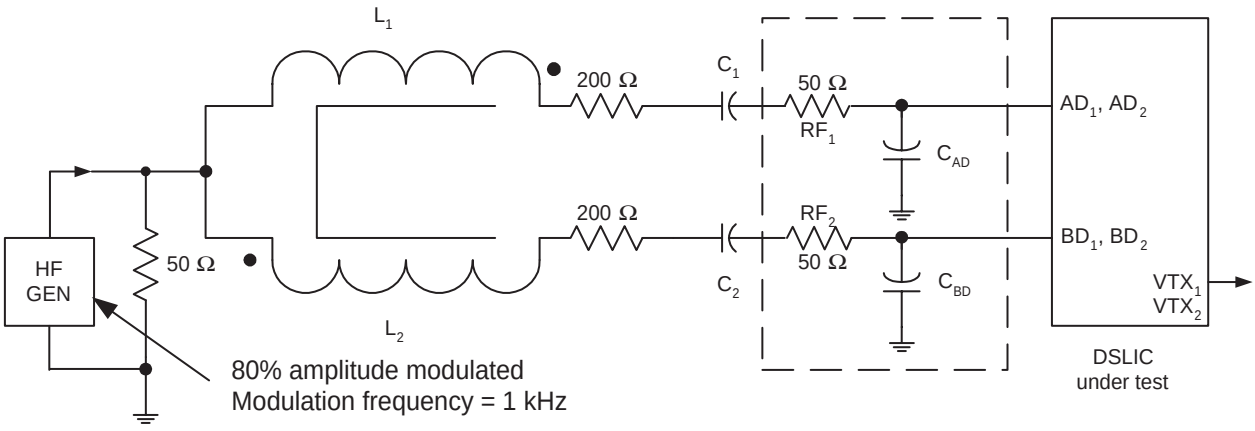
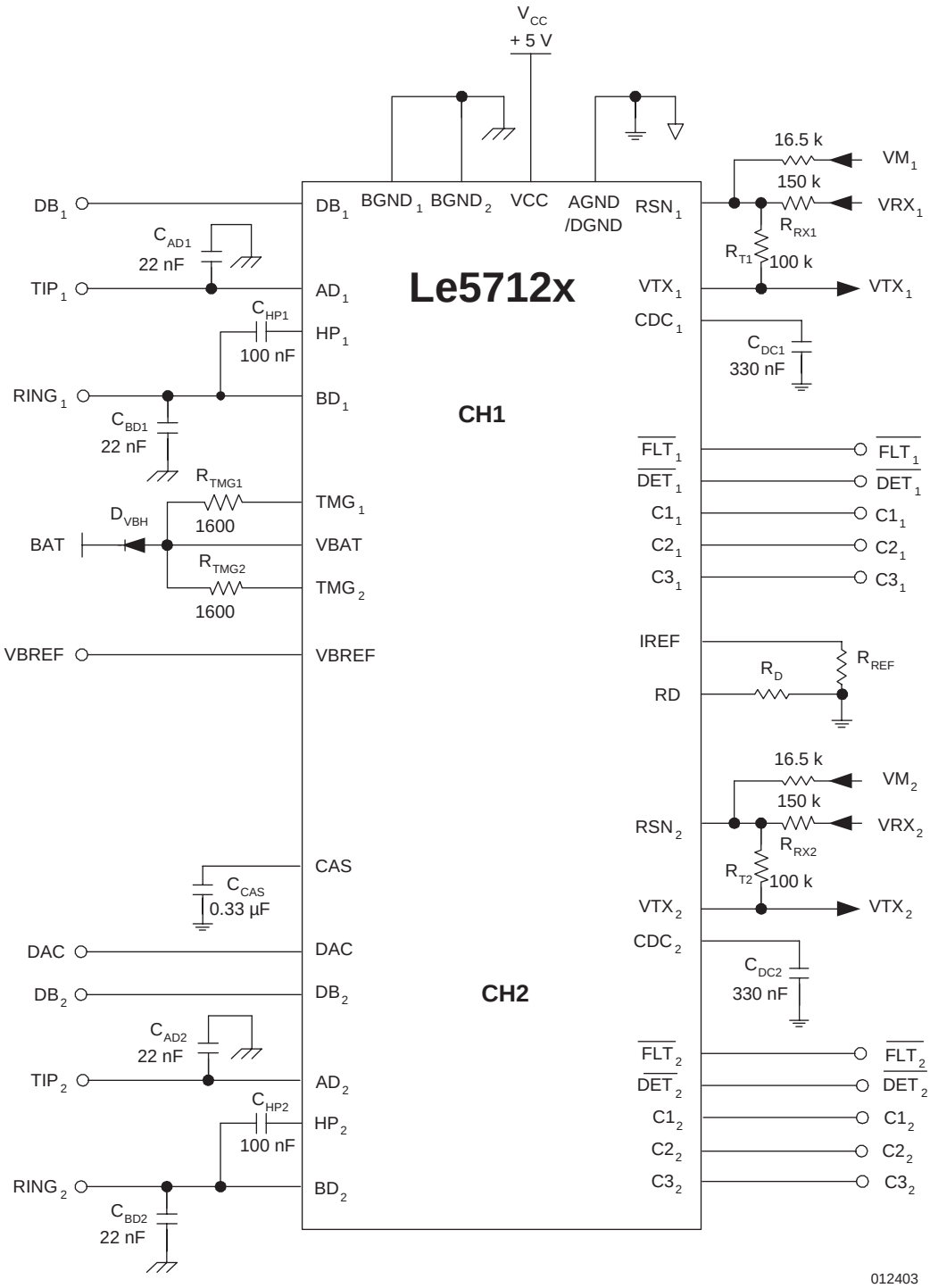
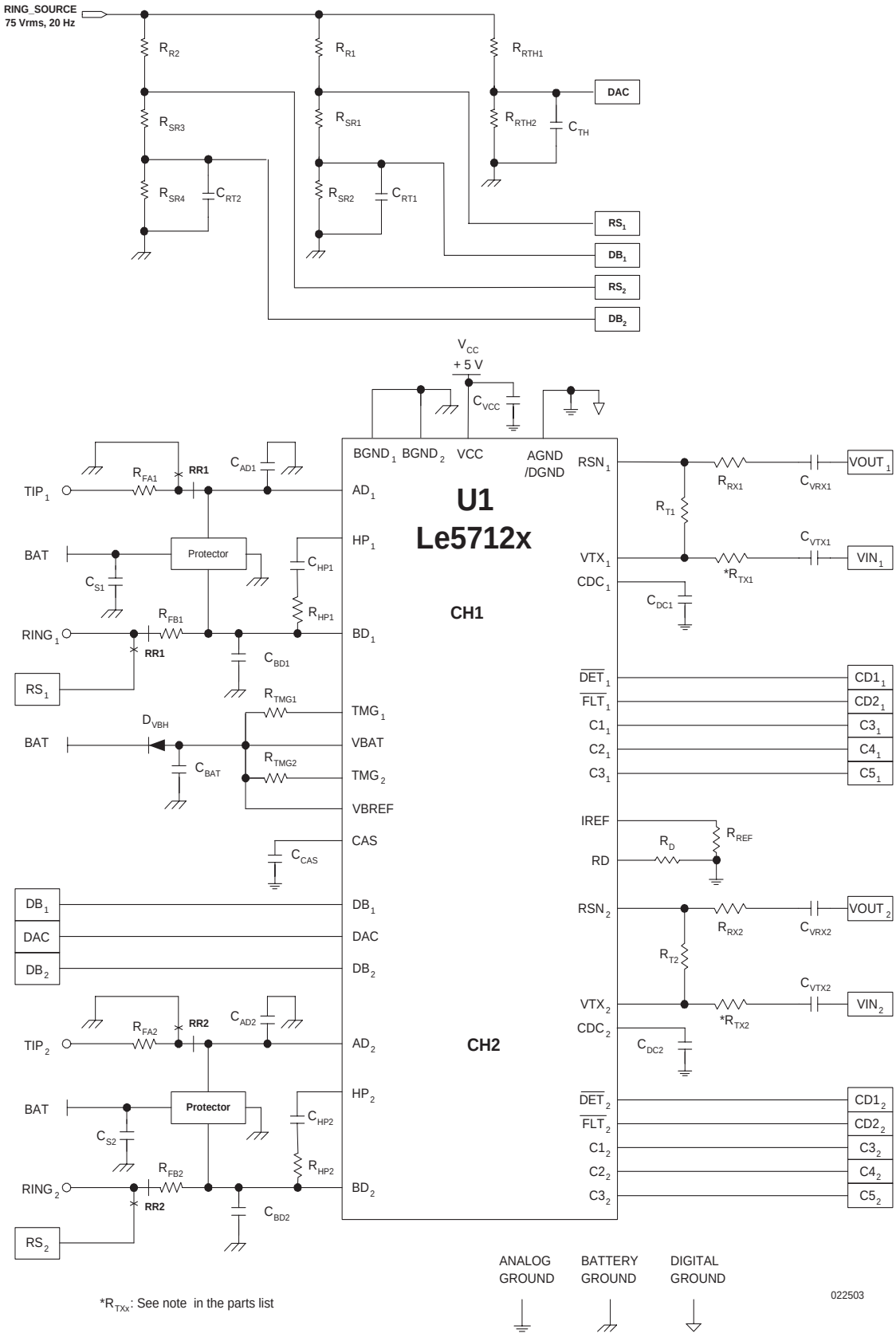


Figure 7. Le5712 Test Circuit



POTS APPLICATION CIRCUIT (POTS WITH NO METERING)

For use with a Quad or Octal SLAC device; battery-backed ringing.



*R_{TXx}: See note in the parts list

APPLICATION CIRCUIT PARTS LIST (POTS WITH NO METERING)

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2).

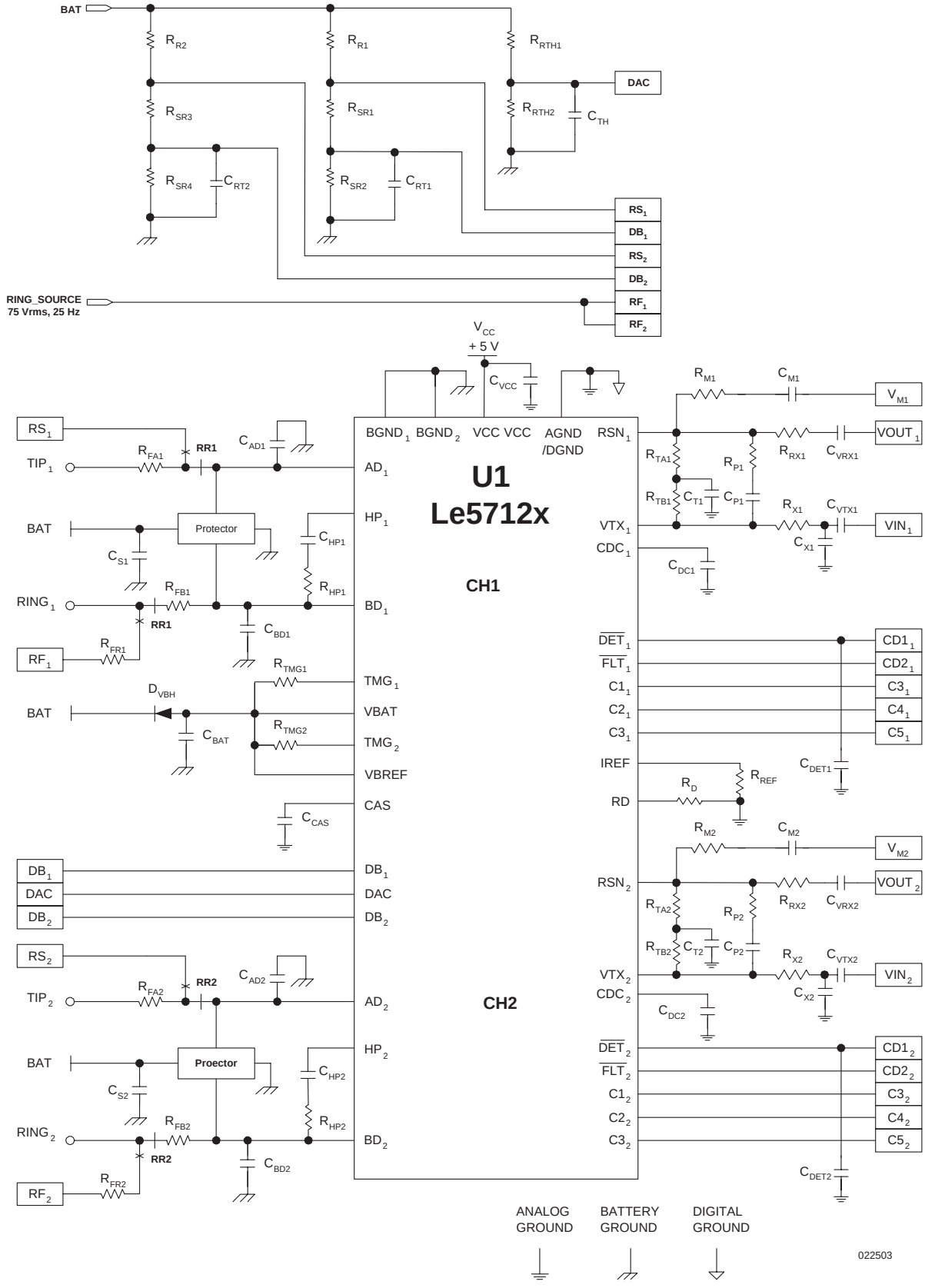
Item	Quantity	Type	Value	Tol.	Rating	Note
Ringing and Ring Trip Sensing						
R_{RTH1}	1	SMT	1 MΩ	1%	1/16 W	
R_{SR1}, R_{SR3}	2	SMT	1.82 MΩ	1%	1/16 W	
R_{SR2}, R_{SR4}	2	SMT	2 MΩ	1%	1/16 W	
R_{RTH2}	1	SMT	909 kΩ	1%	1/16 W	
R_{R1}, R_{R2}	2	Resistor Hybrid	400 Ω	5%	2 W	
C_{TH}	1	Capacitor (X7R)	0.1 µF	20%	50 V	
C_{RT1}, C_{RT2}	2	Capacitor (X7R)	0.047 µF	20%	50 V	
Fault Protection and Power Supplies						
R_{FA1}, R_{FB1}, R_{FA2A} R_{FB2}	4	Resistor Hybrid or PTC	50 Ω	1%		
Protector	1 or 2	Battery referenced thyristor				1
C_{S1}, C_{S2}	1 or 2	Capacitor (X7R)	0.1 µF	20%	100 V	2
C_{BAT}	1	Capacitor (X7R)	0.1 µF	20%	100 V	
C_{VCC}	1	Capacitor (X7R)	0.1 µF	20%	10 V	
D_{VBH}	1	MURS 120 (D0-41) DIODE				3
R_{TMG1}, R_{TMG2}	2	SMT	1.8 kΩ	5%	1 W	4
Other Components						
R_{REF}	1	SMT	14.3 kΩ	1%	1/16 W	5
R_D	1	SMT	82.5 kΩ	1%	1/16 W	6
R_{HP1}, R_{HP2}	2	SMT	15.0 kΩ	1%	1/16 W	7
R_{T1}, R_{T2}	2	SMT	100 kΩ	1%	1/16 W	
R_{RX1}, R_{RX2}	2	SMT	75.0 kΩ	1%	1/16 W	
C_{AD1}, C_{BD1}, C_{AD2}, C_{BD2}	4	Capacitor (X7R)	0.022 µF	20%	100 V	
C_{HP1}, C_{HP2}	2	Capacitor (X7R)	0.1 µF	20%	100 V	
C_{VTX1}, C_{VTX2}	2	Capacitor (X7R)	0.01 µF	20%	10 V	
C_{VRX1}, C_{VRX2}	2	Capacitor (X7R)	0.1 µF	20%	10 V	
C_{DC1}, C_{DC2}	2	Capacitor (X7R)	0.33 µF	20%	5 V	
C_{CAS}	1	Capacitor (X7R)	0.33 µF	20%	100 V	
R_{TX1}, R_{TX2}	2	SMT	2.00 kΩ	1%	1/16 W	8
U1	1	Le5712x				

Notes:

1. *In case of single, one for each channel. In case of dual, one for one Le5712 Dual SLIC.*
2. *Consult protector vendor for recommended value. One for one protector device.*
3. *A Schottky diode with a voltage drop of 0.4V is desirable if Tip to battery fault is concerned.*
4. *Value was chosen to use resistor with 5% tolerance and 1 W rating. See "Thermal Management for the Le5711 and Le5712 Dual SLIC Device" for further details.*
5. *Sets the current limit at 33 mA.*
6. *Sets an off-hook detection threshold of 11 mA.*
7. *RHP will enhance dial pulse crosstalk performance. RHP being 15 k will make G24 from being 1/3 to 1/3.0841. RHB should be present in WinSLAC™ simulations.*
8. *R_{TX} is optional and is required if C_{VTX} is greater than 0.01µF.*

PULSE METERING APPLICATION CIRCUIT (POTS WITH METERING)

For use with a Quad or Octal SLAC device; earth-backed ringing.



APPLICATION CIRCUIT PARTS LIST (POTS WITH METERING)

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2).

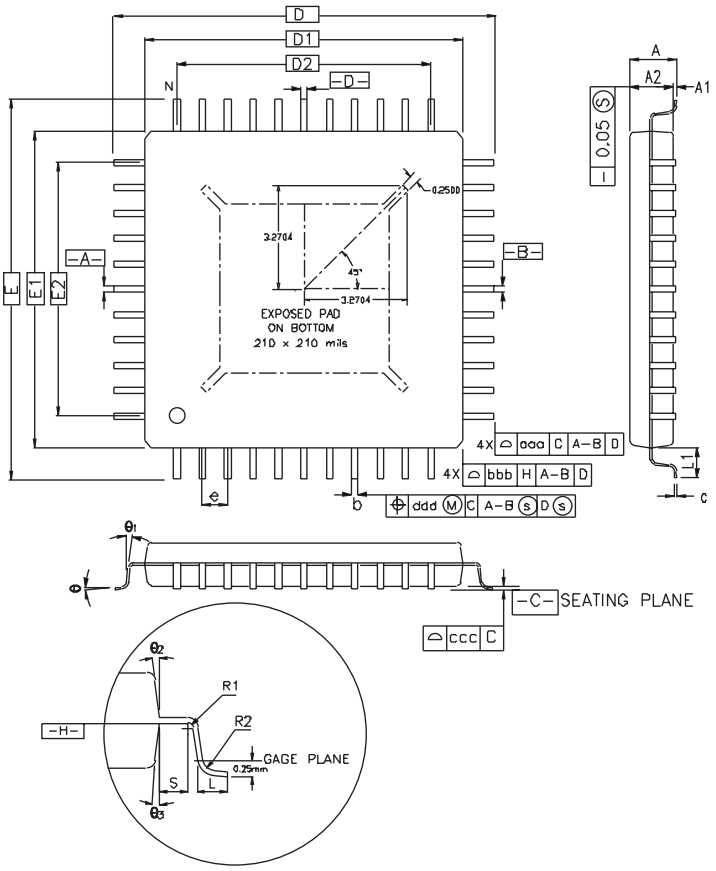
Item	Quantity	Type	Value	Tol.	Rating	Note
Ringing and Ring Trip Sensing						
R_{RTH1}	1	SMT	1 MΩ	1%	1/16 W	
R_{SR1}, R_{SR3}	2	SMT	1.82 MΩ	1%	1/16 W	
R_{SR2}, R_{SR4}	2	SMT	2 MΩ	1%	1/16 W	
R_{RTH2}	1	SMT	909 kΩ	1%	1/16 W	
R_{R1}, R_{R2}	2	Resistor Hybrid	400 Ω	5%	2 W	
C_{TH}	1	Capacitor (X7R)	0.1 µF	20%	50 V	
C_{RT1}, C_{RT2}	2	Capacitor (X7R)	0.047 µF	20%	50 V	
Fault Protection and Power Supplies						
R_{FA1}, R_{FB1}, R_{FA2A} R_{FB2}	4	Resistor Hybrid or PTC	50 Ω	1%		
Protector	1 or 2	Battery referenced thyristor				1
C_{S1}, C_{S2}	1 or 2	Capacitor (X7R)	0.1 µF	20%	100 V	2
C_{BAT}	1	Capacitor (X7R)	0.1 µF	20%	100 V	
C_{VCC}	1	Capacitor (X7R)	0.1 µF	20%	10 V	
D_{VBH}	1	MURS 120 (D0-41) DIODE				3
R_{TMG1}, R_{TMG2}	2	SMT	1.8 kΩ	5%	1 W	4
Components specific to Metering application circuit						
C_{M1}, C_{M2}	2	Capacitor (X7R)	0.01 µF	20%	10 V	
C_{T1}, C_{T2},	2	Capacitor (X7R)	1000 pF	10%	10 V	
C_{X1}, C_{X2}	2	Capacitor (X7R)	1500 pF	10%	10 V	
C_{P1}, C_{P2}	2	Capacitor (X7R)	390 pF	10%	10 V	
C_{DET1}, C_{DET2}	2	Capacitor (X7R)	0.022 µF	20%	10V	
R_{M1}, R_{M2}	2	SMT	16.5 kΩ	1%	1/16 W	5
R_{TA1}, R_{TA2}, R_{TB1}, R_{TB2}	4	SMT	49.9 kΩ	1%	1/16 W	
R_{RX1}, R_{RX2}	2	SMT	71.5 kΩ	1%	1/16 W	
R_{P1}, R_{P2}	2	SMT	22.1 kΩ	1%	1/16 W	
R_{X1}, R_{X2}	2	SMT	4.99 kΩ	1%	1/16 W	
Other Components						
R_{REF}	1	SMT	14.3 kΩ	1%	1/16 W	6
R_D	1	SMT	82.5 kΩ	1%	1/16 W	7
R_{HP1}, R_{HP2}	2	SMT	15.0 kΩ	1%	1/16 W	8
C_{AD1}, C_{BD1}, C_{AD2}, C_{BD2}	4	Capacitor (X7R)	0.022 µF	20%	100 V	
C_{HP1}, C_{HP2}	2	Capacitor (X7R)	0.1 µF	20%	100 V	
C_{VTX1}, C_{VTX2}	2	Capacitor (X7R)	0.1 µF	20%	10 V	
C_{VRX1}, C_{VRX2}	2	Capacitor (X7R)	0.1 µF	20%	10 V	
C_{DC1}, C_{DC2}	2	Capacitor (X7R)	0.33 µF	20%	5 V	
C_{CAS}	1	Capacitor (X7R)	0.33 µF	20%	100 V	
U1	1	Le5712x				

Notes:

1. *In case of single, one for each channel. In case of dual, one for one Le5712 Dual SLIC.*
2. *Consult protector vendor for recommended value. One for one protector device.*
3. *A Schottky diode with a voltage drop of 0.4V is desirable if Tip to battery fault is concerned.*
4. *Value was chosen to use resistor with 5% tolerance and 1 W rating. See "Thermal Management for the Le5711 and Le5712 Dual SLIC Device" for further details.*
5. *Sets a gain of about 5.5 dB into a load of 200 Ω at tip-ring (20LOG(200/16.5/1000*500/(1+500/3.0841*(200+100)/22.1/1000)).*
6. *Sets the current limit at 33 mA.*
7. *Sets an off-hook detection threshold of 11 mA.*
8. *RHP will enhance dial pulse crosstalk performance. RHP being 15 k will make G24 from being 1/3 to 1/3.0841. RHB should be present in WinSLAC™ simulations.*

PHYSICAL DIMENSIONS

44-Pin eTQFP



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D		12 BSC	
D1		10 BSC	
E		12 BSC	
E1		10 BSC	
R2	0.08	-	0.20
R1	0.08	-	-
θ	0 deg	3.5 deg	7 deg
θ 1	0 deg	-	-
θ 2	11 deg	12 deg	13 deg
θ 3	11 deg	12 deg	13 deg

Symbol	Min	Nom	Max
c	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	-	-
b	0.17	0.20	0.27
e		0.80 BSC	
D2		8.00	
E2		8.00	
aaa		0.20	
bbb		0.20	
ccc		0.10	
ddd		0.20	
N		44	

Notes:
1. Controlling dimension in millimeter unless otherwise specified.
2. Dimensions “D1” and “E1” do not include mold protrusion. Allowable protrusion is 0.25mm per side.
   “D1” and “E1” are maximum plastic body size dimensions including mold mismatch.
3. Dimension “b” does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08mm.
4. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
5. Square dotted line is E-Pad outline.
6. “N” is the total number of terminals.

44-Pin eTQFP

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision C1 to D1

- Page 9, *Supply Currents and Power Dissipation*, (On-hook), regarding disconnect operational state, I_{VBAT} max from 0.7mA to 0.8mA; SLIC Device Power max from 50mW to 62mW.
- In *Device Specifications*, page 11, I_{GSD}, Ground Start Detection Threshold, changed max from 15.2mA to 16.0mA.
- In *Device Specifications*, page 11, I_{FAULT}, changed max from 18mA to 20mA.
- In *Device Specifications*, page 11, I_{IH}, Input High Current of C1/2/3, changed max from 40µA to 90µA, min from -100µA to -110 µA, with test condition to be V_{IH}=2.0V.
- In *Device Specifications*, page 11, I_{IL}, Input Low Current of C1/2/3, changed test condition to be V_{IL}=0.8V.

Revision D1 to E1

- Added green package OPNs to *Ordering Information*, on page 1
- Added *Package Assembly*, on page 8

Revision E1 to F1

- Removed Le57D123 and Le57D124 devices from *Ordering Information*, on page 1. Removed descriptions related to Le57D123 and Le57D124, such as old note 2 on page 12. The notes on page 12 are re-arranged that are applicable to page 9, page 10, and page 11.
- Removed non-green OPNs from *Ordering Information*, on page 1.
- Modified descriptions regarding FLTs in Pin Descriptions, on page 7.
- Updated and added note about package marking in *Physical Dimensions*, on page 22.
- Separated parts list for with and without metering applications, on page 19 and 21.

Revision F1 to G1

- Added Note 1 to *Pin Descriptions*, on page 7.
- Rearranged notes on page 12 and applicable notes in tables on pages 9, 10, and 11.
- Added *Application Circuit Parts List (Pots with no metering)*, on page 19.
- Modified *Application Circuit Parts List (Pots with metering)*, on page 21".

Revision G1 to G2

- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А