



TJA1083G

FlexRay node transceiver

Rev. 1 — 18 January 2018

Product data sheet

1. General description

The TJA1083G FlexRay node transceiver is compliant with the FlexRay Electrical Physical Layer specification ISO 17458-4:2013 (see [Ref. 1](#) and [Ref. 2](#)). It is primarily intended for communication systems operating at between 2.5 Mbit/s and 10 Mbit/s, and provides an advanced interface between the protocol controller and the physical bus in a FlexRay network. The TJA1083G offers an optimized solution for Electronic Control Unit (ECU) applications that do not need enhanced power management and are typically switched by the ignition or activated by a dedicated wake-up line.

The TJA1083G provides a differential transmit capability to the network and a differential receive capability to the FlexRay controller. It offers excellent ElectroMagnetic Compatibility (EMC) performance as well as high ElectroStatic Discharge (ESD) protection.

The TJA1083G actively monitors system performance using dedicated error and status information (readable via SPI), as well as internal voltage and temperature monitoring.

The TJA1083G is fully functionally and pin compatible with the TJA1083 (see [Ref. 3](#)).

2. Features and benefits

2.1 Optimized for time triggered communication systems

- Compliant with ISO 17458-4:2013 (see [Ref. 2](#))
- Automotive product qualification in accordance with AEC-Q100
- Data transfer rates from 2.5 Mbit/s to 10 Mbit/s
- Supports 60 ns minimum bit time at 400 mV differential input voltage
- Very low ElectroMagnetic Emission (EME) to support unshielded cable, meeting the latest industry standards
- Differential receiver with high common-mode range for excellent ElectroMagnetic Immunity (EMI), meeting the latest industry standards
- Auto I/O level adaptation to host controller supply voltage V_{IO}
- Can be used in 14 V, 24 V and 48 V powered systems
- Instant transmitter shut-down interface (BGE pin)

2.2 Low-power management

- Very low current consumption in Standby mode
- Remote wake-up via a wake-up pattern or dedicated FlexRay data frames on the bus lines



2.3 Diagnosis and robustness

- Enhanced supply voltage monitoring for V_{CC} and V_{IO}
- Two error diagnosis modes:
 - ◆ Status register readout via the Serial Peripheral Interface (SPI)
 - ◆ Simple error indication via pin ERRN
- Overtemperature detection
- Short-circuit detection on bus lines
- Power-on flag
- Clamping diagnosis for pins TXEN and BGE
- Bus pins protected against ± 6 kV ESD pulses according to IEC61000-4-2 and ± 8 kV according to HBM
- Bus pins protected against transients in automotive environment (according to ISO 7637 class C)
- Bus pins short-circuit proof to battery voltage (14 V, 24 V and 48 V) and ground
- Maximum differential voltage between pins BP or BM and any other pin of ± 60 V
- Bus lines remain passive when the transceiver is not powered
- No reverse currents from the digital input pins to V_{IO} or V_{CC} when the transceiver is not powered

2.4 Functional classes according to FlexRay Electrical Physical Layer specification V3.0.1

- Bus driver - bus guardian control interface
- Bus driver - logic level adaptation
- Bus driver - remote wake-up

3. Ordering information

Table 1. Ordering information

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| TJA1083GTT | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Block diagram

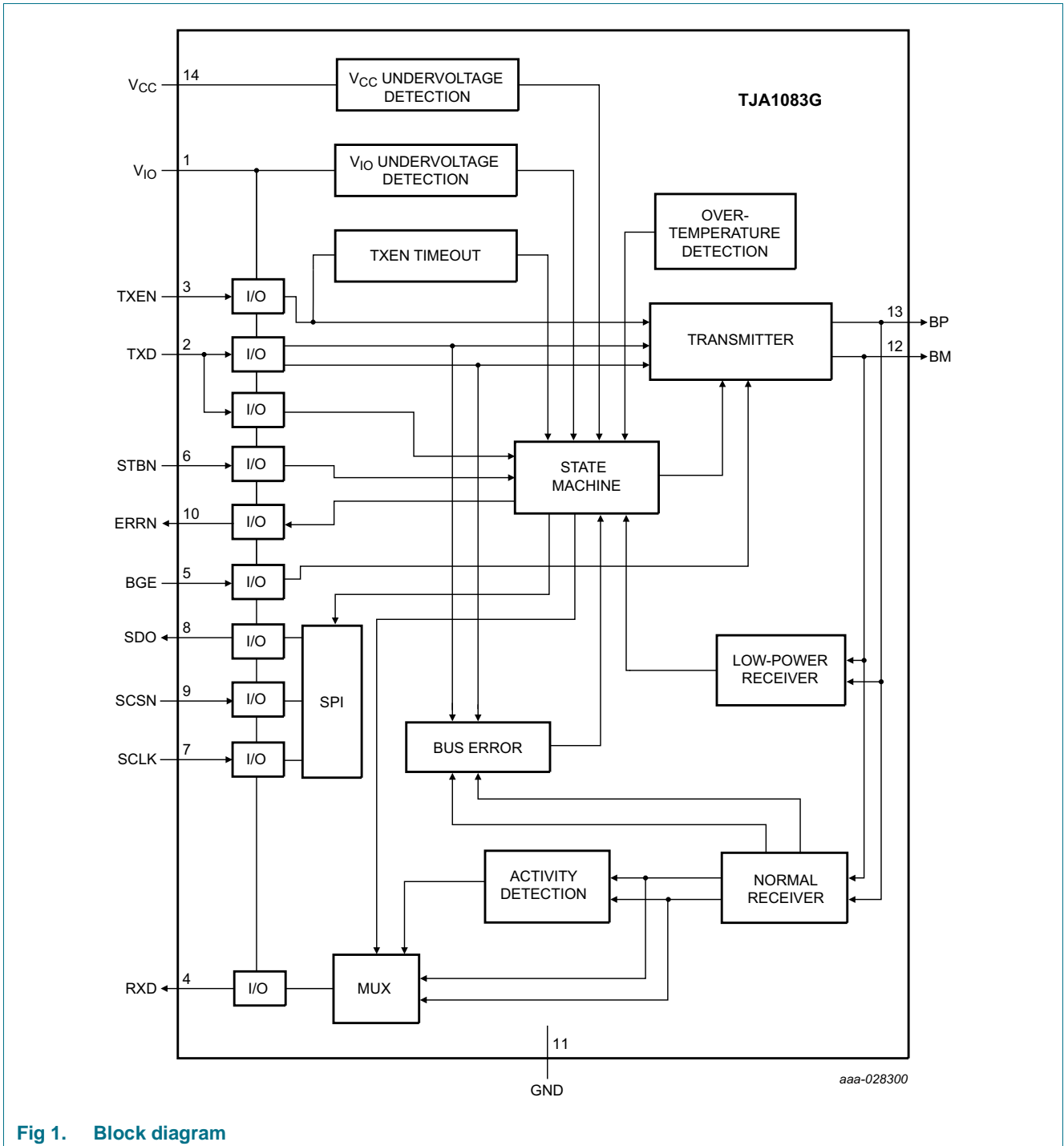
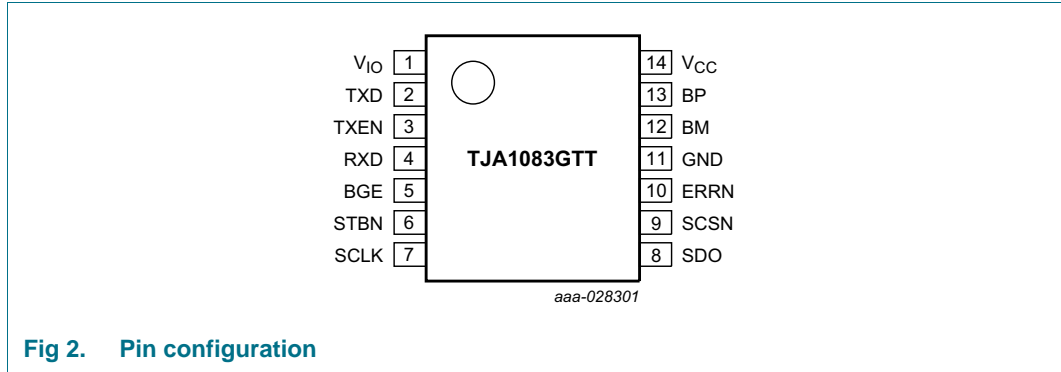


Fig 1. Block diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type | Description |
|-----------------|-----|------|--|
| V _{IO} | 1 | P | supply voltage for V _{IO} voltage level adaptation |
| TXD | 2 | I | transmit data input; internal pull-down |
| TXEN | 3 | I | transmitter enable input; when HIGH transmitter disabled; internal pull-up |
| RXD | 4 | O | receive data output |
| BGE | 5 | I | bus guardian enable input; when LOW transmitter disabled; internal pull-down |
| STBN | 6 | I | mode control input; transceiver in Normal mode when HIGH; internal pull-down |
| SCLK | 7 | I | SPI clock signal; internal pull-up |
| SDO | 8 | O | SPI data output |
| SCSN | 9 | I | SPI chip select input; internal pull-up/pull-down |
| ERRN | 10 | O | error diagnosis output and wake-up indication |
| GND | 11 | P | ground |
| BM | 12 | I/O | bus line minus |
| BP | 13 | I/O | bus line plus |
| V _{CC} | 14 | P | supply voltage (+5 V) |

6. Functional description

6.1 Power modes

The TJA1083G features three power modes: Normal, Standby and Power-off. Normal and Standby modes can be selected via the STBN input (HIGH for Normal mode) once the transceiver has been powered up. See [Table 3](#) for a detailed description of pin signaling in the three power modes.

Table 3. Pin signaling in the different power modes

| Mode | STBN | UV at V _{Io} | UV at V _{CC} | ERRN | | RXD | | SDO | Biasing BP, BM | UV-det | Transmitter | Low-power receiver |
|-----------|------|-----------------------|-----------------------|------------------------------|--------------------------------|------------------------------|--------------------------------|---|---------------------|----------|-------------|------------------------|
| | | | | LOW | HIGH | LOW | HIGH | | | | | |
| Normal | HIGH | no | no | error flag set | error flag reset | bus DATA_0 | bus DATA_1 or idle | high-impedance (in simple error indication mode) or enabled (in SPI mode) | V _{CC} / 2 | enabled | enabled | enabled ^[1] |
| Standby | LOW | no | no | wake flag set | wake flag reset | wake flag set | wake flag reset | high-impedance | GND | | disabled | enabled ^[2] |
| | LOW | no | yes ^[3] | wake flag set ^[4] | wake flag reset ^[4] | wake flag set ^[4] | wake flag reset ^[4] | | | | | disabled |
| | HIGH | no | yes ^[3] | error flag set | error flag reset | wake flag set ^[4] | wake flag reset ^[4] | | | | | enabled ^[2] |
| | X | yes ^[5] | no | LOW | | LOW | | | | | | disabled |
| | X | yes ^[5] | yes ^[3] | LOW | | LOW | | | | | | disabled |
| Power-off | X | X ^[5] | yes | high-impedance | | HIGH | | | GND ^[6] | disabled | | disabled |

- [1] The wake flag is set if a valid wake-up event is detected while switching to Standby mode.
- [2] The wake flag is set if a valid wake-up event is detected.
- [3] $V_{uvd}(V_{CC}) > V_{CC} > V_{th(det)POR}$.
- [4] Pins ERRN and RXD reflect the state of the wake flag prior to the V_{CC} undervoltage event.
- [5] The internal signals at pins STBN, BGE and TXD are set LOW; the internal signals at pins TXEN, SCLK and SCSN are set HIGH.
- [6] Except when V_{CC} = 0; in this case BP and BM are floating.

6.1.1 Normal mode

In Normal mode, the transceiver transmits and receives data via the bus lines BP and BM. The transmitter and the normal receiver are enabled, along with the undervoltage detection function. The timing diagram for Normal mode is illustrated in [Figure 3](#).

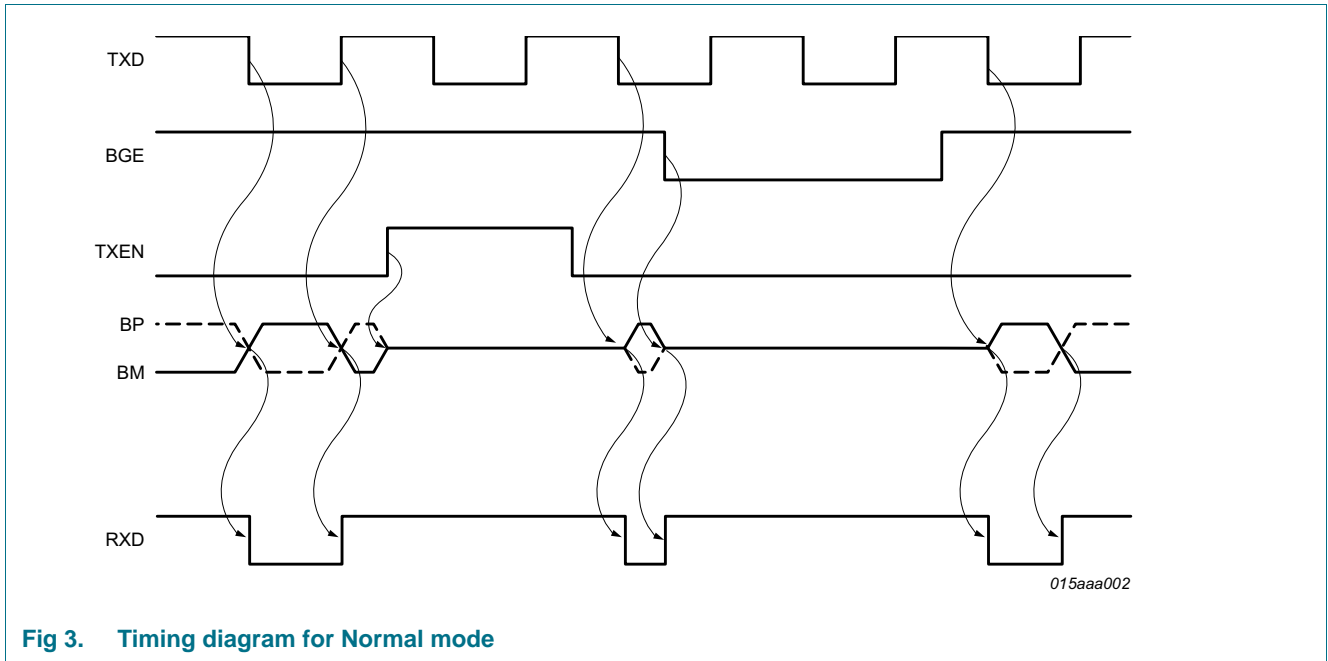


Fig 3. Timing diagram for Normal mode

Table 4 describes the behavior of the transmitter in Normal mode, when the temperature flag (TEMP HIGH) is not set and with no timeout on pin TXEN. Transmitter behavior is illustrated in Figure 13.

Table 4. Transmitter operation in Normal mode

| BGE | TXEN | TXD | Bus state | Transmitter |
|-----|------|-----|-----------|---|
| L | X | X | idle | transmitter is disabled |
| X | H | X | idle | transmitter is disabled |
| H | L | H | DATA_1 | transmitter is enabled; the bus lines are actively driven; BP is driven HIGH and BM is driven LOW |
| H | L | L | DATA_0 | transmitter is enabled; the bus lines are actively driven; BP is driven LOW and BM is driven HIGH |

The transmitter is activated during the first LOW level on pin TXD while pin BGE is HIGH and pin TXEN is LOW.

In Normal mode, the normal receiver output is connected directly to pin RXD (see Table 5). Receiver behavior is illustrated in Figure 14.

Table 5. Behavior of normal receiver in Normal mode

| Bus state | RXD |
|-----------|-----|
| DATA_0 | L |
| DATA_1 | H |
| idle | H |

When V_{IO} and V_{CC} are within their operating ranges, pin ERRN indicates the status of the error flag. See Section 6.8 for a detailed description of error signaling in Normal mode.

6.1.1.1 Bus activity and idle detection

In Normal mode, bus activity and bus idle are detected as follows:

- Bus activity is detected when the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$:
 - If the differential voltage on the bus lines is lower than $V_{L(dif)}$ after bus activity has been detected, pin RXD switches LOW.
 - If the differential voltage on the bus lines is higher than $V_{H(dif)}$ after bus activity has been detected, pin RXD remains HIGH.
- Bus idle is detected when the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$. This results in pin RXD being switched HIGH or staying HIGH.

6.1.2 Standby mode

Standby mode is a low-power mode featuring very low current consumption. In Standby mode, the transceiver is unable to transmit or receive data since both the transmitter and the normal receiver are switched off. The low-power receiver is activated to monitor the bus for wake-up activity, provided an undervoltage has not been detected on pin V_{CC} .

The low-power receiver is deactivated if an undervoltage is detected on pin V_{CC} - with the result that the wake flag is not set if a wake-up pattern or dedicated data frame is received.

Pins ERRN and RXD indicate the status of the wake flag when V_{IO} and V_{CC} are within their operating ranges. See [Table 3](#) for a description of pins ERRN and RXD when an undervoltage is detected on pin V_{IO} or pin V_{CC} .

The status register cannot be read via the SPI interface if an undervoltage is detected on pin V_{IO} .

The BGE input has no effect in Standby mode.

6.1.3 Power-off mode

The transmitter and the two receivers (normal and low-power) are deactivated in Power-off mode. As a result, the wake flag is not set if a wake-up pattern or dedicated data frame is received. If the voltage at V_{CC} rises above $V_{th(rec)POR}$, the transceiver switches to Standby mode and the digital section is reset. If V_{CC} later drops below $V_{th(det)POR}$, the transceiver reverts to Power-off mode (see [Section 6.2](#)).

The status register cannot be read via the SPI interface in Power-off mode.

6.1.4 State transitions

[Figure 4](#) shows the TJA1083G state transition diagram. The timing diagram for the ERRN indication signal during transitions between Normal and Standby modes, when the error flag is set and the wake flag is not set, is illustrated in [Figure 5](#) and described in [Table 6](#).

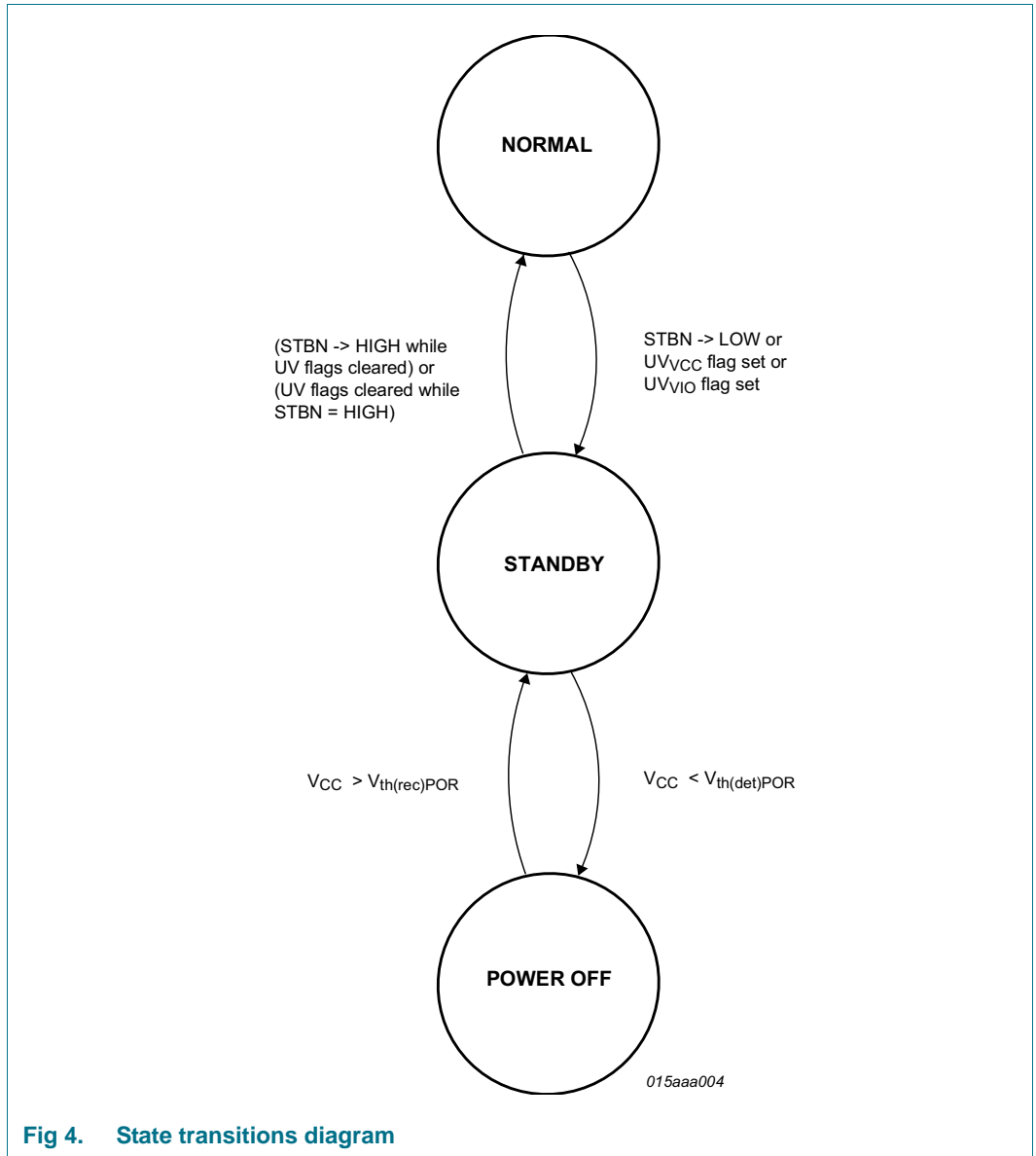


Fig 4. State transitions diagram

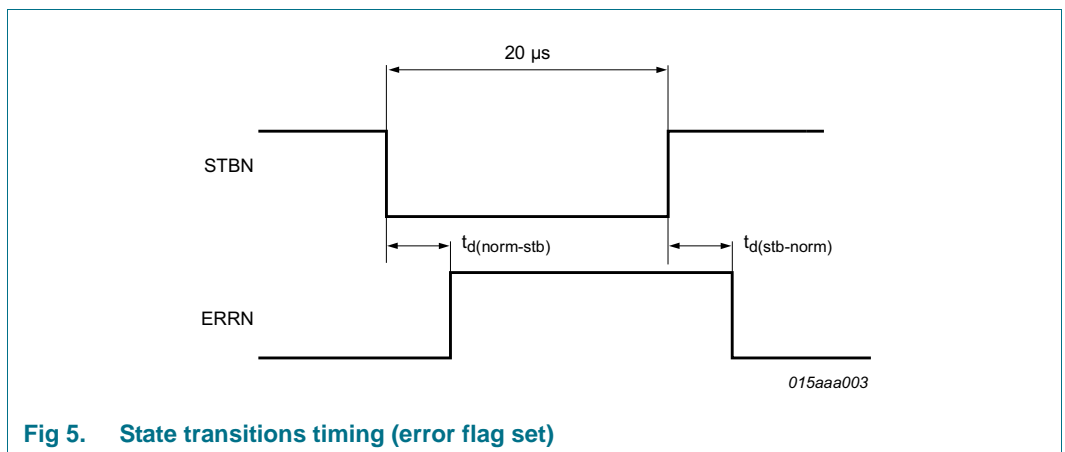


Fig 5. State transitions timing (error flag set)

Table 6. State transitions

→ indicates the action that initiates a transaction; 1 → and 2 → are the consequences of a transaction.

| Transition | UVV _{IO} flag ^[1] | UVV _{CC} flag ^[1] | wake flag ^[1] | PWON flag ^[1] | STBN | VCC level |
|----------------------|---------------------------------------|---------------------------------------|--------------------------|--------------------------|------|---|
| Normal to Standby | cleared | cleared | cleared | cleared | → L | $V_{CC} > V_{uvd}(V_{CC})$ |
| | → set | cleared | cleared | cleared | H | $V_{CC} > V_{uvd}(V_{CC})$ |
| | cleared | → set | cleared | cleared | H | $V_{uvd}(V_{CC}) > V_{CC} > V_{th(det)POR}$ |
| Standby to Normal | cleared | cleared | 1 → cleared | 2 → cleared | → H | $V_{CC} > V_{uvd}(V_{CC})$ |
| | → cleared | cleared | 1 → cleared | 2 → cleared | H | $V_{CC} > V_{uvd}(V_{CC})$ |
| | cleared | → cleared | 1 → cleared | 2 → cleared | H | $V_{uvd}(V_{CC}) > V_{CC} > V_{th(det)POR}$ |
| Standby to Power-off | X | set | X | X | X | → $V_{CC} < V_{th(det)POR}$ |
| Power-off to Standby | X | set | X | 1 → set | X | → $V_{CC} > V_{th(rec)POR}$ |

[1] See [Table 7](#) for set and reset conditions of all flags.

6.2 Power-up and power-down behavior

6.2.1 Power-up

The TJA1083G has two supply pins: V_{CC} (+5 V) and V_{IO} (for the voltage level adaptation). The ramp up of the different power supplies can vary, depending on the state or value of a number of signals and parameters. The power-up behavior of the TJA1083G is not affected by the sequence in which power is supplied to these pins or by the voltage ramp up.

As an example, [Figure 6](#) shows one possible power supply ramp-up scenario. The digital section of the TJA1083G is supplied by V_{CC}. The voltage on pin V_{CC} ramps up before the voltage on pin V_{IO}. As long as the voltage on V_{CC} remains below the power-on reset recovery threshold, V_{th(rec)POR}, the internal state machine is inactive and the transceiver is totally passive, remaining in Power-off mode. As soon as the voltage rises above the V_{th(rec)POR} threshold, the internal state machine starts running, setting the PWON flag and switching the TJA1083G to Standby mode. This initializes the V_{CC} and V_{IO} under-voltage flags to the set state (since both V_{CC} and V_{IO} are actually in undervoltage state just after power-on).

Once both V_{IO} and V_{CC} have reached their operating ranges, the under-voltage flags are reset. The operating mode is then determined by the level on STBN (the TJA1083G switches to Normal mode if STBN is HIGH and remains in Standby mode if STBN is LOW), provided V_{IO} and V_{CC} are above their respective undervoltage recovery levels (V_{uvr(VIO)} and V_{uvr(VCC)}).

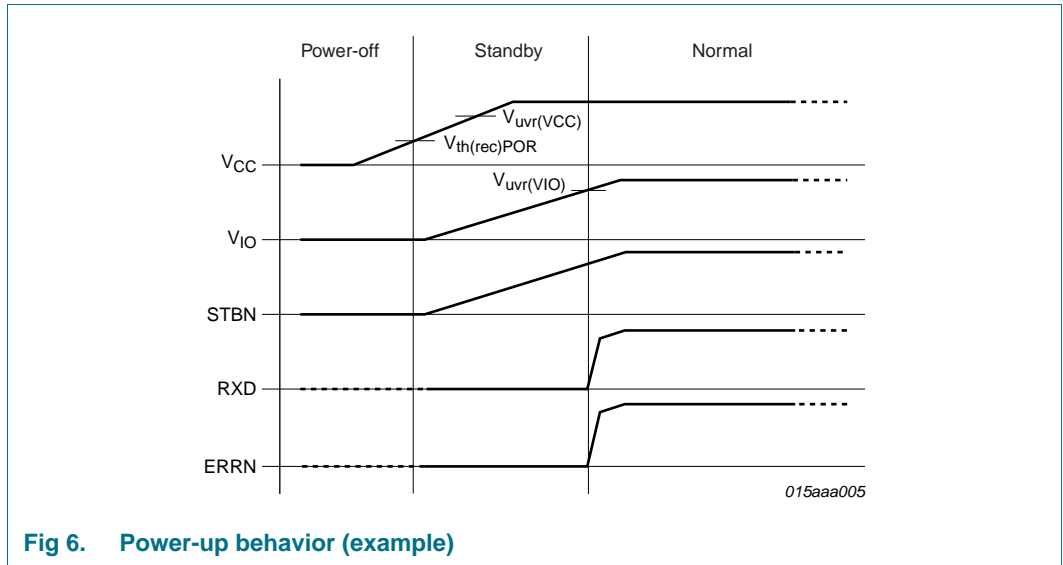


Fig 6. Power-up behavior (example)

6.2.2 Power-down

The behavior of the TJA1083G during power-down is illustrated in [Figure 7](#).

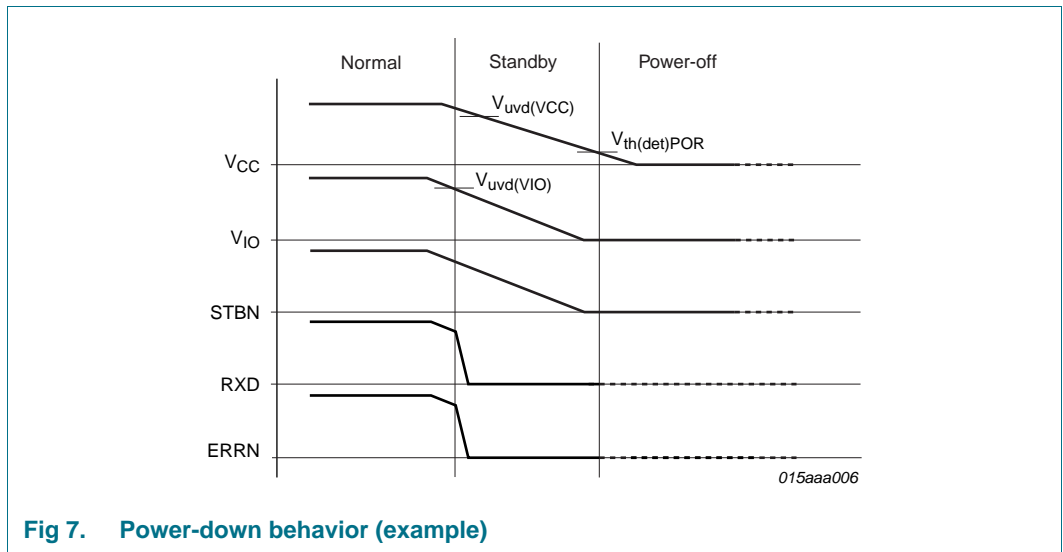


Fig 7. Power-down behavior (example)

6.3 Remote wake-up

6.3.1 Bus wake-up via wake-up pattern

A valid remote wake-up event occurs when a wake-up pattern is received. A wake-up pattern consists of at least two consecutive wake-up symbols. A wake-up symbol comprises a DATA_0 phase lasting longer than $t_{det(wake)DATA_0}$ followed by an idle phase lasting longer than $t_{det(wake)idle}$, provided both wake-up symbols occur within a time span of $t_{det(wake)tot}$ (see Figure 8). The transceiver also wakes up if DATA_1 phases are substituted for the idle phases.

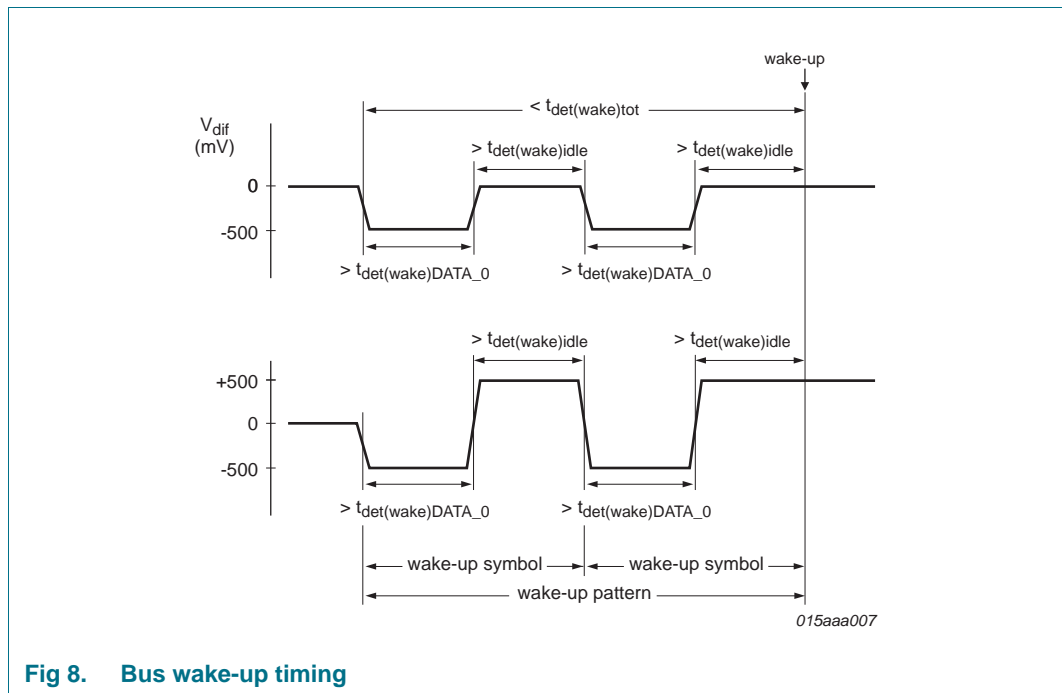


Fig 8. Bus wake-up timing

See Ref. 1 for more details of the wake-up mechanism.

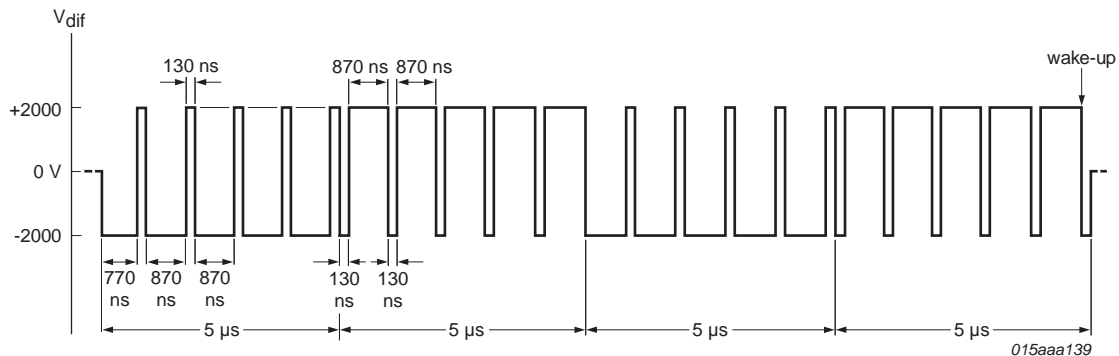
6.3.2 Bus wake-up via dedicated FlexRay data frame

The TJA1083G wake flag is set when a dedicated data frame emulating a valid wake-up pattern, as shown in Figure 9, is received.

The DATA_0 and DATA_1 phases of the emulated wake-up symbol are interrupted by the Byte Start Sequence (BSS) preceding each byte in the data frame. With a data rate of 10 Mbit/s, the interruption has a maximum duration of 130 ns and does not prevent the transceiver from recognizing the wake-up pattern in the payload.

For longer interruptions at lower data rates (5 Mbit/s and 2.5 Mbit/s), the wake-up pattern should be used (see Section 6.3.1).

The wake flag is not set if an invalid wake-up pattern is received. See Ref. 1 for more details on invalid wake-up patterns.



The duration of each interruption is 130 ns.
 The transition time from DATA_0 to DATA_1 and vice versa is about 20 ns.
 The TJA1083G wake-up flag is set on receipt of the following frame payload:
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

Fig 9. Minimum bus pattern for bus wake-up via dedicated FlexRay data frame

6.4 Bus error detection

The TJA1083G detects the following bus errors during transmission:

- Short-circuit BP to BM at the ECU connector or on the bus
- Short-circuit BP to GND at the ECU connector or on the bus
- Short-circuit BM to GND at the ECU connector or on the bus
- Short-circuit BP to V_{CC} at the ECU connector or on the bus
- Short-circuit BM to V_{CC} at the ECU connector or on the bus

The bus error flag is not set when a wake-up pattern or a FlexRay Collision Avoidance Symbol (CAS) is being transmitted or received.

6.5 Fail silent behavior

Three mechanisms guarantee the 'fail silent' behavior of the TJA1083G:

- The TXEN clamped flag is set if pin TXEN goes LOW for longer than $t_{detCL}(TXEN)$ in Normal mode; the transmitter is disabled.
- The BGE clamped flag is set if pin BGE goes HIGH for longer than $t_{detCL}(BGE)$ in Normal mode; no action is taken.
- If a loss-of-ground occurs at the transceiver, resulting in the TJA1083G switching to Power-off mode, no current flows out of the digital input pins (TXD, TXEN, BGE, STBN, SCLK, SCSN); see [Table 3](#) for details of the behavior of the bus pins.

6.6 TJA1083G flags

The TJA1083G has 11 status/error flags, described in [Table 7](#).

Table 7. TJA1083G flags and set/reset conditions

| Flag name | Flag type | Flag description | Set condition | Reset condition ^[1] | Consequence of flag set |
|---------------------|-------------|--|--|--|---|
| bus wake | status flag | indicates if a wake-up event has occurred | wake-up event on bus in Standby mode ^[2] | transition to Normal mode | RXD → LOW; ERRN → LOW ^[3] |
| Normal mode | status flag | indicates if the transceiver is in Normal mode | entering Normal mode | leaving Normal mode | - |
| transmitter enabled | status flag | indicates the transmitter status | transmitter enabled ^[4] | transmitter disabled | - |
| BGE clamped | status flag | indicates if pin BGE is clamped | BGE HIGH for longer than $t_{detCL}(BGE)$ ^[5] | BGE LOW ^[5] | - |
| PWON | status flag | indicates when the digital section is initialized | $V_{CC} > V_{th(rec)POR}$ | transition to Normal mode | - |
| bus error | error flag | indicates if a bus error has been detected | bus error detected ^[5] | no bus error detected or positive edge on TXEN ^[5] | ERRN → LOW ^[6] |
| TEMP HIGH | error flag | indicates if the max. junction temperature has been reached | $T_{vj} > T_{j(dis)(high)}$ ^[5] | TXEN = HIGH while $T_{vj} < T_{j(dis)(high)}$ ^[5] | ERRN → LOW ^[6] ; transmitter disabled |
| TXEN clamped | error flag | indicates if pin TXEN is clamped | TXEN LOW for longer than $t_{detCL}(TXEN)$ ^[5] | TXEN = HIGH ^[5] | ERRN → LOW ^[6] ; transmitter disabled |
| UVV _{CC} | error flag | indicates if there is an undervoltage at pin V _{CC} | $V_{CC} < V_{uvd}(V_{CC})$ for longer than $t_{det}(uv)(V_{CC})$ | $V_{CC} > V_{uvr}(V_{CC})$ for longer than $t_{rec}(uv)(V_{CC})$ | ERRN → LOW ^[6] ; entering Standby mode |
| UVV _{IO} | error flag | indicates if there is an undervoltage at pin V _{IO} | $V_{IO} < V_{uvd}(V_{IO})$ for longer than $t_{det}(uv)(V_{IO})$ | $V_{IO} > V_{uvr}(V_{IO})$ for longer than $t_{rec}(uv)(V_{IO})$ | ERRN → LOW ^[6] ; entering Standby mode |
| SPI error | error flag | indicates if an SPI error has occurred | SPI error detected ^[8] | falling edge on SCSN | ERRN → LOW ^[7] ; SDO goes to a high impedance state |

[1] All flags, except for the PWON flag, are reset after a power-on reset.

[2] If an undervoltage has not been detected on pin V_{CC}.

[3] If STBN = LOW.

[4] If BGE = HIGH, the Normal mode flag is set, the TEMP HIGH flag is not set, and the TXEN clamped flag is not set.

[5] Flag can only be set or reset in Normal mode or on leaving Normal mode.

[6] If STBN = HIGH.

[7] If STBN = HIGH in SPI mode

[8] The SPI error flag is set when:

- more than 16 falling edges occur on pin SCLK while pin SCSN = LOW
- less than 16 falling edges occur on pin SCLK while pin SCSN = LOW.

6.7 TJA1083G status register

The TJA1083G contains a 16-bit status register, of which bits S0 to S4 reflects the state of the status flags, bits S5 to S10 reflect the state of the error flags and bit S15 is a parity bit. All flags can be individually read out on pin SDO via a 16-bit SPI interface when the transceiver is configured in SPI mode. The status register bits are described in [Table 8](#).

Table 8. TJA1083G status register

| Status bit | Flag name | Set condition | Reset condition |
|------------|---------------------|------------------------------|--|
| S0 | bus wake | bus wake flag set | bus wake flag cleared |
| S1 | Normal mode | Normal mode flag set | Normal mode flag cleared |
| S2 | transmitter enabled | transmitter enabled flag set | transmitter enabled flag cleared |
| S3 | BGE clamped | BGE clamped flag set | BGE clamped flag cleared |
| S4 | PWON | PWON flag set | PWON flag cleared and successful readout ^[1] |
| S5 | bus error | bus error flag set | bus error flag cleared and successful readout ^[1] |
| S6 | TEMP HIGH | TEMP HIGH flag set | TEMP HIGH flag cleared and successful readout ^[1] |
| S7 | TXEN clamped | TXEN clamped flag set | TXEN clamped flag cleared and successful readout ^[1] |
| S8 | UVV _{CC} | UVV _{CC} flag set | UVV _{CC} flag cleared and successful readout ^[1] |
| S9 | UVV _{IO} | UVV _{IO} flag set | UVV _{IO} flag cleared and successful readout ^[1] |
| S10 | SPI error | SPI error flag set | SPI error flag cleared and successful readout ^[1] |
| S11 | reserved | always LOW | |
| S12 | reserved | always HIGH | |
| S13 | reserved | always LOW | |
| S14 | reserved | always HIGH | |
| S15 | parity bit | odd parity of status bits | even parity of status bits |

[1] Also cleared during Power-off.

6.8 Error signaling

The TJA1083G provides two modes for error indication:

- Simple error indication mode
- SPI mode (default mode)

SPI mode is active on power-up.

To switch to simple error indication mode, SCSN must be held LOW (connected to GND) and SCLK held HIGH (connected to V_{IO}) for longer than $t_{\text{det(L)}(\text{SCLK})}$ (provided a V_{IO} undervoltage has not occurred). When the TJA1083G is in simple error indication mode, a rising edge on SCSN initiates a transition to SPI mode (again provided a V_{IO} undervoltage has not occurred); see [Figure 10](#).

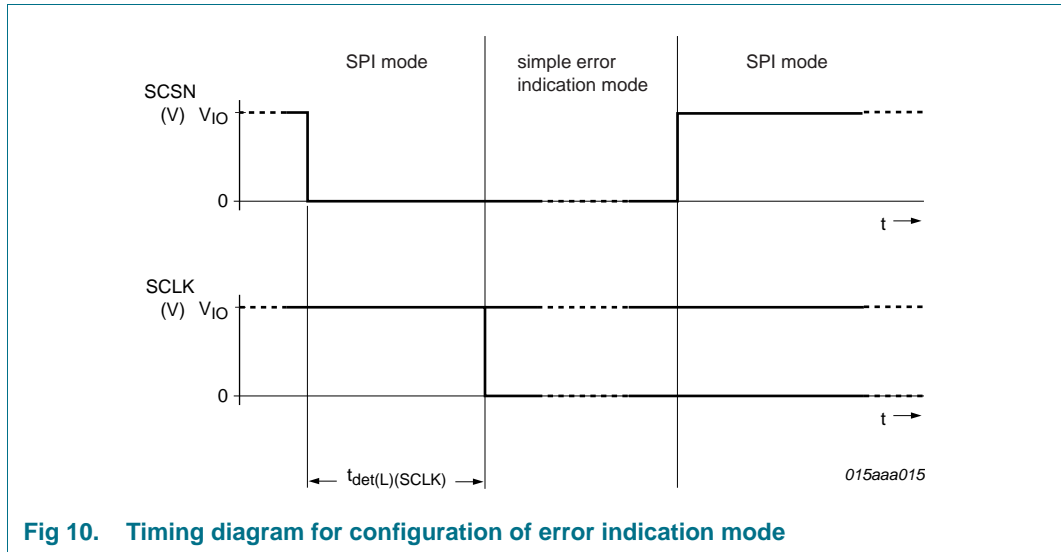


Fig 10. Timing diagram for configuration of error indication mode

If a V_{IO} undervoltage condition is detected, it is not possible to switch between SPI mode and simple error indication mode.

6.8.1 SPI mode

The error flag information in the status register is latched in SPI mode. This means that the status bit is reset once the status register has been completely read (provided the corresponding error flag has been reset). If an error condition is detected in Normal mode, pin ERRN goes LOW (provided one of the error bits, S5 to S10, is set). Pin ERRN goes HIGH again once all the error bits have been reset.

6.8.2 Simple error indication mode

If an error condition is detected in Normal mode, pin ERRN goes LOW once the relevant error flag has been set. Pin ERRN stays stable for at least $t_{ERRNL(min)}$ and goes HIGH again when all error conditions have been cleared and all flags have been reset. Error flags are not latched. It is not possible to read-out the status bits in this mode.

6.9 SPI interface

The TJA1083G includes a 16-bit SPI interface to enable a host to read the status register when the transceiver is in SPI mode (see [Section 6.8](#)).

While pin SCSN is HIGH, the SDO output is in a high-impedance state. To begin a status register readout, the host must force pin SCSN LOW. This action causes the SDO pin to output a LOW level by default. The data on pin SDO is then shifted out on the rising edge of the clock signal on pin SCLK.

The status bits shifted out on pin SDO are active HIGH. The status bits are refreshed and pin SDO returned to a high-impedance state once the status register has been read successfully (after exactly 16 clock cycles) and SCSN has been forced HIGH again. Clock signals on SCLK are ignored while SCSN is HIGH. The timing diagram for the SPI readout is illustrated in [Figure 11](#).

The SCLK period ranges from 500 ns to 100 μ s (10 kbit/s to 2 Mbit/s).

If SCSN remains LOW for longer than 16 clock cycles, it is recognized as an SPI error. When this happens, the SPI error flag is set and pin SDO goes to a high-impedance state until the next falling edge on pin SCSN.

An SPI error is also assumed if fewer than 16 clock cycles are received while SCSN is LOW. If this happens, the SPI error flag is set.

All status bits are refreshed once the status register has been successfully read.

When the transceiver is in simple error indication mode the SDO output is in a high-impedance state and pin SCSN is in pull-down mode. In SPI mode pin SCSN is in pull-up mode.

SPI readout is not possible when the transceiver has detected an undervoltage on V_{IO} .

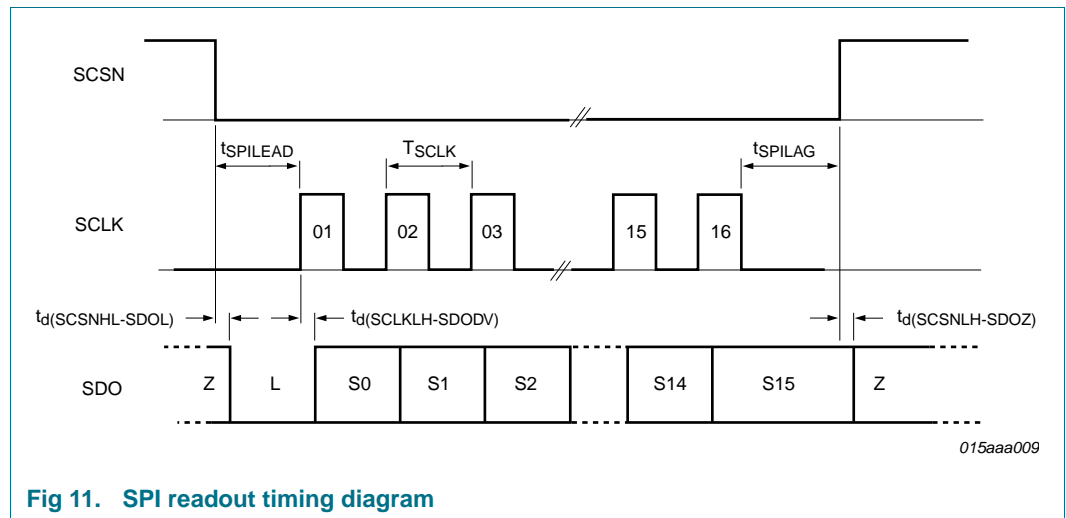


Fig 11. SPI readout timing diagram

7. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|--------------------------------|---|------|----------------|------|
| V_{CC} | supply voltage | no time limit | -0.3 | +5.5 | V |
| V_{IO} | supply voltage on pin V_{IO} | no time limit | -0.3 | +5.5 | V |
| V_{ERRN} | voltage on pin ERRN | no time limit | -0.3 | $V_{IO} + 0.3$ | V |
| V_{RXD} | voltage on pin RXD | no time limit | -0.3 | $V_{IO} + 0.3$ | V |
| V_{SDO} | voltage on pin SDO | no time limit | -0.3 | $V_{IO} + 0.3$ | V |
| V_{TXEN} | voltage on pin TXEN | no time limit | -0.3 | +5.5 | V |
| V_{TXD} | voltage on pin TXD | no time limit | -0.3 | +5.5 | V |
| V_{STBN} | voltage on pin STBN | no time limit | -0.3 | +5.5 | V |
| V_{SCSN} | voltage on pin SCSN | no time limit | -0.3 | +5.5 | V |
| V_{SCLK} | voltage on pin SCLK | no time limit | -0.3 | +5.5 | V |
| V_{BGE} | voltage on pin BGE | no time limit | -0.3 | +5.5 | V |
| V_{BP} | voltage on pin BP | no time limit (with respect to pins BM and GND) | -60 | +60 | V |

Table 9. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------------|---------------------------------|---|-----------|-------|------|
| V _{BM} | voltage on pin BM | no time limit (with respect to pins BP and GND) | -60 | +60 | V |
| I _{I(ERRN)} | input current on pin ERRN | no time limit; V _{IO} = 0 V | -10 | 10 | mA |
| I _{I(RXD)} | input current on pin RXD | no time limit; V _{IO} = 0 V | -10 | 10 | mA |
| I _{I(SDO)} | input current on pin SDO | no time limit; V _{IO} = 0 V | -10 | 10 | mA |
| V _{trt} | transient voltage | on pins BM and BP | [1] -100 | - | V |
| | | | [2] - | 75 | V |
| | | | [3] -150 | - | V |
| | | | [4] - | 100 | V |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| T _{vj} | virtual junction temperature | | [5] -40 | +150 | °C |
| T _{amb} | ambient temperature | | -40 | +125 | °C |
| V _{ESD} | electrostatic discharge voltage | IEC61000-4-2 on pins BP and BM to ground | [6] -6.0 | +6.0 | kV |
| | | HBM on pins BP and BM to ground | [7] -8.0 | +8.0 | kV |
| | | HBM on any other pin | [7] -4.0 | +4.0 | kV |
| | | MM on all pins | [8] -200 | +200 | V |
| | | CDM on all pins | [9] -1000 | +1000 | V |

- [1] According to ISO7637, test pulse 1, class C; verified by an external test house.
- [2] According to ISO7637, test pulse 2a, class C; verified by an external test house.
- [3] According to ISO7637, test pulse 3a, class C; verified by an external test house.
- [4] According to ISO7637, test pulse 3b, class C; verified by an external test house.
- [5] In accordance with IEC 60747-1. An alternative definition of T_{vj} is: T_{vj} = T_{amb} + P × R_{th(j-a)}, where R_{th(j-a)} is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
- [6] IEC61000-4-2: C = 150 pF; R = 330 Ω; verified by an external test house; the test results were equal to or better than ±6 kV (unaided).
- [7] HBM: C = 100 pF; R = 1.5 kΩ.
- [8] MM: C = 200 pF; L = 0.75 μH; R = 10 Ω.
- [9] CDM: R = 1 Ω.

8. Thermal characteristics

Table 10. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|----------------------|---|------------------|-----------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | dual-layer board | [1] 109.5 | K/W |
| | | four-layer board | [2] 83.0 | K/W |

- [1] According to JEDEC JESD51-2 and JESD51-3 at natural convection on 1s board.
- [2] According to JEDEC JESD51-2 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm).

9. Static characteristics

Table 11. Static characteristics

All parameters are guaranteed for $V_{CC} = 4.45\text{ V to }5.25\text{ V}$; $V_{IO} = 2.55\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ °C to }+150\text{ °C}$; $R_{bus} = 40\ \Omega\text{ to }55\ \Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---|---|-------------|-----|-------|---------------|
| Pin V_{CC} | | | | | | |
| I_{CC} | supply current | Standby mode with no undervoltage; $T_{vj} \leq 85\text{ °C}$ | - | 20 | 30 | μA |
| | | Standby mode with no undervoltage; $T_{vj} \leq 150\text{ °C}$ | - | 20 | 40 | μA |
| | | Power-off mode; $T_{vj} \leq 85\text{ °C}$ | - | - | 30 | μA |
| | | Power-off mode; $T_{vj} \leq 150\text{ °C}$ | - | - | 40 | μA |
| | | Normal mode; $V_{BGE} = 0\text{ V}$ or $V_{TXEN} = V_{IO}$ | - | 13 | 21 | mA |
| | | Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$ | - | 36 | 50 | mA |
| | | Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$; $R_{bus} > 10\ \text{M}\Omega$ | - | 14 | 22 | mA |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin V_{CC} | | 4.45 | - | 4.729 | V |
| $V_{uvr(VCC)}$ | undervoltage recovery voltage on pin V_{CC} | | 4.47 | - | 4.749 | V |
| $V_{uvhys(VCC)}$ | undervoltage hysteresis voltage on pin V_{CC} | | 20 | - | 290 | mV |
| $V_{th(det)POR}$ | power-on reset detection threshold voltage | | 3.75 | - | 4.15 | V |
| $V_{th(rec)POR}$ | power-on reset recovery threshold voltage | | 3.85 | - | 4.25 | V |
| $V_{hys(POR)}$ | power-on reset hysteresis voltage | | 100 | - | 500 | mV |
| Pin V_{IO} | | | | | | |
| I_{IO} | supply current on pin V_{IO} | Normal mode; $V_{TXEN} = V_{IO}$; $V_{BGE} = V_{IO}$; $R_{RXD} > 10\ \text{M}\Omega$ | - | - | 1000 | μA |
| | | Normal mode; $V_{TXEN} = 0\text{ V}$; $V_{BGE} = V_{IO}$; $R_{RXD} > 10\ \text{M}\Omega$ | - | - | 1000 | μA |
| | | Standby mode with no undervoltage | - | 2.2 | 7 | μA |
| | | Power-off mode; $V_{IO} = 5\text{ V}$ | - | 3 | 7 | μA |
| $V_{uvd(VIO)}$ | undervoltage detection voltage on pin V_{IO} | | 2.55 | - | 2.774 | V |
| $V_{uvr(VIO)}$ | undervoltage recovery voltage on pin V_{IO} | | 2.575 | - | 2.799 | V |
| $V_{uvhys(VIO)}$ | undervoltage hysteresis voltage on pin V_{IO} | | 25 | - | 240 | mV |
| Pin SCSN | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |

Table 11. Static characteristics ...continued

All parameters are guaranteed for $V_{CC} = 4.45\text{ V to }5.25\text{ V}$; $V_{IO} = 2.55\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|--|------|-----|-------------|---------------|
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{IO}$ | V |
| I_{IH} | HIGH-level input current | Simple error indication mode; $V_{SCSN} = 0.7V_{IO}$ | 3 | - | 15 | μA |
| I_{IL} | LOW-level input current | SPI mode; $V_{SCSN} = 0.3V_{IO}$ | -15 | - | -3 | μA |
| I_r | reverse current | Power-off mode; to V_{CC}/V_{IO} ; $V_{SCSN} = 5\text{ V}$; $V_{CC} = V_{IO} = 0\text{ V}$ | -5 | 0 | +5 | μA |

Pin SCLK

| | | | | | | |
|----------|--------------------------|--|-------------|---|-------------|---------------|
| V_{IH} | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{IO}$ | V |
| I_{IH} | HIGH-level input current | $V_{SCLK} = V_{IO}$ | -1 | 0 | +1 | μA |
| I_{IL} | LOW-level input current | $V_{SCLK} = 0.3V_{IO}$ | -15 | - | -3 | μA |
| I_r | reverse current | Power-off mode; to V_{CC}/V_{IO} ; $V_{SCLK} = 5\text{ V}$; $V_{CC} = V_{IO} = 0\text{ V}$ | -5 | 0 | +5 | μA |

Pin STBN

| | | | | | | |
|----------|--------------------------|--|-------------|---|-------------|---------------|
| V_{IH} | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{IO}$ | V |
| I_{IH} | HIGH-level input current | $V_{STBN} = 0.7V_{IO}$ | 3 | - | 15 | μA |
| I_{IL} | LOW-level input current | $V_{STBN} = 0\text{ V}$ | -1 | 0 | +1 | μA |
| I_r | reverse current | Power-off mode; to V_{CC}/V_{IO} ; $V_{STBN} = 5\text{ V}$; $V_{CC} = V_{IO} = 0\text{ V}$ | -5 | 0 | +5 | μA |

Pin TXEN

| | | | | | | |
|----------|--------------------------|--|-------------|---|-------------|---------------|
| V_{IH} | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{IO}$ | V |
| I_{IH} | HIGH-level input current | $V_{TXEN} = V_{IO}$ | -1 | 0 | +1 | μA |
| I_{IL} | LOW-level input current | $V_{TXEN} = 0.3V_{IO}$ | -300 | - | -50 | μA |
| I_r | reverse current | Power-off mode; to V_{CC}/V_{IO} ; $V_{TXEN} = 5\text{ V}$; $V_{CC} = V_{IO} = 0\text{ V}$ | -5 | 0 | +5 | μA |

Pin BGE

| | | | | | | |
|----------|--------------------------|---|-------------|---|-------------|---------------|
| V_{IH} | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{IO}$ | V |
| I_{IH} | HIGH-level input current | $V_{BGE} = 0.6V_{IO}$ | 3 | - | 15 | μA |
| I_{IL} | LOW-level input current | $V_{BGE} = 0\text{ V}$ | -1 | 0 | +1 | μA |
| I_r | reverse current | Power-off mode; to V_{CC}/V_{IO} ; $V_{BGE} = 5\text{ V}$; $V_{CC} = V_{IO} = 0\text{ V}$ | -5 | 0 | +5 | μA |

Pin TXD

| | | | | | | |
|----------|--------------------------|------------------------|-------------|---|-------------|---------------|
| V_{IH} | HIGH-level input voltage | Normal mode | $0.6V_{IO}$ | - | 5.5 | V |
| V_{IL} | LOW-level input voltage | Normal mode | -0.3 | - | $0.4V_{IO}$ | V |
| I_{IH} | HIGH-level input current | $V_{TXD} = 0.6V_{IO}$ | 3 | - | 15 | μA |
| I_{IL} | LOW-level input current | $V_{TXD} = 0\text{ V}$ | -1 | 0 | +1 | μA |

Table 11. Static characteristics ...continued

All parameters are guaranteed for $V_{CC} = 4.45\text{ V}$ to 5.25 V ; $V_{IO} = 2.55\text{ V}$ to 5.25 V ; $T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $R_{bus} = 40\text{ }\Omega$ to $55\text{ }\Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|---|----------------|-----|----------|---------------|
| I_r | reverse current | Power-off mode; to V_{CC}/V_{IO} ; $V_{TXD} = 5\text{ V}$; $V_{CC} = V_{IO} = 0\text{ V}$ | -5 | 0 | +5 | μA |
| C_i | input capacitance | with respect to all other pins at ground; $V_{TXD} = 100\text{ mV}$; $f = 5\text{ MHz}$ | [1] - | - | 10 | pF |
| Pin RXD | | | | | | |
| V_{OH} | HIGH-level output voltage | $I_{OH(RXD)} = -1.5\text{ mA}$ | $V_{IO} - 0.4$ | - | V_{IO} | V |
| V_{OL} | LOW-level output voltage | $I_{OL(RXD)} = 1.5\text{ mA}$ | - | - | 0.4 | V |
| I_{OH} | HIGH-level output current | $V_{RXD} = V_{IO} - 0.4\text{ V}$; $V_{IO} = V_{CC}$ | -15 | - | -1.0 | mA |
| I_{OL} | LOW-level output current | $V_{RXD} = 0.4\text{ V}$ | 1.0 | - | 15 | mA |
| V_O | output voltage | when undervoltage on V_{IO} ; $R_L = 100\text{ k}\Omega$ to GND | - | - | 500 | mV |
| | | Power-off mode; $R_L = 100\text{ k}\Omega$ to V_{IO} | $V_{IO} - 500$ | - | V_{IO} | mV |
| Pin ERRN | | | | | | |
| V_{OH} | HIGH-level output voltage | $I_{OH(ERRN)} = -100\text{ }\mu\text{A}$ | $V_{IO} - 0.4$ | - | V_{IO} | V |
| V_{OL} | LOW-level output voltage | $I_{OL(ERRN)} = 200\text{ }\mu\text{A}$ | - | - | 0.4 | V |
| I_{OH} | HIGH-level output current | $V_{ERRN} = V_{IO} - 0.4\text{ V}$; $V_{IO} = V_{CC}$ | -1500 | - | -100 | μA |
| I_{OL} | LOW-level output current | $V_{ERRN} = 0.4\text{ V}$ | 200 | - | 1700 | μA |
| I_L | leakage current | Power-off mode; $V_{ERRN} \leq V_{IO}$ | -5 | - | +5 | μA |
| V_O | output voltage | when undervoltage on V_{IO} ; $R_L = 100\text{ k}\Omega$ to GND | - | - | 500 | mV |
| | | Power-off mode; $R_L = 100\text{ k}\Omega$ to GND | - | - | 500 | mV |
| Pin SDO | | | | | | |
| V_{OH} | HIGH-level output voltage | $I_{OH(SDO)} = -0.5\text{ mA}$ | $V_{IO} - 0.4$ | - | V_{IO} | V |
| V_{OL} | LOW-level output voltage | $I_{OL(SDO)} = 0.8\text{ mA}$ | - | - | 0.4 | V |
| I_{OH} | HIGH-level output current | $V_{SDO} = V_{IO} - 0.4\text{ V}$ | -8 | -3 | -0.5 | mA |
| I_{OL} | LOW-level output current | $V_{SDO} = 0.4\text{ V}$ | 0.8 | 3 | 9 | mA |
| I_L | leakage current | high-impedance state; $0\text{ V} < V_{SDO} < V_{IO}$ | -5 | - | +5 | μA |

Table 11. Static characteristics ...continued

All parameters are guaranteed for $V_{CC} = 4.45\text{ V to }5.25\text{ V}$; $V_{IO} = 2.55\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|--|---|-------------|-------------|-------------|------------|
| V_O | output voltage | when undervoltage on V_{IO} ; $V_{CC} > 4.75\text{ V}$; $R_L = 100\text{ k}\Omega$ to GND | -500 | - | +500 | mV |
| | | Power-off mode; $R_L = 100\text{ k}\Omega$ to GND | - | - | 500 | mV |
| Pins BP and BM | | | | | | |
| $V_{o(idle)(BP)}$ | idle output voltage on pin BP | Normal mode; $V_{TXEN} = V_{IO}$ | $0.4V_{CC}$ | $0.5V_{CC}$ | $0.6V_{CC}$ | V |
| | | Standby mode with no undervoltage on pin V_{CC} | -0.1 | 0 | +0.1 | V |
| $V_{o(idle)(BM)}$ | idle output voltage on pin BM | Normal mode; $V_{TXEN} = V_{IO}$ | $0.4V_{CC}$ | $0.5V_{CC}$ | $0.6V_{CC}$ | V |
| | | Standby mode with no undervoltage on pin V_{CC} | -0.1 | 0 | +0.1 | V |
| $I_{o(idle)BP}$ | idle output current on pin BP | Normal and Standby modes with no undervoltage; $-60\text{ V} \leq V_{BP} \leq +60\text{ V}$ | -7.5 | - | +7.5 | mA |
| $I_{o(idle)BM}$ | idle output current on pin BM | Normal and Standby modes with no undervoltage; $-60\text{ V} \leq V_{BM} \leq +60\text{ V}$ | -7.5 | - | +7.5 | mA |
| $V_{o(idle)(dif)}$ | differential idle output voltage | Normal mode | -25 | 0 | +25 | mV |
| $V_{OH(dif)}$ | differential HIGH-level output voltage | $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ | 600 | - | 2000 | mV |
| | | $4.45\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ | 530 | - | 2000 | mV |
| $V_{OL(dif)}$ | differential LOW-level output voltage | $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ | -2000 | - | -600 | mV |
| | | $4.45\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ | -2000 | - | -530 | mV |
| $V_{IH(dif)}$ | differential HIGH-level input voltage | Normal mode; $-10\text{ V} \leq V_{cm} \leq +15\text{ V}$ | [2] 150 | 225 | 300 | mV |
| $V_{IL(dif)}$ | differential LOW-level input voltage | Normal mode; $-10\text{ V} \leq V_{cm} \leq +15\text{ V}$ | [2] -300 | -225 | -150 | mV |
| | | Standby mode with no undervoltage on pin V_{CC} ; $-10\text{ V} \leq V_{cm} \leq +15\text{ V}$ | [2] -400 | -225 | -100 | mV |
| $ \Delta V_{i(dif)(H-L)} $ | differential input volt. diff. betw. HIGH- and LOW-levels (abs. value) | $V_{cm} = 2.5\text{ V}$ | [2] - | - | 30 | mV |
| $ V_{i(dif)det(act)} $ | activity detection differential input voltage (absolute value) | | 150 | 225 | 300 | mV |
| $ I_{O(sc)} $ | short-circuit output current (absolute value) | on pin BP; $-5\text{ V} \leq V_{BP} \leq +60\text{ V}$; $R_{sc} \leq 1\text{ }\Omega$; $t_{sc} \geq 1500\text{ }\mu\text{s}$ | [4][6] - | - | 60 | mA |
| | | on pin BM; $-5\text{ V} \leq V_{BM} \leq +60\text{ V}$; $R_{sc} \leq 1\text{ }\Omega$; $t_{sc} \geq 1500\text{ }\mu\text{s}$ | [4][6] - | - | 60 | mA |
| | | on pins BP and BM; $V_{BP} = V_{BM}$; $R_{sc} \leq 1\text{ }\Omega$; $t_{sc} \geq 1500\text{ }\mu\text{s}$ | [5][6] - | - | 60 | mA |
| $R_{i(BP)}$ | input resistance on pin BP | $R_{bus} = \infty\text{ }\Omega$ | 10 | 20 | 40 | k Ω |
| $R_{i(BM)}$ | input resistance on pin BM | $R_{bus} = \infty\text{ }\Omega$ | 10 | 20 | 40 | k Ω |

Table 11. Static characteristics ...continued

All parameters are guaranteed for $V_{CC} = 4.45\text{ V to }5.25\text{ V}$; $V_{IO} = 2.55\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|---|-------------|-------------|--------------|--------------------|
| $R_{i(dif)(BP-BM)}$ | differential input resistance between pin BP and pin BM | $R_{bus} = \infty\text{ }\Omega$ | 20 | 40 | 80 | k Ω |
| $I_{Li(BP)}$ | input leakage current on pin BP | Power-off mode; $V_{CC} = V_{IO} = 0\text{ V}$; $0\text{ V} \leq V_{BP} \leq 5\text{ V}$ | -5 | 0 | +5 | μA |
| | | loss of ground; $V_{BP} = V_{BM} = 0\text{ V}$; all other pins connected to 16 V via $0\text{ }\Omega$ | [1] -1600 | - | +1600 | μA |
| $I_{Li(BM)}$ | input leakage current on pin BM | Power-off mode; $V_{CC} = V_{IO} = 0\text{ V}$; $0\text{ V} \leq V_{BM} \leq 5\text{ V}$ | -5 | 0 | +5 | μA |
| | | loss of ground; $V_{BP} = V_{BM} = 0\text{ V}$; all other pins connected to 16 V via $0\text{ }\Omega$ | [1] -1600 | - | +1600 | μA |
| $V_{cm(bus)(DATA_0)}$ | DATA_0 bus common-mode voltage | Normal mode | $0.4V_{CC}$ | $0.5V_{CC}$ | $0.65V_{CC}$ | V |
| $V_{cm(bus)(DATA_1)}$ | DATA_1 bus common-mode voltage | Normal mode | $0.4V_{CC}$ | $0.5V_{CC}$ | $0.65V_{CC}$ | V |
| $\Delta V_{cm(bus)}$ | bus common-mode voltage difference | Normal mode; DATA_1 – DATA_0 | -25 | 0 | +25 | mV |
| $C_{i(BP)}$ | input capacitance on pin BP | with respect to all other pins at ground; $V_{BP} = 100\text{ mV}$; $f = 5\text{ MHz}$ | [1] - | - | 15 | pF |
| $C_{i(BM)}$ | input capacitance on pin BM | with respect to all other pins at ground; $V_{BM} = 100\text{ mV}$; $f = 5\text{ MHz}$ | [1] - | - | 15 | pF |
| $C_{i(dif)(BP-BM)}$ | differential input capacitance between pin BP and pin BM | with respect to all other pins at ground; $V_{BP} = 100\text{ mV}$; $V_{BM} = 100\text{ mV}$; $f = 5\text{ MHz}$ | [1] - | - | 5 | pF |
| $Z_{o(eq)TX}$ | transmitter equivalent output impedance | Normal mode; $C_{bus} = 100\text{ pF}$; $R_{bus} = 40\text{ }\Omega\text{ or }100\text{ }\Omega$ | [3] 35 | - | 100 | Ω |
| Temperature protection | | | | | | |
| $T_{j(dis)(high)}$ | high disable junction temperature | | 180 | - | 200 | $^{\circ}\text{C}$ |

[1] Guaranteed by design.

[2] V_{cm} is the BP/BM common mode voltage.

[3] $Z_{o(TX)(eq)} = 50\text{ }\Omega \times (V_{bus(100)} - V_{bus(40)}) / (2.5 \times V_{bus(40)} - V_{bus(100)})$, where:
 $V_{bus(100)}$ = the differential output voltage on a load of 100 Ω and 100 pF in parallel.
 $V_{bus(40)}$ = the differential output voltage on a load of 40 Ω and 100 pF in parallel, when driving a DATA_1.

[4] R_{sc} is the short-circuit resistance; voltage difference between bus pins BP and BM is 60 V max.

[5] R_{sc} is the short-circuit resistance between BP and BM.

[6] t_{sc} is the minimum duration of the short-circuit

10. Dynamic characteristics

Table 12. Dynamic characteristics

All parameters are guaranteed for $V_{CC} = 4.45\text{ V to }5.25\text{ V}$; $V_{IO} = 2.55\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 40\text{ }\Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|--|---------------------------|-----|-------|---------------|
| Pins BP and BM | | | | | | |
| $t_{d(\text{TXD-bus})}$ | delay time from TXD to bus | Normal mode | [1][2] | | | |
| | | DATA_0 | - | - | 60 | ns |
| | | DATA_1 | - | - | 60 | ns |
| $\Delta t_{d(\text{TXD-bus})}$ | delay time difference from TXD to bus | Normal mode; between DATA_0 and DATA_1; Normal mode | [1][2] -4 | - | +4 | ns |
| $t_{d(\text{bus-RXD})}$ | delay time from bus to RXD | Normal mode; $C_{\text{RXD}} = 25\text{ pF}$; $V_{\text{cm}} = 2.5\text{ V}$ | [3][4] | | | |
| | | DATA_0 | - | - | 75 | ns |
| | | DATA_1 | - | - | 75 | ns |
| $\Delta t_{d(\text{bus-RXD})}$ | delay time difference from bus to RXD | between DATA_0 and DATA_1; Normal mode; $C_{\text{RXD}} = 25\text{ pF}$; $V_{\text{cm}} = 2.5\text{ V}$ | [3][4] -5 | - | 5 | ns |
| $t_{d(\text{TXEN-busidle})}$ | delay time from TXEN to bus idle | Normal mode; $V_{\text{TXD}} = 0\text{ V}$ | [5] | - | - | 75 ns |
| $t_{d(\text{TXEN-busact})}$ | delay time from TXEN to bus active | Normal mode; $V_{\text{TXD}} = 0\text{ V}$ | [5] | - | - | 75 ns |
| $ \Delta t_{d(\text{TXEN-bus})} $ | delay time difference from TXEN to bus (absolute value) | Normal mode; between TXEN to bus active and TXEN to bus idle; $V_{\text{TXD}} = 0\text{ V}$ | [6][5] | | 50 | ns |
| $t_{d(\text{BGE-busidle})}$ | delay time from BGE to bus idle | Normal mode; $V_{\text{TXD}} = 0\text{ V}$ | [5] | - | - | 75 ns |
| $t_{d(\text{BGE-busact})}$ | delay time from BGE to bus active | Normal mode; $V_{\text{TXD}} = 0\text{ V}$ | [5] | - | - | 75 ns |
| $t_{r(\text{dif})(\text{bus})}$ | bus differential rise time | DATA_0 to DATA_1; 20 % to 80 % | [5] 6 | - | 18.75 | ns |
| $t_{f(\text{dif})(\text{bus})}$ | bus differential fall time | DATA_1 to DATA_0; 80 % to 20 % | [5] 6 | - | 18.75 | ns |
| $\Delta t_{(r-f)(\text{dif})}$ | difference between differential rise and fall time | on bus; 80 % to 20 % | [5] -3 | - | 3 | ns |
| $t_{f(\text{bus})(\text{idle-act})}$ | bus fall time from idle to active | bus idle to DATA_0; $-30\text{ mV} > V_{\text{dif}} > -300\text{ mV}$ | [5][7] | - | 30 | ns |
| $t_{f(\text{bus})(\text{act-idle})}$ | bus fall time from active to idle | DATA_1 to bus idle; $300\text{ mV} > V_{\text{dif}} > 30\text{ mV}$ | [5][7] | - | 30 | ns |
| $t_{r(\text{bus})(\text{act-idle})}$ | bus rise time from active to idle | DATA_0 to bus idle; $-300\text{ mV} < V_{\text{dif}} < -30\text{ mV}$ | [5][7] | - | 30 | ns |
| Wake-up detection | | | | | | |
| $t_{\text{det}(\text{wake})\text{DATA}_0}$ | DATA_0 wake-up detection time | Standby mode with no undervoltage on pin V_{CC} ; $-10\text{ V} \leq V_{\text{cm}} \leq +15\text{ V}$ | [3][8] 1 | - | 4 | μs |
| $t_{\text{det}(\text{wake})\text{idle}}$ | idle wake-up detection time | Standby mode with no undervoltage on pin V_{CC} ; $-10\text{ V} \leq V_{\text{cm}} \leq +15\text{ V}$ | [3][8] 1 | - | 4 | μs |

Table 12. Dynamic characteristics ...continued

All parameters are guaranteed for $V_{CC} = 4.45\text{ V to }5.25\text{ V}$; $V_{IO} = 2.55\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 40\ \Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|---|------------|-----|------|---------------|
| $t_{det(wake)tot}$ | total wake-up detection time | Standby mode with no undervoltage on pin V_{CC} ; $-10\text{ V} \leq V_{cm} \leq +15\text{ V}$ | [3][8] 50 | - | 115 | μs |
| $t_{sup(int)wake}$ | wake-up interruption suppression time | Standby mode with no undervoltage on pin V_{CC} ; $-10\text{ V} \leq V_{cm} \leq +15\text{ V}$ | [3][9] 130 | - | 1000 | ns |
| $t_{d(wake-ERRN)}$ | delay time from wake-up to ERRN | Standby mode | - | - | 100 | μs |
| $t_{d(wake-RXD)}$ | delay time from wake-up to RXD | Standby mode | - | - | 100 | μs |
| Undervoltage | | | | | | |
| $t_{det(uv)(VCC)}$ | undervoltage detection time on pin V_{CC} | $0\text{ V} \leq V_{IO} \leq 5.5\text{ V}$; $V_{CC} = 4.35\text{ V}$ | 2 | - | 100 | μs |
| $t_{rec(uv)(VCC)}$ | undervoltage recovery time on pin V_{CC} | $0\text{ V} \leq V_{IO} \leq 5.5\text{ V}$; $V_{CC} = 4.85\text{ V}$ | 2 | - | 100 | μs |
| $t_{det(uv)(VIO)}$ | undervoltage detection time on pin V_{IO} | $V_{th(det)POR} < V_{CC} < 5.5\text{ V}$; $V_{IO} = 2.45\text{ V}$ | 5 | - | 100 | μs |
| $t_{rec(uv)(VIO)}$ | undervoltage recovery time on pin V_{IO} | $V_{th(det)POR} < V_{CC} < 5.5\text{ V}$; $V_{IO} = 2.9\text{ V}$ | 5 | - | 100 | μs |
| Activity detection | | | | | | |
| $t_{det(act)(bus)}$ | activity detection time on bus pins | Normal mode; $V_{cm} = 2.5\text{ V}$; $V_{dif}: 0\text{ mV} \rightarrow 400\text{ mV}$ | [3][7] 100 | - | 250 | ns |
| $t_{det(idle)(bus)}$ | idle detection time on bus pins | Normal mode; $V_{cm} = 2.5\text{ V}$; $V_{dif}: 400\text{ mV} \rightarrow 0\text{ mV}$ | [3][7] 50 | - | 200 | ns |
| $ \Delta t_{det(act-idle)} $ | active to idle detection time difference (absolute value) | Normal mode; on bus pins; $V_{cm} = 2.5\text{ V}$ | [3] | - | 150 | ns |
| ERRN signaling | | | | | | |
| $t_{det(L)(SCLK)}$ | LOW-level detection time on pin SCLK | Normal or Standby mode with no undervoltage on pin V_{IO} | 95 | - | 310 | μs |
| $t_{ERRNL(min)}$ | minimum ERRN LOW time | simple error indication mode; Normal or Standby mode | 2 | - | 10 | μs |
| $t_{d(errdet-ERRNL)}$ | delay time from error detection to ERRN LOW | all modes | - | - | 100 | μs |
| SPI | | | | | | |
| $t_{d(SCSNHL-SDOL)}$ | SCSN falling edge to SDO LOW-level delay time | $V_{uvd(VIO)} < V_{IO} < 5.5\text{ V}$; $4.45\text{ V} < V_{CC} < 5.5\text{ V}$; $C_{SDO} = 50\text{ pF}$ | [10] | - | 250 | ns |
| $t_{d(SCLKLH-SDODV)}$ | SCLK rising edge to SDO data valid delay time | $V_{uvd(VIO)} < V_{IO} < 5.5\text{ V}$; $4.45\text{ V} < V_{CC} < 5.5\text{ V}$; $C_{SDO} = 50\text{ pF}$ | [10] | - | 200 | ns |
| $t_{d(SCSNLH-SDOZ)}$ | SCSN rising edge to SDO three-state delay time | $V_{uvd(VIO)} < V_{IO} < 5.5\text{ V}$; $4.45\text{ V} < V_{CC} < 5.5\text{ V}$; $C_{SDO} = 50\text{ pF}$ | [10] | - | 500 | ns |
| T_{SCLK} | SCLK period | $V_{uvd(VIO)} < V_{IO} < 5.5\text{ V}$; $4.45\text{ V} < V_{CC} < 5.5\text{ V}$; $C_{SDO} = 50\text{ pF}$ | [10] 0.5 | - | 100 | μs |

Table 12. Dynamic characteristics ...continued

All parameters are guaranteed for $V_{CC} = 4.45\text{ V to }5.25\text{ V}$; $V_{IO} = 2.55\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 40\ \Omega$ and $C_{bus} = 100\text{ pF}$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---------------------------------------|---|--------------|-----|------|---------------|
| $t_{SPILEAD}$ | SPI enable lead time | $V_{uvd(VIO)} < V_{IO} < 5.5\text{ V}$; $4.45\text{ V} < V_{CC} < 5.5\text{ V}$; $C_{SDO} = 50\text{ pF}$ | [10] 250 | - | - | ns |
| t_{SPILAG} | SPI enable lag time | $V_{uvd(VIO)} < V_{IO} < 5.5\text{ V}$; $4.45\text{ V} < V_{CC} < 5.5\text{ V}$; $C_{SDO} = 50\text{ pF}$ | [10] 250 | - | - | ns |
| RXD | | | | | | |
| t_r | rise time | 20 % to 80 %; $C_{RXD} = 15\text{ pF}$ | [6] | - | - | 9 ns |
| | | 20 % to 80 %; $C_{RXD} = 25\text{ pF}$ | [6] | - | - | 10.75 ns |
| t_f | fall time | 80 % to 20 %; $C_{RXD} = 15\text{ pF}$ | [6] | - | - | 9 ns |
| | | 80 % to 20 %; $C_{RXD} = 25\text{ pF}$ | [6] | - | - | 10.75 ns |
| $\Delta t_{(r-f)}$ | difference between rise and fall time | $C_{RXD} = 15\text{ pF}$ | [6] | - | - | 5 ns |
| | | $C_{RXD} = 25\text{ pF}$ | [6] | - | - | 5 ns |
| | | $C_{RXD} = 10\text{ pF}$; simulated | [6][11] ↓ | - | - | 5 ns |
| $t_{(r+f)}$ | sum of rise and fall time | $C_{RXD} = 15\text{ pF}$ | [6] | - | - | 13 ns |
| | | $C_{RXD} = 25\text{ pF}$ | [6] | - | - | 16.5 ns |
| | | $C_{RXD} = 10\text{ pF}$; simulated | [6][11] ↓ | - | - | 16.5 ns |
| Bus error flag | | | | | | |
| $t_{d(norm-stb)}$ | normal mode to standby delay time | bus error flag set | 3 | - | 10 | μs |
| $t_{d(stb-norm)}$ | standby to normal mode delay time | bus error flag set | 3 | - | 10 | μs |
| Miscellaneous | | | | | | |
| $t_{detCL(TXEN)}$ | TXEN clamp detection time | | 650 | - | 2600 | μs |
| $t_{detCL(BGE)}$ | BGE clamp detection time | | 650 | - | 2600 | μs |
| $t_{d(TXENH-RXDH)}$ | delay time from TXEN HIGH to RXD HIGH | idle loop delay; Normal mode; $TXD = \text{LOW}$; $V_{cm} = 2.5\text{ V}$; $C_{RXD} = 25\text{ pF}$ | [3] | - | 300 | ns |

[1] Sum of TXD rise and fall times (20 % to 80 %); $t_{r(TXD)} + t_{f(TXD)} = \text{max. } 9\text{ ns}$.

[2] See [Figure 13](#).

[3] V_{cm} is the BP/BM common mode voltage.

[4] See [Figure 14](#).

[5] See [Figure 13](#).

[6] Guaranteed by design.

[7] $V_{dif} = V_{BP} - V_{BM}$.

[8] See [Figure 8](#).

[9] See [Figure 9](#).

[10] See [Figure 11](#).

[11] Load at end of 50 Ω microstrip with a propagation delay of 1 ns; 20 % to 80 % and 80 % to 20 %.

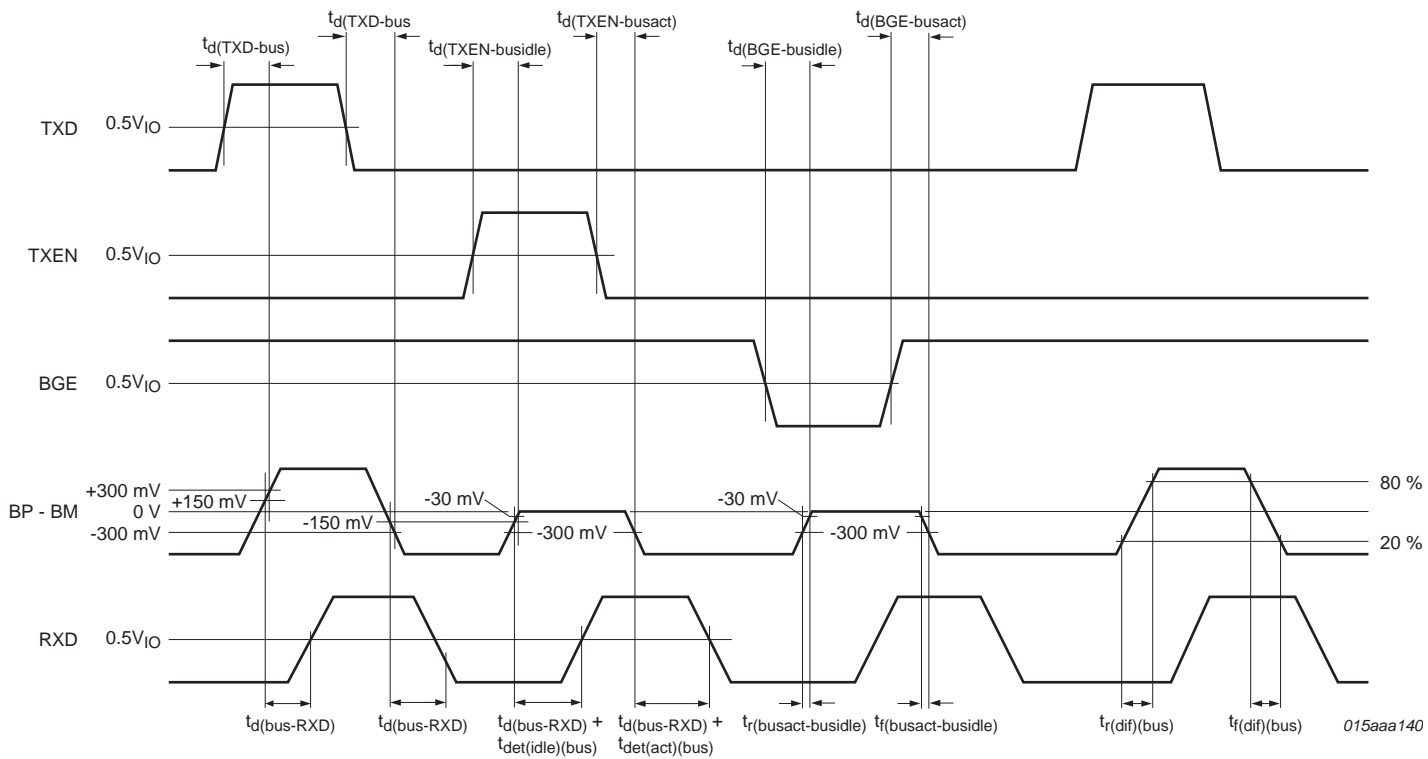
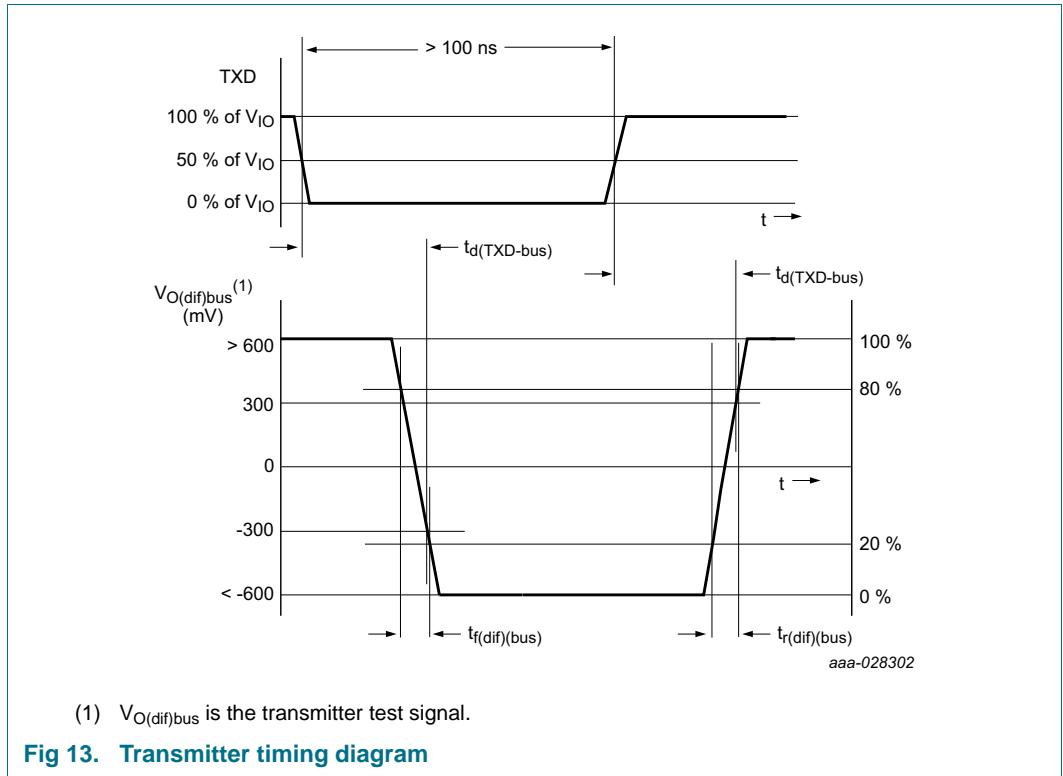
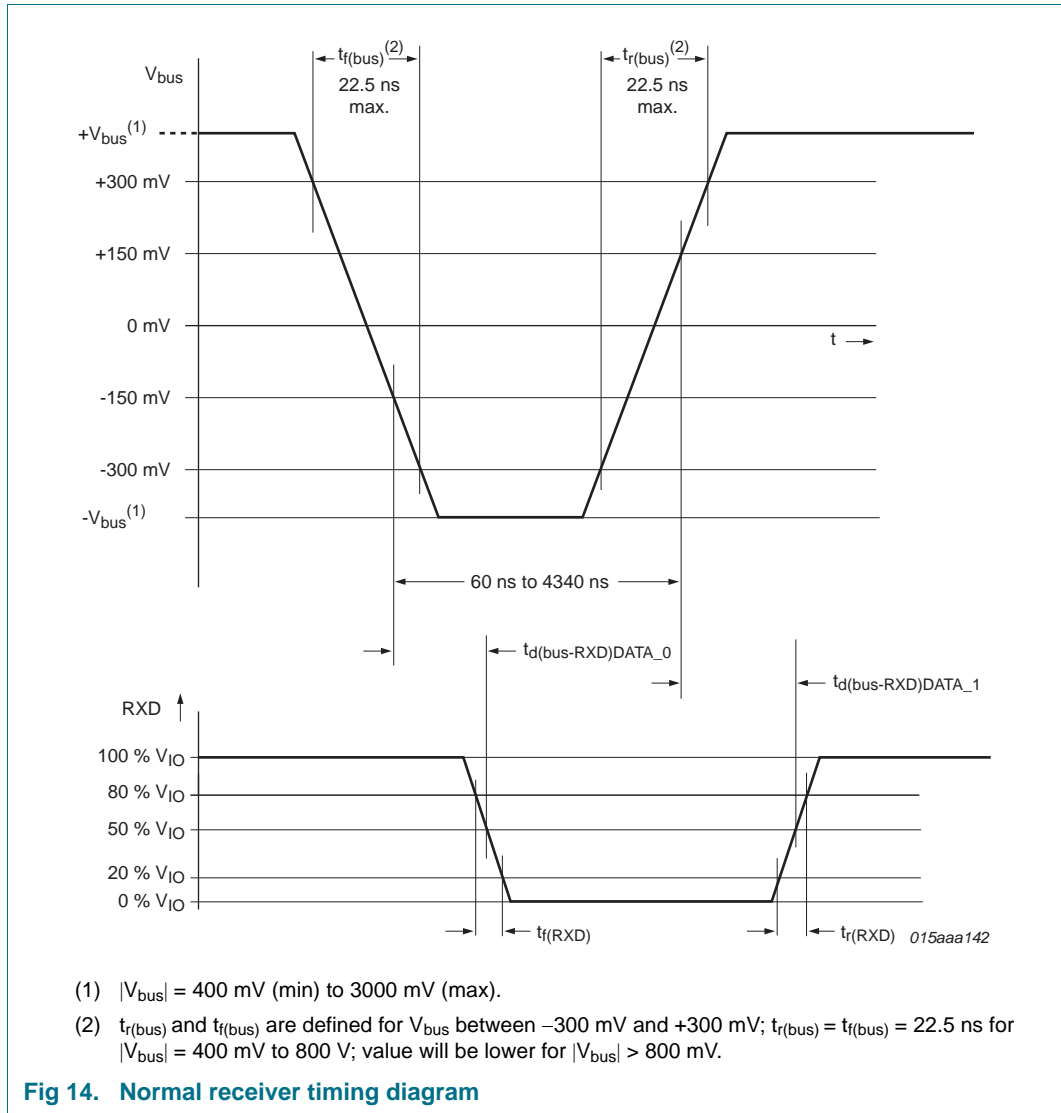


Fig 12. Detailed timing diagram





11. Application information

Further information on the application of the TJA1083G can be found in NXP application hints AH1101 TJA1083/TJA1083G FlexRay node transceiver ([Ref. 4](#)).

12. Test information

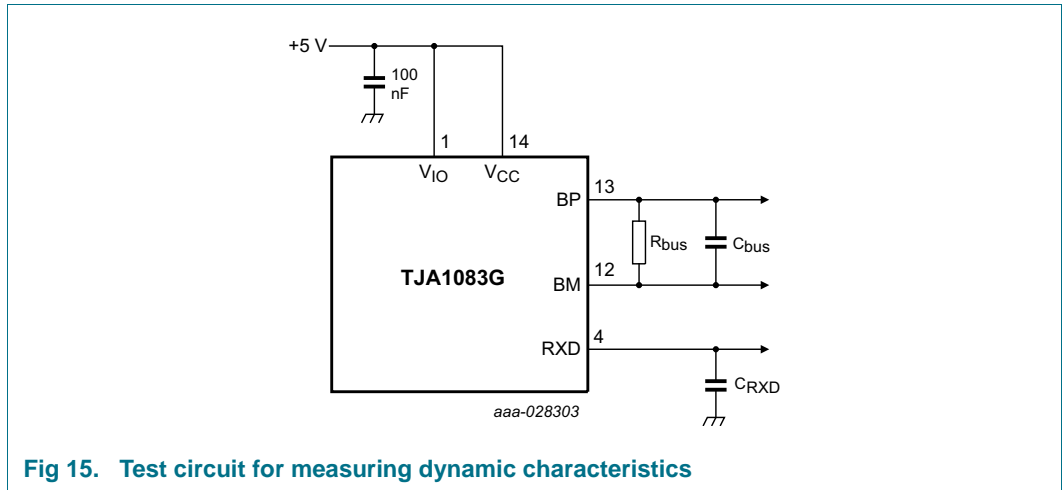
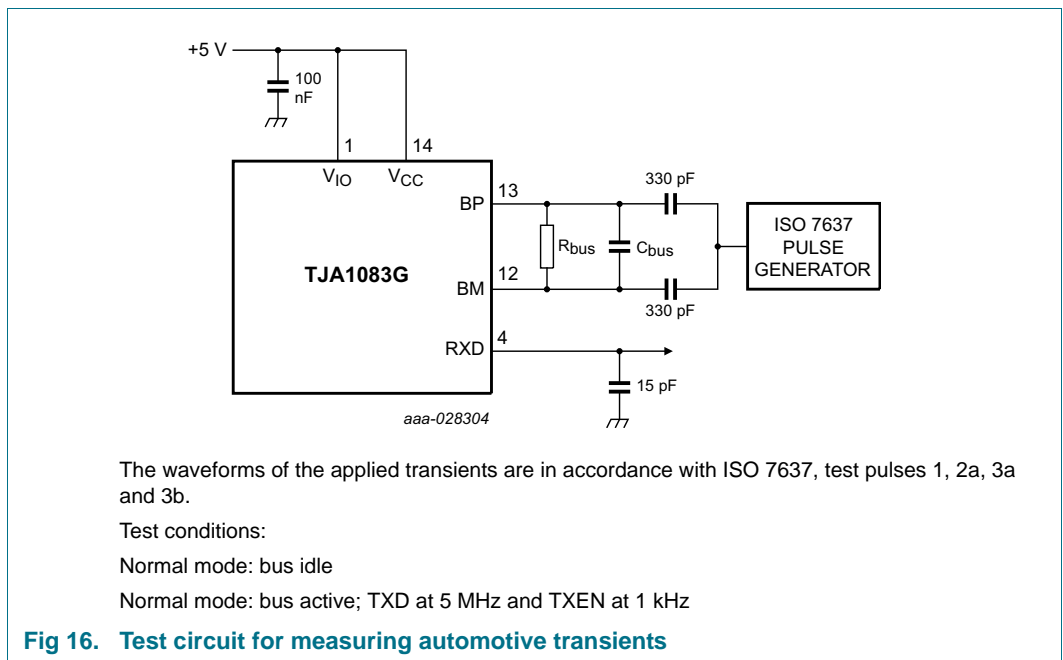


Fig 15. Test circuit for measuring dynamic characteristics



The waveforms of the applied transients are in accordance with ISO 7637, test pulses 1, 2a, 3a and 3b.

Test conditions:

Normal mode: bus idle

Normal mode: bus active; TXD at 5 MHz and TXEN at 1 kHz

Fig 16. Test circuit for measuring automotive transients

13. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

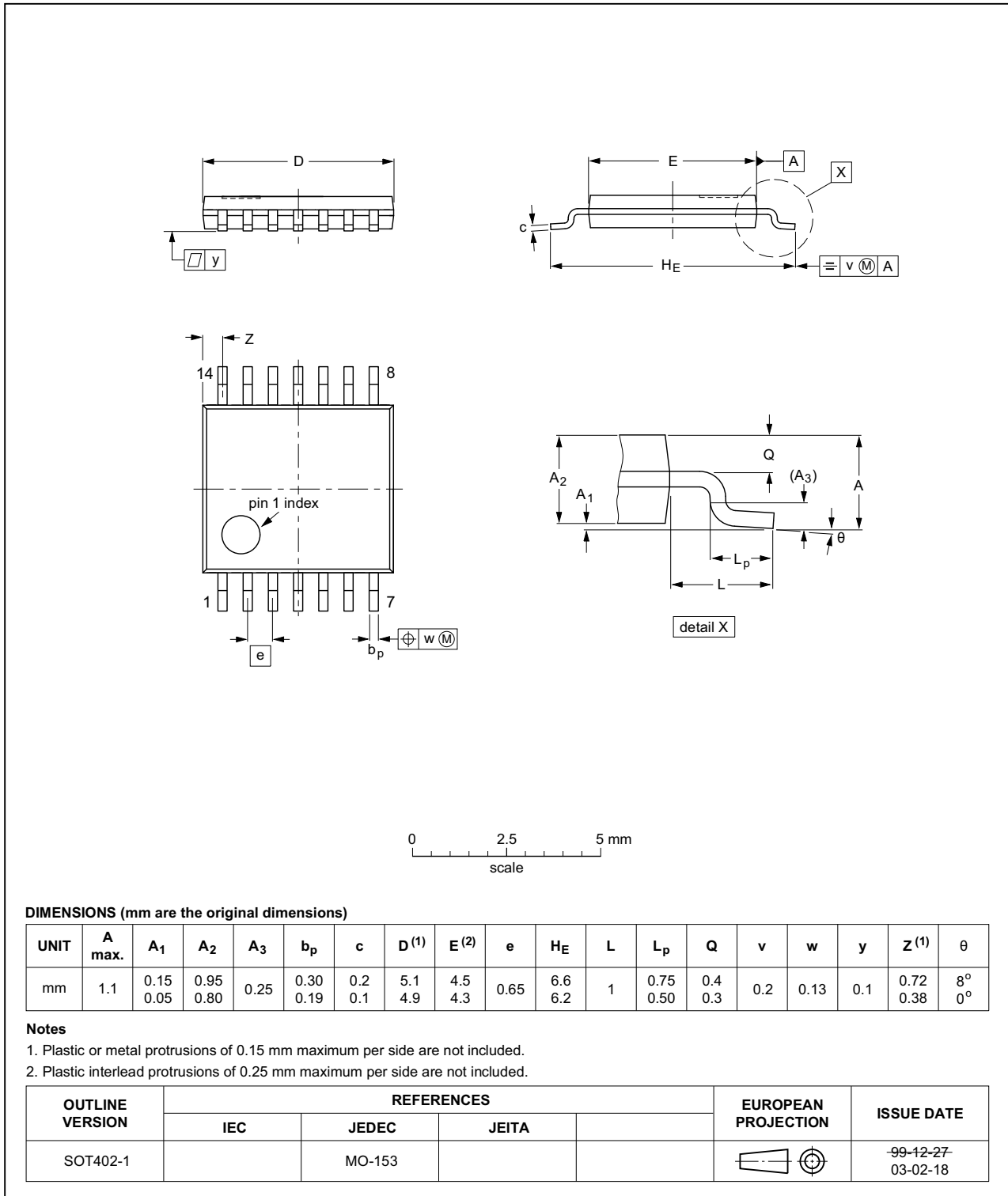


Fig 17. Package outline SOT402-1 (TSSOP14)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 18](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 13](#) and [14](#)

Table 13. SnPb eutectic process (from J-STD-020D)

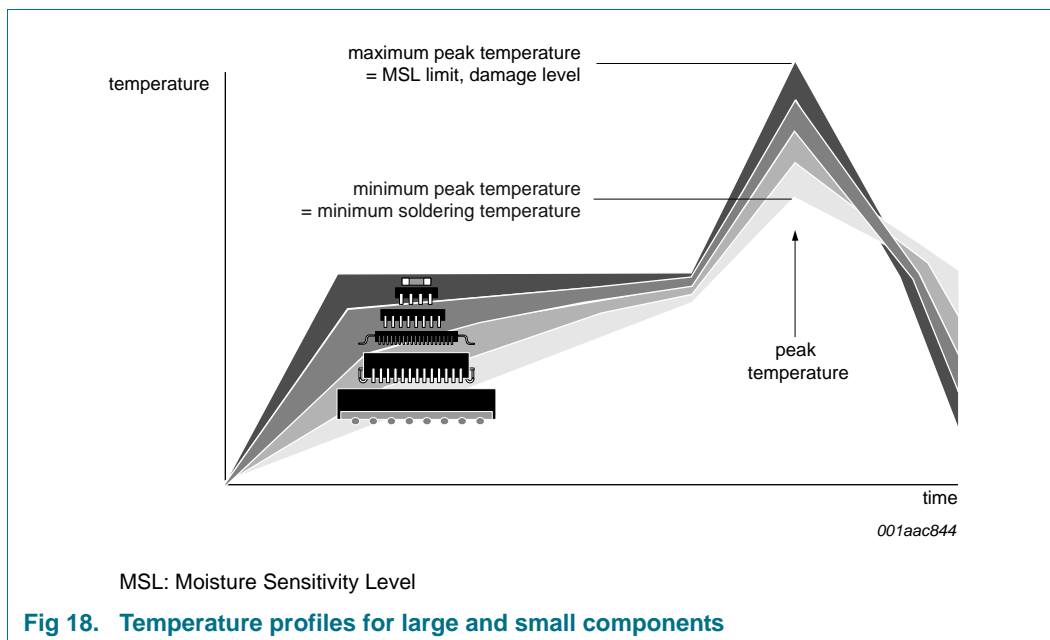
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 14. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 18](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

15. Appendix

15.1 Differences between TJA1083 and TJA1083G

The main differences between the TJA1083 and the TJA1083G are:

- The TJA1083 is JASPAR compliant (minimum transmitter output voltage of 900 mV) whereas the TJA1083G is not (minimum transmitter output voltage of 600 mV).
- The TJA1083G has improved EMC behavior.

15.2 Implementation of EPL 3.0.1 requirements in the TJA1083G

Table 15. EPL 3.0.1 implementation in TJA1083G

| EPL 3.0.1 | Min | Max | Unit | TJA1083G | | | |
|-------------------------------------|------|-------|------|---|-----------------------|---------------------|------|
| | | | | Symbol | Min | Max | Unit |
| dBDRxAsym | - | 5 | ns | $ \Delta t_{d(\text{bus-RXD})} $ | 0 | 5 | ns |
| dBDRx10 | - | 75 | ns | $t_{d(\text{bus-RXD})}$ | - | 75 | ns |
| dBDRx01 | - | 75 | ns | $t_{d(\text{bus-RXD})}$ | - | 75 | ns |
| dBDRxai | 50 | 275 | ns | $t_{\text{det}(\text{idle})(\text{bus})} + t_{d(\text{bus-RXD})}$ | 100 | 275 | ns |
| dBDRxia | 100 | 325 | ns | $t_{\text{det}(\text{act})(\text{bus})} + t_{d(\text{bus-RXD})}$ | 100 | 325 | ns |
| dBDTxAsym | - | 4 | ns | $ \Delta t_{d(\text{TXD-bus})} $ | 0 | 4 | ns |
| dBDTx10 | - | 75 | ns | $t_{d(\text{TXD-bus})}$ | - | 60 | ns |
| dBDTx01 | - | 75 | ns | $t_{d(\text{TXD-bus})}$ | - | 60 | ns |
| dBDTxai | - | 75 | ns | $t_{d(\text{TXEN-busidle})}$ | - | 75 | ns |
| dBDTxia | - | 75 | ns | $t_{d(\text{TXEN-busact})}$ | - | 75 | ns |
| dBusTxai | - | 30 | ns | $t_{r(\text{bus})(\text{act-idle})}$ | - | 30 | ns |
| dBusTxia | - | 30 | ns | $t_{f(\text{bus})(\text{idle-act})}$ | - | 30 | ns |
| dBusTx01 | 6 | 18.75 | ns | $t_{r(\text{dif})(\text{bus})}$ | 6 | 18.75 | ns |
| dBusTx10 | 6 | 18.75 | ns | $t_{f(\text{dif})(\text{bus})}$ | 6 | 18.75 | ns |
| uBDTx _{active} | 600 | 2000 | mV | $V_{\text{OH}(\text{dif})}$ | 600 | 2000 | mV |
| uBDTx _{idle} | 0 | 30 | mV | $ V_{\text{O}(\text{idle})(\text{dif})} $ | 0 | 25 | mV |
| uVDIG-OUT-HIGH | 80 | 100 | % | $V_{\text{OH}(\text{RXD})}$ | $V_{\text{IO}} - 0.4$ | V_{IO} | V |
| | | | | $V_{\text{OH}(\text{ERRN})}$ | $V_{\text{IO}} - 0.4$ | V_{IO} | V |
| uVDIG-OUT-LOW | - | 20 | % | $V_{\text{OL}(\text{RXD})}$ | - | 0.4 | V |
| | | | | $V_{\text{OL}(\text{ERRN})}$ | - | 0.4 | V |
| uVDIG-IN-HIGH | - | 70 | % | $V_{\text{IH}(\text{TXEN})}$ | $0.7V_{\text{IO}}$ | 5.5 | V |
| | | | | $V_{\text{IH}(\text{STBN})}$ | $0.7V_{\text{IO}}$ | 5.5 | V |
| | | | | $V_{\text{IH}(\text{BGE})}$ | $0.7V_{\text{IO}}$ | 5.5 | V |
| uVDIG-IN-LOW | 30 | - | % | $V_{\text{IL}(\text{TXEN})}$ | -0.3 | $+0.3V_{\text{IO}}$ | V |
| | | | | $V_{\text{IL}(\text{STBN})}$ | -0.3 | $+0.3V_{\text{IO}}$ | V |
| | | | | $V_{\text{IL}(\text{BGE})}$ | -0.3 | $+0.3V_{\text{IO}}$ | V |
| uData0 | -300 | -150 | mV | $V_{\text{IL}(\text{dif})}$ | -300 | -150 | mV |
| uData1 | 150 | 300 | mV | $V_{\text{IH}(\text{dif})}$ | 150 | 300 | mV |
| uData1- uData0 | -30 | 30 | mV | $ \Delta V_{i(\text{dif})(\text{H-L})} $ | - | 30 | mV |
| dBDActivityDetection | 100 | 250 | ns | $t_{\text{det}(\text{act})(\text{bus})}$ | 100 | 250 | ns |
| dBDDIdleDetection | 50 | 200 | ns | $t_{\text{det}(\text{idle})(\text{bus})}$ | 100 | 200 | ns |
| R _{CM1} , R _{CM2} | 10 | 40 | kΩ | $R_{i(\text{BP})}$, $R_{i(\text{BM})}$ | 10 | 40 | kΩ |
| uCM | -10 | 15 | V | V_{cm} ^[1] | -10 | +15 | V |
| iBM _{GNDShortMax} | - | 60 | mA | $ I_{\text{O}(\text{sc})(\text{BM})} $ | - | 60 | mA |
| iBP _{GNDShortMax} | - | 60 | mA | $ I_{\text{O}(\text{sc})(\text{BP})} $ | - | 60 | mA |
| iBM _{BAT48ShortMax} | - | 72 | mA | $ I_{\text{O}(\text{sc})(\text{BM})} $ | - | 60 | mA |
| iBP _{BAT48ShortMax} | - | 72 | mA | $ I_{\text{O}(\text{sc})(\text{BP})} $ | - | 60 | mA |
| iBM _{BAT27ShortMax} | - | 60 | mA | $ I_{\text{O}(\text{sc})(\text{BM})} $ | - | 60 | mA |

Table 15. EPL 3.0.1 implementation in TJA1083G

| EPL 3.0.1 | | | | TJA1083G | | | |
|--|------|------|------|---|--------------------|--------------------|------|
| | Min | Max | Unit | Symbol | Min | Max | Unit |
| iBP _{BAT27ShortMax} | - | 60 | mA | I _{O(sc)} (BP) | - | 60 | mA |
| uBias, non low-power modes | 1800 | 3200 | mV | V _{O(idle)} (BP), V _{O(idle)} (BM) ^[2] | 1800 | 3150 | mV |
| uBias, low-power modes | -200 | 200 | mV | V _{O(idle)} (BP), V _{O(idle)} (BM) ^[3] | -0.1 | +0.1 | V |
| dWU _{0Detect} | 1 | 4 | μs | t _{det(wake)DATA_0} | 1 | 4 | μs |
| dWU _{IdleDetect} | 1 | 4 | μs | t _{det(wake)idle} | 1 | 4 | μs |
| dWU _{Timeout} | 48 | 140 | μs | t _{det(wake)tot} | 50 | 115 | μs |
| uBDUVV _{CC} | 4 | - | V | V _{uvd} (VCC) | 4.45 | 4.729 | V |
| dBDUVV _{CC} | - | 1000 | ms | t _{det(uv)} (VCC) | 2 | 100 | μs |
| iBP _{Leak} | - | 25 | μA | I _{LI} (BP) | -5 | +5 | μA |
| iBM _{Leak} | - | 25 | μA | I _{LI} (BM) | -5 | +5 | μA |
| Functional class 'bus driver logic level adaptation' | | | | implemented; see Section 2.4 | | | |
| Functional class 'bus driver - bus guardian interface' | | | | implemented; see Section 2.4 | | | |
| Device qualification according to AEC-Q100 (Rev. F) | | | | see Section 2.1 | | | |
| T _{AMB_Class1} | -40 | 125 | °C | T _{amb} | -40 | +125 | °C |
| dBDTxDM | -50 | 50 | ns | Δt _d (TXEN-bus) | -50 | 50 | ns |
| iBM _{-5VshortMax} | - | 60 | mA | I _{O(sc)} (BM) | - | 60 | mA |
| iBP _{-5VshortMax} | - | 60 | mA | I _{O(sc)} (BP) | - | 60 | mA |
| iBM _{BPSshortMax} | - | 60 | mA | I _{O(sc)} (BM) | - | 60 | mA |
| iBP _{BMSshortMax} | - | 60 | mA | I _{O(sc)} (BP) | - | 60 | mA |
| iBM _{BAT60ShortMax} | - | 90 | mA | I _{O(sc)} (BM) | - | 60 | mA |
| iBP _{BAT60ShortMax} | - | 90 | mA | I _{O(sc)} (BP) | - | 60 | mA |
| uUV _{IO} | 2 | - | V | V _{uvd} (VIO) | 2.55 | 2.774 | V |
| dBDUVV _{IO} | - | 1000 | ms | t _{det(uv)} (VIO) | 5 | 100 | μs |
| dBDWakeupReaction _{remote} | - | 100 | μs | t _d (wake-ERRN), t _d (wake-RXD) | - | 100 | μs |
| dBDTxActiveMax | 650 | 2600 | μs | t _{detCL} (TXEN) | 650 | 2600 | μs |
| dBDModeChange | 100 | 100 | μs | t _d (norm-stb), t _d (stb-norm) | 3 | 10 | μs |
| dBDERRN _{Stable} | 1 | 10 | μs | t _{ERRN} (min) | 2 | 10 | μs |
| dReactionTime _{ERRN} | - | 100 | μs | t _d (errdet-ERRNL) | - | 100 | μs |
| uData0_LP | -400 | -100 | mV | V _{IL} (dif) | -400 | -100 | mV |
| dWU _{Interrupt} | 0.13 | 1 | μs | t _{sup} (int)wake | 130 | 1000 | ns |
| uBDLogic_1 | - | 60 | % | V _{IH} (TXD) | 0.6V _{IO} | 5.5 | V |
| uBDLogic_0 | 40 | - | % | V _{IL} (TXD) | -0.3 | 0.4V _{IO} | V |
| dBDRV _{CC} | - | 10 | ms | t _{rec} (uv)(VCC) | 2 | 100 | μs |
| dBDRV _{IO} | - | 10 | ms | t _{rec} (uv)(VIO) | 5 | 100 | μs |
| iBP _{LeakGND} | - | 1600 | μA | I _{LI} (BP) | -1600 | 1600 | μA |
| iBM _{LeakGND} | - | 1600 | μA | I _{LI} (BM) | -1600 | 1600 | μA |
| Functional class 'bus driver remote wakeup' | | | | implemented; see Section 2.4 | | | |

Table 15. EPL 3.0.1 implementation in TJA1083G

| EPL 3.0.1 | | | | TJA1083G | | | |
|---|------------------|------|------|--|-----------------------|-----------------|----------|
| | Min | Max | Unit | Symbol | Min | Max | Unit |
| $\mu\text{ESD}_{\text{Ext}}$ | 6 | - | kV | $ V_{\text{ESD}} $: HBM on pins BP and BM to GND | - | 8 | kV |
| $\mu\text{ESD}_{\text{Int}}$ | 2 | - | kV | $ V_{\text{ESD}} $: HBM on any other pin | - | 4 | kV |
| $\mu\text{ESD}_{\text{IEC}}$ | 6 | - | kV | $ V_{\text{ESD}} $: IEC61000-4-2 on pins BP and BM to GND | - | 8 | kV |
| $\text{dBDRxD}_{\text{R15}} + \text{dBDRxD}_{\text{F15}}$ | - | 13 | ns | $\sum t_{(r+f)}$ (pin RXD; 15 pF load) | - | 13 | ns |
| $ \text{dBDRxD}_{\text{R15}} - \text{dBDRxD}_{\text{F15}} $ | - | 5 | ns | $ \Delta t_{(r-f)} $ (pin RXD; 15 pF load) | - | 5 | ns |
| C_{BDTXD} | - | 10 | pF | $C_{i(\text{TXD})}$ | - | 10 | pF |
| dBDTxRxai | - | 325 | ns | $t_{\text{d}(\text{TXENH-RXDH})}$ | - | 300 | ns |
| $\mu\text{VDIG-OUT-UV}$ | - | 500 | mV | $V_{\text{O}(\text{UVVIO})\text{RXD}}$ | - | 500 | mV |
| | | | | $V_{\text{O}(\text{UVVIO})\text{ERRN}}$ | - | 500 | mV |
| | | | | $V_{\text{O}(\text{UVVIO})\text{SDO}}$ | - | 500 | mV |
| $\mu\text{VDIG-OUT-OFF}$ | product specific | | | $V_{\text{OL}(\text{RXD})}$ ^[4] | $V_{\text{IO}} - 500$ | V_{IO} | mV |
| | | | | $V_{\text{OL}(\text{ERRN})}$ ^[4] | - | 500 | mV |
| | | | | $V_{\text{OL}(\text{SDO})}$ ^[4] | - | 500 | mV |
| $R_{\text{BDTransmitter}}$ | product specific | | | $Z_{\text{o}(\text{TX})(\text{eq})}$ | 35 | 100 | Ω |
| RxD signal sum of rise and fall time at TP4_CC | - | 16.5 | ns | $\sum t_{(r+f)}$ (pin RXD; 10 pF load; simulated) | - | 16.5 | ns |
| $\text{dBDRxD}_{\text{R25}} + \text{dBDRxD}_{\text{F25}}$ | - | 16.5 | ns | $\sum t_{(r+f)}$ (pin RXD; 25 pF load) | - | 16.5 | ns |
| $ \text{dBDRxD}_{\text{R25}} - \text{dBDRxD}_{\text{F25}} $ | - | 5 | ns | $ \Delta t_{(r-f)} $ (pin RXD; 25 pF load) | - | 5 | ns |
| dBusTxDif | - | 3 | ns | $ \Delta t_{(r-f)(\text{dif})} $ | - | 3 | ns |
| RxD signal difference of rise and fall time at TP4_CC | - | 5 | ns | $ \Delta t_{(r-f)} $ (pin RXD; 10 pF load; simulated) | - | 5 | ns |

- [1] V_{cm} is the BP/BM common mode voltage, $(V_{\text{BP}} + V_{\text{BM}}) / 2$, and is specified in conditions column of parameters $V_{\text{IH}(\text{dif})}$ and $V_{\text{IL}(\text{dif})}$ for pins BP and BM; see Table 11. V_{cm} is tested on a receiving bus driver with a transmitting bus driver that has a ground offset voltage in the range -12.5 V to $+12.5\text{ V}$ and transmits a 50/50 pattern.
- [2] Min. value: $V_{\text{o}(\text{idle})(\text{BP})} = V_{\text{o}(\text{idle})(\text{BM})} = 0.4V_{\text{CC}} = 0.4 \times 4.5\text{ V} = 1800\text{ mV}$; max value: $V_{\text{o}(\text{idle})(\text{BP})} = V_{\text{o}(\text{idle})(\text{BM})} = 0.6V_{\text{CC}} = 0.6 \times 5.25\text{ V} = 3150\text{ mV}$; the nominal voltage is 2500 mV.
- [3] The normal voltage is 0 mV.
- [4] Power-off mode.

16. Abbreviations

Table 16. Abbreviations

| Abbreviation | Description |
|--------------|---|
| CDM | Charged Device Model |
| ECU | Electronic Control Unit |
| EMC | ElectroMagnetic Compatibility |
| EME | ElectroMagnetic Emission |
| EMI | ElectroMagnetic Immunity |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| JASPAR | Japan Automotive Software Platform Architecture |
| MM | Machine Model |
| PWON | Power-on |

17. References

- [1] **EPL** — FlexRay Communications System Electrical Physical Layer Specification Version 3.0.1
- [2] **ISO 17458-4:2013** — Road vehicles - FlexRay communications system - Part 4: Electrical physical layer specification
- [3] **TJA1083** — FlexRay transceiver data sheet, www.nxp.com
- [4] **AH1101** — TJA1083/TJA1083G FlexRay node transceiver application hints, available from NXP Semiconductors

18. Revision history

Table 17. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------|--------------|--------------------|---------------|------------|
| TJA1083G v.1 | 20180118 | Product data sheet | - | - |

19. Legal information

19.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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