19-2130; Rev 2; 11/10

EVALUATION KIT AVAILABLE

10-Bit Bus LVDS Deserializers

General Description

The MAX9206/MAX9208 deserializers transform a high-speed serial bus low-voltage differential signaling (BLVDS) data stream into 10-bit-wide parallel LVCMOS/LVTTL data and clock. The deserializers pair with serializers such as the MAX9205/MAX9207, which generate a serial BLVDS signal from 10-bit-wide parallel data. The serializer/deserializer combination reduces interconnect, simplifies PCB layout, and reduces board size.

The MAX9206/MAX9208 receive serial data at 450Mbps and 600Mbps, respectively, over board traces or twisted-pair cables. These devices combine frequency lock, bit lock, and frame lock to produce a parallel-rate clock and word-aligned 10-bit data. Serialization eliminates parallel bus clock-to-data and data-to-data skew.

A power-down mode reduces typical supply current to less than 600µA. Upon power-up (applying power or driving $\overline{PWRDN}$ high), the MAX9206/MAX9208 establish lock after receiving synchronization signals or serial data from the MAX9205/MAX9207. An output enable allows the outputs to be disabled, putting the parallel data outputs and recovered output clock into a high-impedance state without losing lock.

The MAX9206/MAX9208 operate from a single +3.3V supply and are specified for operation from -40°C to +85°C. The MAX9206/MAX9208 are available in 28-pin SSOP packages.

Applications

Cellular Phone Base Stations

Add/Drop Muxes

Digital Cross-Connects

DSLAMs

Network Switches and Routers

Backplane Interconnect

Features

- **Stand-Alone Deserializer (vs. SerDes) Ideal for Unidirectional Links**
- **Automatic Clock Recovery**
- **Allow Hot Insertion and Synchronization Without System Interruption**
- **BLVDS Serial Input Rated for Point-to-Point and Bus Applications**
- **Fast Pseudorandom Lock**
- **Wide Reference Clock Input Range**
  - **16MHz to 45MHz (MAX9206)**
  - **40MHz to 60MHz (MAX9208)**
- **High 720ps (p-p) Jitter Tolerance (MAX9206)**
- **Low 30mA Supply Current (MAX9206 at 16MHz)**
- **10-Bit Parallel LVCMOS/LVTTL Output**
- **Up to 600Mbps Throughput (MAX9208)**
- **Programmable Output Strobe Edge**
- **Pin Compatible to DS92LV1212A and DS92LV1224**

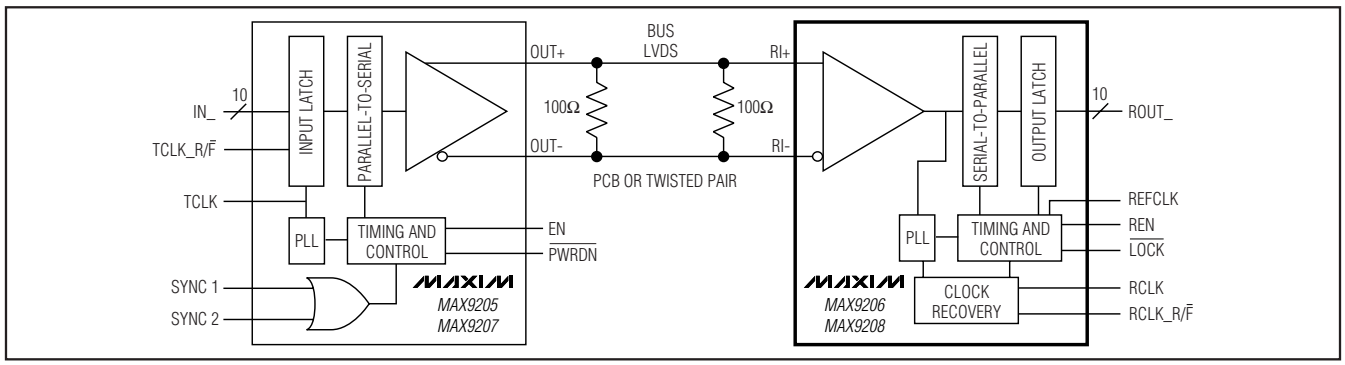
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	REF CLOCK RANGE (MHz)
MAX9206EAI+	-40°C to +85°C	28 SSOP	16 to 40
MAX9206EAI/V+	-40°C to +85°C	28 SSOP	16 to 40
MAX9208EAI+	-40°C to +85°C	28 SSOP	40 to 66

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

AVCC, DVCC to AGND, DGND .....-0.3V to +4V
RI+, RI- to AGND, DGND .....-0.3V to +4V
All Other Pins to DGND .....-0.3V to DV_{CC} + 0.3V
ROUT_ Short-Circuit Duration (Note 1) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.5mW/°C above +70°C) 762mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Rating (Human Body Model, RI+, RI-) .....±8kV
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{AVCC} = V_{DVCC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVCC} = V_{DVCC} = +3.3V, V_{CM} = 1.1V, $|V_{ID}|$ = 0.2V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER SUPPLY								
Supply Current	I_{CC}	C_L = 15pF, worst-case pattern, Figure 1	MAX9206	16MHz		30	45	mA
				45MHz		57	75	
			MAX9208	40MHz		55	75	
				60MHz		80	100	
Power-Down Supply Current	I_{CCX}	$\overline{PWRDWN}$ = low					1	mA
LVCMOS/LVTTL LOGIC INPUTS (REN, REFCLK, RCLK_R/$\overline{F}$, $\overline{PWRDN}$)								
High-Level Input Voltage	V_{IH}				2.0		V_{CC}	V
Low-Level Input Voltage	V_{IL}				0		0.8	V
Input Current	I_{IN}	V_{IN} = 0V, V_{AVCC}, or V_{DVCC}			-15		15	µA
LVCMOS/LVTTL LOGIC OUTPUTS (ROUT_, RCLK, $\overline{LOCK}$)								
High-Level Output Voltage	V_{OH}	I_{OH} = -5mA			2.2	2.9	V_{CC}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 5mA			0	0.33	0.5	V
Output Short-Circuit Current	I_{OS}	$V_{ROUT\_}$ = 0V			-15	-38	-85	mA
Output High-Impedance Current	I_{OZ}	$\overline{PWRDN}$ = low, $V_{ROUT\_}$ = V_{RCLK} = $V_{\overline{LOCK}}$ = 0V, V_{AVCC}, or V_{DVCC}			-1		1	µA
BLVDS SERIAL INPUT (RI+, RI-)								
Differential Input High	V_{TH}					9	100	mV
Differential Input Low Threshold	V_{TL}				-100	-9		mV
Input Current	I_{RI+}, I_{RI-}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.45V			-64		64	µA
		0.45V < $\|V_{ID}\|$ ≤ 0.6V			-82		82	
Power-Off Input Current	I_{RI+OFF}, I_{RI-OFF}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.45V, V_{AVCC} = V_{DVCC} = 0V			-64		64	µA
		0.45V < $\|V_{ID}\|$ ≤ 0.6V, V_{AVCC} = V_{DVCC} = 0V			-82		82	
Input Resistor 1	R_{IN1}	V_{AVCC} = V_{DVCC} = 3.6V or 0V, Figure 2			4			kΩ
Input Resistor 2	R_{IN2}	V_{AVCC} = V_{DVCC} = 3.6V or 0V, Figure 2			150			kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{AVCC} = V_{DVCC} = +3.0V to +3.6V, C_L = 15pF, differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVCC} = V_{DVCC} = +3.3V, V_{CM} = 1.1V, $|V_{ID}|$ = 0.2V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE CLOCK TIMING REQUIREMENTS (REFCLK)							
REFCLK Frequency	f_{RFF}	MAX9206		16		45	MHz
		MAX9208		40		60	
REFCLK Frequency Variation	RFFV			-200		200	ppm
REFCLK Period	t_{RFCP}	MAX9206		22.222		62.500	ns
		MAX9208		16.666		25	
REFCLK Duty Cycle	RFDC			30	50	70	%
REFCLK Input Transition Time	t_{RFTT}				3	6	ns
SWITCHING CHARACTERISTICS							
Recovered Clock (RCLK) Period (Note 6)	t_{RCP}	MAX9206		22.222		62.500	ns
		MAX9208		16.666		25	
Low-to-High Transition Time	t_{CLH}	Figure 3			1.5	3	ns
High-to-Low Transition Time	t_{CHL}	Figure 3			2	3	ns
Deserializer Delay	t_{DD}	Figure 4	MAX9206, 45MHz	1.75 x t_{RCP} + 2	1.75 x t_{RCP} + 3.3	1.75 x t_{RCP} + 6.5	ns
			MAX9208, 60MHz	1.75 x t_{RCP} + 1.1	1.75 x t_{RCP} + 3.3	1.75 x t_{RCP} + 5.6	
ROUT_ Data Valid Before RCLK	t_{ROS}	Figure 5		0.4 x t_{RCP}	0.5 x t_{RCP}		ns
ROUT_ Data Valid After RCLK	t_{ROH}	Figure 5		0.4 x t_{RCP}	0.5 x t_{RCP}		ns
RCLK Duty Cycle	t_{RDC}			43	50	57	%
OUTPUT High-to-High Impedance Delay	t_{HZR}	C_L = 5pF, Figure 6				8	ns
OUTPUT Low-to-High Impedance Delay	t_{LZR}	C_L = 5pF, Figure 6				8	ns
OUTPUT High-Impedance to High-State Delay	t_{ZHR}	C_L = 5pF, Figure 6				6	ns
OUTPUT High-Impedance to Low-State Delay	t_{ZLR}	C_L = 5pF, Figure 6				6	ns
PLL Lock Time (from $\overline{PWRDN}$ Transition High)	t_{DSR1}	Sync patterns at input; supply and REFCLK stable; measured from $\overline{PWRDN}$ transition high to $\overline{LOCK}$ transition low; Figure 7				(2048 + 42) x t_{RFCP}	ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVCC} = V_{DVCC} = +3.0V to +3.6V, C_L = 15pF, differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVCC} = V_{DVCC} = +3.3V, V_{CM} = 1.1V, $|V_{ID}|$ = 0.2V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
PLL Lock Time (from Start of Sync Patterns)	t_{DSR2}	PLL locked to stable REFCLK; supply stable; static input; measured from start of sync patterns at input to $\overline{LOCK}$ transition low; Figure 8					42 x t_{RFCP}	ns
$\overline{LOCK}$ High-Z to High-State Delay	t_{ZHLK}	Figure 7					30	ns
Input Jitter Tolerance	t_{JT}	Figure 9	MAX9206	16MHz	1300			ps
				45MHz	720			
			MAX9208	40MHz	720			
				60MHz	320			

Note 1: Short one output at a time. Do not exceed the Absolute Maximum continuous power dissipation.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. Voltages are referenced to ground except V_{TH}, V_{TL}, and V_{ID}, which are differential input voltages.

Note 3: DC parameters are production tested at T_A = +25°C and guaranteed by design and characterization over operating temperature range.

Note 4: AC parameters guaranteed by design and characterization.

Note 5: C_L includes scope probe and test jig capacitance.

Note 6: t_{RCP} is determined by the period of TCLK, which is the reference clock of the serializer driving the deserializer. The frequency of TCLK must be within ±400ppm of the REFCLK frequency.

Pin Description

PIN	NAME	FUNCTION
1, 12, 13	AGND	Analog Ground
2	RCLK_R/$\overline{F}$	Recovered Clock Strobe Edge Select. LVTTL/LVCMOS level input. Drive RCLK_ R/$\overline{F}$ high to strobe ROUT_ on the rising edge of RCLK. Drive RCLK_R/$\overline{F}$ low to strobe ROUT_ on the falling edge of RCLK.
3	REFCLK	PLL Reference Clock. LVTTL/LVCMOS level input.
4, 11	AVCC	Analog Power Supply. Bypass AVCC with a 0.1µF and a 0.001µF capacitor to AGND.
5	RI+	Serial Data Input. Noninverting BLVDS differential input.
6	RI-	Serial Data Input. Inverting BLVDS differential input.
7	$\overline{PWRDN}$	Power Down. LVTTL/LVCMOS level input. Drive $\overline{PWRDN}$ low to stop the PLL and put ROUT_, $\overline{LOCK}$, and RCLK in high impedance.
8	REN	Output Enable. LVTTL/LVCMOS level input. Drive REN low to put ROUT_ and RCLK in high impedance. $\overline{LOCK}$ remains active, indicating the status of the serial input.
9	RCLK	Recovered Clock. LVTTL/LVCMOS level output. Use RCLK to strobe ROUT_.
10	$\overline{LOCK}$	Lock Indicator. LVTTL/LVCMOS level output. $\overline{LOCK}$ goes low when the PLL has achieved frequency and phase lock to the serial input, and the framing bits have been identified.
14, 20, 22	DGND	Digital Ground
15–19, 24–28	ROUT9–ROUT0	Parallel Output Data. LVTTL/LVCMOS level outputs. ROUT_ is valid on the second selected strobe edge of RCLK after $\overline{LOCK}$ goes low.
21, 23	DVCC	Digital Power Supply. Bypass DVCC with a 0.1µF and a 0.001µF capacitor to DGND.

Test Circuits/Timing Diagrams

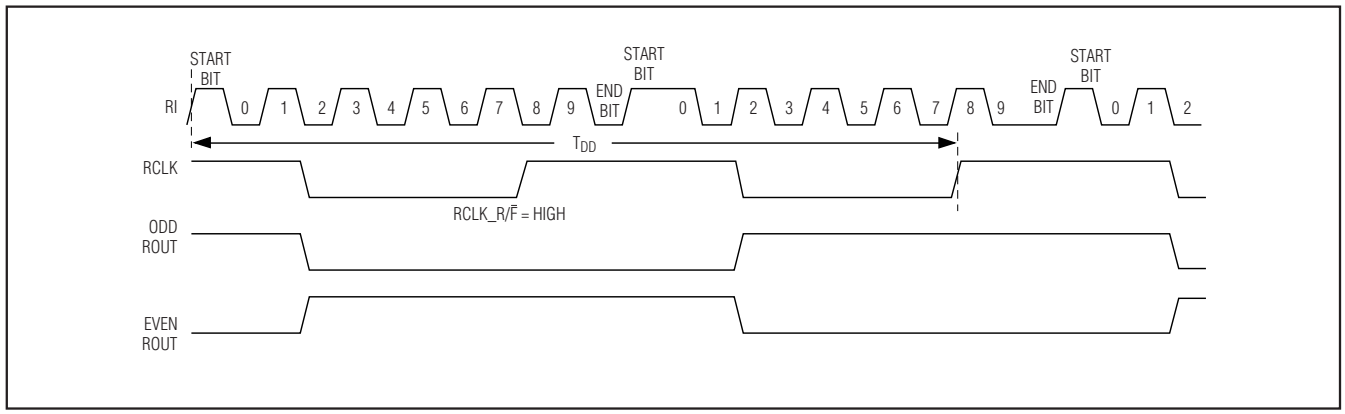


Figure 1. Worst-Case I_{CC} Test Pattern

Test Circuits/Timing Diagrams (continued)

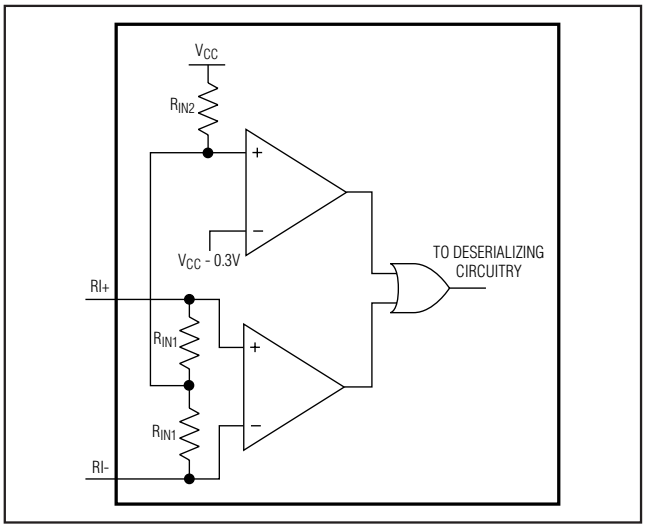


Figure 2. Input Fail-Safe Circuit

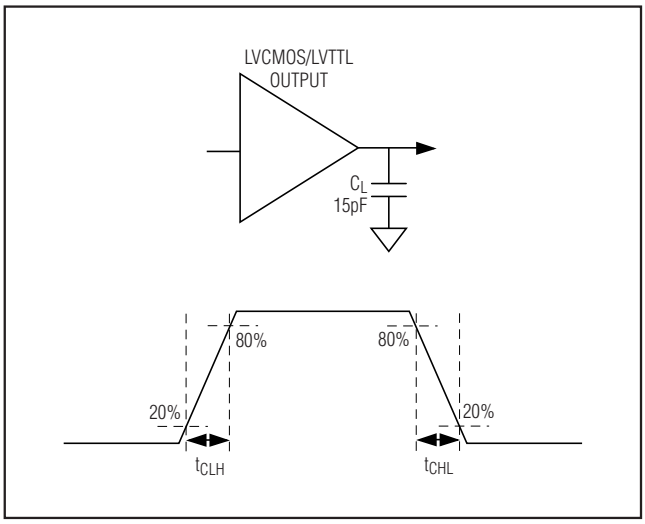


Figure 3. LVCMOS/LVTTL Output Load and Transition Times

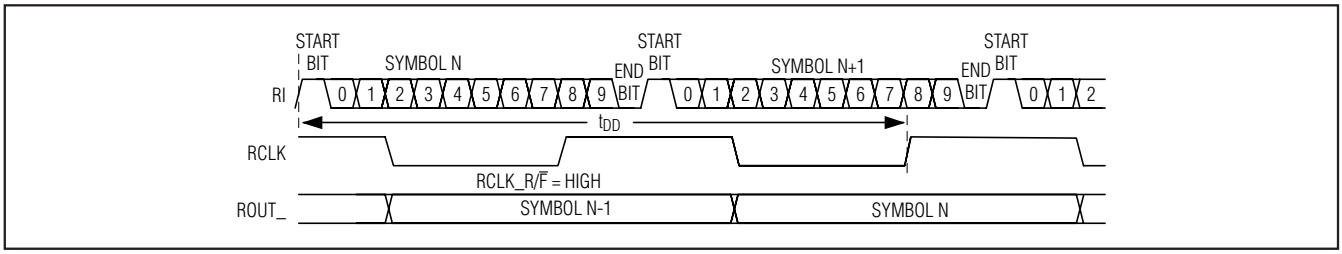


Figure 4. Input-to-Output Delay

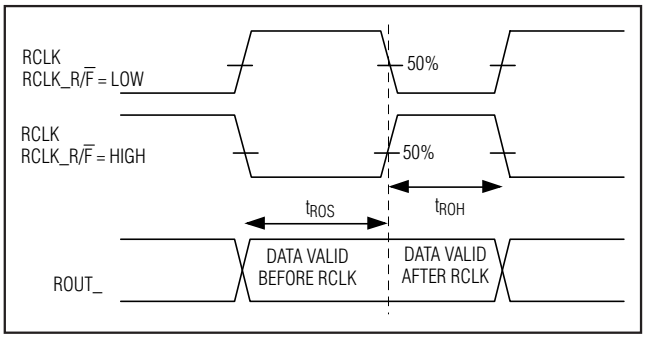


Figure 5. Data Valid Times

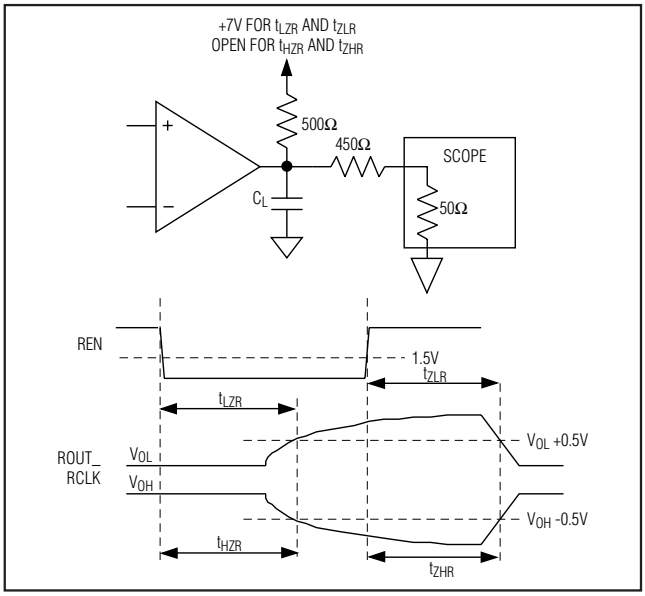


Figure 6. High-Impedance Test Circuit and Timing

Test Circuits/Timing Diagrams (continued)

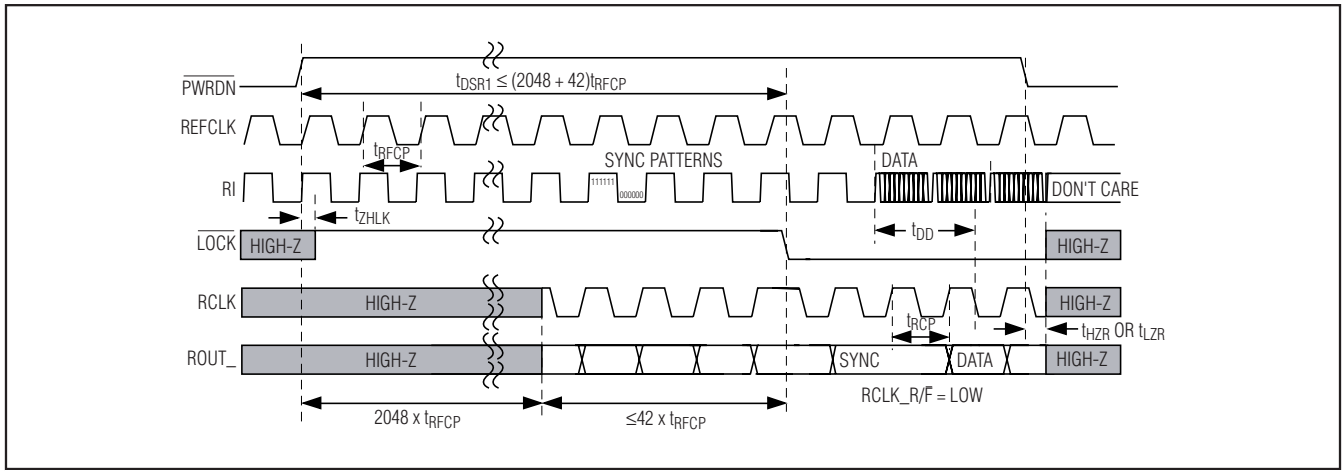


Figure 7. PLL Lock Time from $\overline{PWRDN}$

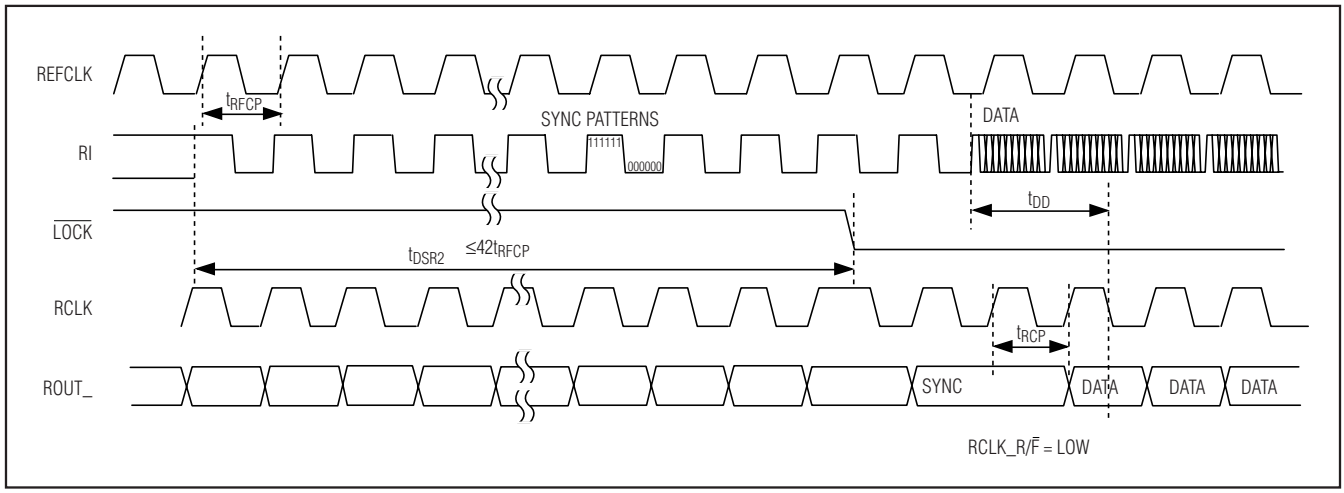


Figure 8. Deserializer PLL Lock Time from Sync Patterns

Detailed Description

The MAX9206/MAX9208 deserialize a BLVDS serializer's output into 10-bit wide parallel LVCMOS/LVTTL data and a parallel rate clock. The MAX9206/MAX9208 include a PLL that locks to the frequency and phase of the serial input, and digital circuits that deserialize and deframe the data. The MAX9206/MAX9208 have high-input jitter tolerance while receiving data at speeds from 160Mbps to 600Mbps. Combination with the MAX9205/MAX9207 BLVDS serializers allows data transmission across backplanes using PCB traces, or across twin-ax or twisted-pair cables.

The MAX9206/MAX9208 deserializers provide a power-saving, power-down mode when $\overline{PWRDN}$ is driven low. The output enable, REN, allows the parallel data outputs (ROUT_) and recovered clock (RCLK) to be enabled or disabled while maintaining lock to the serial input. $\overline{LOCK}$, along with RCLK, indicates when data is valid at ROUT_. Parallel, deserialized data at ROUT_ is strobed out on the selected strobe edge of RCLK. The strobe edge of RCLK is programmable. The falling edge is selected when RCLK_R/$\overline{F}$ is low and the rising edge is selected when RCLK_R/$\overline{F}$ is high.

The interface may be point-to-point or a heavily loaded bus. The characteristic impedance of the media and connections can range from 100Ω for a point-to-point interface to 54Ω for a heavily loaded bus. A double-terminated point-to-point interface uses a 100Ω termination resistor at each end of the interface, resulting in a total load of 50Ω. A heavily loaded bus with a termination as low as 54Ω at each end of the bus (resulting in a total load of 27Ω) can be driven.

A high state bit and a low state bit, added by the BLVDS serializer, frame each 10 bits of serial data and create a guaranteed transition for clock recovery. The high bit is prepended at the start and the low bit is appended at the end of the 10-bit data. The rising edge formed at the end/start bit boundary functions as an embedded clock. Twelve serial bits (10 data + 2 frame) are transmitted by the serializer and received by the deserializer for each 10 bits of data transferred. The MAX9206 accepts a 16MHz to 45MHz reference clock, and receives serial data at 160Mbps (10 data bits x 16MHz) to 450Mbps (10 data bits x 45MHz). The MAX9208 accepts a 40MHz to 60MHz reference clock, and receives serial data at a rate of 400Mbps to 600Mbps.

Initialization

Initialize the MAX9206/MAX9208 before receiving data. When power is applied, with REFCLK stable and $\overline{PWRDN}$ high, RCLK and ROUT_ are held in high impedance, $\overline{LOCK}$ goes high, and the on-chip PLL locks to REFCLK in 2048 cycles. After locking to REFCLK, ROUT_ is active, RCLK tracks REFCLK, and $\overline{LOCK}$ remains high. If transitions are detected at the serial input, the PLL locks to the phase and frequency of the serial input, finds the frame bits, and drives $\overline{LOCK}$ low. If the serial input is sync patterns, $\overline{LOCK}$ goes low in 42 or fewer cycles of RCLK. When $\overline{LOCK}$ goes low, RCLK switches from tracking REFCLK to tracking the serializer reference clock (TCLK). Deserialized data at ROUT_ is valid on the second selected strobe edge of RCLK after $\overline{LOCK}$ goes low. Initialization restarts when power is cycled or on the rising edge of $\overline{PWRDN}$.

Lock to Pseudorandom Data

The MAX9206/MAX9208 lock to pseudorandom serial input data by deductively eliminating rising edges due to data until the embedded end/start edge is found. The end/start edge is identified unless the data contains a permanent, consecutive, frame-to-frame rising edge at the same bit position. Send sync patterns to guarantee lock. A sync pattern is six consecutive ones followed by six consecutive zeros, repeating every RCLK period with only one rising edge (at the end/start boundary). The MAX9205/MAX9207 serializers generate sync patterns when SYNC1 or SYNC2 is driven high.

Since sending sync patterns to initialize a deserializer disrupts data transfer to all deserializers receiving the same serial input (Figure 11, for example), lock to pseudorandom data is preferred in many applications. Lock to pseudorandom data allows initialization of a deserializer after hot insertion without disrupting data communication on other links.

The MAX9206/MAX9208s' deductive algorithm provides very fast pseudorandom data lock times. Table 1 compares typical lock times for pseudorandom and sync pattern inputs.

Power-Down

Drive $\overline{PWRDN}$ low to enter the power-down mode. In power-down, the PLL is stopped and the outputs (ROUT_, RCLK, and $\overline{LOCK}$) are put in high impedance, disabling drive current and also reducing supply current.

Output Enable

When the deserializer is initialized and REN is high, ROUT_ is active, RCLK tracks the serializer reference clock (TCLK), and $\overline{LOCK}$ is low. Driving REN low disables the ROUT_ and RCLK output drivers and does not affect state machine timing. ROUT_ and RCLK go

Table 1. Typical Lock Times

REFCLK FREQUENCY	16MHz	35MHz	40MHz	40MHz
DATA PATTERN	PSEUDORANDOM DATA	PSEUDORANDOM DATA	PSEUDORANDOM DATA	SYNC PATTERNS
Maximum	0.749µs	0.375µs	0.354µs	0.134µs
Maximum (Clock Cycles)	11.99	13.14	14.18	5.37
Average	0.318µs	0.158µs	0.144µs	0.103µs
Average (Clock Cycles)	5.09	5.52	5.76	4.11
Minimum	0.13µs	0.068µs	0.061µs	0.061µs
Minimum (Clock Cycles)	2.08	2.37	2.44	2.45

Note: *Pseudorandom lock performed with 2^{15}-1 PRBS pattern, 10,000 lock time tests.*

into high impedance but $\overline{LOCK}$ continues to reflect the status of the serial input. Driving REN high again enables the ROUT_ and RCLK drivers.

Losing Lock on Serial Data

If one embedded clock edge (rising edge formed by end/start bits) is not detected, $\overline{LOCK}$ goes high, RCLK tracks REFCLK, and ROUT_ stays active but with invalid data. $\overline{LOCK}$ stays high for a minimum of two RCLK cycles. Then, if transitions are detected at the serial input, the PLL attempts to lock to the serial input. When the PLL locks to serial input data, $\overline{LOCK}$ goes low, RCLK tracks the serializer reference clock (TCLK), and ROUT_ is valid on the second selected strobe edge of RCLK after $\overline{LOCK}$ goes low. A minimum of two embedded clock edges in a row are required to regain lock to the serial input after $\overline{LOCK}$ goes high.

For automatic resynchronization, $\overline{LOCK}$ can be connected to the MAX9205/MAX9207 serializer SYNC1 or SYNC2 input. With this connection, when $\overline{LOCK}$ goes high, the serializer sends sync patterns until the deserializer locks to the serial input and drives $\overline{LOCK}$ low.

Input Fail-Safe

When the serial input is undriven (a disconnected cable or serializer output in high impedance, for example) an on-chip fail-safe circuit (Figure 2) drives the serial input high. The response time of the fail-safe circuit depends on interconnect characteristics. With an undriven input, $\overline{LOCK}$ may switch high and low until the fail-safe circuit takes effect. The undriven condition of the link can be detected in spite of $\overline{LOCK}$ switching since $\overline{LOCK}$ is high long enough to be sampled ($\overline{LOCK}$ is high for at least two RCLK cycles after a missed clock edge and RCLK keeps running, allowing sampling). If it is required that $\overline{LOCK}$ remain high for an undriven input, the on-chip fail-safe circuit can be supplemented with external pullup bias resistors.

Deserializer Jitter Tolerance

The t_{JT} parameter specifies the total zero-to-peak input jitter the deserializer can tolerate before a sampling error occurs (Figure 9). Zero-to-peak jitter is measured from the mean value of the deterministic jitter distribution. Sources of jitter include the serializer (supply noise, reference clock jitter, pulse skew, and intersymbol interference), the interconnect (intersymbol interference, crosstalk, within-pair skew, ground shift), and the deserializer (supply noise). The sum of the zero-to-peak individual jitter sources must be less than or equal to the minimum value of t_{JT}.

For example, at 40MHz, the MAX9205 serializer has 140ps (p-p) maximum deterministic output jitter. The zero-to-peak value is 140ps/2 = 70ps. If the interconnect jitter is 100ps (p-p) with a symmetrical distribution, the zero-to-peak jitter is 50ps. The MAX9206 deserializer jitter tolerance is 720ps at 40MHz. The total zero-to-peak input jitter is 70ps + 50ps = 120ps, which is less than the jitter tolerance. In this case, the margin is 720ps - 120ps = 600ps.

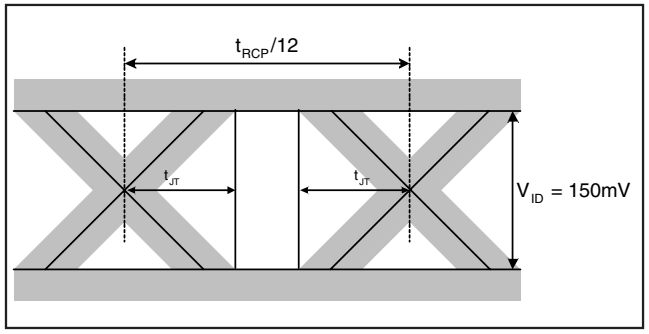


Figure 9. Input Jitter Tolerance

Applications Information

Power-Supply Bypassing

Bypass each supply pin with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor the closest to the supply pin.

Differential Traces and Termination

Trace characteristics affect the performance of the MAX9206/MAX9208. Use controlled-impedance media. Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by a differential receiver.

Eliminate reflections and ensure that noise couples as common mode by running differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

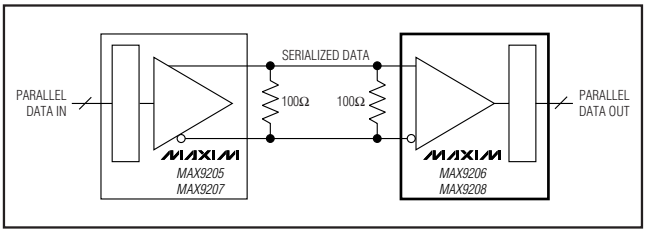


Figure 10. Double-Termination Point-to-Point

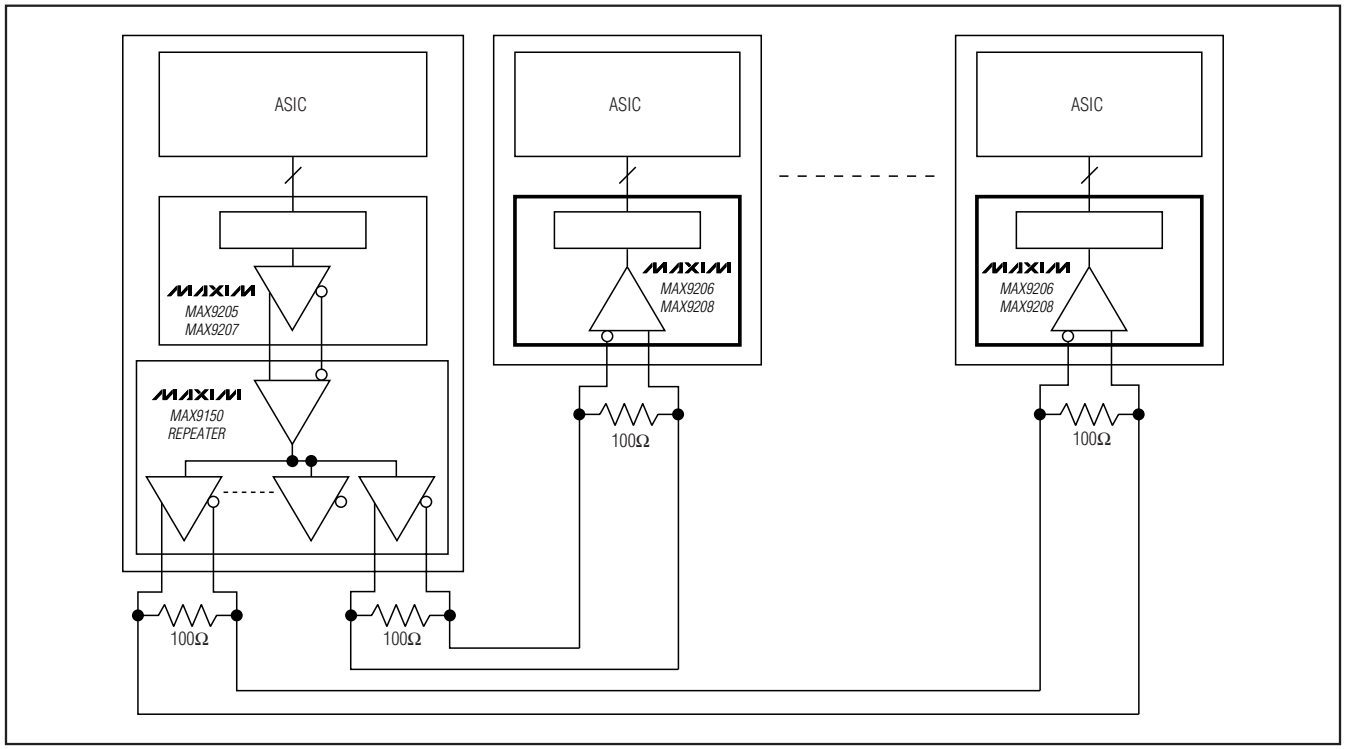


Figure 11. Point-to-Point Broadcast Using MAX9150 Repeater

Table 2. Input/Output Function Table

LOGIC INPUTS		CONDITIONS	OUTPUTS
REN	$\overline{PWRDN}$		
X	Low	Power applied and stable	Power-down mode. PLL is stopped. Current consumption is reduced to 400µA (typ). ROUT_, RCLK, and $\overline{LOCK}$ are high impedance.
Low	High	Deserializer initialized	RCLK and ROUT_ are high impedance. $\overline{LOCK}$ is active, indicating the serial input status.
High	High	Deserializer initialized	RCLK and ROUT_ are active. $\overline{LOCK}$ is active, indicating the serial input status.

X = Don't care.

Topologies

The MAX9206/MAX9208 deserializers can operate in a variety of topologies. Examples of double-terminated point-to-point and point-to-point broadcast are shown in Figures 10 and 11. Use 1% surface-mount termination resistors.

A point-to-point interface terminated at each end in the characteristic impedance of the cable or PCB traces is shown in Figure 10. The total load seen by the serializer is 50Ω. The double termination typically reduces reflections compared to a single 100Ω termination. A single 100Ω termination at the deserializer input is feasible and makes the differential signal swing larger.

A point-to-point version of a multidrop bus is shown in Figure 11. The low-jitter MAX9150 10-port repeater is used to reproduce and transmit the serializer output over 10 double-terminated point-to-point links. Compared to a bus, more interconnect is traded for robust hot-plug capability.

The repeater eliminates nine serializers compared to 10 individual point-to-point serializer-to-deserializer connections. Since repeater jitter is a component of the total jitter seen at the deserializer input (along with other sources of jitter), a low-jitter repeater is essential in most high data-rate applications.

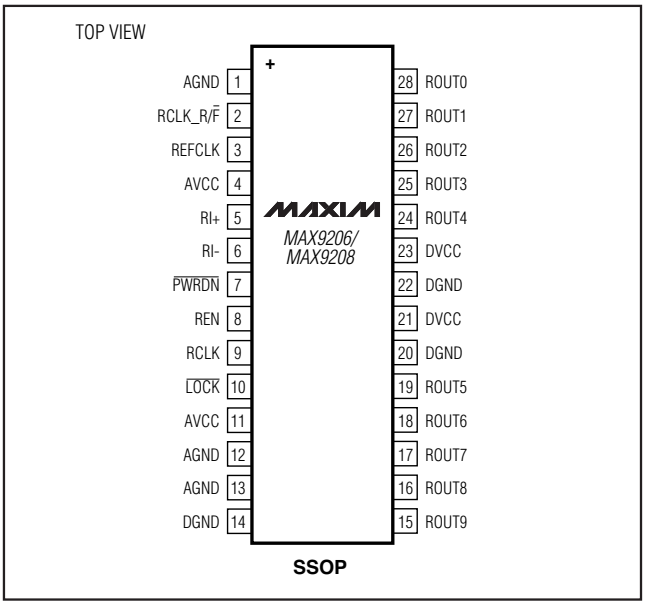
Board Layout

A four-layer PCB providing separate power, ground, and signal layers is recommended. Keep the LVTTL/LVCMOS inputs and outputs separated from the BLVDS inputs to prevent coupling into the BLVDS lines.

Chip Information

PROCESS: CMOS

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 SSOP	A28+4	21-0056	90-0095

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/01	Initial release	—
1	12/07	Max clock frequency increased to 45MHz; min values decreased for REFCLK and RCLK period; updated package outline; updated names for pins 2 and 3.	1–5, 8, 12
2	11/10	Updated *Ordering Information*, *Absolute Maximum Ratings*, and *Package Information*	1, 2, 12

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