



## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V) at $T_J$ max.	560	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	1
$Q_g$ (Max.) (nC)	34	
$Q_{gs}$ (nC)	7.8	
$Q_{gd}$ (nC)	10.4	
Configuration	Single	

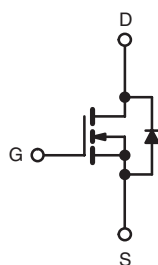
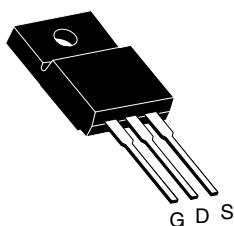
## FEATURES

- Low Figure-of-Merit  $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Gate Charge Improved
- $T_{rr}/Q_{rr}$  Improved
- Compliant to RoHS Directive 2002/95/EC



Available  
RoHS\*  
COMPLIANT

TO-220 FULLPAK



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF8N50L-E3

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
Pulsed Drain Current <sup>b</sup>			
Linear Derating Factor		0.32	W/°C
Single Pulse Avalanche Energy <sup>c</sup>	$E_{AS}$	180	mJ
Maximum Power Dissipation		$T_C = 25$ °C	W
Peak Diode Recovery $dV/dt$ <sup>d</sup>	$dV/dt$	24	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) <sup>e</sup>	for 10 s	300	

## Notes

- Drain current limited by maximum junction temperature.
- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 10$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 6$  A.
- $I_{SD} \leq 8$  A,  $dI/dt \leq 460$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

## SiHF8N50L


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## THERMAL RESISTANCE RATINGS

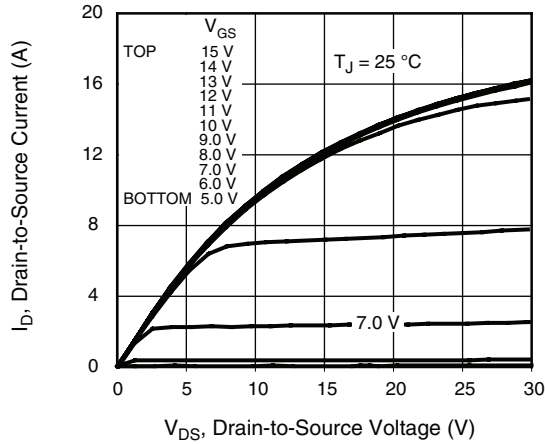
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.1	

SPECIFICATIONS  $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted

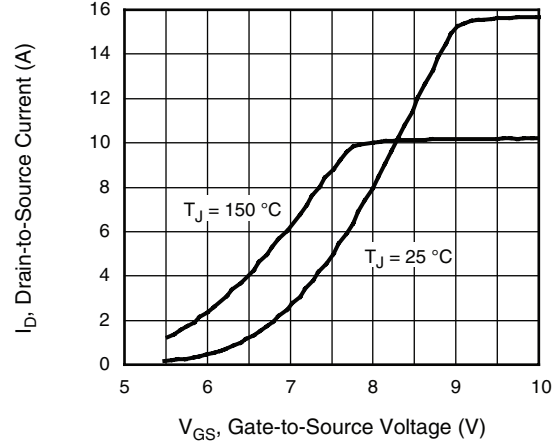
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.5	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	50	$\mu\text{A}$
		$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$   $I_D = 4.0\text{ A}$	-	0.85	1	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 3\text{ A}$	-	2	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$	-	873	-	pF
Output Capacitance	$C_{oss}$		-	105	-	
Reverse Transfer Capacitance	$C_{rss}$		-	11	-	
Total Gate Charge	$Q_g$	$V_{GS} = 0\text{ V}$   $I_D = 6\text{ A}$ , $V_{DS} = 400\text{ V}$	-	22	34	nC
Gate-Source Charge	$Q_{GS}$		-	7.8	-	
Gate-Drain Charge	$Q_{GD}$		-	10.4	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$ , $I_D = 6\text{ A}$ $R_G = 14\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	17.3	-	ns
Rise Time	$t_r$		-	35	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23.6	-	
Fall Time	$t_f$		-	17	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	-	0.7	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8	A
Pulsed Diode Forward Current	$I_{SM}$		-	-	22	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 8\text{ A}$ , $V_{GS} = 0\text{ V}$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = I_S$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 15\text{ V}$	-	63	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	114	-	nC
Body Diode Reverse Recovery Current	$I_{RRM}$		-	3.3	-	A



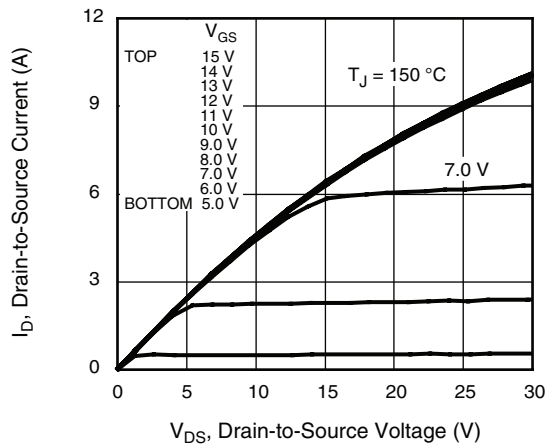
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



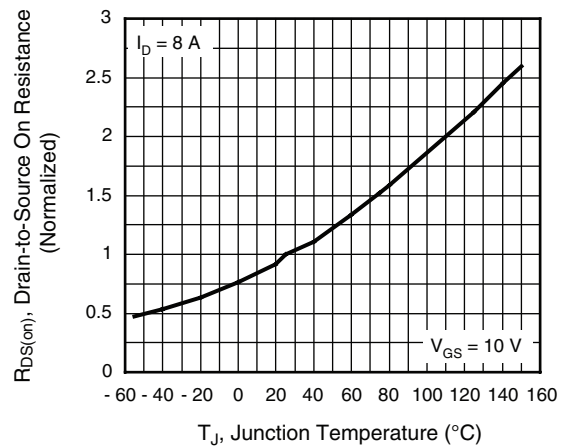
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

# SiHF8N50L

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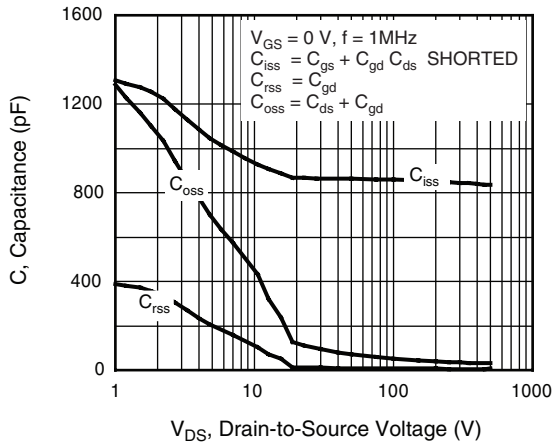


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

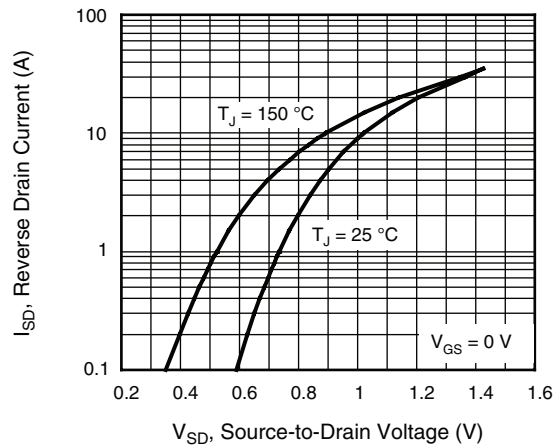


Fig. 7 - Typical Source-Drain Diode Forward Voltage

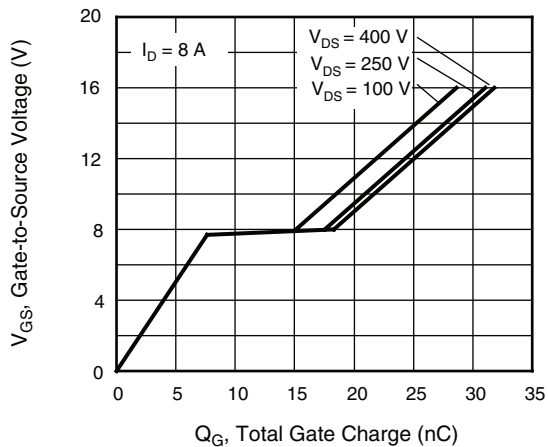


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

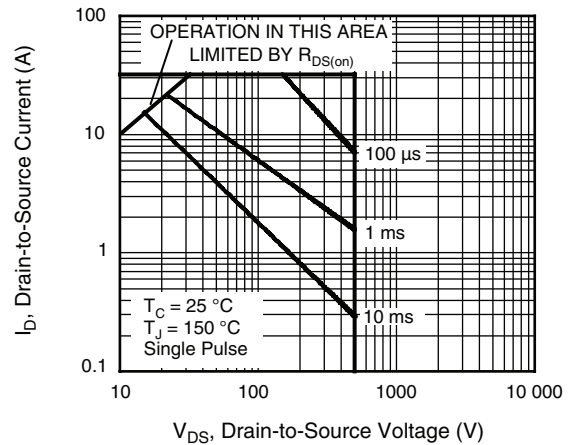


Fig. 8 - Maximum Safe Operating Area

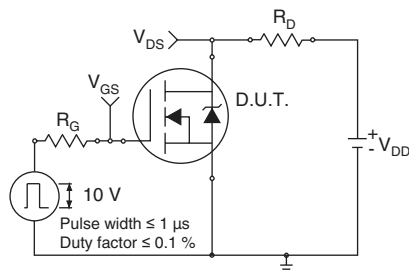


Fig. 9a - Switching Time Test Circuit

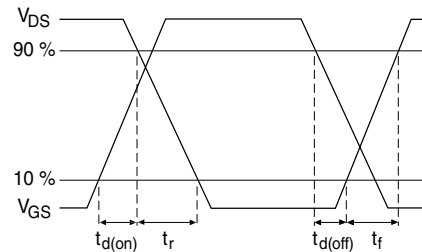
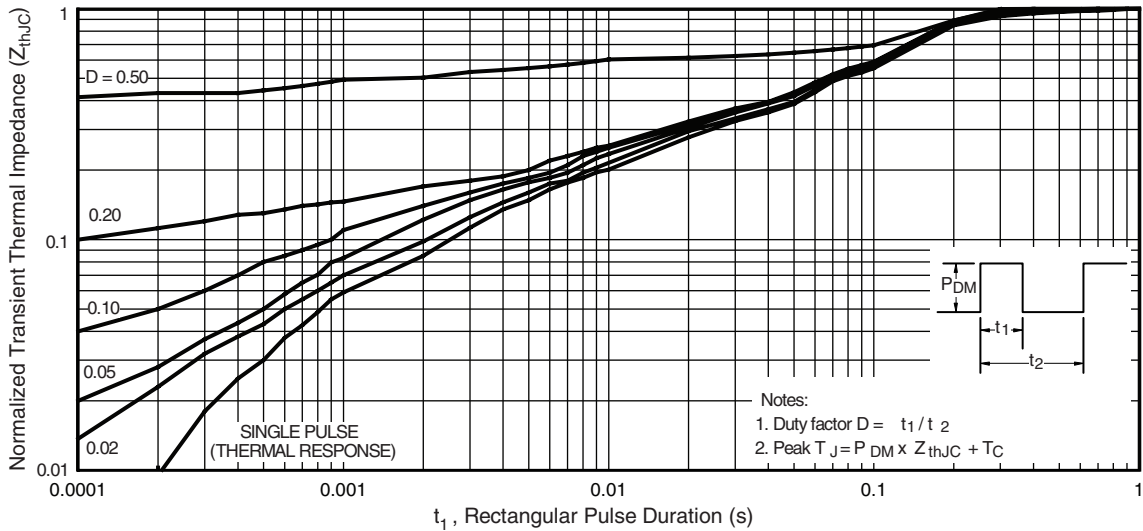
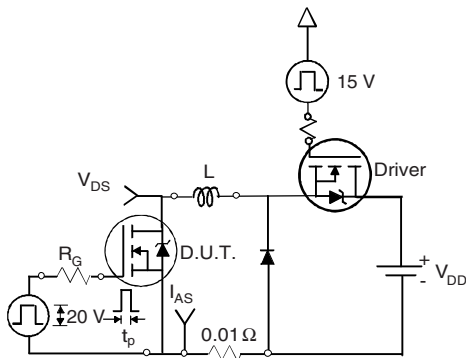


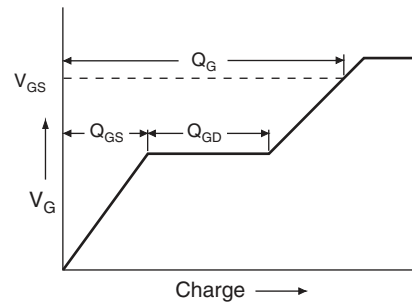
Fig. 9b - Switching Time Waveforms



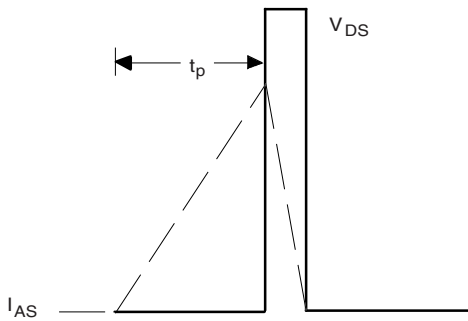
**Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



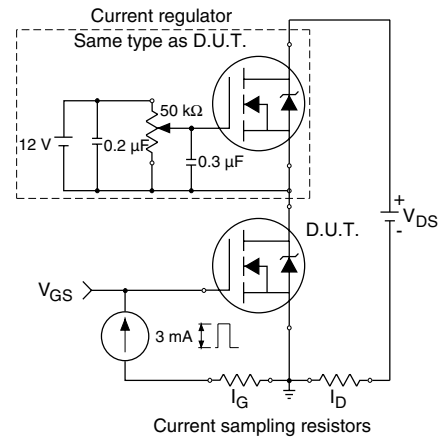
**Fig. 11a - Unclamped Inductive Test Circuit**



**Fig. 12a - Basic Gate Charge Waveform**

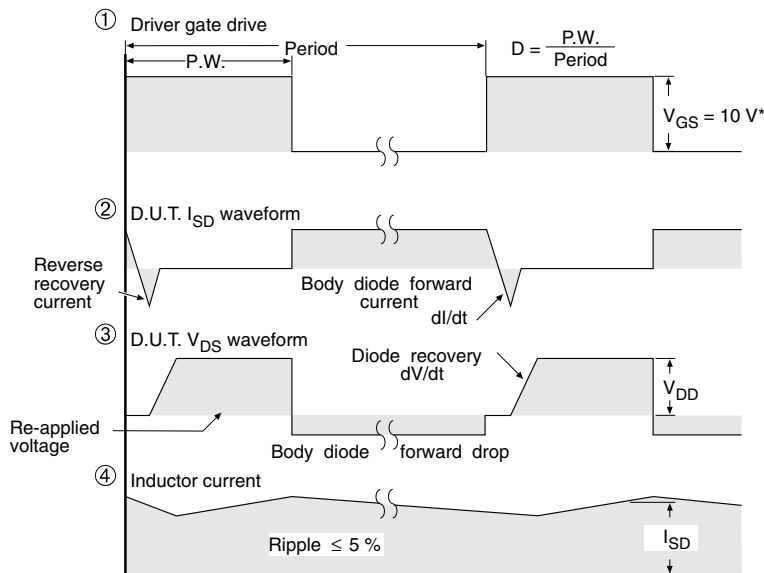
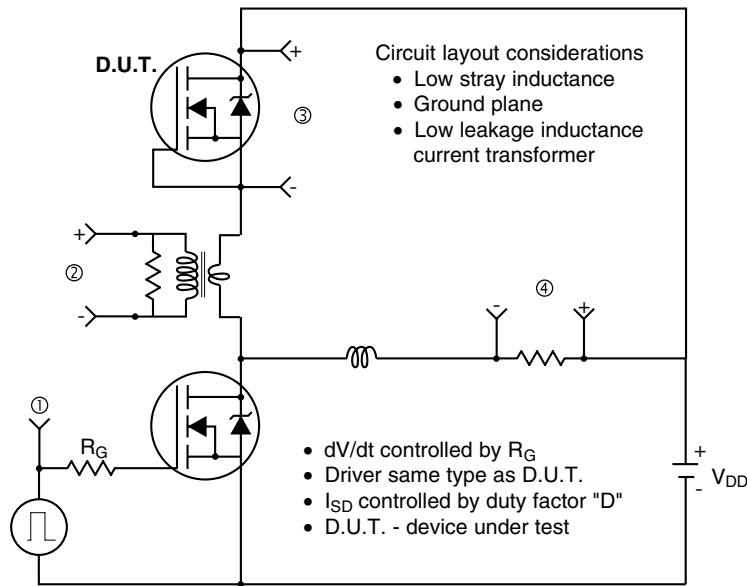


**Fig. 11b - Unclamped Inductive Waveforms**



**Fig. 12b - Gate Charge Test Circuit**

Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 13 - For N-Channel

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## JONHON

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