80C31BH/80C51BH/87C51
MCS® 51
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Automotive

- **Extended Automotive Temperature Range (−40°C to +125°C Ambient)**
- **High Performance CHMOS Process**
- **Power Control Modes**
- **4 Kbyte On-Chip ROM/EPROM**
- **128 x 8-bit RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **5 Interrupt Sources**
- **Quick-Pulse EPROM Programming**
- **2-Level Program Memory Lock EPROM**
- **Boolean Processor**
- **Programmable Serial Port**
- **TTL- and CMOS-Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **IDLE and POWER DOWN Modes**
- **ONCE Mode Facilitates System Testing**
- **Available in 12 MHz and 16 MHz Versions**
- **Available in PLCC and DIP Packages**
  (See Packaging Specification, Order #231369)

The MCS® 51 CHMOS microcontroller products are fabricated on Intel's reliable CHMOS process and are functionally compatible with the standard MCS 51 HMOS microcontroller products. This technology combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS 51 microcontroller architecture and instruction set.

Like the MCS 51 HMOS microcontroller versions, the MCS 51 CHMOS microcontroller products have the following features: 4 Kbytes of EPROM/ROM (87C51/80C51BH respectively); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS 51 CHMOS microcontroller products exhibit low operating power, along with two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The 87C51 is the EPROM version of the 80C51BH. It contains 4 Kbytes of on-chip program memory that can be electrically programmed, and can be erased by exposure to ultraviolet light. The 87C51 EPROM array uses a modified Quick-Pulse Programming algorithm, by which the entire 4 Kbyte array can be programmed in about 12 seconds.

NOTICE:
This datasheet contains information on products in full production. Specifications within this datasheet are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

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January 1995 **Order Number: 270419-007**

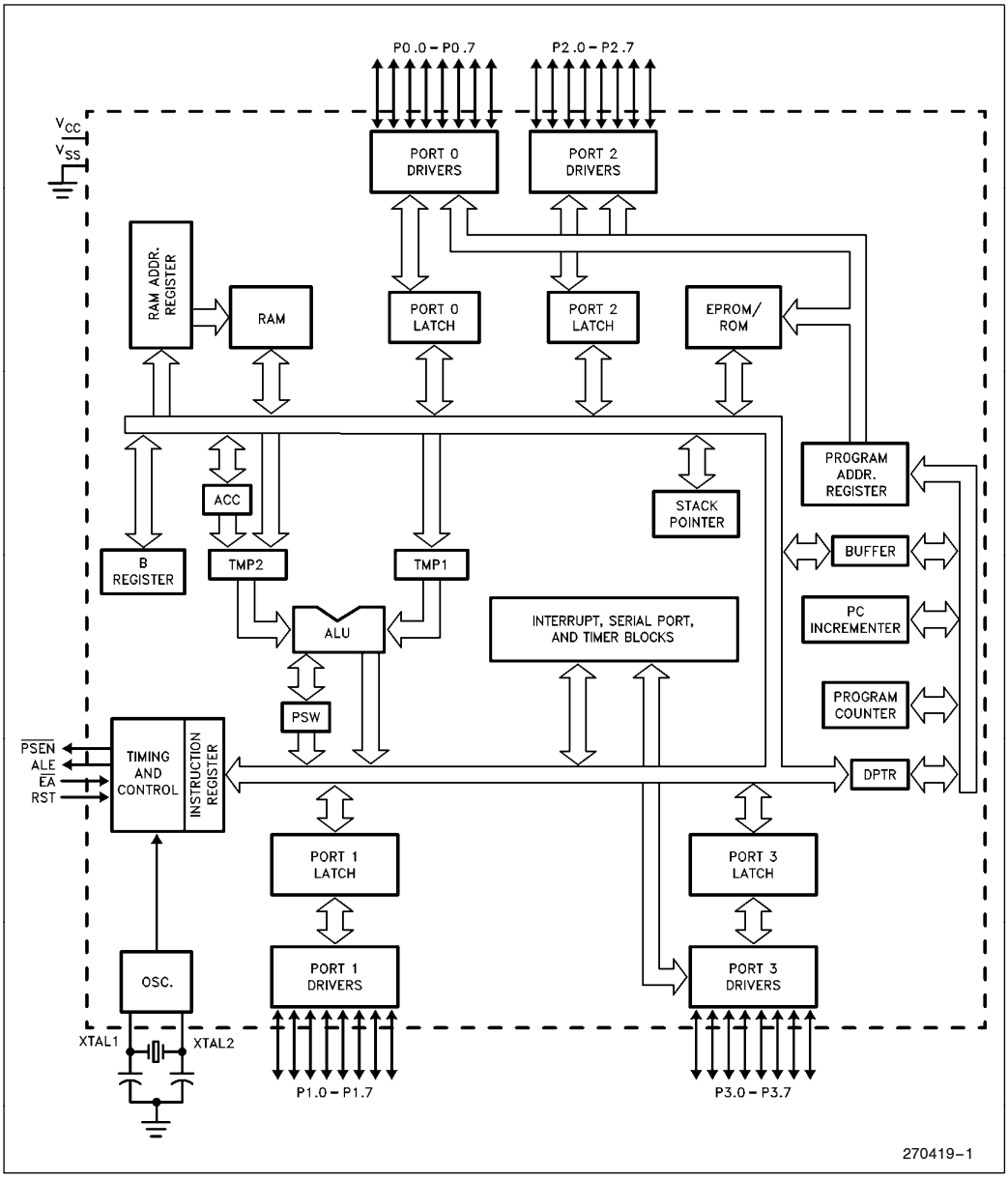


Figure 1. MCS® 51 Microcontroller Architectural Block Diagram

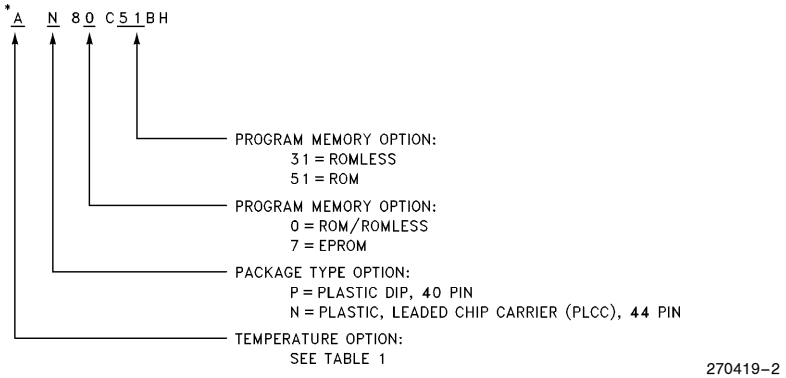
80C31BH/80C51BH/87C51 PRODUCT OPTIONS

Intel's extended and automotive temperature range products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C ambient. For the automotive temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +125°C ambient.

The automotive and extended temperature versions of the MCS 51 microcontroller product families are available with or without burn-in options as listed in Table 1.

As shown in Figure 2, temperature, burn-in, and package options are identified by a one- or two-letter prefix to the part number.



***Example:**
AN80C51 indicates an automotive temperature range version of the 80C51 in a PLCC package with 4 Kbyte ROM program memory.

Figure 2. MCS® 51 Microcontroller Product Family Nomenclature

Table 1. Temperature Options

Temperature Classification	Temperature Designation	Operating Temperature °C Ambient	Burn-In Options
Extended	T	−40 to +85	Standard
	L	−40 to +85	Extended
Automotive	A	−40 to +125	Standard
	B	−40 to +125	Extended

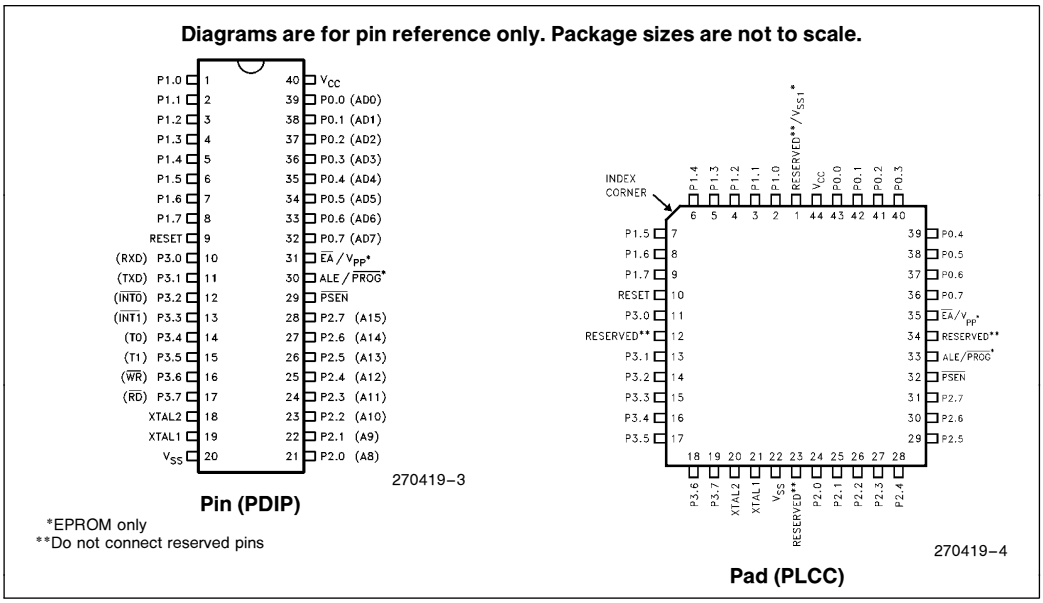


Figure 3. Pin Connections

PIN DESCRIPTION

V_{CC}: Supply voltage during normal, Idle, and Power Down operations.

V_{SS}: Circuit ground.

V_{SS1}: V_{SS1}—(EPROM PLCC only) secondary ground. Provided to reduce ground bounce and improve power supply bypassing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22). For ROM and ROMless, pin 1 is reserved—do not connect.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1s.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the datasheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s.

During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives some control signals and the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the datasheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS 51 microcontroller family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial Input Line
P3.1	TXD	Serial Output Line
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 External Input
P3.5	T1	Timer 1 External Input
P3.6	$\overline{WR}$	External Data Memory Write Strobe
P3.7	$\overline{RD}$	External Data Memory Read Strobe

Port 3 also receives some control signals for EPROM programming and program verification.

RESET: Reset input. A logic high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset to be generated using only an external capacitor to V_{CC}.

ALE/$\overline{PROG}$ (EPROM Only): Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the Read strobe to External Program Memory. When the 87C51/80C51BH is executing from Internal Program Memory, $\overline{PSEN}$ is inactive (high). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the 87C51/80C51BH to fetch code from External Program Memory locations starting at 0000H up to 0FFFFH. [Note, however, that if either of the Lock Bits is programmed, the logic level at $\overline{EA}$ is internally latched during reset.] (EPROM only.)

$\overline{EA}$ must be strapped to V_{CC} for internal program execution.

V_{PP} (EPROM Only): This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.

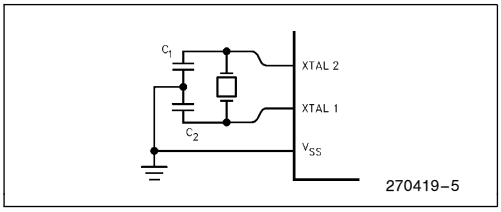


Figure 4. Using the On-Chip Oscillator

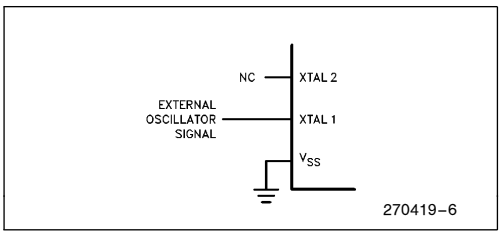


Figure 5. External Clock Drive

XTAL1: Input to the inverting oscillator amplifier and input to the internal clock generating circuits.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Datasheet must be observed.

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Functions Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when Idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to

Table 2. Status of the External Pins During Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Applications Handbook, and Application Note AP-252, ''Designing with the 80C51BH.''

internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

DESIGN CONSIDERATIONS

- At power on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.
- Before entering the Power Down mode the contents of the Carry Bit and B.7 must be equal.
- When the Idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins in not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.
- For EPROM versions exposure to light when the device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.

PROGRAM MEMORY LOCK (EPROM Only)

The 87C51 contains two program memory lock schemes: Encrypted Verify and Lock Bits.

Encrypted Verify: The 87C51 implements a 32-byte EPROM array that can be programmed by the customer, and which can then be used to encrypt the program code bytes during EPROM verification. The EPROM verification procedure is performed as usual, except that each code byte comes out logically X-NORed with one of the 32 key bytes. The key bytes are gone through in sequence. Therefore, to read the ROM code, one has to know the 32 key bytes in their proper sequence.

Lock Bits: Also on the chip are two Lock Bits which can be left unprogrammed (U) or can be programmed (P) to obtain the following additional features:

Bit 1	Bit 2	Additional Features
U	U	none
P	U	• Externally fetched code can not access internal Program Memory. • Further programming disabled.
U	P	(Reserved for Future definition.)
P	P	• Externally fetched code can not access internal Program Memory. • Further programming disabled. • Program verification is disabled.

When Lock Bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ONCE MODE

The ONCE (“on-circuit emulation”) mode facilitates testing and debugging of systems using the 87C51 without the 87C51 having to be removed from the circuit. The ONCE mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias −40°C to +125°C

Storage Temperature .....−65°C to +150°C

Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} .....0V to +13.0V

Voltage on Any Other Pin to V_{SS} ..−0.5V to +6.5V

I_{OL} per I/O pin .....15 mA

Power Dissipation.....1.5W
(Based on package heat transfer limitations, not device power consumption).

Typical Junction Temperature (T_J) .....+135°C

(Based upon ambient temperature at +125°C)

Typical Thermal Resistance Junction-to-Ambient (θ_{JA}):

PDIP .....75°C/W

PLCC.....46°C/W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the ''Absolute Maximum Ratings'' may cause permanent damage. These are stress ratings only. Operation beyond the ''Operating Conditions'' is not recommended and extended exposure beyond the ''Operating Conditions'' may affect device reliability.*

DC CHARACTERISTICS:

(T_A = −40°C to +125°C; V_{CC} = 5V ±10% (5V ±20% EPROM Only); V_{SS} = 0V)

Symbol	Parameter	Min	Typ(1)	Max (87C51/80C51BH)	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	−0.5		0.2 V_{CC}−0.25	V	
V_{IL1}	Input Low Voltage to $\overline{EA}$	0		0.2 V_{CC}−0.45	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2V_{CC}+1.0		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}+0.1		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45(7)	V	I_{OL} = 1.6 mA(2)
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)			0.45(7)	V	I_{OL} = 3.2 mA(2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	2.4			V	I_{OH} = −60 μA
		0.9 V_{CC}			V	I_{OH} = −10 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −800 μA
		0.9 V_{CC}			V	I_{OH} = −80 μA(3)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			−75	μA	V_{IN} = 0.45 V
I_{TL}	Logical 1-to-0 transition current (Ports 1, 2, 3)			−750	μA	(4)
I_{LI}	Input Leakage Current (Port 0)			±10	μA	V_{IN} = V_{IL} or V_{IH}
I_{CC}	Power Supply Current: Active Mode @ 12 MHz (5) Idle Mode @ 12 MHz (5) Power Down Mode		 11.5 1.3 3	 25/20 6/5 100/75	 mA mA μA	 (6) V_{CC} = 2.2V to 5.5V
RRST	Internal Reset Pulldown Resistor	50		300	KΩ	
CIO	Pin Capacitance			10	pF	

NOTES:

1. ''Typicals'' are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temp, 5V.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

NOTES: (Continued)
4. Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. ICCMAX at other frequencies is given by:

Active Mode: 87C51 ICCMAX = 0.94 × FREQ + 13.71
80Cx1BH ICCMAX = 1.47 × FREQ + 2.36
Idle Mode: ICCMAX = 0.14 × FREQ + 3.81

where FREQ is the external oscillator frequency in MHz. ICCMAX is given in mA. See Figure 6.
6. See Figures 7 through 10 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2.0V.
7. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port
Port 0: 26 mA
Ports 1, 2, and 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

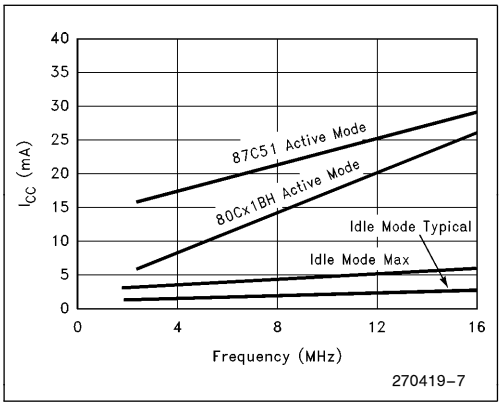


Figure 6. I_{CC} vs. FREQ. Valid only within frequency specifications of the device under test.

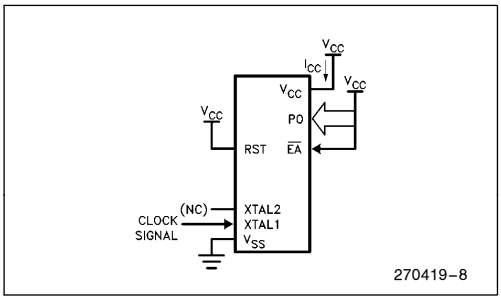


Figure 7. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

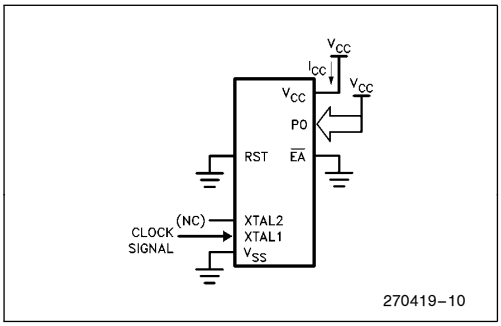


Figure 8. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

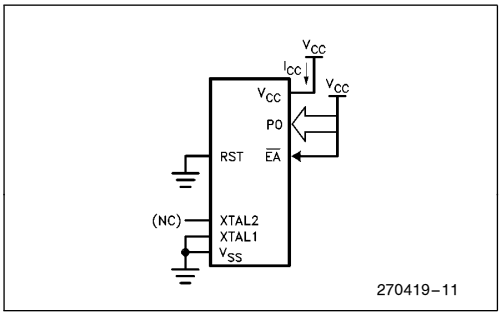


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected.

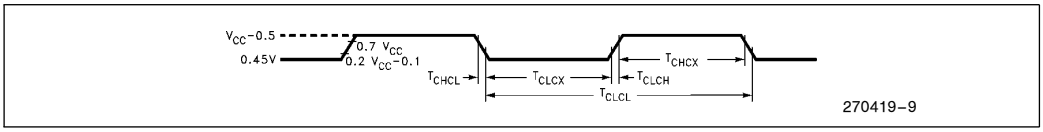


Figure 10. Clock Signal Waveform for I_{CC} tests in Active and Idle Modes. $T_{CLCH} = T_{CHCL} = 5$ ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A:Address.
C:Clock.
D:Input data.
H:Logic level HIGH.
I:Instruction (program memory contents).
L:Logic level LOW, or ALE.
P:$\overline{\text{PSEN}}$.
Q:Output data.
R:$\overline{\text{RD}}$ signal.
T:Time.
V:Valid.
W:$\overline{\text{WR}}$ signal.
X:No longer a valid logic level.
Z:Float.

For example,

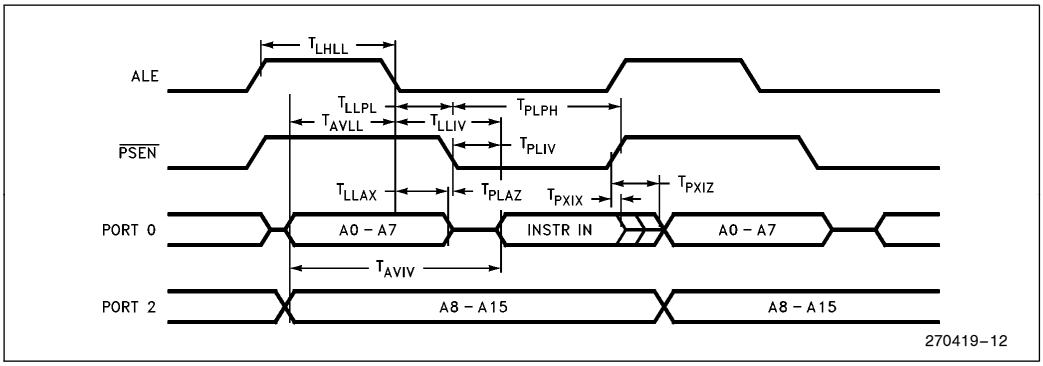
T_{AVLL} = Time from Address Valid to ALE Low.
T_{LLPL} = Time from ALE Low to PSEN Low.

AC CHARACTERISTICS: (T_A = −40°C to +125°C; V_{CC} = 5V ±10% (5V ±20% EPROM Only); V_{SS} = 0V; Load Capacitance for Port 0, ALE, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

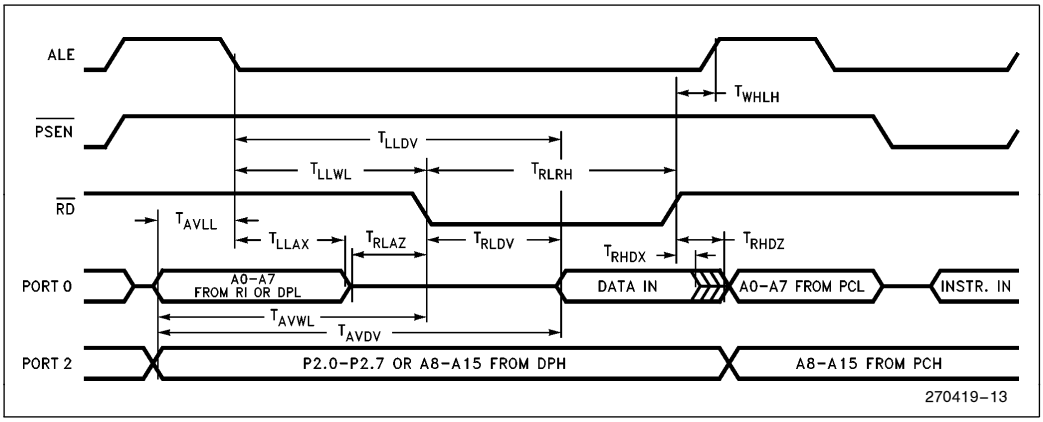
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/T_{CLCL}$	Oscillator Frequency 87C51/80C51BH/80C31BH			3.5	12–16	MHz
T_{LHLL}	ALE Pulse Width	127		$2T_{CLCL}-40$		ns
T_{AVLL}	Address Valid to ALE Low	28		$T_{CLCL}-55$		ns
T_{LLAX}	Address Hold After ALE Low	48		$T_{CLCL}-35$		ns
T_{LLIV}	ALE Low to Valid Instr In		224		$4T_{CLCL}-110$	ns
T_{LLPL}	ALE Low to $\overline{\text{PSEN}}$ Low	43		$T_{CLCL}-40$		ns
T_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	205		$3T_{CLCL}-45$		ns
T_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instr In		135		$3T_{CLCL}-115$	ns
T_{PXIX}	Input Instr Hold After $\overline{\text{PSEN}}$	0		0		ns
T_{PXIZ}	Input Instr Float After $\overline{\text{PSEN}}$		59		$T_{CLCL}-25$	ns
T_{AVIV}	Address Valid to Valid Instr In		312		$5T_{CLCL}-105$	ns
T_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
T_{RLRH}	$\overline{\text{RD}}$ Pulse Width	400		$6T_{CLCL}-100$		ns
T_{WLWH}	$\overline{\text{WR}}$ Pulse Width	400		$6T_{CLCL}-100$		ns
T_{RLDV}	$\overline{\text{RD}}$ Low to Valid Data In		252		$5T_{CLCL}-165$	ns
T_{RHDX}	Data Hold After $\overline{\text{RD}}$ High	0		0		ns
T_{RHDZ}	Data Float After $\overline{\text{RD}}$ High		97		$2T_{CLCL}-70$	ns
T_{LLDV}	ALE Low to Valid Data In		517		$8T_{CLCL}-150$	ns
T_{AVDV}	Address Valid to Valid Data In		585		$9T_{CLCL}-165$	ns
T_{LLWL}	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3T_{CLCL}-50$	$3T_{CLCL}+50$	ns
T_{AVWL}	Address Valid to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		$4T_{CLCL}-130$		ns
T_{QVWX}	Data Valid to $\overline{\text{WR}}$ Transition	23		$T_{CLCL}-60$		ns
T_{WHQX}	Data Hold After $\overline{\text{WR}}$ High	33		$T_{CLCL}-50$		ns
T_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
T_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	$T_{CLCL}-40$	$T_{CLCL}+40$	ns

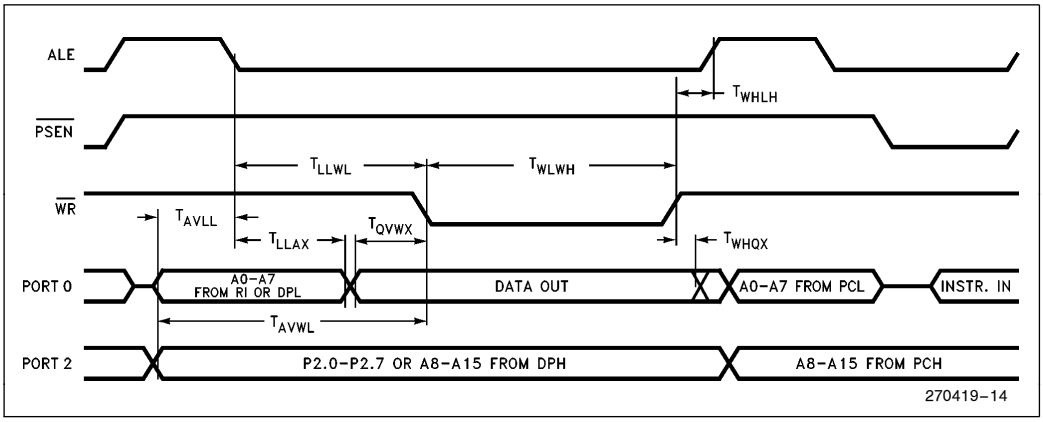
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



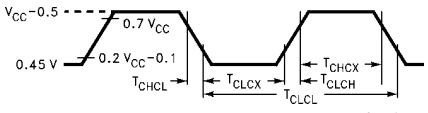
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency	3.5 3.5	12 16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		20	ns
T_{CHCL}	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM

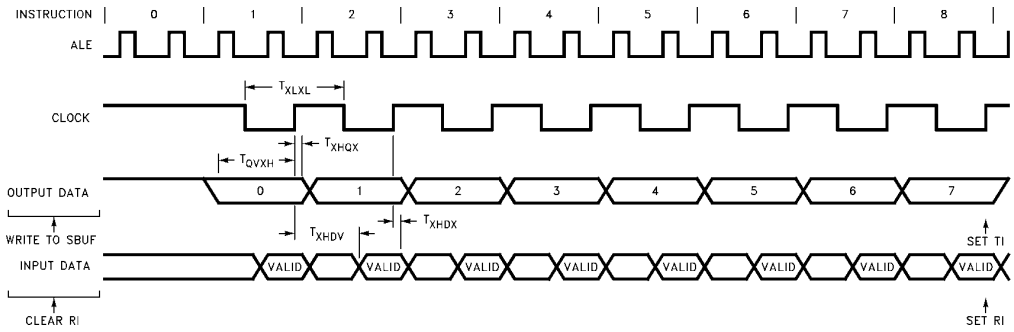


270419–17

SERIAL PORT TIMING—SHIFT REGISTER MODE

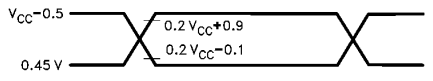
Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1.0		$12T_{CLCL}$		μs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10T_{CLCL}-133$		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2T_{CLCL}-117$		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10T_{CLCL}-133$	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



270419–15

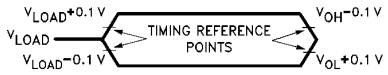
AC TESTING INPUT, OUTPUT WAVEFORMS



270419–16

AC inputs during testing are driven at V_{CC} − 0.5 for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270419–18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

EPROM CHARACTERISTICS (EPROM Only)

The 87C51 is programmed by a modified Quick-Pulse Programming algorithm. It differs from older methods in the value used for V_{PP} (Programming Supply Voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C51 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C51 manufactured by Intel.

Table 3 shows the logic levels for reading the signature byte, and for programming the Program Memory, the Encryption Table, and the Lock Bits. The circuit configuration and waveforms for Quick-Pulse Programming are shown in Figures 11 and 12. Figure 13 shows the circuit configuration for normal Program Memory verification.

Table 3. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read Signature	1	0	1	1	0	0	0	0
Program Code Data	1	0	0*	V_{PP}	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Pgm Encryption Table	1	0	0*	V_{PP}	1	0	1	0
Pgm Lock Bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm Lock Bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
"1" = Valid high for that pin
"0" = Valid low for that pin
V_{PP} = 12.75V ± 0.25V
V_{CC} = 5V ±20% during programming and verification
*ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100 µs (±10 µs) and high for a minimum of 10 µs.

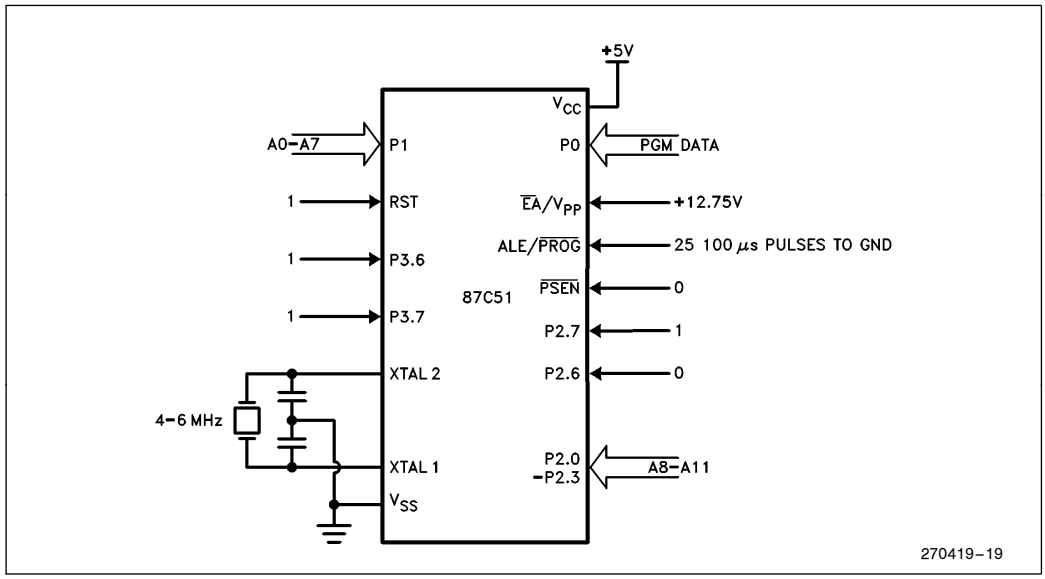


Figure 11. Programming Configuration

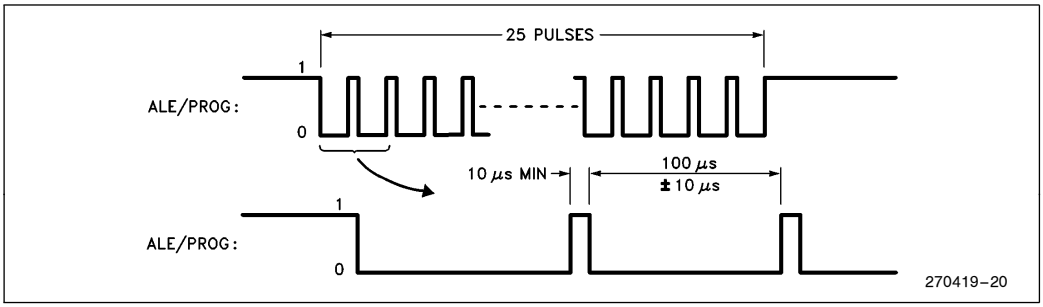


Figure 12. $\overline{\text{PROG}}$ Waveforms

Quick-Pulse Programming (EPROM Only)

The setup for Microcontroller Quick-Pulse Programming is shown in Figure 11. Note that the 87C51 is running with a 4 to 6 MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to Ports 1 and 2, as shown in Figure 11. The code byte to be programmed into that location is applied to Port 0. RST, $\overline{\text{PSEN}}$, and pins of Ports 2 and 3 specified in Table 3 are held at the ''Program Code Data'' levels indicated in Table 2. Then ALE/$\overline{\text{PROG}}$ is pulsed low 25 times as shown in Figure 12.

To program the Encryption Table, repeat the 25-pulse programming sequence for addresses 0 through 1FH, using the ''Pgm Encryption Table'' levels. Don't forget that after the Encryption Table is programmed, verify cycles will produce only encrypted data.

To program the Lock Bits, repeat the 25-pulse programming sequence using the ''Pgm Lock Bit'' levels. After one Lock Bit is programmed, further programming of the Code Memory and Encryption Table is disabled. However, the other Lock Bit can still be programmed.

Note that the $\overline{\text{EA}}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

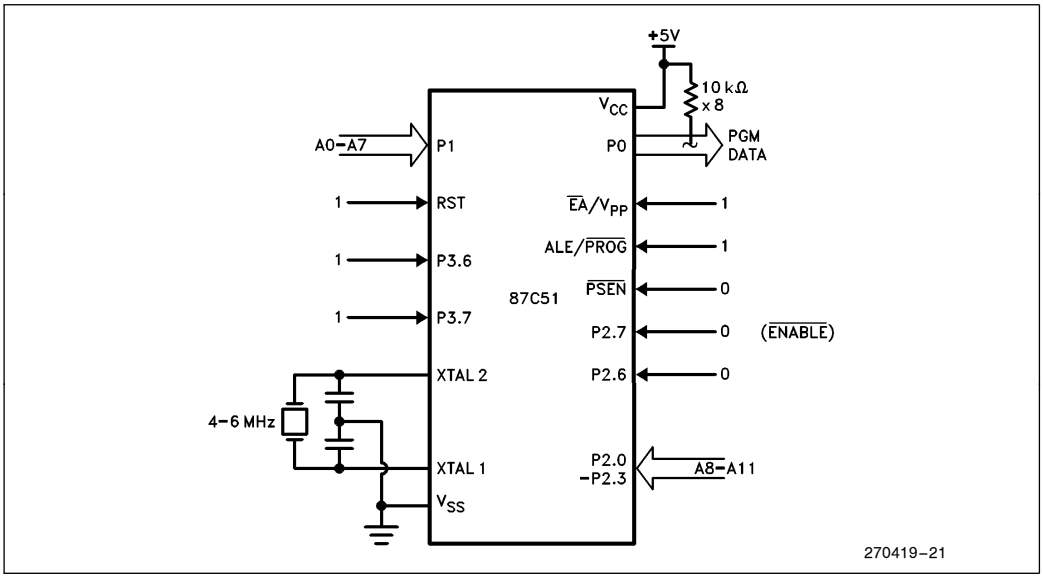


Figure 13. Program Verification

Program Verification (EPROM Only)

If Lock Bit 2 has not been programmed, the on-chip Program Memory can be read out for program verification. The address of the Program Memory location to be read is applied to Ports 1 and 2 as shown in Figure 13. The other pins are held at the ''Verify Code Data'' levels indicated in Table 3. The contents of the addressed location will be emitted on Port 0. External pullups are required on Port 0 for this operation. Detailed timing specifications are shown in later sections of this datasheet.

If the Encryption Table has been programmed, the data presented at Port 0 will be the Exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the Encryption Table contents in order to correctly decode the verification data. The Encryption Table itself can not be read out.

Reading the Signature Bytes (EPROM Only)

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

(030H) = 89H indicates manufactured by Intel

(031H) = 57H indicates 87C51

Program/Verify Algorithms (EPROM Only)

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics (EPROM Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

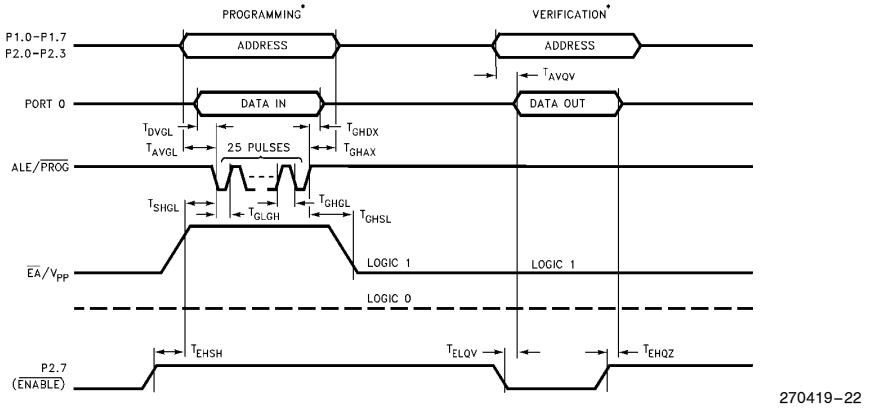
Erasure leaves the array in an all 1s state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS:

(T_A = 21°C to 27°C, V_{CC} = 5V ±20%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		50	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48T_{CLCL}$		
T_{GHAX}	Address Hold After $\overline{PROG}$	$48T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48T_{CLCL}$		
T_{GHDX}	Data Hold After $\overline{PROG}$	$48T_{CLCL}$		
T_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
T_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		μs
T_{GLGH}	$\overline{PROG}$ Width	90	110	μs
T_{AVQV}	Address to Data Valid		$48T_{CLCL}$	
T_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48T_{CLCL}$	
T_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48T_{CLCL}$	
T_{GHGL}	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*FOR PROGRAMMING CONDITIONS SEE FIGURE 11.
FOR VERIFICATION CONDITIONS SEE FIGURE 13.

DATASHEET REVISION SUMMARY

The following are the key differences between this datasheet and the -006 version:

1. The ''preliminary'' status was removed and replaced with production status (no label).
2. Trademark was updated.

The following are the key differences between the -005 and the -006 version of the datasheet:

1. Preliminary notice added to Title page.
2. Figure 3 Pin Connections the NC** pins are now Reserved** pins.
3. Figure 3 Pin Connections RST pin is now RESET pin.
4. RST pin description is now RESET pin description.
5. Figure 4 the capacitor values have been removed.
6. CERDIP part reference in the D.C. Characteristics section has been removed.
7. I_{CC} Max characteristics have been corrected to reflect test program conditions.
8. T_{AVIV} and T_{RLDV} formulas changed to correlate 12 MHz timings.

The following are the key differences between the -004 and the -005 version of this datasheet:

1. Removed references to burn-in options in Table 1 and added explanation of burn-in offered. Removed references to commercial temperatures.
2. Deleted reference to ''−1'' designation 16 MHz.
3. Differentiated V_{CC} for ROM/ROMless and EPROM.

The following are the key differences between the -002 and the -003 version of this datasheet:

1. Changed the title to 80C31BH/80C51BH/87C51 CHMOS Single-Chip 8-Bit Microcontroller.
2. Added the pin count for each package version in Figure 2.
3. Removed references to burn-in options in Table 1.
4. Added external oscillator start-up design considerations.

The following are the key differences between the -002 and the -001 version of the 80C51BH datasheet:

1. Maximum I_{OL} per I/O pin added.
2. Note 7 on Maximum Current Specifications added to DC Characterstics.
3. Datasheet Revision Summary added.

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