



16-Mbit (1M words × 16-bit/2M words × 8-bit) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby current
 - Typical standby current: 5.5 μA
 - Maximum standby current: 16 μA
- High speed: 45 ns/55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- 48-pin TSOP I package configurable as 1M × 16 or 2M × 8 SRAM
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

CY62167G and CY62167GE are high-performance CMOS, low-power (MoBL[®]) SRAM devices with embedded ECC^[1]. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62167GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable (\overline{CE}) input LOW. To access dual chip enable devices, assert both chip enable inputs – \overline{CE}_1 as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable (\overline{WE}) input LOW, and provide the data and address on the device data pins (I/O₀

through I/O₁₅) and address pins (A₀ through A₁₉) respectively. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O₈ through I/O₁₅ and BLE controls I/O₀ through I/O₇.

To perform data reads, assert the Output Enable (\overline{OE}) input and provide the required address on the address lines. You can access read data on the I/O lines (I/O₀ through I/O₁₅). To perform byte accesses, assert the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH for a single chip enable device and \overline{CE}_1 HIGH / CE_2 LOW for a dual chip enable device), or the control signals are de-asserted (\overline{OE} , BLE, BHE).

These devices have a unique Byte Power-down feature where, if both the Byte Enables (BHE and BLE) are disabled, the devices seamlessly switch to the standby mode irrespective of the state of the chip enables, thereby saving power.

On the CY62167GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the Truth Table – CY62167G/CY62167GE on page 16 for a complete description of read and write modes.

The CY62167G and CY62167GE devices are available in a Pb-free 48-pin TSOP I package and 48-ball VFBGA packages. The logic block diagrams are on page 2.

The device in the 48-pin TSOP I package can also be configured to function as a 2M words × 8-bit device. Refer to the Pin Configurations section for details.

For a complete list of related documentation, click [here](#).

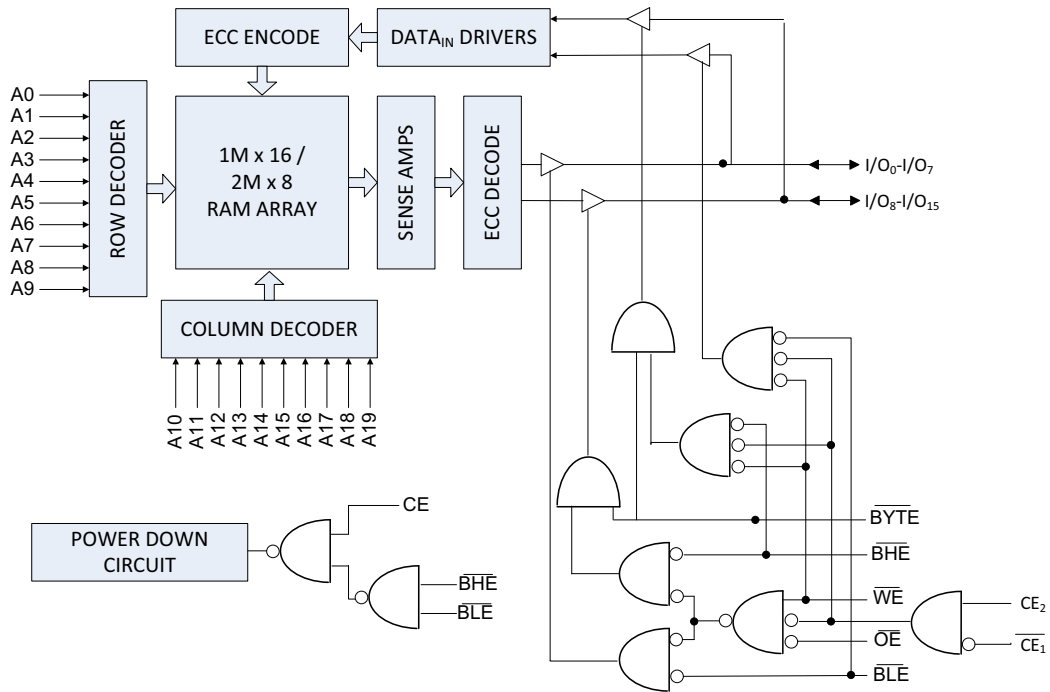
Product Portfolio

| Product | Features and Options (see the Pin Configurations section) | Range | V _{CC} Range (V) | Speed (ns) | Current Consumption | | | |
|---------------|---|------------|---------------------------|------------|--------------------------------|-----|--------------------------------|-----|
| | | | | | Operating I _{CC} (mA) | | Standby, I _{SB2} (μA) | |
| | | | | | f = f _{max} | | | |
| | | | | | Typ ^[2] | Max | Typ ^[2] | Max |
| CY62167G(E)18 | Single or dual Chip Enables Optional ERR pin | Industrial | 1.65 V–2.2 V | 55 | 29 | 32 | 7 | 26 |
| CY62167G(E)30 | | | 2.2 V–3.6 V | 45 | 29 | 36 | 5.5 | 16 |
| CY62167G(E) | | | 4.5 V–5.5 V | | | | | |

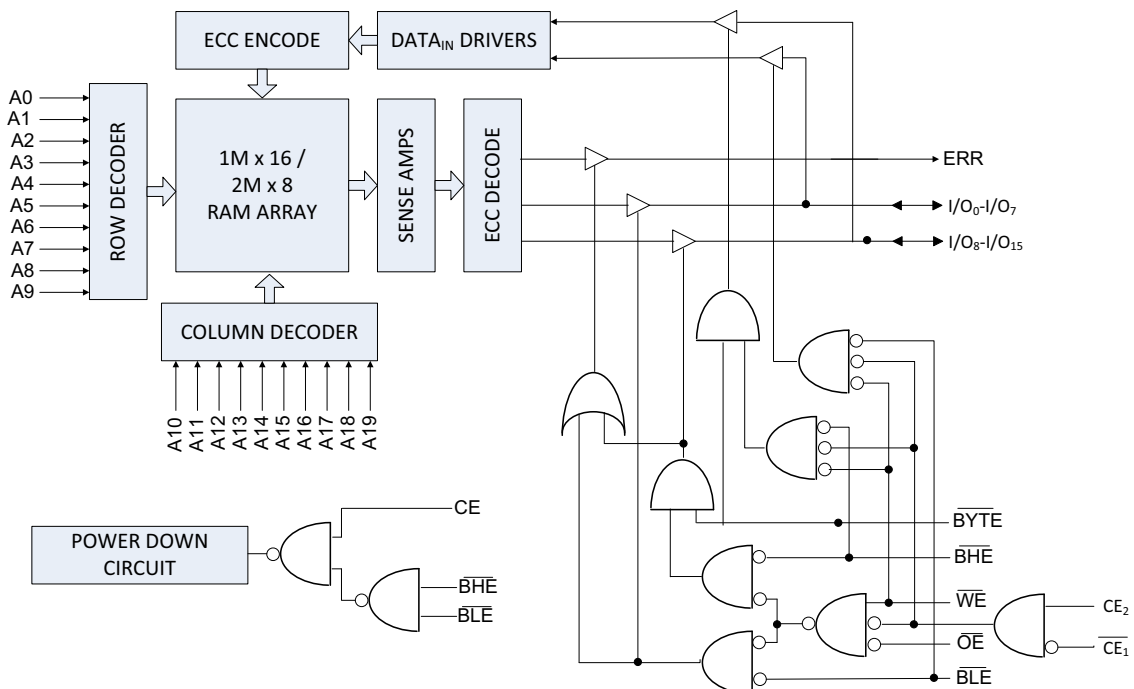
Notes

1. This device does not support automatic write-back on error detection.
2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY62167G



Logic Block Diagram – CY62167GE



Contents

| | | | |
|---|-----------|--|-----------|
| Pin Configuration – CY62167G | 4 | Ordering Information | 17 |
| Pin Configuration – CY62167GE | 5 | Ordering Code Definitions | 18 |
| Maximum Ratings | 7 | Package Diagrams | 19 |
| Operating Range | 7 | Acronyms | 21 |
| DC Electrical Characteristics | 7 | Document Conventions | 21 |
| Capacitance | 9 | Units of Measure | 21 |
| Thermal Resistance | 9 | Document History Page | 22 |
| AC Test Loads and Waveforms | 9 | Sales, Solutions, and Legal Information | 23 |
| Data Retention Characteristics | 10 | Worldwide Sales and Design Support | 23 |
| Data Retention Waveform | 10 | Products | 23 |
| Switching Characteristics | 11 | PSoC® Solutions | 23 |
| Switching Waveforms | 12 | Cypress Developer Community | 23 |
| Truth Table – CY62167G/CY62167GE | 16 | Technical Support | 23 |
| ERR Output – CY62167GE | 16 | | |

Pin Configuration – CY62167G

Figure 1. 48-ball VFBGA Pinout (Dual Chip Enable without ERR) – CY62167G [3]

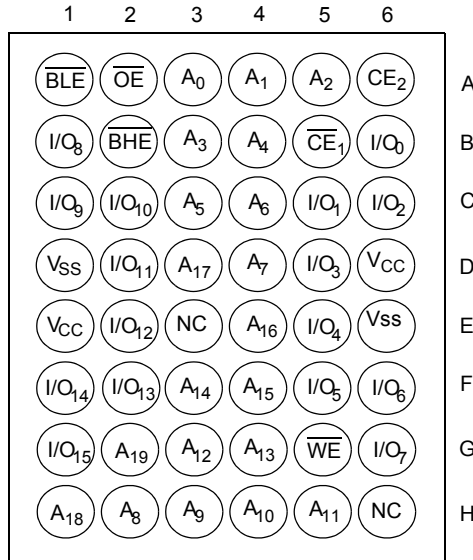


Figure 2. 48-pin TSOP I Pinout (Dual Chip Enable without ERR) – CY62167G [3, 4]



Notes

- 3. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- 4. Tie the BYTE pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, pin 45 is the extra address line A20, while BHE, BLE, and I/O₈ to I/O₁₄ pins are not used and can be left floating.

Pin Configuration – CY62167GE

Figure 3. 48-ball VFBGA Pinout (Single Chip Enable with ERR) – CY62167GE [5, 6]

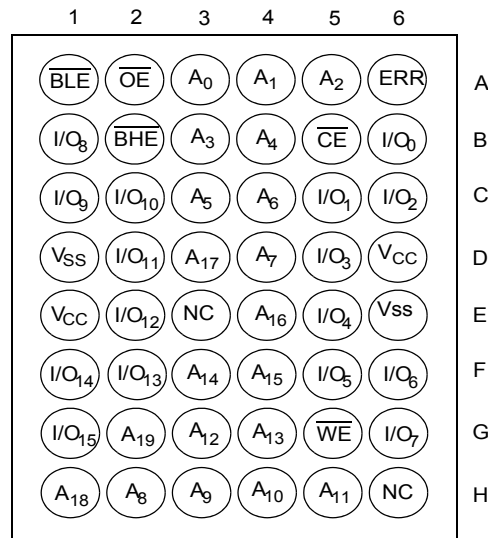
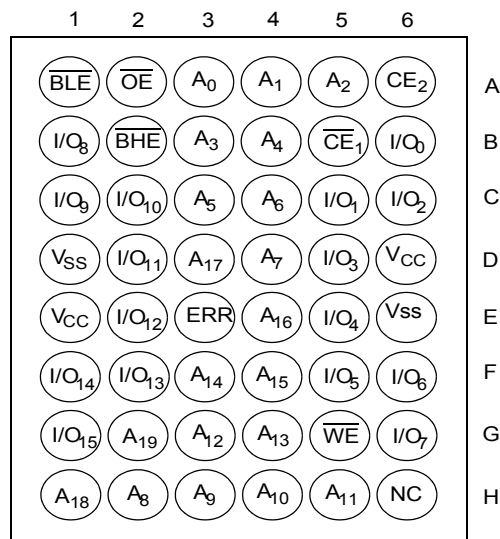


Figure 4. 48-ball VFBGA Pinout (Dual Chip Enable with ERR) – CY62167GE [5, 6]

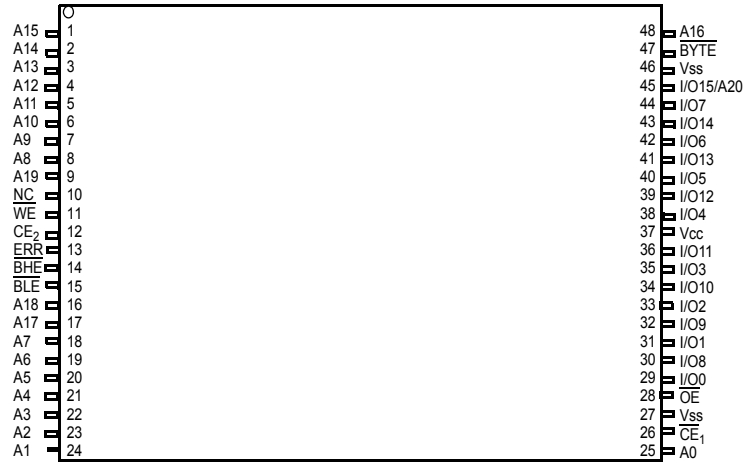


Note

- 5. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- 6. ERR is an Output pin. If not used, this pin should be left floating.

Pin Configuration – CY62167GE (continued)

Figure 5. 48-pin TSOP I Pinout (Dual Chip Enable with ERR) – CY62167GE [7, 8]



Notes

7. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
8. Tie the BYTE pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, pin 45 is the extra address line A20, while the BHE, BLE, and I/O₈ to I/O₁₄ pins are not used and can be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| | |
|--|----------------------------|
| Storage temperature | -65 °C to + 150 °C |
| Ambient temperature with power applied | -55 °C to + 125 °C |
| Supply voltage to ground potential | -0.5 V to $V_{CC} + 0.5$ V |
| DC voltage applied to outputs in High Z state ^[9] | -0.5 V to $V_{CC} + 0.5$ V |

| | |
|---|----------------------------|
| DC input voltage ^[9] | -0.5 V to $V_{CC} + 0.5$ V |
| Output current into outputs (LOW) | 20 mA |
| Static discharge voltage (MIL-STD-883, Method 3015) | >2001 V |
| Latch-up current | >140 mA |

Operating Range

| Grade | Ambient Temperature | V_{CC} ^[10] |
|------------|---------------------|---|
| Industrial | -40 °C to +85 °C | 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V |

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

| Parameter | Description | Test Conditions | 45/55 ns | | | Unit | |
|-----------|-----------------------------------|--|---|--------------------------------|------|----------------|---------|
| | | | Min | Typ ^[11] | Max | | |
| V_{OH} | Output HIGH voltage | 1.65 V to 2.2 V | $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA | 1.4 | - | - | V |
| | | 2.2 V to 2.7 V | $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA | 2.0 | - | - | |
| | | 2.7 V to 3.6 V | $V_{CC} = \text{Min}, I_{OH} = -1.0$ mA | 2.4 | - | - | |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OH} = -1.0$ mA | 2.4 | - | - | |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA | $V_{CC} - 0.4$ ^[12] | - | - | |
| V_{OL} | Output LOW voltage | 1.65 V to 2.2 V | $V_{CC} = \text{Min}, I_{OL} = 0.1$ mA | - | - | 0.2 | |
| | | 2.2 V to 2.7 V | $V_{CC} = \text{Min}, I_{OL} = 0.1$ mA | - | - | 0.4 | |
| | | 2.7 V to 3.6 V | $V_{CC} = \text{Min}, I_{OL} = 2.1$ mA | - | - | 0.4 | |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OL} = 2.1$ mA | - | - | 0.4 | |
| V_{IH} | Input HIGH voltage ^[9] | 1.65 V to 2.2 V | - | 1.4 | - | $V_{CC} + 0.2$ | |
| | | 2.2 V to 2.7 V | - | 1.8 | - | $V_{CC} + 0.3$ | |
| | | 2.7 V to 3.6 V | - | 2.0 | - | $V_{CC} + 0.3$ | |
| | | 4.5 V to 5.5 V | - | 2.2 | - | $V_{CC} + 0.5$ | |
| V_{IL} | Input LOW voltage ^[9] | 1.65 V to 2.2 V | - | -0.2 | - | 0.4 | |
| | | 2.2 V to 2.7 V | - | -0.3 | - | 0.6 | |
| | | 2.7 V to 3.6 V | - | -0.3 | - | 0.8 | |
| | | 4.5 V to 5.5 V | - | -0.5 | - | 0.8 | |
| I_{IX} | Input leakage current | $GND \leq V_{IN} \leq V_{CC}$ | | -1.0 | - | +1.0 | μ A |
| I_{OZ} | Output leakage current | $GND \leq V_{OUT} \leq V_{CC}$, Output disabled | | -1.0 | - | +1.0 | |
| I_{CC} | V_{CC} operating supply current | $V_{CC} = \text{Max}, I_{OUT} = 0$ mA, CMOS levels | f = 22.22 MHz (45 ns) | - | 29.0 | 36.0 | mA |
| | | | f = 18.18 MHz (55 ns) | - | 29.0 | 32.0 | |
| | | | f = 1 MHz | - | 7.0 | 9.0 | |

Notes

- $V_{IL(\text{min})} = -2.0$ V and $V_{IH(\text{max})} = V_{CC} + 2$ V for pulse durations of less than 20 ns.
- Full device AC operation assumes a 100- μ s ramp time from 0 to $V_{CC}(\text{min})$ and 200- μ s wait time after V_{CC} stabilizes to its operational value.
- Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
- This parameter is guaranteed by design and is not tested.

DC Electrical Characteristics (continued)

Over the operating range of -40 °C to 85 °C

| Parameter | Description | Test Conditions | 45/55 ns | | | Unit |
|------------------|--|---|----------|---------------------|------|----------------------|
| | | | Min | Typ ^[11] | Max | |
| $I_{SB1}^{[13]}$ | Automatic Power-down Current – CMOS Inputs; $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$ | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V, } V_{IN} \leq 0.2\text{ V}$, | – | 5.5 | 16.0 | μA |
| | Automatic Power-down Current – CMOS Inputs $V_{CC} = 1.65\text{ V to }2.2\text{ V}$ | $f = f_{\text{max}}$ (address and data only), $f = 0$ (\overline{OE} , and \overline{WE}), $V_{CC} = V_{CC(\text{max})}$ | – | 7.0 | 26.0 | |
| $I_{SB2}^{[13]}$ | Automatic Power-down Current – CMOS Inputs $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$ | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V or }(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V}$, $f = 0, V_{CC} = V_{CC(\text{max})}$ | 25 °C | – | 5.5 | 6.5 ^[14] |
| | | | 40 °C | – | 6.3 | 8.0 ^[14] |
| | | | 70 °C | – | 8.4 | 12.0 ^[14] |
| | | | 85 °C | – | 12.0 | 16.0 |
| | Automatic Power-down Current – CMOS Inputs $V_{CC} = 1.65\text{ V to }2.2\text{ V}$ | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V}$, $f = 0, V_{CC} = V_{CC(\text{max})}$ | – | 7.0 | 26.0 | |

Notes

13. Chip enables (\overline{CE}_1 and CE_2) and \overline{BYTE} must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.
 14. The I_{SB2} maximum limits at 25 °C, 40 °C, and 70 °C are guaranteed by design and not 100% tested.

Capacitance

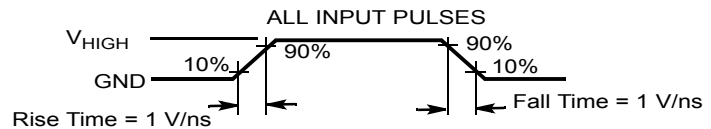
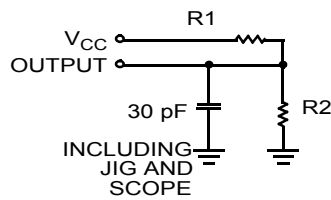
| Parameter ^[15] | Description | Test Conditions | Max | Unit |
|---------------------------|--------------------|---|------|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10.0 | pF |
| C _{OUT} | Output capacitance | | 10.0 | pF |

Thermal Resistance

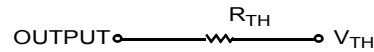
| Parameter ^[15] | Description | Test Conditions | 48-ball VFBGA | 48-pin TSOP I | Unit |
|---------------------------|--|---|---------------|---------------|------|
| Θ _{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 31.50 | 57.99 | °C/W |
| Θ _{JC} | Thermal resistance (junction to case) | | 15.75 | 13.42 | °C/W |

AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



| Parameters | 1.8 V | 2.5 V | 3.0 V | 5.0 V | Unit |
|-------------------|-------|-------|-------|-------|------|
| R1 | 13500 | 16667 | 1103 | 1800 | Ω |
| R2 | 10800 | 15385 | 1554 | 990 | Ω |
| R _{TH} | 6000 | 8000 | 645 | 639 | Ω |
| V _{TH} | 0.80 | 1.20 | 1.75 | 1.77 | V |
| V _{HIGH} | 1.8 | 2.5 | 3.0 | 5.0 | V |

Note

15. Tested initially and after any design or process changes that may affect these parameters.

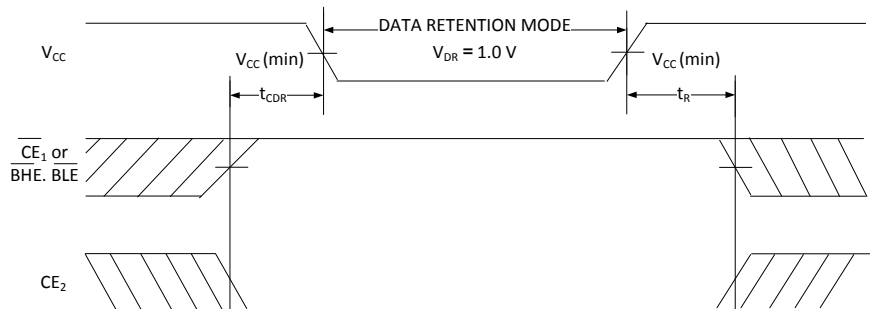
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[16] | Max | Unit |
|--------------------------------|--------------------------------------|--|-------|---------------------|------|---------------|
| V_{DR} | V_{CC} for data retention | – | 1.0 | – | – | V |
| I_{CCDR} ^[17, 18] | Data retention current | $1.2\text{ V} \leq V_{CC} \leq 2.2\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 7.0 | 26.0 | μA |
| | | $2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$ or $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 5.5 | 16.0 | μA |
| t_{CDR} ^[19] | Chip deselect to data retention time | – | 0.0 | – | – | – |
| t_R ^[19, 20] | Operation recovery time | – | 45/55 | – | – | ns |

Data Retention Waveform

Figure 7. Data Retention Waveform^[21]



Notes

16. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
17. Chip enables (\overline{CE}_1 and CE_2) and \overline{BYTE} must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.
18. I_{CCDR} is guaranteed only after the device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR} .
19. These parameters are guaranteed by design and are not tested.
20. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\ \mu\text{s}$ or stable at $V_{CC(min)} \geq 100\ \mu\text{s}$.
21. $\overline{BHE}.\overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

| Parameter ^[22] | Description | 45 ns | | 55 ns | | Unit |
|--|--|-------|------|-------|------|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t_{RC} | Read cycle time | 45.0 | – | 55.0 | – | ns |
| t_{AA} | Address to data valid/Address to ERR valid | – | 45.0 | – | 55.0 | ns |
| t_{OHA} | Data hold from address change/ERR hold from address change | 10.0 | – | 10.0 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid / \overline{CE} LOW to ERR valid | – | 45.0 | – | 55.0 | ns |
| t_{DOE} | \overline{OE} LOW to data valid/ \overline{OE} LOW to ERR valid | – | 22.0 | – | 25.0 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[23, 24] | 5.0 | – | 5.0 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[23, 24, 25] | – | 18.0 | – | 18.0 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[23, 24] | 10.0 | – | 10.0 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to High Z ^[23, 24, 25] | – | 18.0 | – | 18.0 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to power-up ^[26] | 0.0 | – | 0.0 | – | ns |
| t_{PD} | \overline{CE}_1 HIGH and CE_2 LOW to power-down ^[26] | – | 45.0 | – | 55.0 | ns |
| t_{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to data valid | – | 45.0 | – | 55.0 | ns |
| t_{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[23] | 5.0 | – | 5.0 | – | ns |
| t_{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[23, 25] | – | 18.0 | – | 18.0 | ns |
| Write Cycle ^[27, 28] | | | | | | |
| t_{WC} | Write cycle time | 45.0 | – | 55.0 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 35.0 | – | 40.0 | – | ns |
| t_{AW} | Address setup to write end | 35.0 | – | 40.0 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 35.0 | – | 40.0 | – | ns |
| t_{BW} | $\overline{BLE}/\overline{BHE}$ LOW to write end | 35.0 | – | 40.0 | – | ns |
| t_{SD} | Data setup to write end | 25.0 | – | 25.0 | – | ns |
| t_{HD} | Data hold from write end | 0.0 | – | 0.0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[23, 24, 25] | – | 18.0 | – | 20.0 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[23, 24] | 10.0 | – | 10.0 | – | ns |

Notes

22. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use the output loading shown in Figure 6 on page 9, unless specified otherwise.
23. At any temperature and voltage condition, t_{HZOE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
24. Tested initially and after any design or process changes that may affect these parameters.
25. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
26. These parameters are guaranteed by design and are not tested.
27. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
28. The minimum write cycle pulse width for Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 8. Read Cycle No. 1 of CY62167G (Address Transition Controlled) [29, 30]



Figure 9. Read Cycle No. 1 of CY62167GE (Address Transition Controlled) [29, 30]



Notes

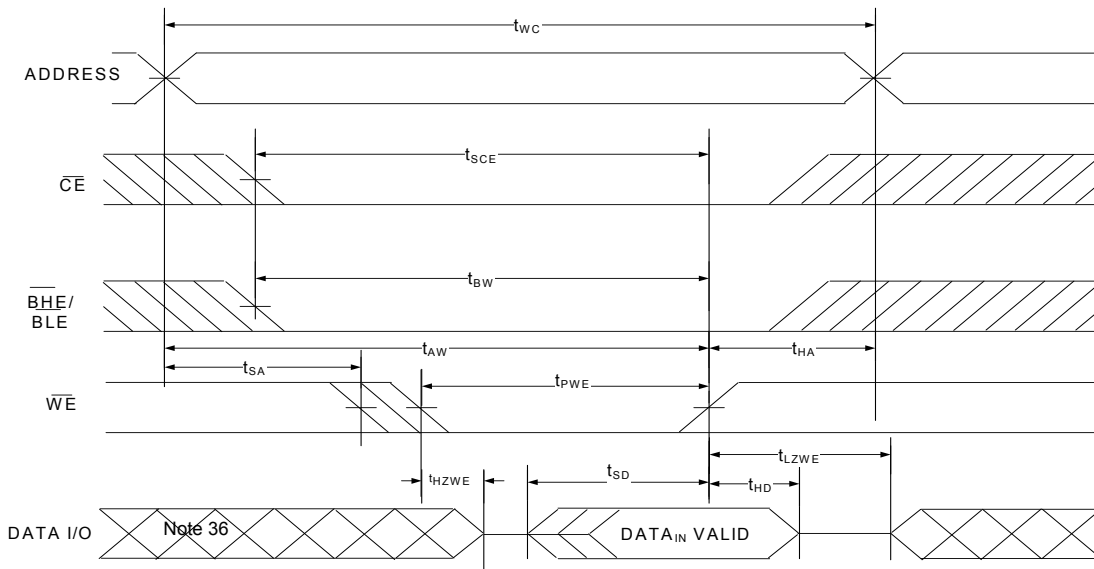
- 29. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} , or both = V_{IL} .
- 30. \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)

Figure 10. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [31, 32, 33, 35]



Figure 11. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [32, 34, 35, 33]

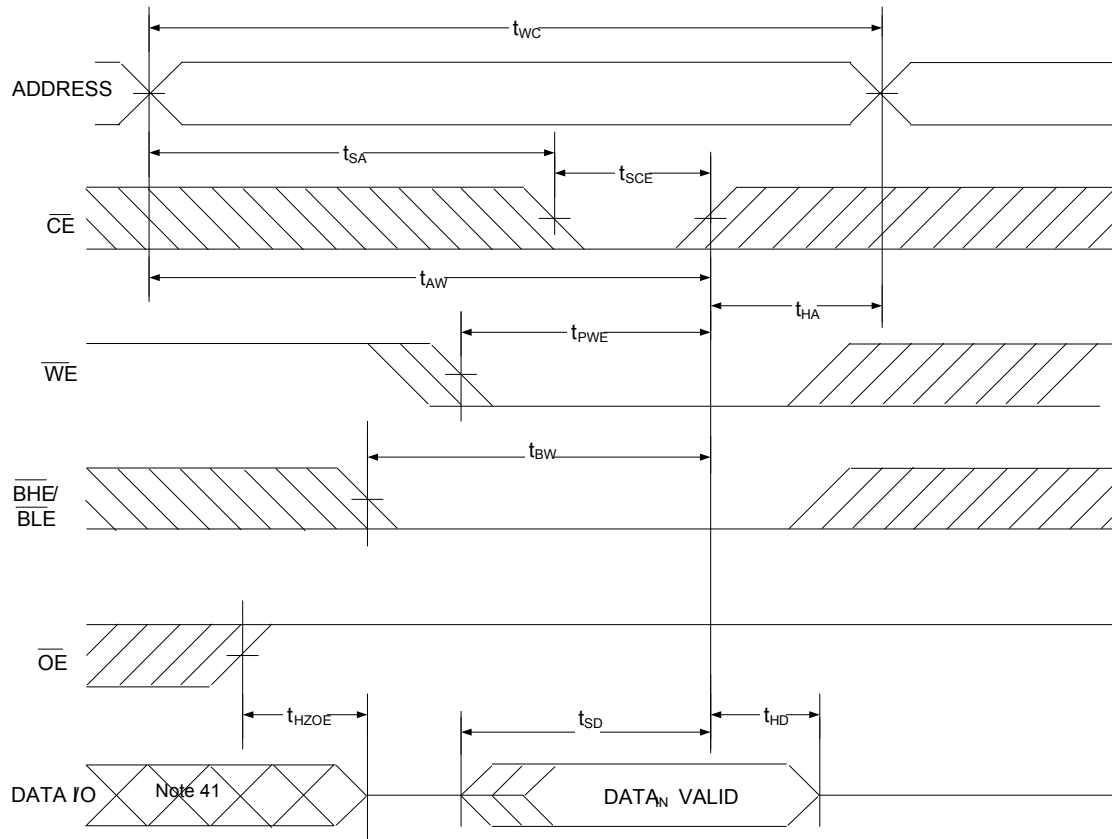


Notes

31. $\overline{\text{WE}}$ is HIGH for read cycle.
32. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
33. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.
34. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}}_1 = V_{IL}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$, or both = V_{IL} , and $\text{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
35. Data I/O is in the high-impedance state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$, or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
36. During this period, the I/Os are in the output state. Do not apply input signals.
37. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms (continued)

Figure 12. Write Cycle No. 2 (\overline{CE} Controlled) [38, 39, 40]



Notes

- 38. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 39. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 40. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
- 41. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW) [42, 43, 44]

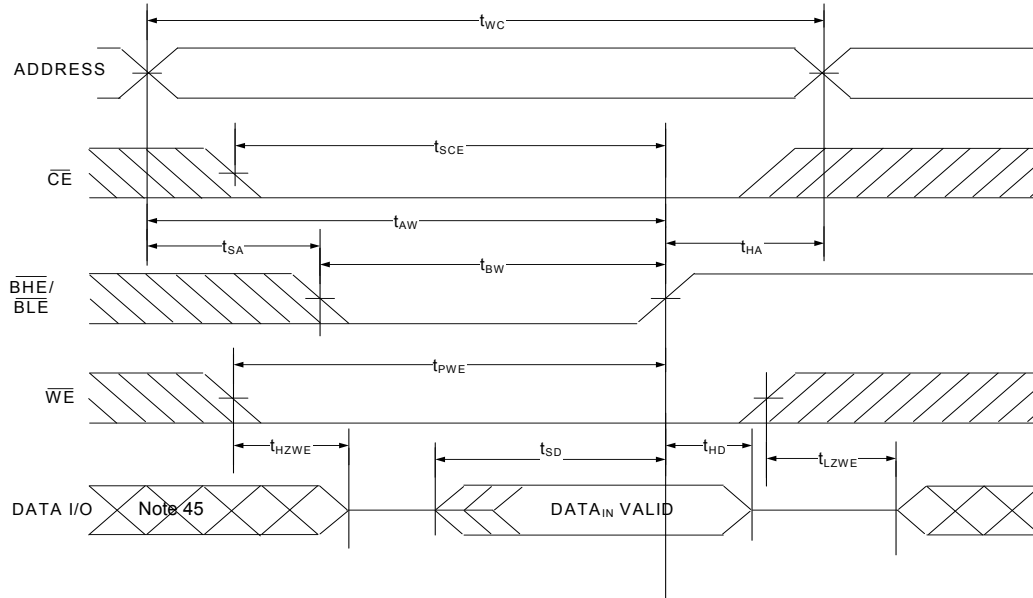


Figure 14. Write Cycle No. 5 ($\overline{\text{WE}}$ Controlled) [42, 43, 44]



Notes

- 42. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
- 43. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{\text{IH}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 44. Data I/O is in the high-impedance state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$, or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
- 45. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table – CY62167G/CY62167GE

| BYTE ^[46] | \overline{CE}_1 | CE_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power | Configuration |
|----------------------|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|----------------|
| X ^[47] | H | X ^[47] | X | X | X | X | High-Z | Deselect/Power-down | Standby (I_{SB}) | 2M × 8/1M × 16 |
| X | X ^[47] | L | X | X | X | X | High-Z | Deselect/Power-down | Standby (I_{SB}) | 2M × 8/1M × 16 |
| X | X ^[47] | X ^[47] | X | X | H | H | High-Z | Deselect/Power-down | Standby (I_{SB}) | 1M × 16 |
| H | L | H | H | L | L | L | Data Out (I/O ₀ –I/O ₁₅) | Read | Active (I_{CC}) | 1M × 16 |
| H | L | H | H | L | H | L | Data Out (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅) | Read | Active (I_{CC}) | 1M × 16 |
| H | L | H | H | L | L | H | High Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅) | Read | Active (I_{CC}) | 1M × 16 |
| H | L | H | H | H | L | H | High-Z | Output disabled | Active (I_{CC}) | 1M × 16 |
| H | L | H | H | H | H | L | High-Z | Output disabled | Active (I_{CC}) | 1M × 16 |
| H | L | H | H | H | L | L | High-Z | Output disabled | Active (I_{CC}) | 1M × 16 |
| H | L | H | L | X | L | L | Data In (I/O ₀ –I/O ₁₅) | Write | Active (I_{CC}) | 1M × 16 |
| H | L | H | L | X | H | L | Data In (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅) | Write | Active (I_{CC}) | 1M × 16 |
| H | L | H | L | X | L | H | High-Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅) | Write | Active (I_{CC}) | 1M × 16 |
| L | L | H | H | L | X | X | Data Out (I/O ₀ –I/O ₇) | Read | Active (I_{CC}) | 2M × 8 |
| L | L | H | H | H | X | X | High-Z | Output disabled | Active (I_{CC}) | 2M × 8 |
| L | L | H | L | X | X | X | Data In (I/O ₀ –I/O ₇) | Write | Active (I_{CC}) | 2M × 8 |

ERR Output – CY62167GE

| Output ^[48] | Mode |
|------------------------|--|
| 0 | Read operation, no single-bit error in the stored data. |
| 1 | Read operation, single-bit error detected and corrected. |
| High-Z | Device deselected / outputs disabled / Write operation |

Notes

46. This pin is available only in the 48-pin TSOP I package. Tie the \overline{BYTE} to V_{CC} to configure the device in the 1M × 16 option. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the \overline{BYTE} signal to V_{SS} .

47. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

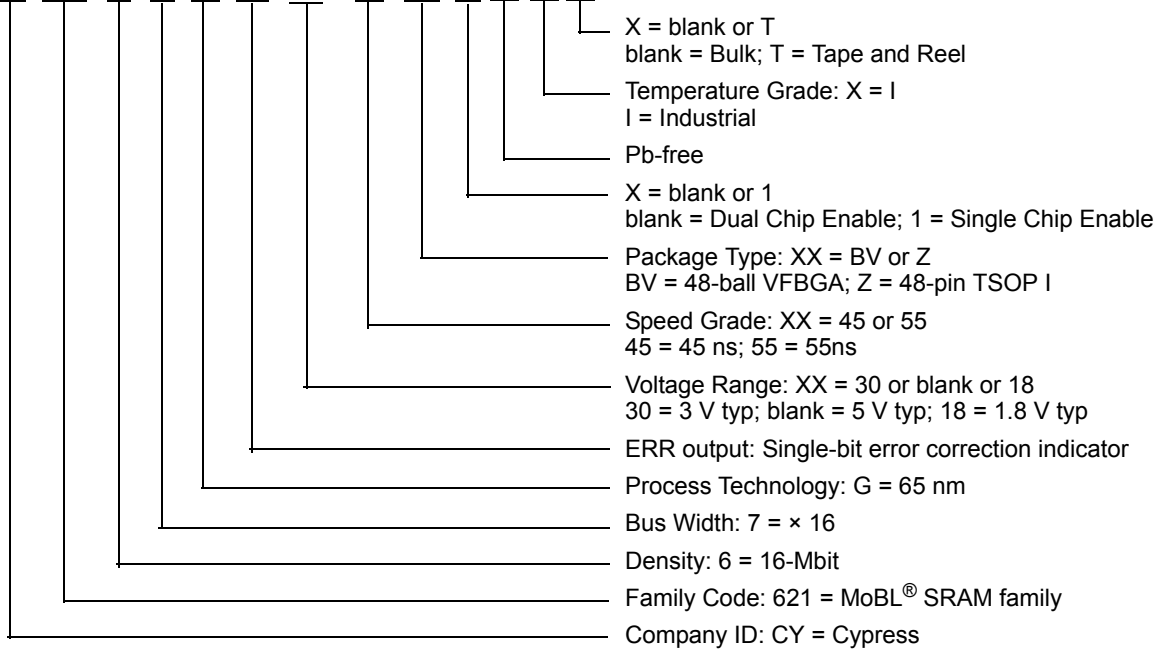
48. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type (all Pb-free) | Key Features / Differentiators | ERR Pin / Ball | Operating Range | | |
|------------------|-------------------|----------------------|-----------------|----------------------------|--------------------------------|-----------------|-----------------|------------------|-----|
| 45 | 2.2 V–3.6 V | CY62167GE30-45BV1XI | 51-85150 | 48-ball VFBGA | Sing Chip Enable | Yes | Industrial | | |
| | | CY62167GE30-45BV1XIT | | | Dual Chip Enable | Yes | | | |
| | | CY62167GE30-45BVXI | | | | No | | | |
| | | CY62167GE30-45BVXIT | | | | | | | |
| | | CY62167G30-45BVXI | | | | | | | |
| | | CY62167G30-45BVXIT | | | | | | | |
| | | CY62167GE30-45ZXI | | | 51-85183 | 48-pin TSOP I | | Dual Chip Enable | Yes |
| | | CY62167GE30-45ZXIT | | | | | | No | |
| | CY62167G30-45ZXI | | | | | | | | |
| | CY62167G30-45ZXIT | | | | | | | | |
| | 4.5 V–5.5 V | CY62167G-45BVXI | 51-85150 | 48-ball VFBGA | Dual Chip Enable | No | | | |
| | | | | | | | | CY62167G-45BVXIT | |
| CY62167G-45ZXI | | 51-85183 | 48-pin TSOP I | Dual Chip Enable | No | | | | |
| | | | | | | CY62167G-45ZXIT | | | |
| CY62167GE-45ZXI | | | Yes | | | | | | |
| CY62167GE-45ZXIT | | | | | | | | | |
| 55 | 1.65 V–2.2 V | CY62167GE18-55BVXI | 51-85150 | 48-ball VFBGA | Dual Chip Enable | Yes | | | |
| | | CY62167GE18-55BVXIT | | | | No | | | |
| | | CY62167G18-55BVXI | | | | | | | |
| | | CY62167G18-55BVXIT | | | | | | | |
| | | CY62167G18-55ZXI | 51-85183 | 48-pin TSOP I | No | | | | |
| | | CY62167G18-55ZXIT | | | | | | | |

Ordering Code Definitions

CY 621 6 7 G E XX - XX XX X X X X



Package Diagrams

Figure 15. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150

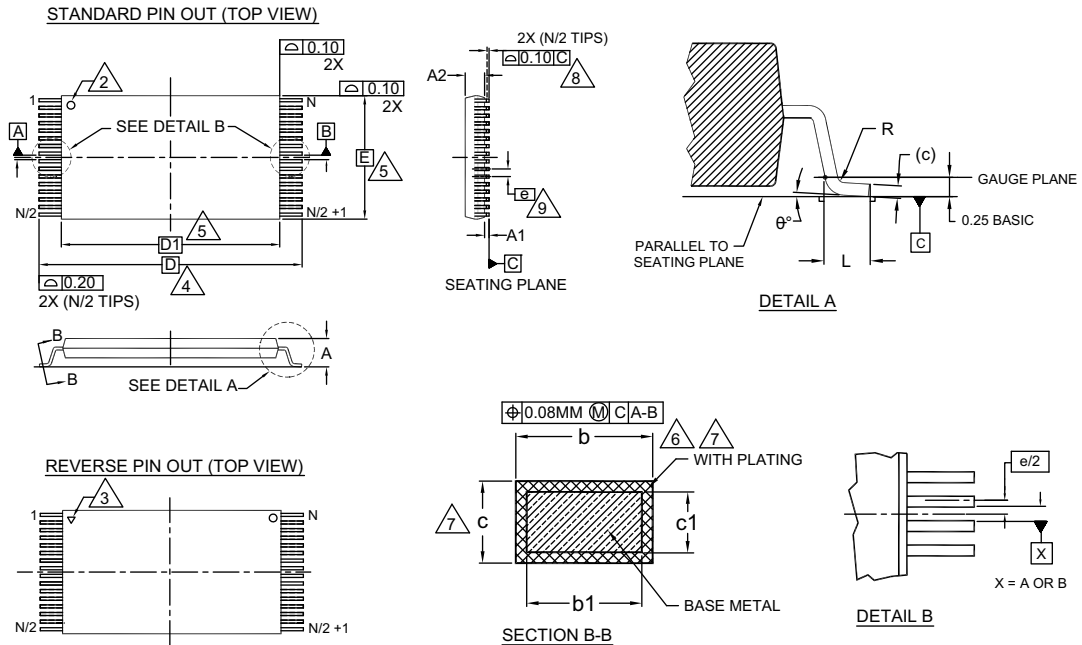


NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
 posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 16. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



| SYMBOL | DIMENSIONS | | |
|--------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 20.00 BASIC | | |
| D1 | 18.40 BASIC | | |
| E | 12.00 BASIC | | |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8 |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN); INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

| Acronym | Description |
|-------------------------|---|
| $\overline{\text{BHE}}$ | Byte High Enable |
| $\overline{\text{BLE}}$ | Byte Low Enable |
| $\overline{\text{CE}}$ | Chip Enable |
| CMOS | Complementary metal oxide semiconductor |
| I/O | Input/output |
| $\overline{\text{OE}}$ | Output Enable |
| SRAM | Static random access memory |
| TSOP | Thin small outline package |
| VFBGA | Very fine-pitch ball grid array |
| $\overline{\text{WE}}$ | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY62167G/CY62167GE MoBL®, 16-Mbit (1M words × 16-bit/2M words × 8-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81537 | | | | |
|--|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| *M | 4791835 | NILE | 06/15/2015 | Changed status from Preliminary to Final. |
| *N | 5027105 | NILE | 11/25/2015 | Updated DC Electrical Characteristics : Changed minimum value of V_{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V” and Test Condition “ $V_{CC} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$ ”. |
| *O | 5439177 | VINI | 09/16/2016 | Updated DC Electrical Characteristics : Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Note 9 (Replaced 2 ns with 20 ns). Updated Ordering Information : Updated part numbers. Updated Ordering Code Definitions . Updated to new template. |
| *P | 5751153 | VINI | 05/26/2017 | Updated Package Diagrams : spec 51-85183 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|-------------------------------|--|
| ARM® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2012–2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А