

DUAL LOW VOLTAGE POWER AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2073 is a monolithic integrated circuit in 8 lead dual-in-line package, which is designed for dual audio power amplifier in portable radio and handy cassette player.

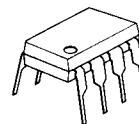
■ FEATURES

- Operating Voltage
- Low Crossover Distortion
- Low Operating Current
- Bridge or Stereo Configuration
- No Turn-on Noise
- Package Outline
- Bipolar Technology

($V^+ = 1.8V \sim 15V$)

DIP8, DMP8

■ PACKAGE OUTLINE

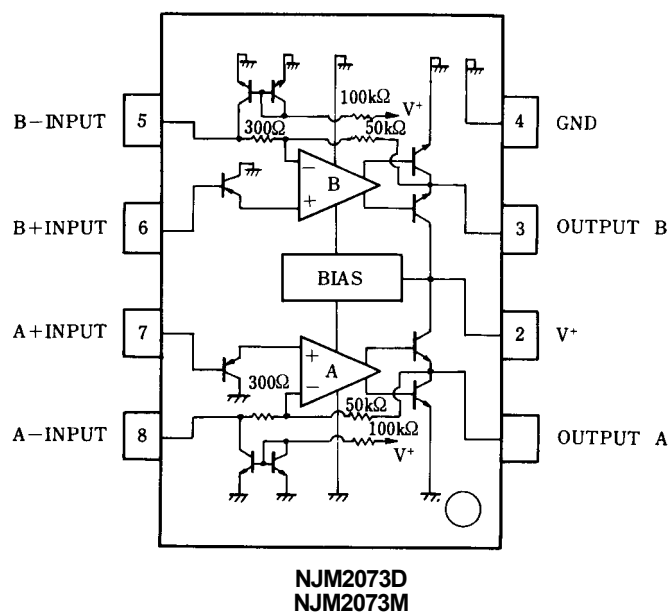


NJM2073D



NJM2073M

■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Output Peak Current	I_{OP}	1	A
Power Dissipation	P_D	(DIP8) 700 (DMP8) 300	mW
Input Voltage Range	V_{IN}	± 0.4	V
Operating Temperature Range	T_{opr}	-40~+85	°C
Storage Temperature Range	T_{stg}	-40~+125	°C

■ ELECTRICAL CHARACTERISTICS D-Type

(1) BTL Configuration (Test Circuit Fig.1)

($V^+=6V, Ta=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	-	15	V
Operating Current	I_{CC}	$R_L = \infty$	-	6	9	mA
Output Offset Voltage (Between the Outputs)	ΔV_O	$R_L = 8\Omega$	-	10	50	mV
Input Bias Current	I_B		-	100	-	nA
Output Power	P_O	THD=10%, f=1kHz	-	2.0	-	W
	P_O	$V^+=9V, R_L=16\Omega$ (Note)	-	1.2	-	W
	P_O	$V^+=6V, R_L=8\Omega$ (Note)	0.9	0.6	-	W
	P_O	$V^+=4.5V, R_L=8\Omega$	-	0.8	-	W
	P_O	$V^+=4.5V, R_L=4\Omega$ (Note)	-	200	-	mW
	P_O	$V^+=3V, R_L=4\Omega$	-	80	-	mW
	P_O	$V^+=2V, R_L=4\Omega$	-	-	-	-
	P_O	THD=1%, f=40Hz~15kHz	-	1.0	-	W
	P_O	$V^+=6V, R_L=8\Omega$	-	0.6	-	W
	P_O	$V^+=4.5V, R_L=4\Omega$	-	0.2	-	%
Total Harmonic Distortion	THD	$P_O=0.5W, R_L=8\Omega, f=1kHz$	-	44	47	dB
Close Loop Voltage Gain	A_V	f=1kHz	41	-	-	k Ω
Input Impedance	Z_{IN}	f=1kHz	100	-	-	μV
Equivalent Input Noise Voltage	V_{NI1}	$R_S=10k\Omega, A$ Curve	-	2	-	μV
	V_{NI2}	$R_S=10k\Omega, B=22Hz\sim 22kHz$	-	2.5	-	dB
Ripple Rejection	RR	f=100Hz	-	40	-	kHz
Cutoff Frequency	f_H	$A_V=-3dB$ from f=1kHz, $R_L=8\Omega, P_O=1W$	-	130	-	-

(Note) At on PC Board

(2) Stereo Configuration (Test Circuit Fig.2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	-	15	V
Output Voltage	V_O		-	2.7	-	V
Operating Current	I_{CC}	$R_L = \infty$	-	6	9	mA
Input Bias Current	I_B		-	100	-	nA
Output Power (Each Channel)		THD=10%, f=1kHz				
	P_O	$V^+ = 6V, R_L = 4\Omega$ (Note)	0.5	0.65	-	W
	P_O	$V^+ = 4.5V, R_L = 4\Omega$	-	0.32	-	W
	P_O	$V^+ = 3V, R_L = 4\Omega$	-	120	-	mW
	P_O	$V^+ = 2V, R_L = 4\Omega$	-	30	-	mW
		THD=1%, f=1kHz				
	P_O	$V^+ = 6V, R_L = 4\Omega$	-	500	-	mW
	P_O	$V^+ = 4.5V, R_L = 4\Omega$	-	250	-	mW
Total Harmonic Distortion	THD	$P_O = 0.4W, R_L = 4\Omega, f = 1kHz$	-	0.25	-	%
Voltage Gain	A_V	f=1kHz	41	44	47	dB
Channel Balance	ΔA_V		-	-	± 1	dB
Input Impedance	Z_{IN}	f=1kHz	100	-	-	k Ω
Equivalent Input Noise Voltage	V_{NI1}	$R_S = 10k\Omega, A$ Curve	-	2.5	-	μV
	V_{NI2}	$R_S = 10k\Omega, B = 22Hz \sim 22kHz$	-	3	-	μV
Ripple Rejection	RR	f=100Hz, $C_X = 100\mu F$	24	30	-	dB
Cutoff Frequency	f_H	$A_V = -3dB$ from f=1kHz, $R_L = 8\Omega, P_O = 250mW$	-	200	-	kHz

(Note) At on PC Board

■ ELECTRICAL CHARACTERISTICS M-Type

(1) BTL Configuration (Test Circuit Fig.1)

($V^+ = 6V, T_a = 25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	-	15	V
Operating Current	I_{CC}	$R_L = \infty$	-	6	9	mA
Output Offset Voltage	ΔV_O	$R_L = 8\Omega$	-	10	50	mV
(Between the Outputs)						
Input Bias Current	I_B		-	100	-	nA
Output Power		THD=10%, f=1kHz				
	P_O	$V^+ = 6V, R_L = 16\Omega$ (Note)	-	0.8	-	W
	P_O	$V^+ = 4V, R_L = 8\Omega$ (Note)	350	460	-	mW
	P_O	$V^+ = 3V, R_L = 4\Omega$ (Note)	200	300	-	mW
	P_O	$V^+ = 2V, R_L = 4\Omega$	-	80	-	mW
		THD=1%, f=40Hz~15kHz				
	P_O	$V^+ = 4V, R_L = 8\Omega$	-	380	-	mW
Total Harmonic Distortion	THD	$V^+ = 4V, R_L = 8\Omega, P_O = 200mW, f = 1kHz$	-	0.2	-	%
Close Loop Voltage Gain	A_V	f=1kHz	41	44	47	dB
Input Impedance	Z_{IN}	f=1kHz	100	-	-	k Ω
Equivalent Input Noise Voltage	V_{NI1}	$R_S = 10k\Omega, A$ Curve	-	2	-	μV
	V_{NI2}	$R_S = 10k\Omega, B = 22Hz \sim 22kHz$	-	2.5	-	μV
Ripple Rejection	RR	f=100Hz	-	40	-	dB
Cutoff Frequency	f_H	$A_V = -3dB$ from f=1kHz, $R_L = 16\Omega, P_O = 0.5W$	-	130	-	kHz

(Note) At on PC Board

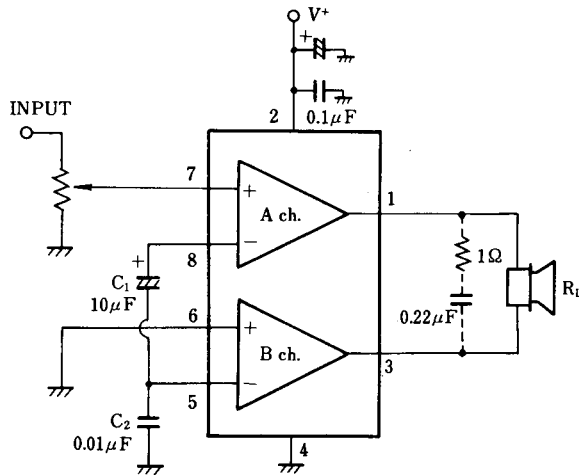
(2) Stereo Configuration (Test Circuit Fig.2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	-	15	V
Output Voltage	V_O		-	2.7	-	V
Operating Current	I_{CC}	$R_L = \infty$	-	6	9	mA
Input Bias Current	I_B		-	100	-	nA
Output Power (Each Channel)	P_O	THD=10%, f=1kHz $V^+=6V, R_L=16\Omega$	-	240	-	mW
	P_O	$V^+=5V, R_L=8\Omega$ (Note)	-	270	-	mW
	P_O	$V^+=4V, R_L=4\Omega$ (Note)	180	250	-	mW
	P_O	$V^+=3V, R_L=4\Omega$	-	120	-	mW
	P_O	$V^+=2V, R_L=4\Omega$	-	30	-	mW
	P_O	THD=1%, f=1kHz $V^+=4V, R_L=4\Omega$	-	180	-	mW
Total Harmonic Distortion	THD	$V^+=4V, R_L=4\Omega, P_O=150mW, f=1kHz$	-	0.25	-	%
Voltage Gain	A_V	f=1kHz	41	44	47	dB
Channel Balance	ΔA_V		-	-	± 1	dB
Input Impedance	Z_{IN}	f=1kHz	100	-	-	k Ω
Equivalent Input Noise Voltage	V_{NI1}	$R_S=10k\Omega, A$ Curve	-	2.5	-	μV
	V_{NI2}	$R_S=10k\Omega, B=22Hz\sim 22kHz$	-	3	-	μV
Ripple Rejection	RR	f=100Hz, $C_X=100\mu F$	24	30	-	dB
Cutoff Frequency	f_H	$A_V=-3dB$ from f=1kHz, $R_L=16\Omega, P_O=125mW$	-	200	-	kHz

(Note) At on PC Board

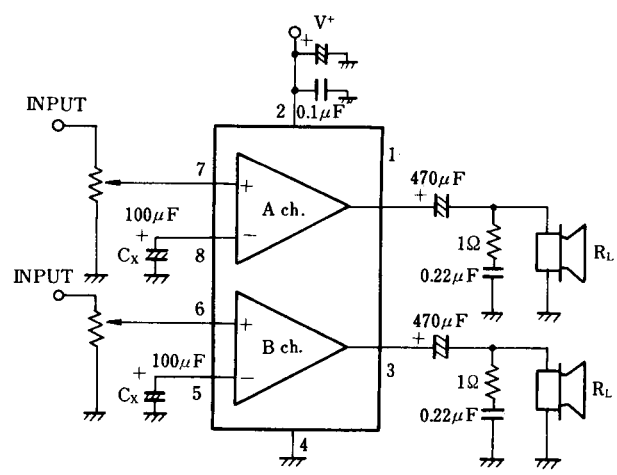
■ TYPICAL APPLICATION & TEST CIRCUIT

Fig.1 BTL Configuration



note: pin No. to D, M-Type

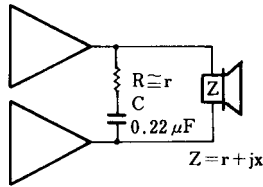
Fig.2 Stereo Configuration



■ PARASTIC OSCILLATION PREVENTING CIRCUIT

Put $1\Omega + 0.22\mu\text{F}$ on parallel to load, if the load is speaker. Recommend putting $0.1\mu\text{F}$ and more than $100\mu\text{F}$ capacitors with good high frequency characteristics in to near ground and supply voltage pins.

In BTL operation of less than 2V supply voltage, parastic oscillation may be occurred with $R=1\Omega$. And so recommended R to be the same value of pure resistance(r) when it is lower than 3V.



■ MUTING CIRCUIT

When Mute ON, OUTPUT level saturates to GND side.

Fig.3 BTL Configuration

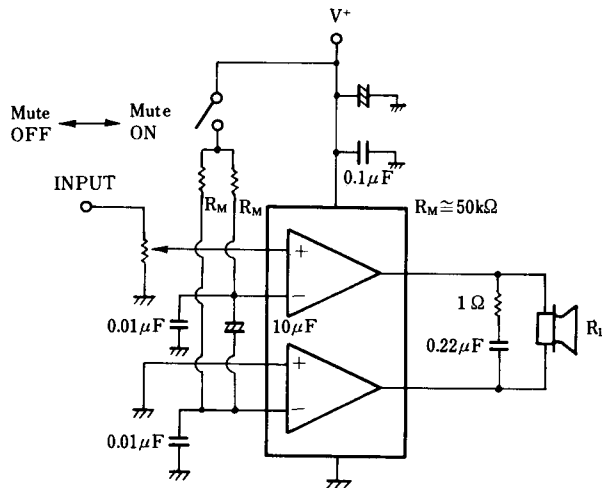
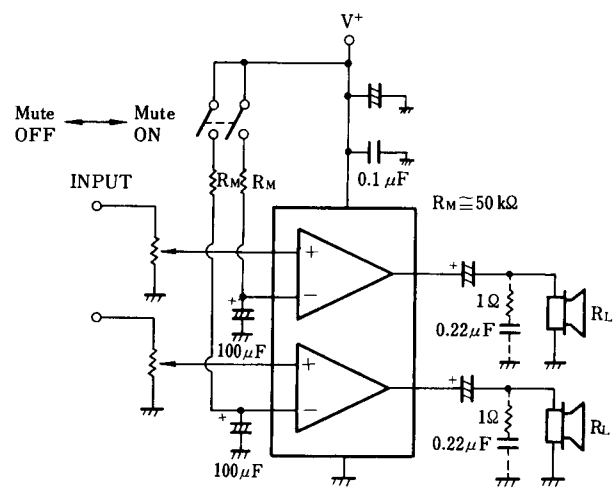


Fig.4 Stereo Configuration



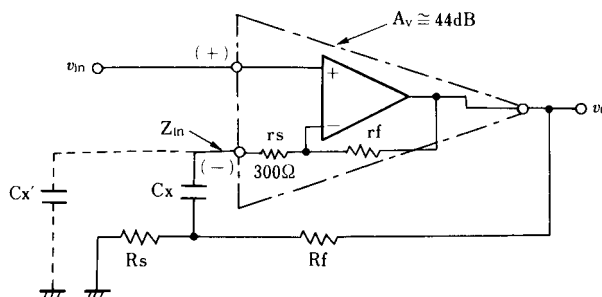
■ VOLTAGE GAIN REDUCTION APPLICATION EXAMPLE

(1) Outline of way to further Reduction

NJM2073 by taking in assumption, as one of OP-AMP (Gain 44dB, minus input impedance about 300Ω), to feedback from output to minus input helps to get reduction of stabilized Voltage Gain. Fig.5 indicates the model example.

Here is the point to be noticed that, in order to get the appropriate output Bias Voltage, it is important to keep the minus input floating as DC condition, (inserting C_X), and also that when extended too much reduction of Gain might cause Oscillation due to high band phase margin. The reduction of voltage gain is limited at around 26dB (20 times), and when oscillation, it is necessary to attach the oscillation stopper. Please examine the C_X value accordingly to the application requirement.

Fig.5 Model of Voltage Gain Reduction



$$A_v = \frac{v_o}{v_{in}} \cong \frac{R_s + R_f}{R_s + \frac{R_s + R_f}{A_v} + \frac{R_s \times R_f}{160 \times 300}} \quad \left(\frac{160}{A_v} \right) (Z_{in})$$

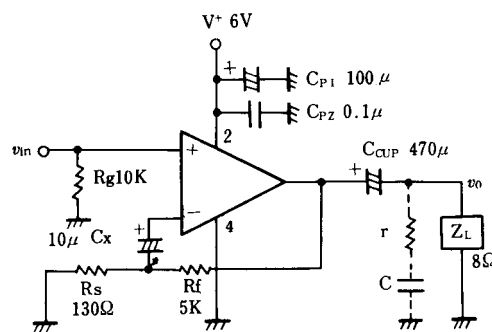
(2) The Application Example of Voltage Gain Reduction. (STEREO)

Fig.6 indicates the application example and Table1 indicates the recommendable value of parts to be attached externally.

Table1,Applying purpose and Recommended Value of Externally parts to be attached.

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_g	Plus input to be grounded by fixed DC	Under about 100k Ω	Catch the noise when much higher.
R_s	AV shall be decided with R_f	-	
R_f	AV shall be decided with R_s	About 5k Ω	The co-temperature of AV becomes higher in case when R_s is higher resistance.The current from output pin to GND becomes higher,in case when R_s is lower resistance.(The current sinks in vain.)
C_x	Minus input to be grounded by fixed DC	-	Low-band Cut off frequency (fL) is to be decided. The rise time becomes longer in case that C_x is big.
C_{CUP}	Output DC Decoupling	When $R_L=8\Omega$,More than 220 μ F	fL shall be decided by C_{CUP} and Z_L .
C_{P1}	Stabilization of V^+	More than about C_{CUP}	Inserting near around V^+ pin and GND pin.
C_{P2}	Prevention of Oscillation	More than 0.1 μ F	
r	Prevention of Oscillation	About R_L	Inserting near around V^+ pin and GND pin.
C	Prevention of Oscillation	0.22 μ F	To be examined by about the resistor volume of the speaker load.

Fig.6 STEREO Application Example.



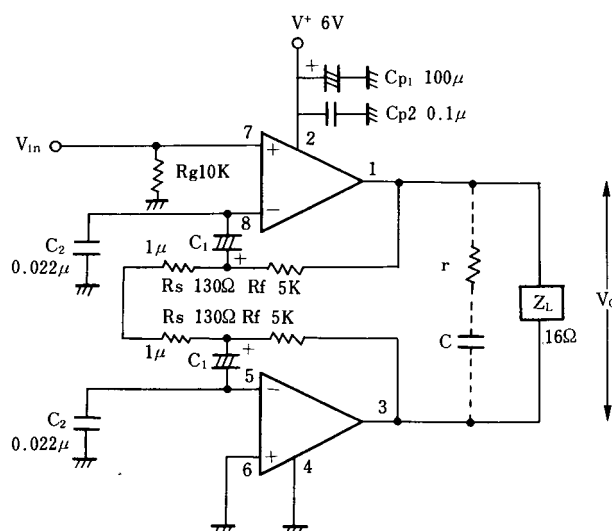
● Application for Voltage Gain Reduction (BTL)

Fig.7 indicates the application example, Table2 shows recommended value of externally attaching parts.

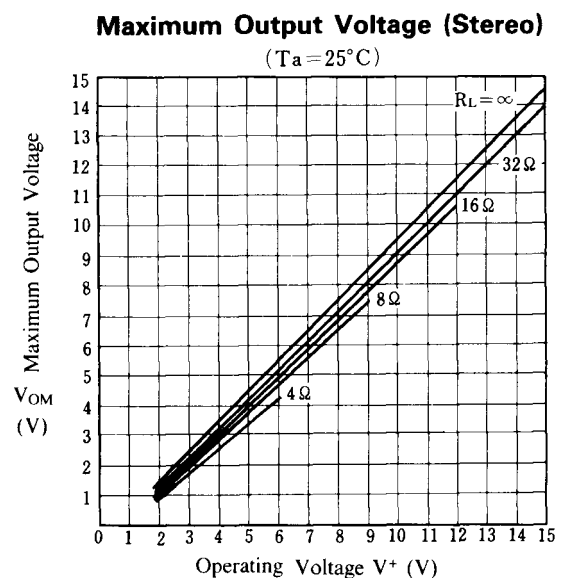
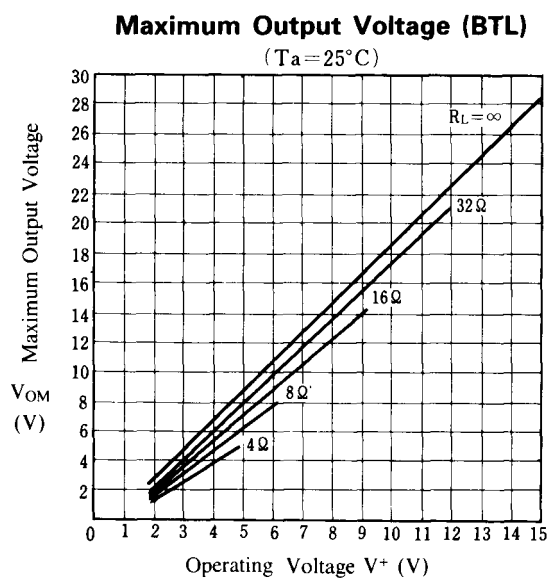
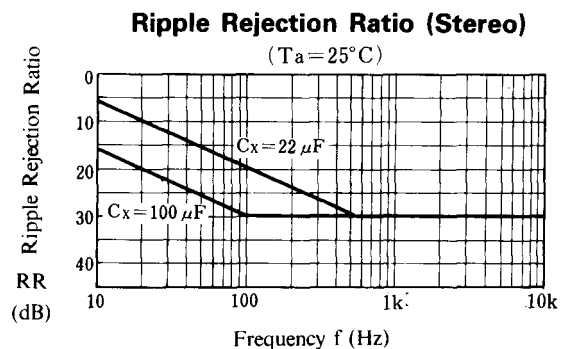
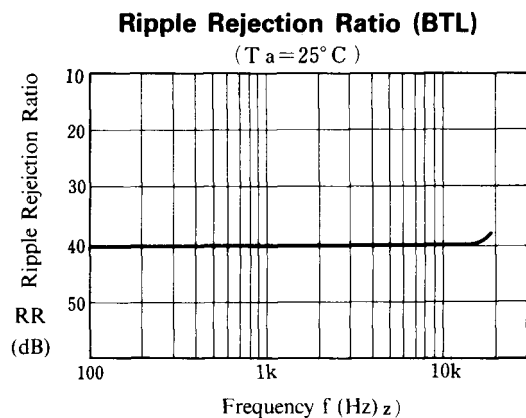
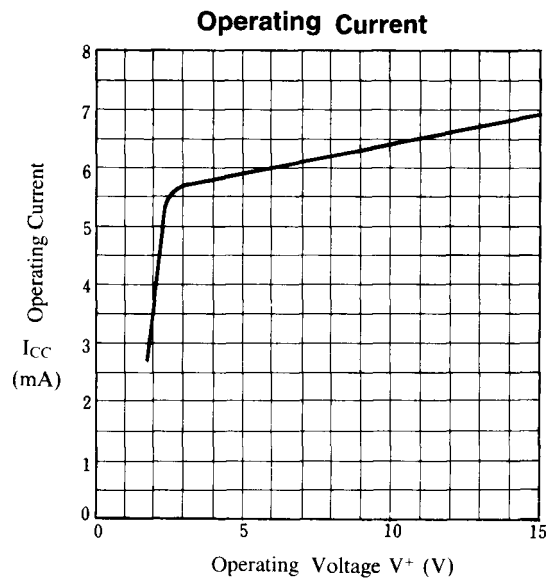
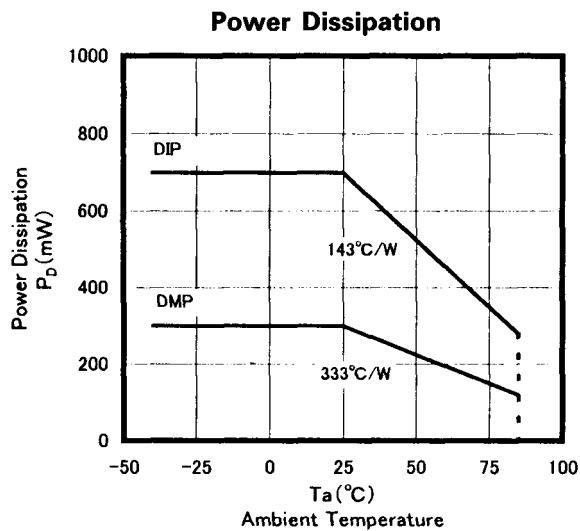
Table2 Applying purpose and Recommended Value of External Part

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_g	DC condition ground of plus input	Below about 10k Ω	Making noise when higher.
R_s	AV shall be decided with R_f	-	
R_f	AV shall be decided with R_s	About 5k Ω	Temperature feature to be increased accordingly as in higher AV value. When lower, to be trended of Oscillation.
C_1	Releasing minus input in to DC condition	-	Setting up low band Cut-off frequency (fL). More higher, the rise time become longer.
C_2	Preventing Oscillation	About 0.02 μ F	The more higher in value, the high band THD, due to phase slipping to be deteriorated. When lower, to be trended of oscillation.
C_{P1}	Stability of V^+ Preventing Oscillation	More than about 100 μ F	Inserting near around at V^+ and the GND pin.
C_{P2}	Preventing Oscillation	More than 0.1 μ F	Inserting near around at V^+ and the GND pin.
r	Preventing Oscillation	About R_L	To be examined at around pure resistor Value of speaker load.
C	Preventing Oscillation	0.22 μ F	

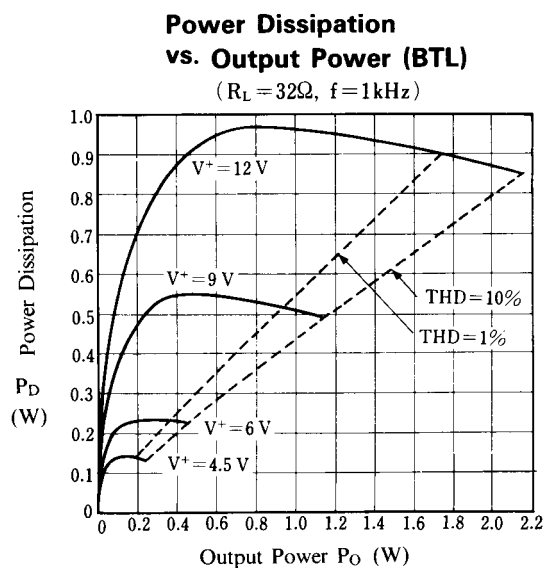
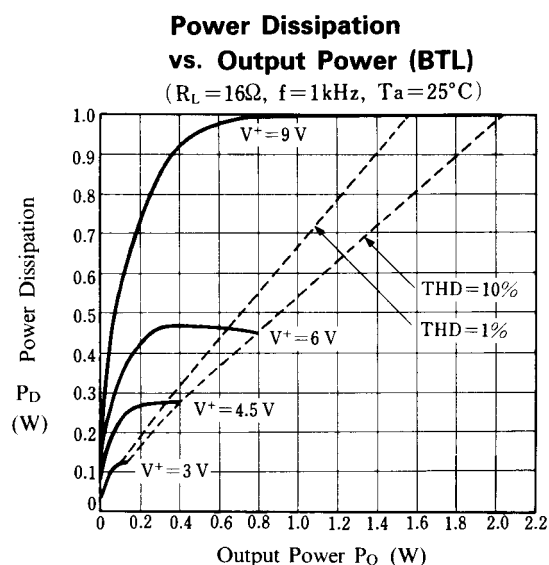
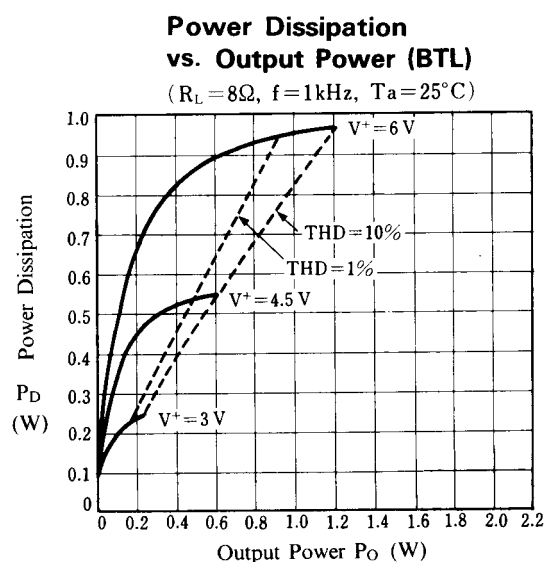
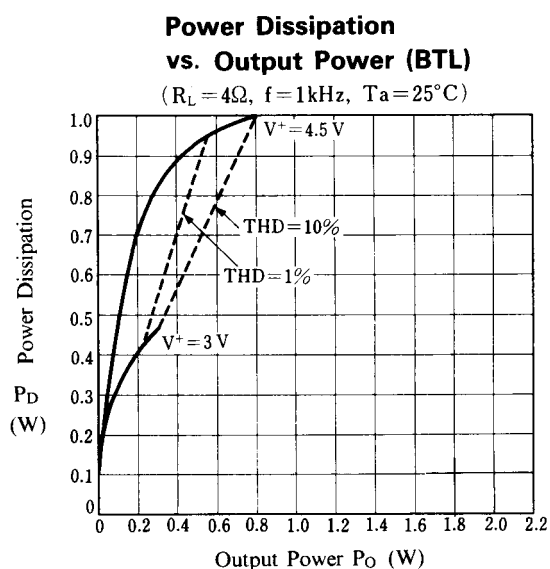
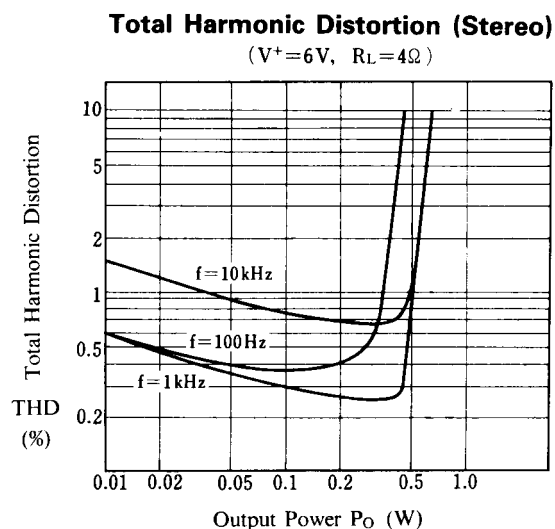
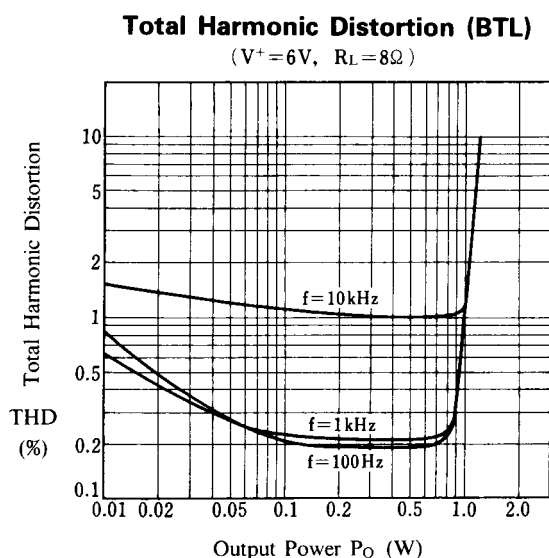
Fig.7 BTL Application



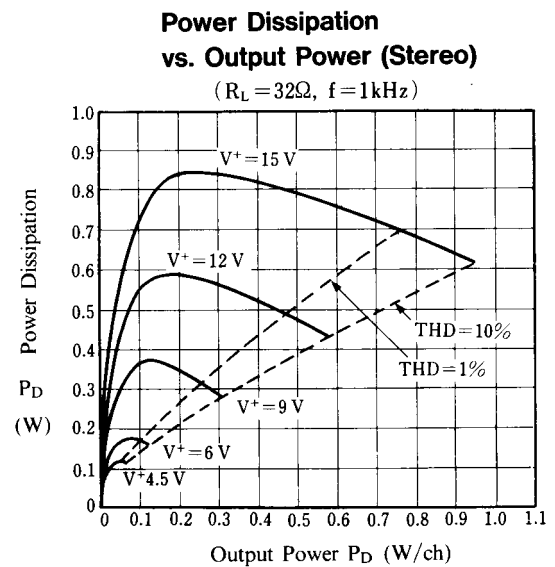
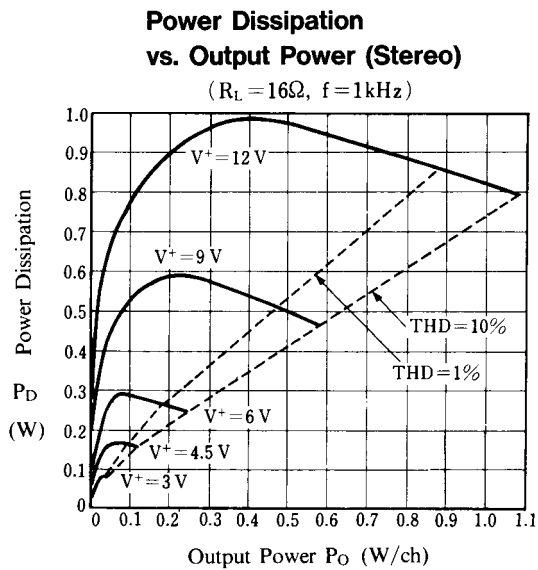
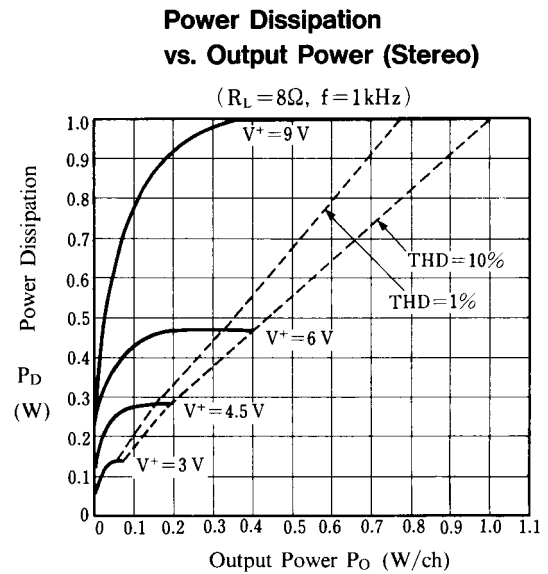
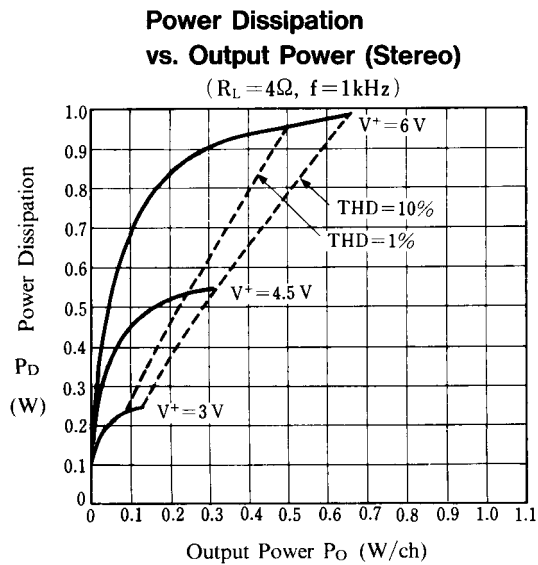
■ TYPICAL CHARACTERISTICS



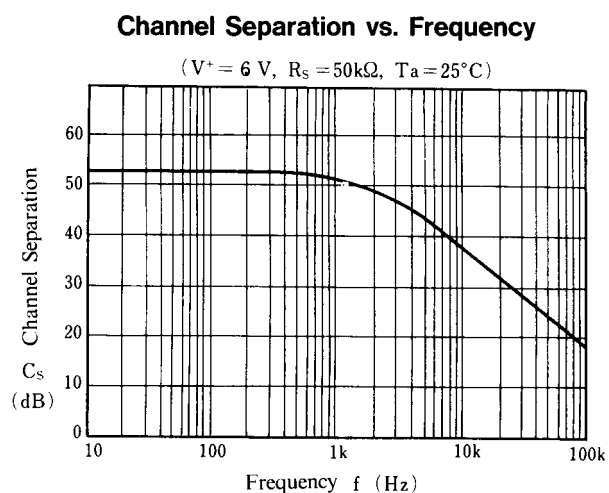
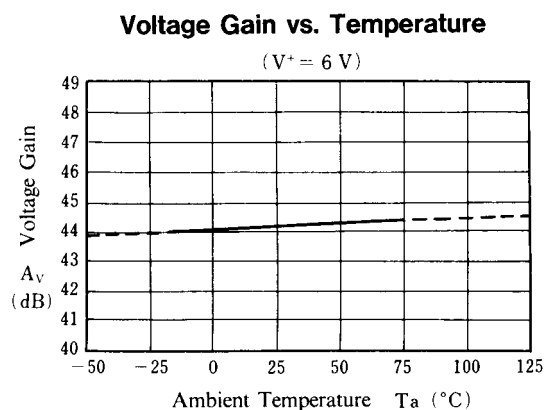
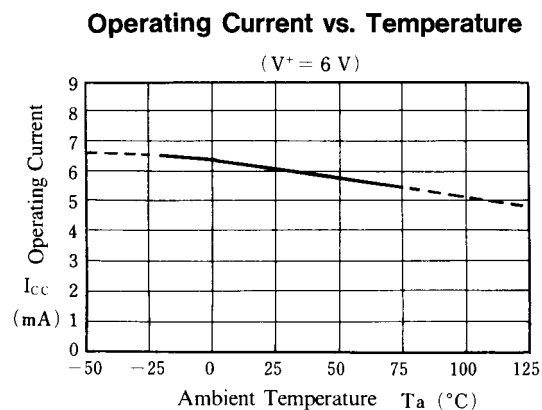
■ TYPICAL CHARACTERISTICS



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■ TYPICAL CHARACTERISTICS



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