PRELIMINARY

T-49-19-07

# MCS®-51
# 8-BIT CONTROL-ORIENTED MICROCOMPUTERS
# 8031/8051
# 8031AH/8051AH
# 8032AH/8052AH
# 8751H/8751H-8

- High Performance HMOS Process
- Internal Timers/Event Counters
- 2-Level Interrupt Priority Structure
- 32 I/O Lines (Four 8-Bit Ports)
- 64K Program Memory Space
- Security Feature Protects EPROM Parts Against Software Piracy
- Boolean Processor
- Bit-Addressable RAM
- Programmable Full Duplex Serial Channel
- 111 Instructions (64 Single-Cycle)
- 64K Data Memory Space

The MCS®-51 products are optimized for control applications. Byte-processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for one-bit variables as a separate data type, allowing direct bit manipulation and testing in control and logic systems that require Boolean processing.

The 8051 is the original member of the MCS-51 family. The 8051AH is identical to the 8051, but it is fabricated with HMOS II technology.

The 8751H is an EPROM version of the 8051AH; that is, the on-chip Program Memory can be electrically programmed, and can be erased by exposure to ultraviolet light. It is fully compatible with its predecessor, the 8751-8, but incorporates two new features: a Program Memory Security bit that can be used to protect the EPROM against unauthorized read-out, and a programmable baud rate modification bit (SMOD). The 8751H-8 is identical to the 8751H but only operates up to 8 MHz.

The 8052AH is an enhanced version of the 8051AH. It is backwards compatible with the 8051AH and is fabricated with HMOS II technology. The 8052AH enhancements are listed in the table below. Also refer to this table for the ROM, ROMless, and EPROM versions of each product.

| Device | Internal Memory | | Timers/ Event Counters | Interrupts |
|---|---|---|---|---|
| | Program | Data | | |
| 8052AH | 8K x 8 ROM | 256 x 8 RAM | 3 x 16-Bit | 6 |
| 8051AH | 4K x 8 ROM | 128 x 8 RAM | 2 x 16-Bit | 5 |
| 8051 | 4K x 8 ROM | 128 x 8 RAM | 2 x 16-Bit | 5 |
| 8032AH | none | 256 x 8 RAM | 3 x 16-Bit | 6 |
| 8031AH | none | 128 x 8 RAM | 2 x 16-Bit | 5 |
| 8031 | none | 128 x 8 RAM | 2 x 16-Bit | 5 |
| 8751H | 4K x 8 EPROM | 128 x 8 RAM | 2 x 16-Bit | 5 |
| 8751H-8 | 4K x 8 EPROM | 128 x 8 RAM | 2 x 16-Bit | 5 |



October 1988
Order Number: 270048-004

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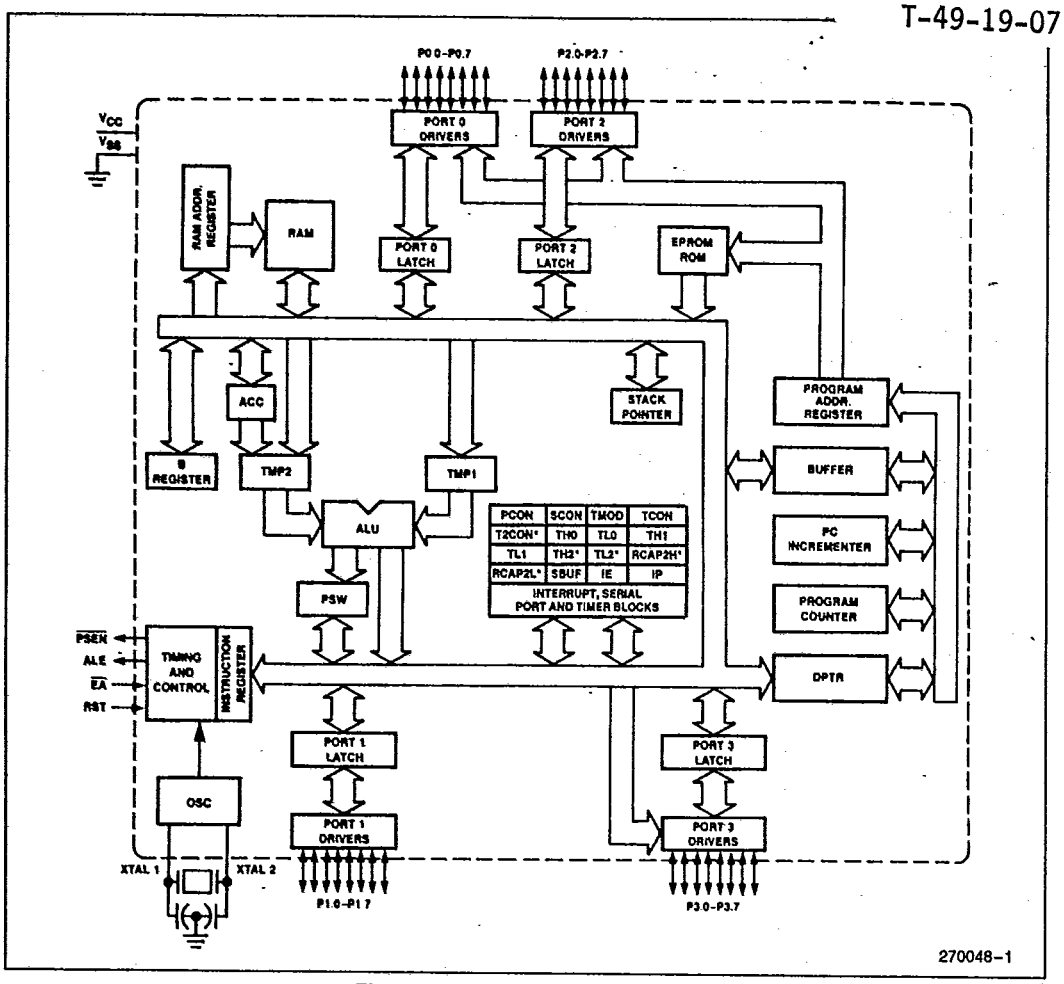



**Figure 1. MCS®-51 Block Diagram**

## PACKAGES

| Part | Prefix | Package Type |
|---|---|---|
| 8051AH/ 8031AH | P | 40-Pin Plastic DIP |
| | D | 40-Pin CERDIP |
| | N | 44-Pin PLCC |
| 8052AH/ 8032AH | P | 40-Pin Plastic DIP |
| | D | 40-Pin CERDIP |
| | N | 44-Pin PLCC |
| 8751H/ 8751H-8 | D | 40-Pin CERDIP |
| | R | 44-Pin LCC |

## PIN DESCRIPTIONS

**$V_{CC}$:** Supply voltage.

**$V_{SS}$:** Circuit ground.

**Port 0:** Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs.

Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during programming of the EPROM parts, and outputs the code bytes during program verification of the ROM and EPROM parts. External pullups are required during program verification.

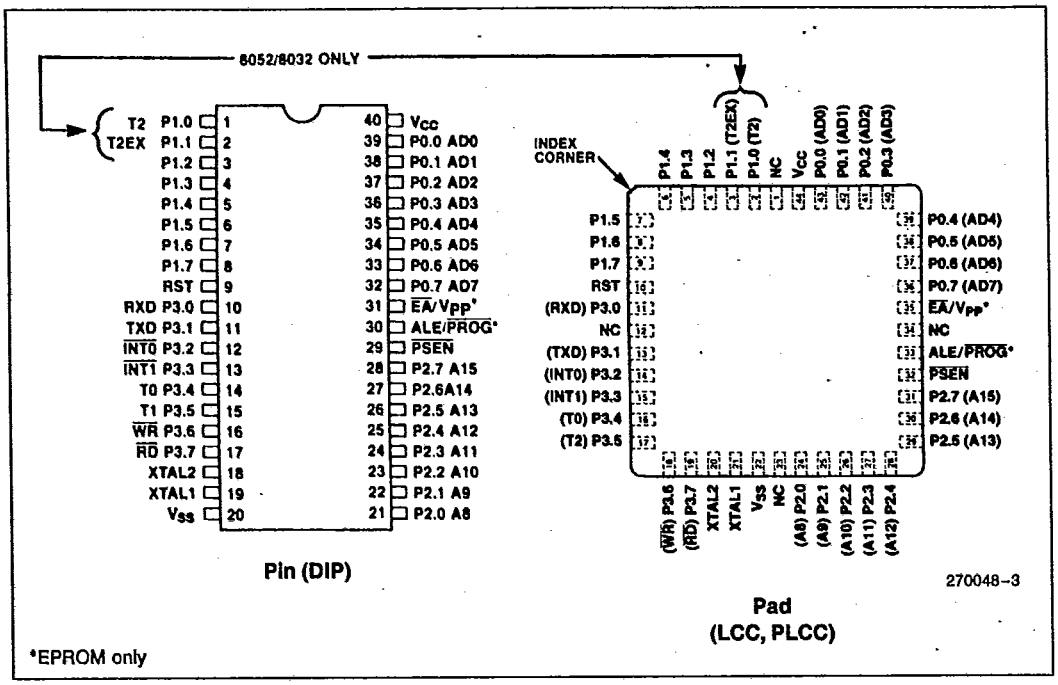



**Figure 2. MCS®-51 Connections**

**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ($I_{IL}$ on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during programming of the EPROM parts and during program verification of the ROM and EPROM parts.

In the 8032AH and 8052AH, Port 1 pins P1.0 and P1.1 also serve the T2 and T2EX functions, respectively.

**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ($I_{IL}$ on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during programming of the EPROM parts and during program verification of the ROM and EPROM parts.

**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$ on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

| Port Pin | Alternative Function |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{INT0}$ (external interrupt 0) |
| P3.3 | $\overline{INT1}$ (external interrupt 1) |
| P3.4 | T0 (Timer 0 external input) |
| P3.5 | T1 (Timer 1 external input) |
| P3.6 | $\overline{WR}$ (external data memory write strobe) |
| P3.7 | $\overline{RD}$ (external data memory read strobe) |

**RST:** Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

**ALE/$\overline{PROG}$:** Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during programming of the EPROM parts.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

**$\overline{PSEN}$:** Program Store Enable is the read strobe to external Program Memory.

When the device is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

**$\overline{EA}$/$V_{PP}$:** External Access enable $\overline{EA}$ must be strapped to $V_{SS}$ in order to enable any MCS-51 device to fetch code from external Program memory locations starting at 0000H up to FFFFH. $\overline{EA}$ must be strapped to $V_{CC}$ for internal program execution.

Note, however, that if the Security Bit in the EPROM devices is programmed, the device will not fetch code from any location in external Program Memory.

This pin also receives the 21V programming supply voltage (VPP) during programming of the EPROM parts.

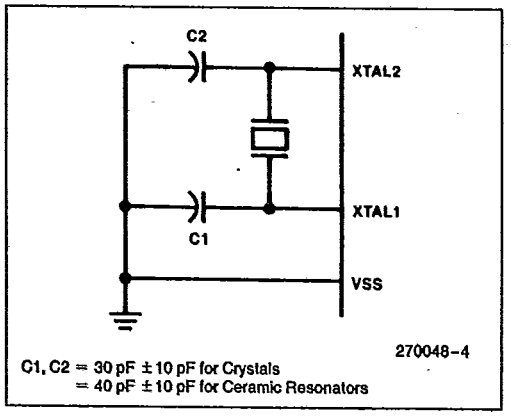



**Figure 3. Oscillator Connections**

**XTAL1:** Input to the inverting oscillator amplifier.

**XTAL2:** Output from the inverting oscillator amplifier.

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

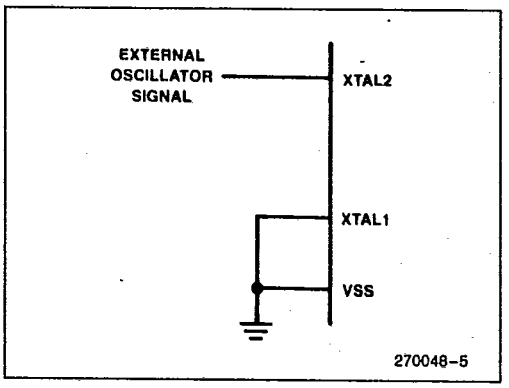



**Figure 4. External Drive Configuration**

## DESIGN CONSIDERATIONS

If an 8751BH or 8752BH may replace an 8751H in a future design, the user should carefully compare both data sheets for DC or AC Characteristic differences. Note that the $V_{IH}$ and $I_{IH}$ specifications for the $\overline{EA}$ pin differ significantly between the devices.

Exposure to light when the EPROM device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to $V_{SS}$ ...−0.5V to +21.5V
Voltage on Any Other Pin to $V_{SS}$ ....−0.5V to +7V
Power Dissipation.....1.5W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D.C. CHARACTERISTICS $T_A$ = 0°C to 70°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V

| Symbol | Parameter | | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (Except $\overline{EA}$ Pin of 8751H & 8751H-8) | | −0.5 | 0.8 | V | |
| $V_{IL1}$ | Input Low Voltage to $\overline{EA}$ Pin of 8751H & 8751H-8 | | 0 | 0.7 | V | |
| $V_{IH}$ | Input High Voltage (Except XTAL2, RST) | | 2.0 | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage to XTAL2, RST | | 2.5 | $V_{CC}$ + 0.5 | V | XTAL1 = $V_{SS}$ |
| $V_{OL}$ | Output Low Voltage (Ports 1, 2, 3)* | | | 0.45 | V | $I_{OL}$ = 1.6 mA |
| $V_{OL1}$ | Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)* | | | | | |
| | | 8751H, 8751H-8 | | 0.60<br>0.45 | V<br>V | $I_{OL}$ = 3.2 mA<br>$I_{OL}$ = 2.4 mA |
| | | All Others | | 0.45 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$) | | 2.4 | | V | $I_{OH}$ = −80 μA |
| $V_{OH1}$ | Output High Voltage (Port 0 in External Bus Mode) | | 2.4 | | V | $I_{OH}$ = −400 μA |
| $I_{IL}$ | Logical 0 Input Current (Ports 1, 2, 3, RST) 8032AH, 8052AH<br>All Others | | | −800<br>−500 | μA<br>μA | $V_{IN}$ = 0.45V<br>$V_{IN}$ = 0.45V |
| $I_{IL1}$ | Logical 0 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8 Only | | | −15 | mA | $V_{IN}$ = 0.45V |
| $I_{IL2}$ | Logical 0 Input Current (XTAL2) | | | −3.2 | mA | $V_{IN}$ = 0.45V |
| $I_{LI}$ | Input Leakage Current (Port 0)<br>8751H & 8751H-8<br>All Others | | | ±100<br>±10 | μA<br>μA | 0.45 ≤ $V_{IN}$ ≤ $V_{CC}$<br>0.45 ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $I_{IH}$ | Logical 1 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8 | | | 500 | μA | $V_{IN}$ = 2.4V |
| $I_{IH1}$ | Input Current to RST to Activate Reset | | | 500 | μA | $V_{IN}$ < ($V_{CC}$ − 1.5V) |
| $I_{CC}$ | Power Supply Current:<br>8031/8051<br>8031AH/8051AH<br>8032AH/8052AH<br>8751H/8751H-8 | | | <br>160<br>125<br>175<br>250 | <br>mA<br>mA<br>mA<br>mA | <br>All Outputs Disconnected; $\overline{EA}$ = $V_{CC}$ |
| $C_{IO}$ | Pin Capacitance | | | 10 | pF | Test freq = 1 MHz |

***NOTE:**
Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

## A.C. CHARACTERISTICS

$T_A$ = 0°C to +70°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V;
Load Capacitance for Port 0, ALE, and PSEN = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

| Symbol | Parameter | 12 MHz Oscillator | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 1/TCLCL | Oscillator Frequency | | | 3.5 | 12.0 | MHz |
| TLHLL | ALE Pulse Width | 127 | | 2TCLCL−40 | | ns |
| TAVLL | Address Valid to ALE Low | 43 | | TCLCL−40 | | ns |
| TLLAX | Address Hold after ALE Low | 48 | | TCLCL−35 | | ns |
| TLLIV | ALE Low to Valid Instr In<br>8751H<br>All Others | | <br>183<br>233 | | <br>4TCLCL−150<br>4TCLCL−100 | <br>ns<br>ns |
| TLLPL | ALE Low to $\overline{PSEN}$ Low | 58 | | TCLCL−25 | | ns |
| TPLPH | $\overline{PSEN}$ Pulse Width<br>8751H<br>All Others | <br>190<br>215 | | <br>3TCLCL−60<br>3TCLCL−35 | | <br>ns<br>ns |
| TPLIV | $\overline{PSEN}$ Low to Valid Instr In<br>8751H<br>All Others | | <br>100<br>125 | | <br>3TCLCL−150<br>3TCLCL−125 | <br>ns<br>ns |
| TPXIX | Input Instr Hold after $\overline{PSEN}$ | 0 | | 0 | | ns |
| TPXIZ | Input Instr Float after $\overline{PSEN}$ | | 63 | | TCLCL−20 | ns |
| TPXAV | $\overline{PSEN}$ to Address Valid | 75 | | TCLCL−8 | | ns |
| TAVIV | Address to Valid Instr In<br>8751H<br>All Others | | <br>267<br>302 | | <br>5TCLCL−150<br>5TCLCL−115 | <br>ns<br>ns |
| TPLAZ | $\overline{PSEN}$ Low to Address Float | | 20 | | 20 | ns |
| TRLRH | $\overline{RD}$ Pulse Width | 400 | | 6TCLCL−100 | | ns |
| TWLWH | $\overline{WR}$ Pulse Width | 400 | | 6TCLCL−100 | | ns |
| TRLDV | $\overline{RD}$ Low to Valid Data In | | 252 | | 5TCLCL−165 | ns |
| TRHDX | Data Hold after $\overline{RD}$ | 0 | | 0 | | ns |
| TRHDZ | Data Float after $\overline{RD}$ | | 97 | | 2TCLCL−70 | ns |
| TLLDV | ALE Low to Valid Data In | | 517 | | 8TCLCL−150 | ns |
| TAVDV | Address to Valid Data In | | 585 | | 9TCLCL−165 | ns |
| TLLWL | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | 3TCLCL−50 | 3TCLCL+50 | ns |
| TAVWL | Address to $\overline{RD}$ or $\overline{WR}$ Low | 203 | | 4TCLCL−130 | | ns |
| TQVWX | Data Valid to $\overline{WR}$ Transition<br>8751H<br>All Others | <br>13<br>23 | | <br>TCLCL−70<br>TCLCL−60 | | <br>ns<br>ns |
| TQVWH | Data Valid to $\overline{WR}$ High | 433 | | 7TCLCL−150 | | ns |
| TWHQX | Data Hold after $\overline{WR}$ | 33 | | TCLCL−50 | | ns |
| TRLAZ | $\overline{RD}$ Low to Address Float | | 20 | | 20 | ns |
| TWHLH | $\overline{RD}$ or $\overline{WR}$ High to ALE High<br>8751H<br>All Others | <br>33<br>43 | <br>133<br>123 | <br>TCLCL−50<br>TCLCL−40 | <br>TCLCL+50<br>TCLCL+40 | <br>ns<br>ns |

**NOTE:**
*This table does not include the 8751-8 A.C. characteristics (see next page).

**This Table is only for the 8751H-8**

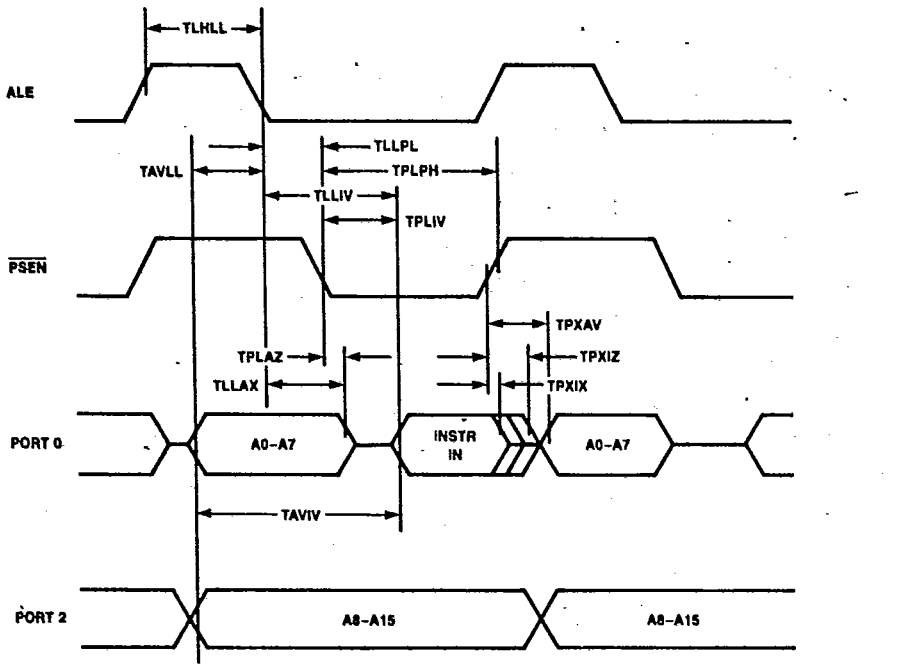
## A.C. CHARACTERISTICS

$T_A$ = 0°C to +70°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V;
Load Capacitance for Port 0, ALE, and PSEN = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

| Symbol | Parameter | 8 MHz Oscillator | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 1/TCLCL | Oscillator Frequency | | | 3.5 | 8.0 | MHz |
| TLHLL | ALE Pulse Width | 210 | | 2TCLCL−40 | | ns |
| TAVLL | Address Valid to ALE Low | 85 | | TCLCL−40 | | ns |
| TLLAX | Address Hold after ALE Low | 90 | | TCLCL−35 | | ns |
| TLLIV | ALE Low to Valid Instr In | | 350 | | 4TCLCL−150 | ns |
| TLLPL | ALE Low to $\overline{PSEN}$ Low | 100 | | TCLCL−25 | | ns |
| TPLPH | $\overline{PSEN}$ Pulse Width | 315 | | 3TCLCL−60 | | ns |
| TPLIV | $\overline{PSEN}$ Low to Valid Instr In | | 225 | | 3TCLCL−150 | ns |
| TPXIX | Input Instr Hold after $\overline{PSEN}$ | 0 | | 0 | | ns |
| TPXIZ | Input Instr Float after $\overline{PSEN}$ | | 105 | | TCLCL−20 | ns |
| TPXAV | $\overline{PSEN}$ to Address Valid | 117 | | TCLCL−8 | | ns |
| TAVIV | Address to Valid Instr In | | 475 | | 5TCLCL−150 | ns |
| TPLAZ | $\overline{PSEN}$ Low to Address Float | | 20 | | 20 | ns |
| TRLRH | $\overline{RD}$ Pulse Width | 650 | | 6TCLCL−100 | | ns |
| TWLWH | $\overline{WR}$ Pulse Width | 650 | | 6TCLCL−100 | | ns |
| TRLDV | $\overline{RD}$ Low to Valid Data In | | 460 | | 5TCLCL−165 | ns |
| TRHDX | Data Hold after $\overline{RD}$ | 0 | | 0 | | ns |
| TRHDZ | Data Float after $\overline{RD}$ | | 180 | | 2TCLCL−70 | ns |
| TLLDV | ALE Low to Valid Data In | | 850 | | 8TCLCL−150 | ns |
| TAVDV | Address to Valid Data In | | 960 | | 9TCLCL−165 | ns |
| TLLWL | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 325 | 425 | 3TCLCL−50 | 3TCLCL+50 | ns |
| TAVWL | Address to $\overline{RD}$ or $\overline{WR}$ Low | 370 | | 4TCLCL−130 | | ns |
| TQVWX | Data Valid to $\overline{WR}$ Transition | 55 | | TCLCL−70 | | ns |
| TQVWH | Data Valid to $\overline{WR}$ High | 725 | | 7TCLCL−150 | | ns |
| TWHQX | Data Hold after $\overline{WR}$ | 75 | | TCLCL−50 | | ns |
| TRLAZ | $\overline{RD}$ Low to Address Float | | 20 | | 20 | ns |
| TWHLH | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 75 | 175 | TCLCL−50 | TCLCL+50 | ns |

## EXTERNAL PROGRAM MEMORY READ CYCLE

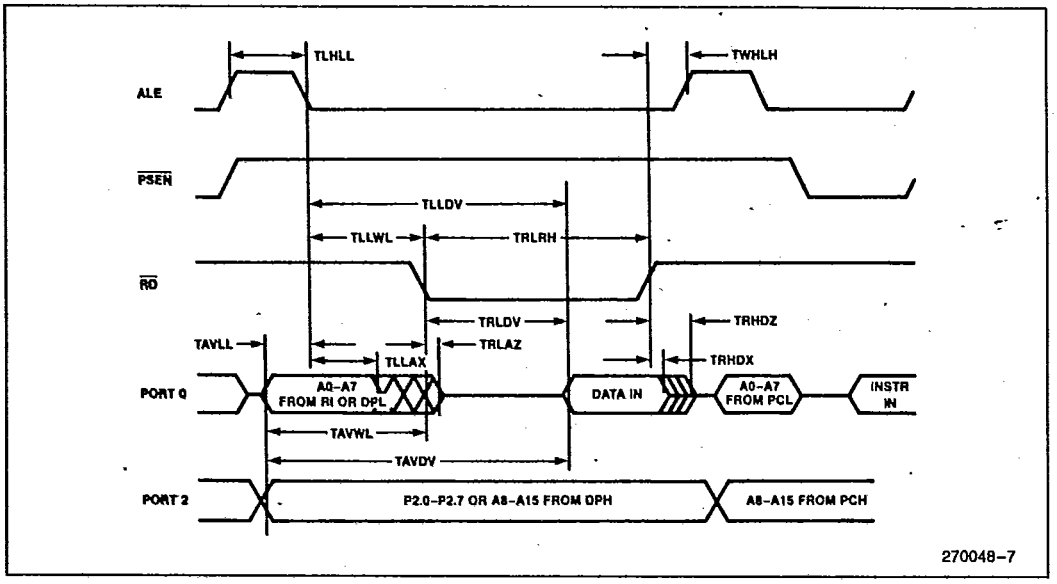
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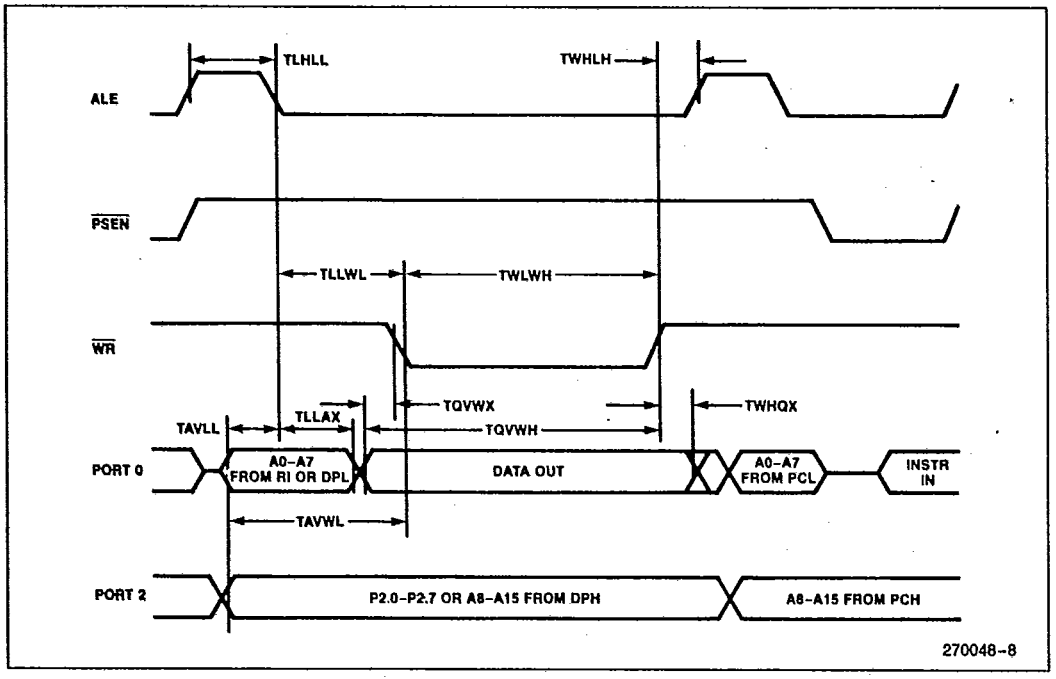

270048-6

T-49-19-07

## EXTERNAL DATA MEMORY READ CYCLE




## EXTERNAL DATA MEMORY WRITE CYCLE

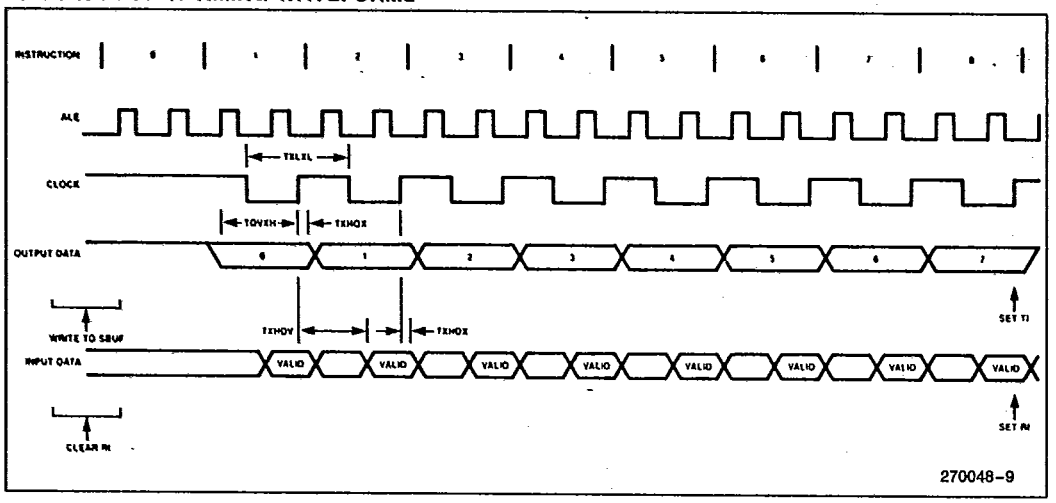


## SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: $T_A$ = 0°C to 70°C; VCC = 5V ±10%; VSS = 0V; Load Capacitance = 80 pF

| Symbol | Parameter | 12 MHz Oscillator | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| TXLXL | Serial Port Clock Cycle Time | 1.0 | | 12TCLCL | | μs |
| TQVXH | Output Data Setup to Clock Rising Edge | 700 | | 10TCLCL−133 | | ns |
| TXHQX | Output Data Hold after Clock Rising Edge | 50 | | 2TCLCL−117 | | ns |
| TXHDX | Input Data Hold after Clock Rising Edge | 0 | | 0 | | ns |
| TXHDV | Clock Rising Edge to Input Data Valid | | 700 | | 10TCLCL−133 | ns |

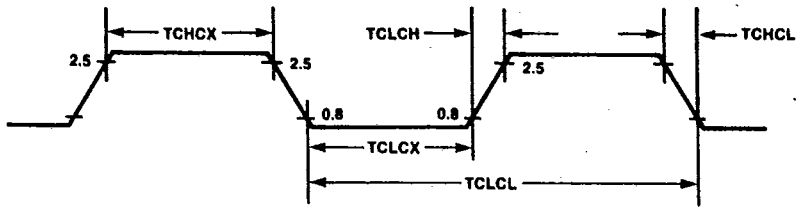
### SHIFT REGISTER TIMING WAVEFORMS



## EXTERNAL CLOCK DRIVE

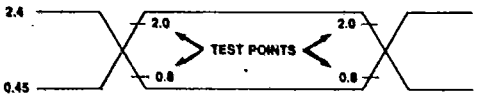
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| 1/TCLCL | Oscillator Frequency (except 8751H-8)<br>8751H-8 | 3.5<br>3.5 | 12<br>8 | MHz<br>MHz |
| TCHCX | High Time | 20 | | ns |
| TCLCX | Low Time | 20 | | ns |
| TCLCH | Rise Time | | 20 | ns |
| TCHCL | Fall Time | | 20 | ns |

## EXTERNAL CLOCK DRIVE WAVEFORM




270048-10

## A.C. TESTING INPUT, OUTPUT WAVEFORM




270048-11

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

## EPROM CHARACTERISTICS

**Table 3. EPROM Programming Modes**

| Mode | RST | PSEN | ALE | EA | P2.7 | P2.6 | P2.5 | P2.4 |
|---|---|---|---|---|---|---|---|---|
| Program | 1 | 0 | 0* | VPP | 1 | 0 | X | X |
| Inhibit | 1 | 0 | 1 | X | 1 | 0 | X | X |
| Verify | 1 | 0 | 1 | 1 | 0 | 0 | X | X |
| Security Set | 1 | 0 | 0* | VPP | 1 | 1 | X | X |

**NOTE:**
"1" = logic high for that pin
"0" = logic low for that pin
"X" = "don't care"
"VPP" = +21V ±0.5V
*ALE is pulsed low for 50 ms.

### Programming the EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0–P2.3 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 pins, and RST, PSEN, and EA should be held at the "Program" levels indicated in Table 3. ALE is **pulsed** low for 50 ms to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally EA is held at a logic high until just before ALE is to be pulsed. Then EA is raised to +21V, ALE is pulsed, and then EA is returned to a logic high. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

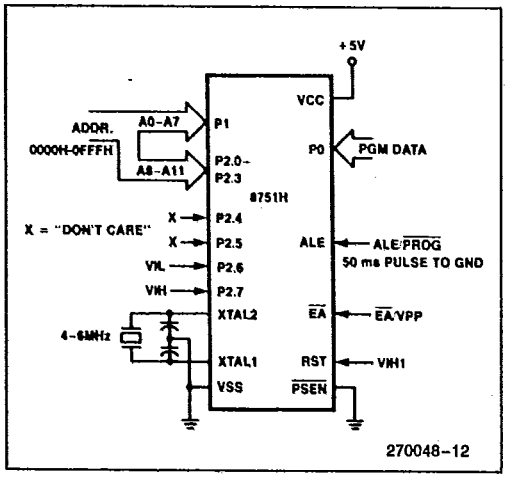



**Figure 5. Programming Configuration**

Note that the EA/VPP pin must not be allowed to go above the maximum specified VPP level of 21.5V for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The VPP source should be well regulated and free of glitches.

### Program Verification

If the Security Bit has not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0–P2.3. The other pins should be held at the "Verify" levels indicated in Table 3. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation.

The setup, which is shown in Figure 6, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active-low read strobe.

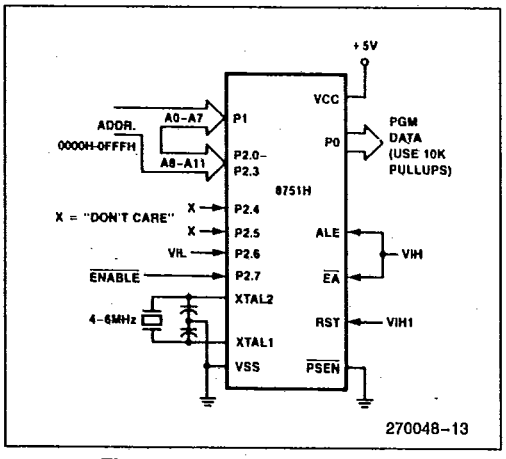



**Figure 6. Program Verification**

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## EPROM Security

The security feature consists of a "locking" bit which when programmed denies electrical access by any external means to the on-chip Program Memory. The bit is programmed as shown in Figure 7. The setup and procedure are the same as for normal EPROM programming, except that P2.6 is held at a logic high. Port 0, Port 1, and pins P2.0–P2.3 may be in any state. The other pins should be held at the "Security" levels indicated in Table 3.

Once the Security Bit has been programmed, it can be cleared only by full erasure of the Program Memory. While it is programmed, the internal Program Memory can not be read out, the device can not be further programmed, and it **can not execute out of external program memory.** Erasing the EPROM, thus clearing the Security Bit, restores the device's full functionality. It can then be reprogrammed.

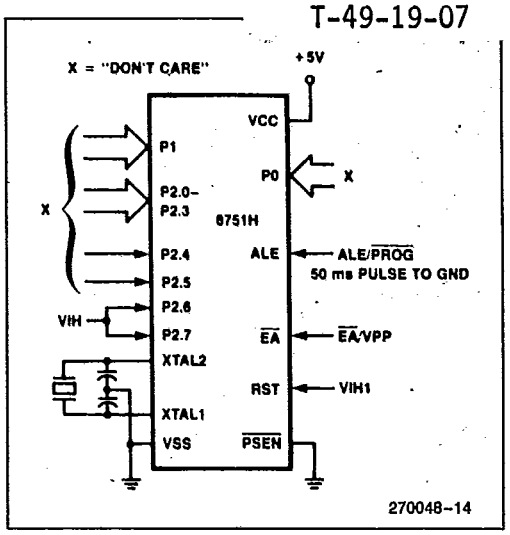



**Figure 7. Programming the Security Bit**

## Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm$^2$. Exposing the EPROM to an ultraviolet lamp of 12,000 $\mu$W/cm$^2$ rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

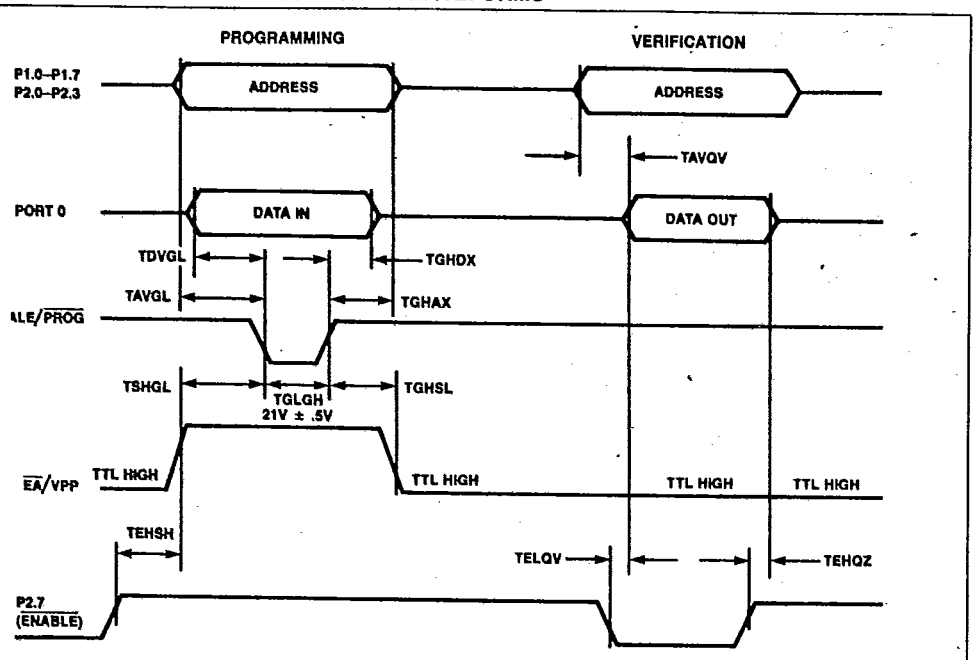
## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_A$ = 21°C to 27°C; VCC = 5V ±10%; VSS = 0V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| VPP | Programming Supply Voltage | 20.5 | 21.5 | V |
| IPP | Programming Supply Current | | 30 | mA |
| 1/TCLCL | Oscillator Frequency | 4 | 6 | MHz |
| TAVGL | Address Setup to $\overline{\text{PROG}}$ Low | 48TCLCL | | |
| TGHAX | Address Hold after $\overline{\text{PROG}}$ | 48TCLCL | | |
| TDVGL | Data Setup to $\overline{\text{PROG}}$ Low | 48TCLCL | | |
| TGHDX | Data Hold after $\overline{\text{PROG}}$ | 48TCLCL | | |
| TEHSH | P2.7 ($\overline{\text{ENABLE}}$) High to VPP | 48TCLCL | | |
| TSHGL | VPP Setup to $\overline{\text{PROG}}$ Low | 10 | | µs |
| TGHSL | VPP Hold after $\overline{\text{PROG}}$ | 10 | | µs |
| TGLGH | $\overline{\text{PROG}}$ Width | 45 | 55 | ms |
| TAVQV | Address to Data Valid | | 48TCLCL | |
| TELQV | $\overline{\text{ENABLE}}$ Low to Data Valid | | 48TCLCL | |
| TEHQZ | Data Float after $\overline{\text{ENABLE}}$ | 0 | 48TCLCL | |

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**EPROM PROGRAMMING AND VERIFICATION WAVEFORMS**




For programming conditions see Figure 5. For verification conditions see Figure 6.

## DATA SHEET REVISION SUMMARY

The following are the key differences between this and the -003 version of this data sheet:

1. Introduction was expanded to include product descriptions.
2. Package table was added.
3. Design Considerations added.
4. Test Conditions for $I_{IL1}$ and $I_{IH}$ specifications added to the DC Characteristics.
5. Data Sheet Revision Summary added.

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