*Click **here** for production status of specific part numbers.*

MAX22502E

100Mbps Full-Duplex RS-485/RS-422 Transceiver for Long Cables

General Description

The MAX22502E full-duplex, ESD-protected, RS-485/RS-422 transceiver is optimized for high-speed (up to 100Mbps) communication over long cables.This transceiver features larger receiver hysteresis for high noise rejection and improved signal integrity. Integrated preemphasis circuitry extends the distance, and increases the data rate, of reliable communication by reducing inter-symbol interference (ISI) caused by long cables when supplied with 5V. Integrated hot-swap protection and a fail-safe receiver ensure a logic-high on the receiver output when input signals are shorted or open for longer than 10µs (typ).

The MAX22502E is available in a 12-pin TDFN-EP (3mm x 3mm) package and operates over the -40°C to +125°C ambient temperature range.

Applications

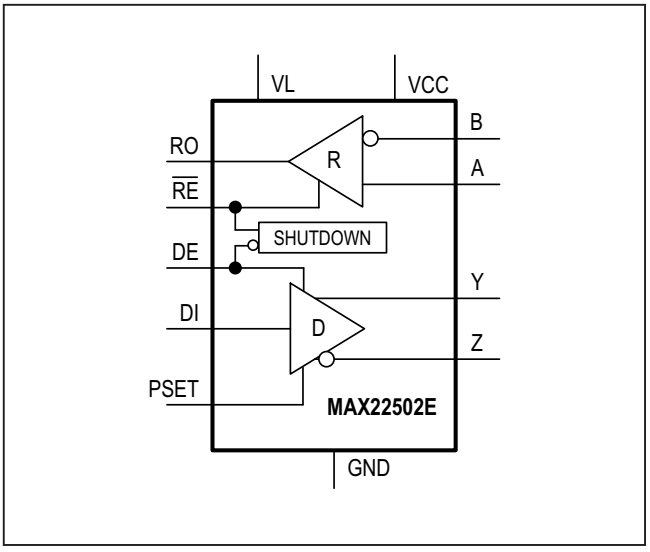
- Motion Control
- Encoder Interfaces
- Field Bus Networks
- Industrial Control Systems
- Backplane Busses

Benefits and Features

- High-Speed Operation Over Long Distances
  - Up to 100Mbps Data Rate
  - Integrated Preemphasis Extends Cable Length
  - High Receiver Sensitivity
  - Wide Receiver Bandwidth
  - Symmetrical Receiver Thresholds
- Integrated Protection Increases Robustness
  - -15V to +15V Common Mode Range
  - ±15kV ESD Protection (Human Body Model)
  - ±7kV IEC61000-4-2 Air-Gap ESD Protection
  - ±6kV IEC61000-4-2 Contact Discharge ESD Protection
  - Driver Outputs are Short-Circuit Protected
- Flexibility for Many Different Applications
  - 3V to 5.5V Supply Range
  - Low Voltage Logic Supply Down to 1.6V
  - Low 5µA (max) Shutdown Current
  - Available in 12-pin TDFN (3mm x 3mm) Package
  - -40°C to +125°C Operating Temperature Range

***Ordering Information** appears at end of data sheet.*

Simplified Block Diagram



19-100135; Rev 1; 4/19

maxim integrated™

Absolute Maximum Ratings

V_{CC} .....-0.3 V to +6 V
$\overline{RE}$, DE, DI, VL .....-0.3 V to +6 V
RO .....-0.3 V to (V_L + 0.3) V
PSET .....-0.3 V to (V_{CC} + 0.3) V
A, B, Y, Z .....-15V to +15V
Short-Circuit Duration (RO, Y, Z) to GND
Continuous Power Dissipation (Single Layer Board
(derate 15.9mW/°C above +70°C)) 1269mW
Continuous Power Dissipation (Multilayer Board (derate
24.4mW/°C above +70°C)).....1951mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Reflow Temperature .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 TDFN-EP

PACKAGE CODE	TD1233+1C
Outline Number	21-0664
Land Pattern Number	90-0397
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	63°C/W
Junction to Case (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, $V_L \le V_{CC}$, T_A = T_{MIN} to T_{MAX}, unless otherwise noted (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER							
Supply Voltage	V_{CC}	Preemphasis disabled		3.0		5.5	V
		Preemphasis enabled		4.5	5	5.5	
Supply Current	I_{CC}	DE = high, $\overline{RE}$ = low, no load			12.7	16.5	mA
Shutdown Supply Current	I_{SHDN}	DE = low, $\overline{RE}$ = high				5	µA
Logic Supply Voltage	V_L			1.6		V_{CC}	V
Logic Supply Current	I_L	No load on RO			16.4	23	µA
DRIVER							
Differential Driver Output	V_{OD}	Figure 1, Figure 2	R_L = 54Ω	1.5			V
			R_L = 100Ω	2.0			
Differential Driver Preemphasis Ratio	D_{PRE}	Preemphasis enabled, 4.5V ≤ V_{CC} ≤ 5.5V (Note 3)	R_L = 54Ω	1.33	1.37	1.41	V/V
			R_L = 100Ω	1.33	1.37	1.41	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 54Ω, Figure 1 (Note 4)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω, Normal mode and preemphasis, Figure 1			V_{CC}/2	3	V
Change In Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1 (Note 4)				0.2	V
Single-Ended Driver Output High	V_{OH}	Y or Z output	I_{OUT} = -20mA	2.2			V
Single-Ended Driver Output Low	V_{OL}	Y or Z output	I_{OUT} = +20mA			0.8	V
Differential Output Capacitance	C_{OD}	DE = $\overline{RE}$ = high, f = 4MHz			50		pF
Driver Short-Circuit Output Current	$\|I_{OST}\|$	-15V ≤ V_{OUT} ≤ +15V				250	mA
RECEIVER							
Input Current (A and B)	$I_{A,B}$	DE = GND, V_{CC} = GND, +3.6V or 5.5V	V_{IN} = +12V			+1100	µA
			V_{IN} = -7V	-1000			
Differential Input Capacitance	$C_{A,B}$	Between A and B, DE = GND, f = 2MHz			50		pF
Common Mode Voltage Range	V_{CM}			-15		+15	V
Receiver Differential Threshold High	V_{TH_H}	-15V ≤ V_{CM} ≤ +15V		+50		+200	mV
Receiver Differential Threshold Low	V_{TH_L}	-15V ≤ V_{CM} ≤ +15V		-200		-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V, time from last transition is < t_{D_FS}			250		mV
Differential Input Fail-Safe Level	V_{TH_FS}	-15V ≤ V_{CM} ≤ +15V		-50		+50	mV

Electrical Characteristics (continued)

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, $V_L \le V_{CC}$, T_A = T_{MIN} to T_{MAX}, unless otherwise noted (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INTERFACE ($\overline{RE}$, RO, DE, DI)						
Input Voltage High	V_{IH}	DE, DI, $\overline{RE}$	2/3 x V_L			V
Input Voltage Low	V_{IL}	DE, DI, $\overline{RE}$			1/3 x V_L	V
Input Current	I_{IN}	DI and DE, $\overline{RE}$ (after first transition)	-2		+2	µA
Input Impedance on First Transition	R_{IN_FT}	DE, $\overline{RE}$			10	kΩ
RO Output Voltage High	V_{OH}	$\overline{RE}$ = GND, (V_A - V_B) > 200mV, I_{OUT} = -1mA	V_L - 0.4			V
RO Output Low Voltage	V_{OL}	$\overline{RE}$ = GND, (V_A - V_B) < -200mV, I_{OUT} = +1mA			0.4	V
Three-State Output Current at Receiver	I_{OZR}	$\overline{RE}$ = high, 0 ≤ V_{RO} ≤ V_L	-1		+1	µA
PROTECTION						
Thermal Shutdown Threshold	T_{SH}			+160		°C
Thermal Shutdown Hysteresis	T_{SH_HYS}			10		°C
ESD Protection (A and B Pins)		Human Body Model		±15		kV
		IEC61000-4-2 Air Gap Discharge to GND		±7		
		IEC61000-4-2 Contact Discharge to GND		±6		
ESD Protection (All Other Pins)		Human Body Model		±2		kV

Electrical Characteristics - Switching

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, $V_L \le V_{CC}$, T_A = T_{MIN} to T_{MAX}, unless otherwise noted (Note 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER (Note 5)							
Driver Propagation Delay	t_{DPLH}	R_L = 54Ω, C_L = 50pF, Figures 3, 4				20	ns
	t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figures 3, 4				20	
Differential Driver Output Skew	t_{DSKEW}	$\lvert t_{DPLH} - t_{DPHL} \rvert$, R_L = 54Ω, C_L = 50pF, Figure 3, Figure 4 (Note 6)	V_L = V_{CC}, V_{CC} ≥ 3V			1.2	ns
		$\lvert t_{DPLH} - t_{DPHL} \rvert$, R_L = 54Ω, C_L = 50pF, Figure 3, Figure 4 (Note 6)	V_L does not equal V_{CC}			1.6	
Driver Differential Output Rise and Fall Time	t_{HL}, t_{LH}	R_L = 54Ω, C_L = 50pF, Figure 4 (Note 6)				3	ns
Data Rate	DR					100	Mbps

Electrical Characteristics - Switching (continued)

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, $V_L \le V_{CC}$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted (Note 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Enable to Output High	t_{DZH}	R_L = 500Ω, C_L = 50pF, Figure 5, Figure 6				30	ns
Driver Enable to Output Low	t_{DZL}	R_L = 500Ω, C_L = 50pF, Figure 5, Figure 6				30	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 500Ω, C_L = 50pF, Figure 5, Figure 6				30	ns
Driver Disable Time from High	t_{DHZ}	R_L = 500Ω, C_L = 50pF, Figure 5, Figure 6				30	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 5, Figure 6				100	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 5, Figure 6				100	µs
Time to Shutdown	t_{SHDN}	(Note 7, Note 8)		50		800	ns
Driver Preemphasis Interval	t_{PRE}	4.5V ≤ V_{CC} ≤ 5.5V, Figure 2	R_{PSET} = 4kΩ	10	13	16	ns
			R_{PSET} = 400kΩ	0.8	1	1.2	µs
RECEIVER (Note 5)							
Delay to Fail-Safe Operation	t_{D_FS}				10		µs
Receiver Propagation Delay	t_{RPLH}	C_L = 15pF, Figure 7, Figure 8				20	ns
	t_{RPHL}	C_L = 15pF, Figure 7, Figure 8				20	
Receiver Output Skew	t_{RSKEW}	$\lvert t_{RPHL} - t_{RPLH} \rvert$, C_L = 15pF, Figure 7, Figure 8				2.5	ns
Data Rate	DR					100	Mbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, Figure 9				30	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, Figure 9				30	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, Figure 9				30	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, Figure 9				30	ns
Receiver Enable from Shutdown to Output High	$t_{RZH\ (SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 9				100	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL\ (SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 9				100	µs
Time to Shutdown	t_{SHDN}	(Note 7, Note 8)		50		800	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications for all temperature limits are guaranteed by design.
Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.
Note 3: V_{ODP} is the differential voltage between Y and Z during the preemphasis interval and is the differential voltage when preemphasis is disabled. $V_{ODP} = D_{PRE} \times V_{OD}$.
Note 4: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.
Note 5: Capacitive load includes test probe and fixture capacitance.
Note 6: Not production tested. Guaranteed by design.
Note 7: Shutdown is enabled by driving $\overline{RE}$ high and DE low. The device is guaranteed to have entered shutdown after t_{SHDN} has elapsed.
Note 8: The timing parameter refers to the driver or receiver enable delay, when the device has exited the initial hot-swap protect state and is in normal operating mode.

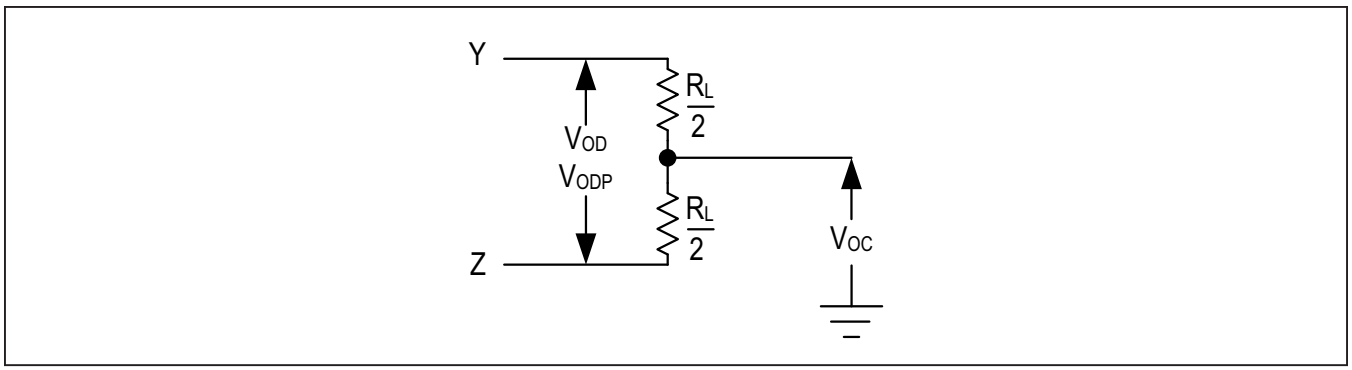


Figure 1. Driver DC Test Load

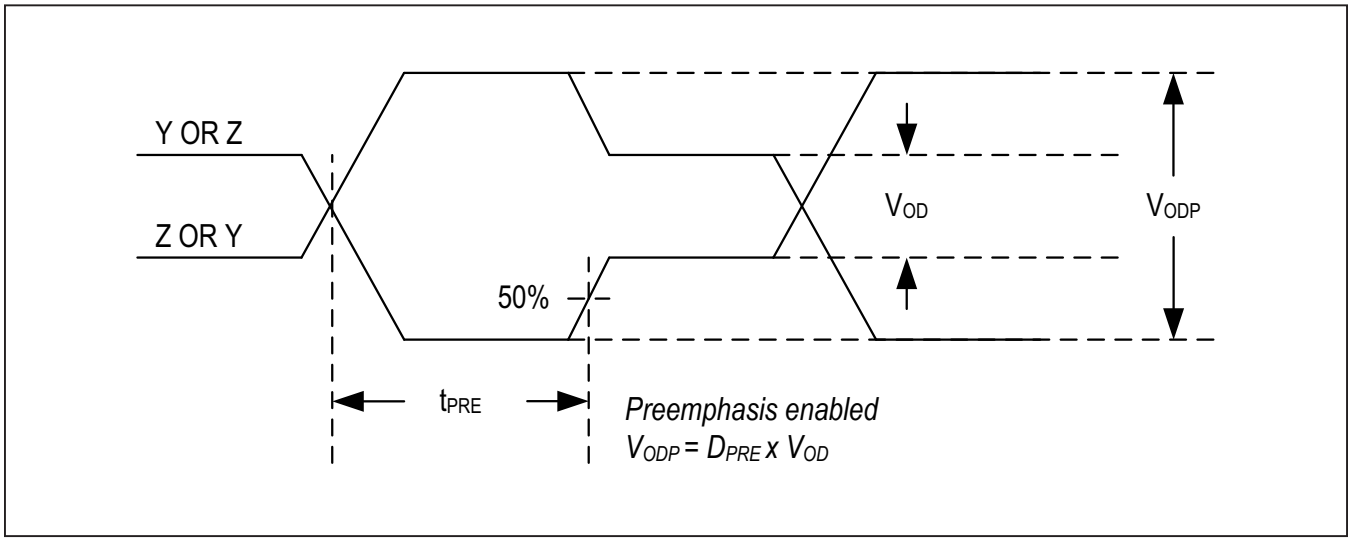


Figure 2. Driver Preemphasis Timing

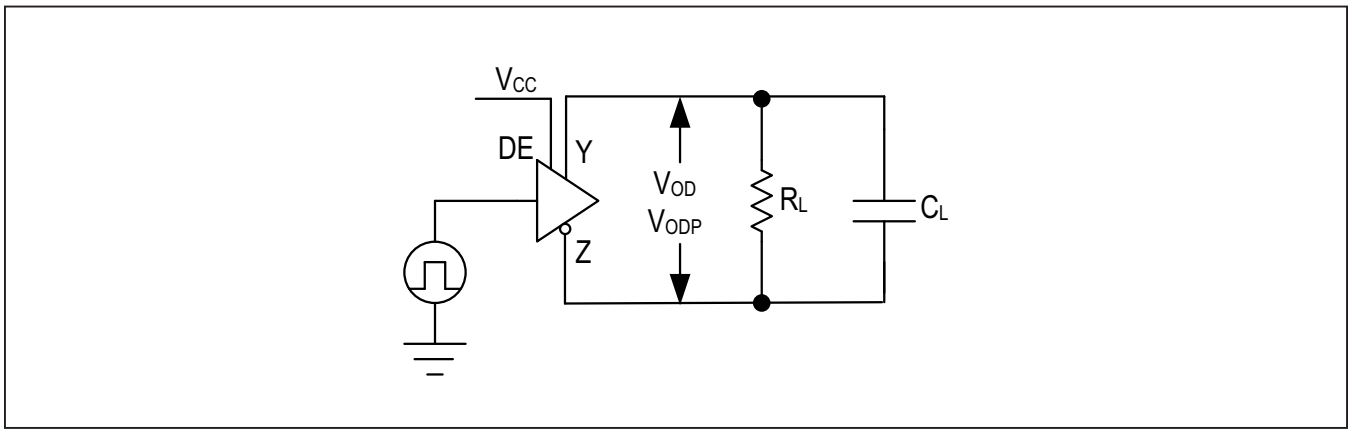


Figure 3. Driver Timing Test Circuit

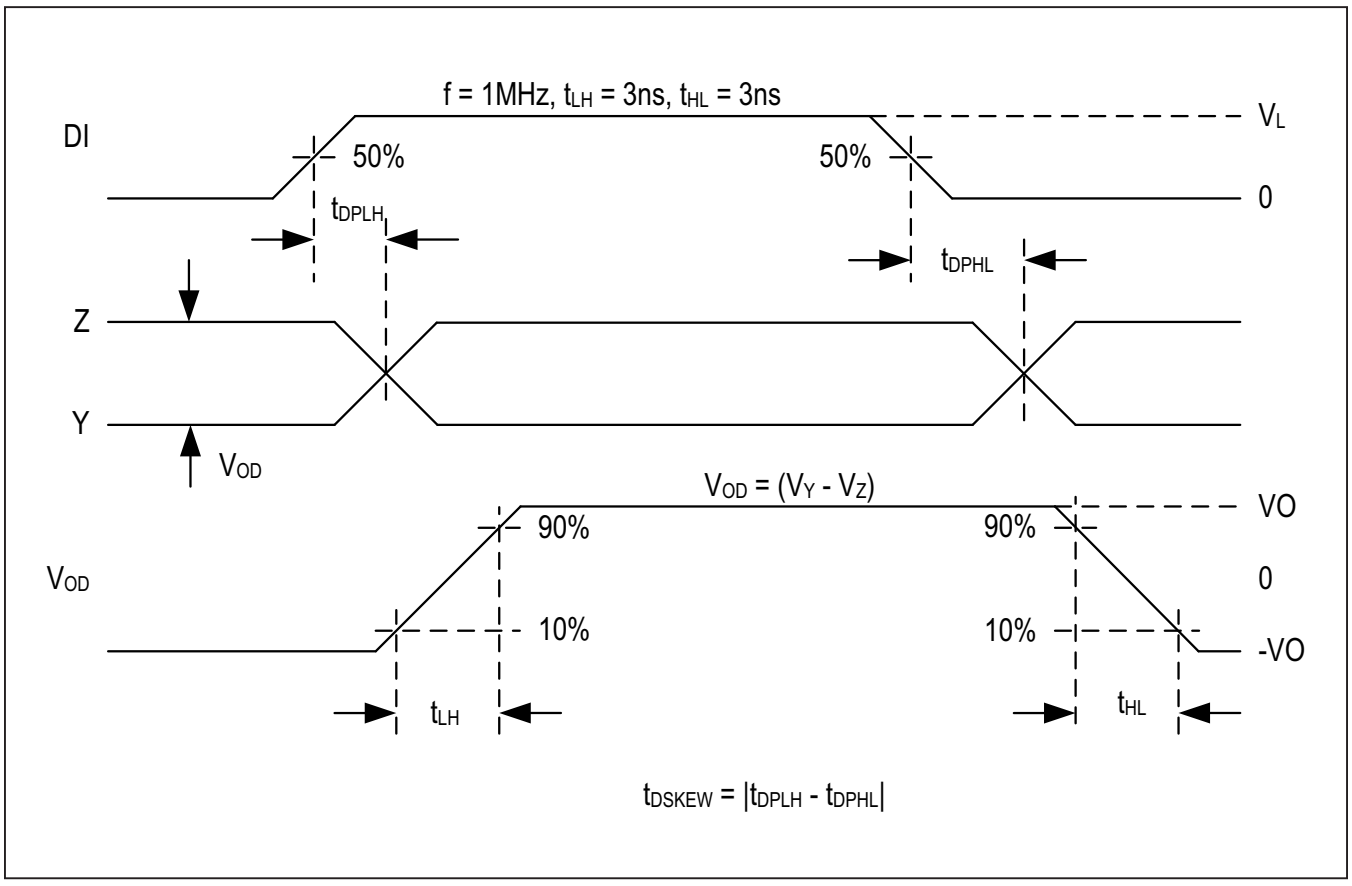


Figure 4. Driver Propagation Delays

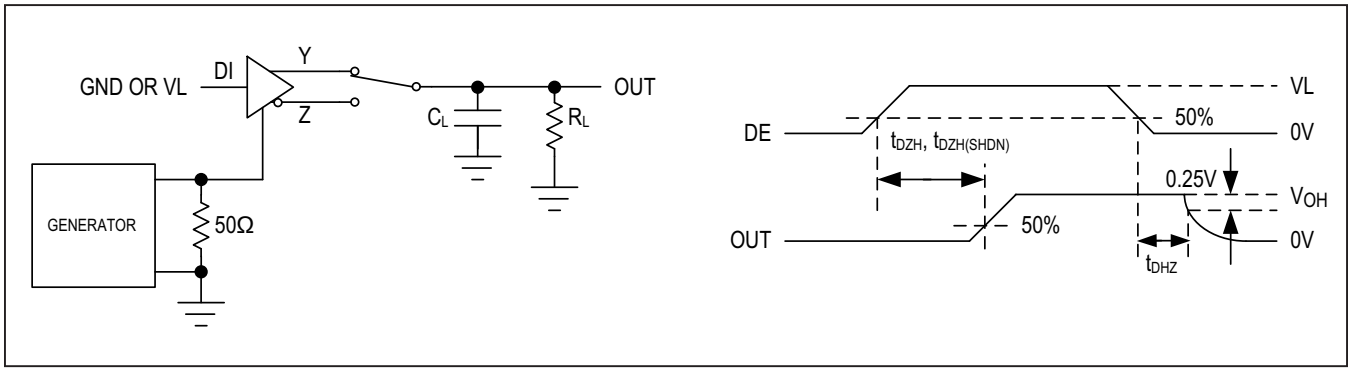


Figure 5. Driver Enable and Disable Times (t_{DZH}, t_{DHZ})

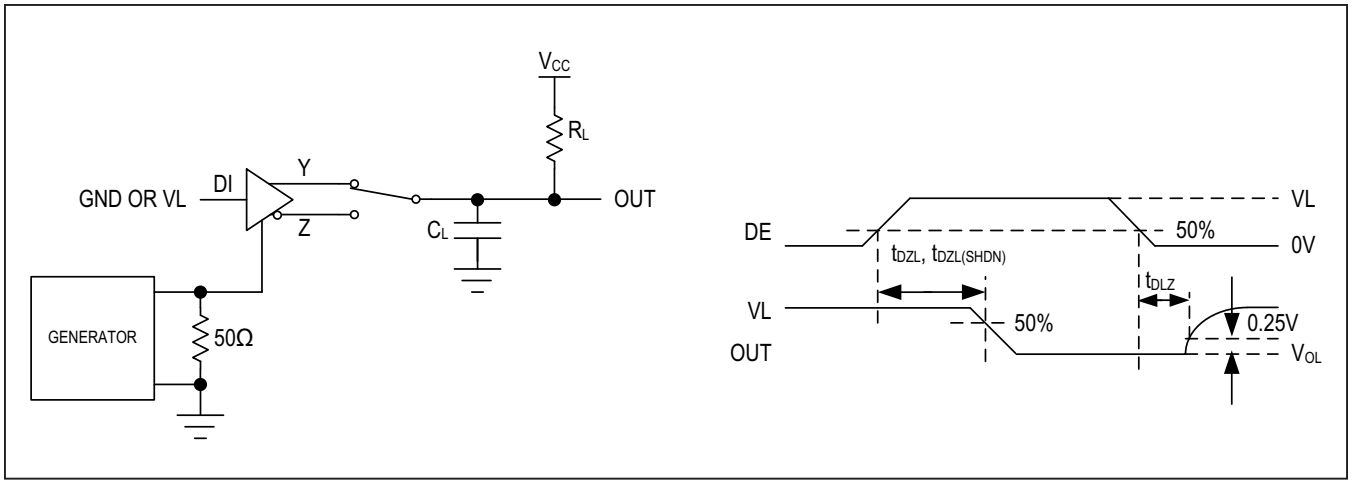


Figure 6. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

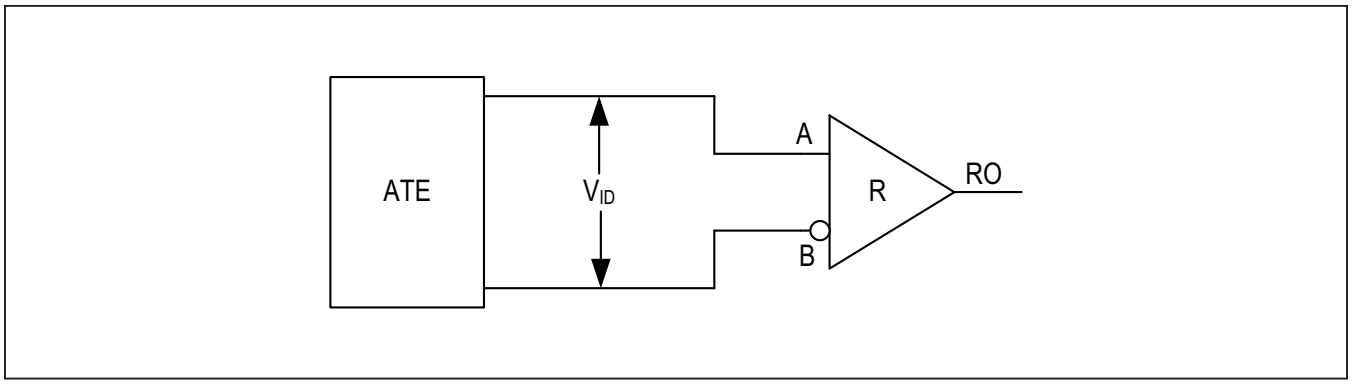


Figure 7. Receiver Propagation Delay Test Circuit

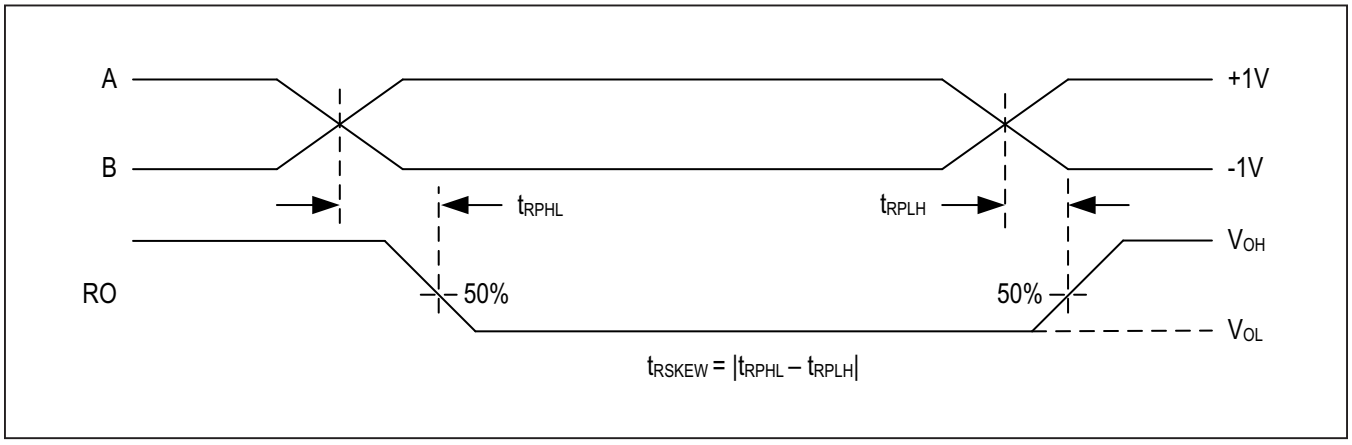


Figure 8. Receiver Propagation Delays

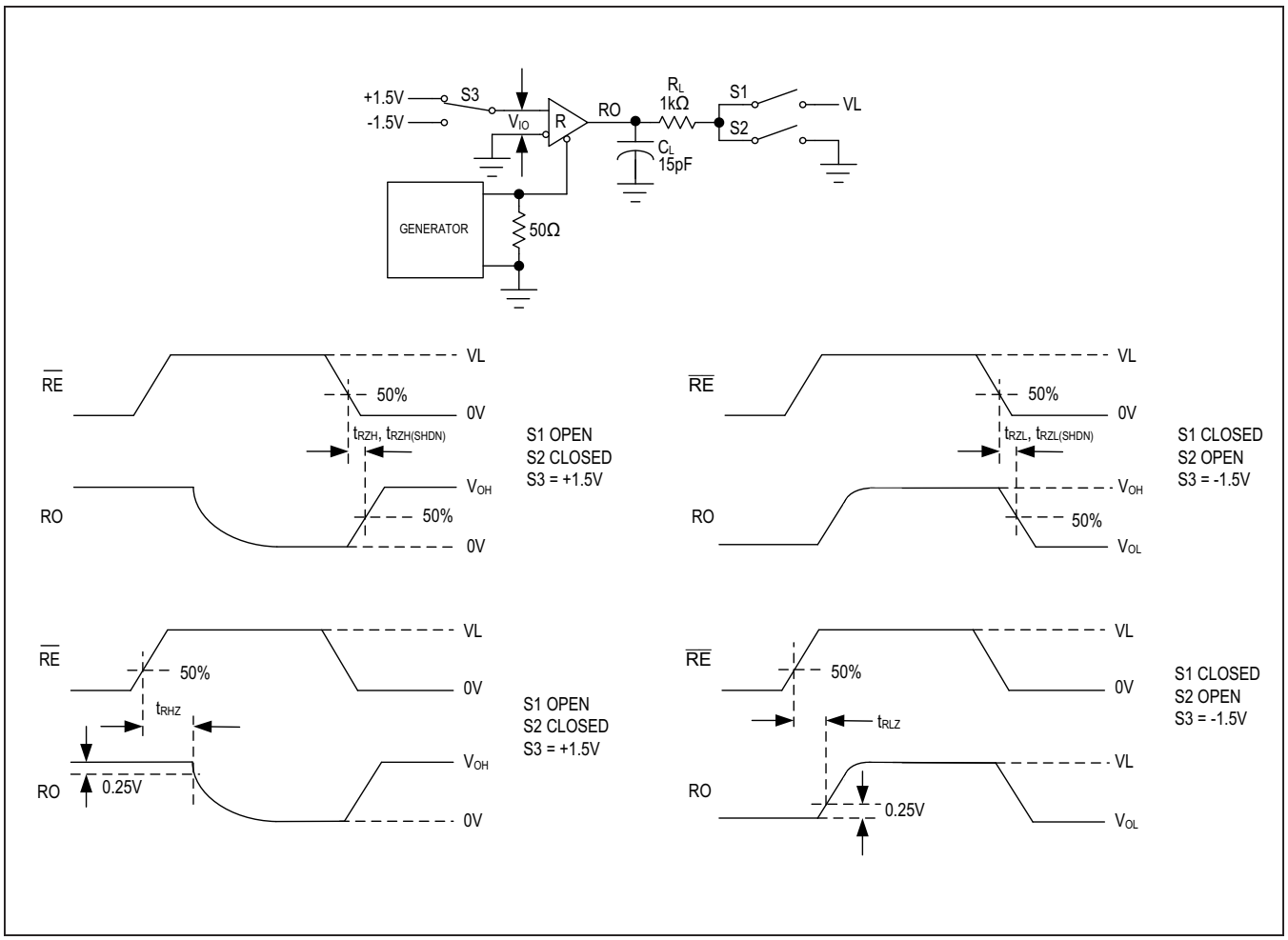
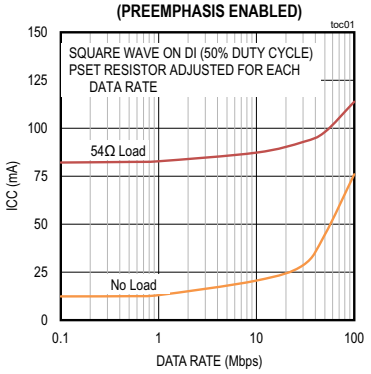


Figure 9. Receiver Enable and Disable Times

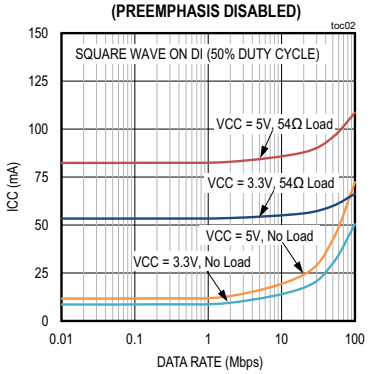
Typical Operating Characteristics

V_{CC} = 5V, VL = V_{CC}, 60Ω termination between Y and Z, T_A = 25°C, unless otherwise noted.

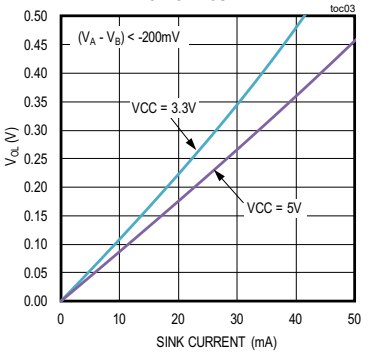
SUPPLY CURRENT vs. DATA RATE (PREEMPHASIS ENABLED)



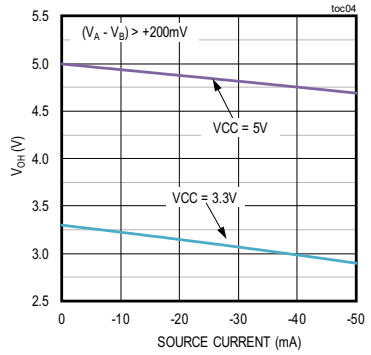
SUPPLY CURRENT vs. DATA RATE (PREEMPHASIS DISABLED)



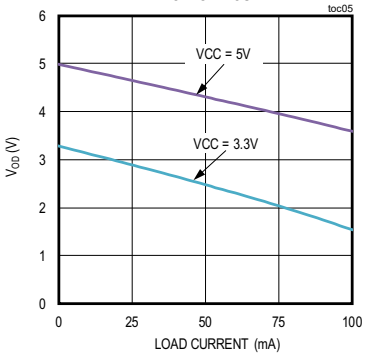
RO OUTPUT VOLTAGE LOW vs. LOAD CURRENT



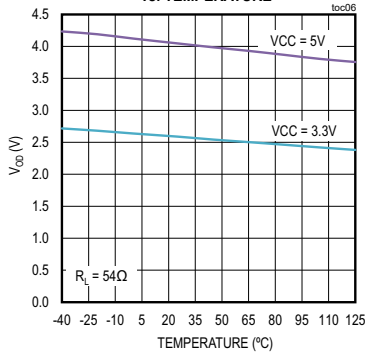
RO OUTPUT VOLTAGE HIGH vs. LOAD CURRENT



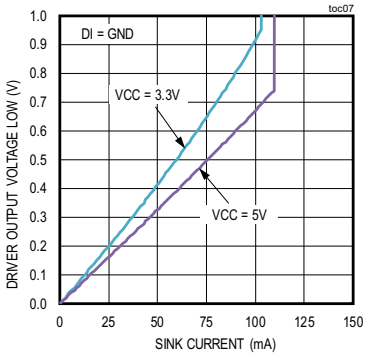
DIFFERENTIAL DRIVER OUTPUT VOLTAGE vs. LOAD CURRENT



DIFFERENTIAL DRIVER OUTPUT VOLTAGE vs. TEMPERATURE



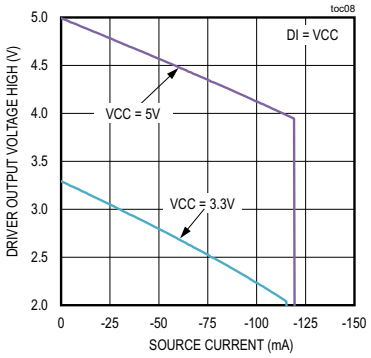
DRIVER OUTPUT VOLTAGE LOW vs. LOAD CURRENT



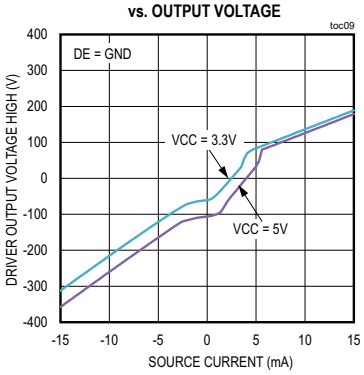
Typical Operating Characteristics (continued)

V_{CC} = 5V, VL = V_{CC}, 60Ω termination between Y and Z, T_A = 25°C, unless otherwise noted.

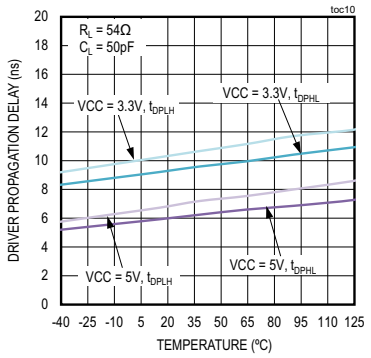
DRIVER OUTPUT VOLTAGE HIGH vs. LOAD CURRENT



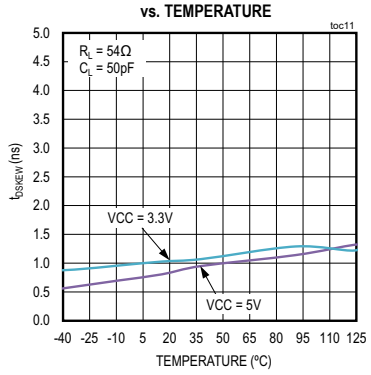
DRIVER OUTPUT LEAKAGE CURRENT vs. OUTPUT VOLTAGE



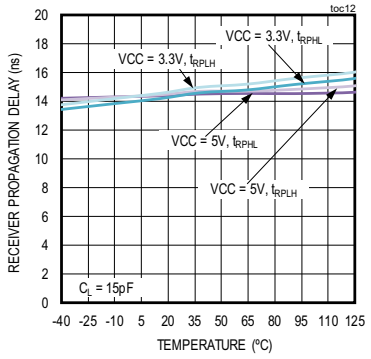
DRIVER PROPAGATION DELAY vs. TEMPERATURE



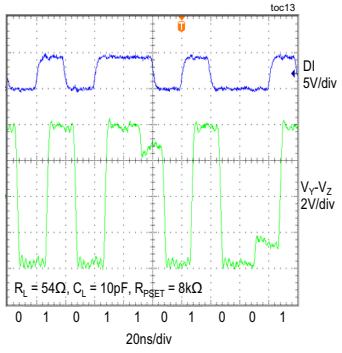
DRIVER PROPAGATION DELAY SKEW vs. TEMPERATURE



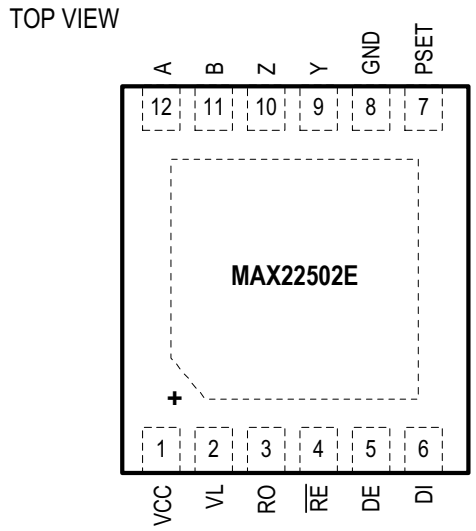
RECEIVER PROPAGATION DELAY vs. TEMPERATURE



DRIVER PREMPHASIS



Pin Configuration



TDFN-EP
3mm x 3mm

Pin Description

MAX22502E

PIN	NAME	FUNCTION
1	V_{CC}	Supply Input. Bypass V_{CC} to ground with a 0.1µF ceramic capacitor as close to the device as possible.
2	V_L	Logic Supply Input. V_L defines the interface logic levels on DE, DI, and RO. Apply a voltage between 1.6V to 5.5V to V_L. Ensure that $V_L \le V_{CC}$ for normal operation. Bypass V_L to ground with a 0.1µF capacitor as close to the device as possible.
3	RO	Receiver Output. See the *Receiving Function Table* for more information.
4	$\overline{RE}$	Receiver Enable. Set $\overline{RE}$ high to disable the receiver and tri-state RO. The device is in low-power shutdown when $\overline{RE}$ = high and DE = low.
5	DE	Driver Output Enable. Set DE high to enable driver. Set DE low to three-state the driver output.
6	DI	Driver Input. See the *Transmitting Function Table* for more information.
7	PSET	Preemphasis Select Control Input. Connect a resistor from PSET to GND to select the preemphasis duration. See the *Layout Recommendations* in the *Applications Information* section for more information. To disable preemphasis, connect PSET to GND or V_{CC}.
8	GND	Ground
9	Y	Noninverting Driver Output
10	Z	Inverting Driver Output
11	B	Inverting Receiver Input
12	A	Noninverting Receiver Input

Functional Diagrams

Transmitting Function Table

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Y	Z
X	1	1	1	0
X	1	0	0	1
0	0	X	High Impedance	High Impedance
1	0	X	Shutdown. Y and Z are high-impedance	

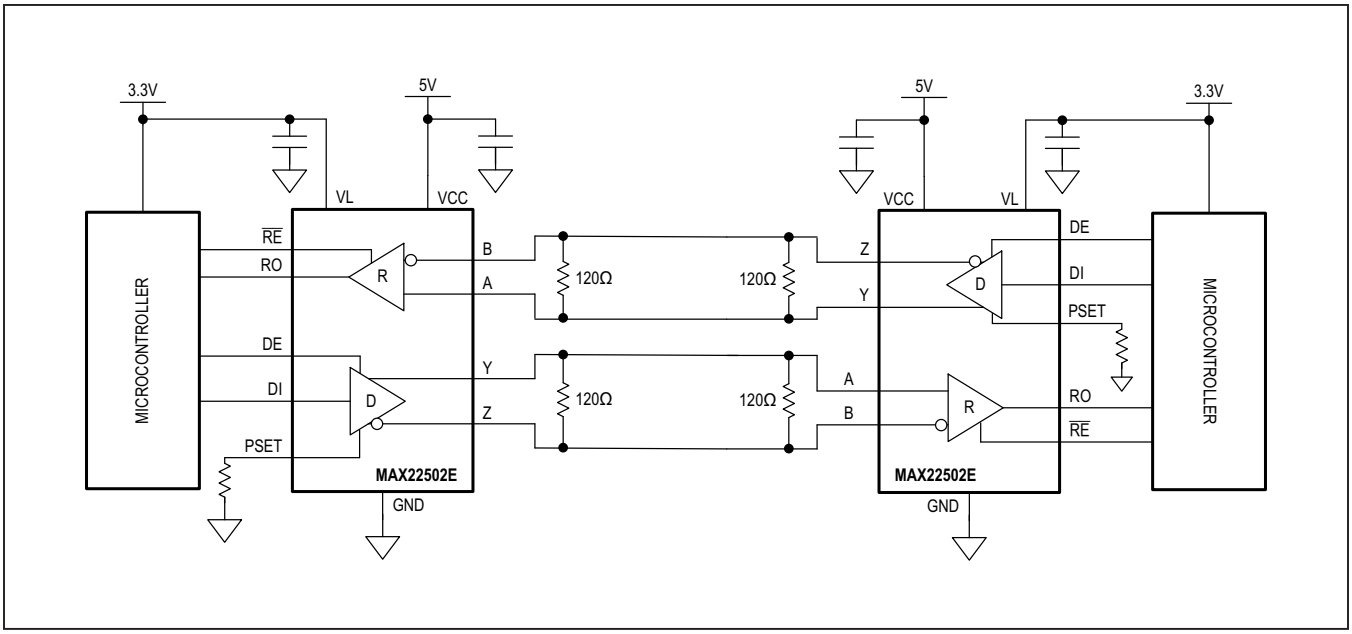
X = Don't care

Receiving Function Table

INPUTS				OUTPUTS
$\overline{RE}$	DE	$(V_A - V_B)$	Time from Last A-B Transition	RO
0	X	$\geq V_{TH\_H}$	Always	1
0	X	$V_{TH\_L} < (V_A - V_B) < V_{TH\_H}$	$< t_{D\_FS}$	Indeterminate RO is latched to previous value
0	X	$-50mV < (V_A - V_B) < +50mV$	$> t_{D\_FS}$	1
0	X	$\leq V_{TH\_L}$	Always	0
0	X	Open/Shorted	$> t_{D\_FS}$	1
1	1	X	X	High Impedance
1	0	X	X	Shutdown. RO is high-impedance

X = Don't care

Full-Duplex Point-to-Point Application Circuit



Detailed Description

The MAX22502E ESD-protected RS-485/RS-422 transceiver is optimized for high-speed, full-duplex communications over long cables. This transceiver features integrated hot-swap functionality to eliminate false transitions on the driver during power-up or during a hot-plug event. Fail-safe receiver inputs guarantee a logic-high on the receiver output when inputs are shorted or open for longer than 10µs (typ).

Receiver Threshold Voltages

The MAX22502E receiver features a large threshold hysteresis of 250mV (typ) for increased differential noise rejection.

Additionally, the receiver features symmetrical threshold voltages. Symmetric thresholds have the advantage that recovered data at the RO output does not have duty cycle distortion. Typically, fail-safe receivers, which have unipolar (non-symmetric) thresholds, show some duty cycle distortion at high signal attenuation due to long cable lengths.

Preemphasis

When powered by 5V, the MAX22502E features integrated driver preemphasis circuitry, which strongly improves signal integrity at high data rates over long distances by reducing intersymbol interference (ISI) caused by long cables. Preemphasis is set by connecting a resistor (R_{PSET}) between PSET and ground.

Long cables attenuate the high-frequency content of transmitted signals due to the cable's limited bandwidth. This causes signal/pulse distortion at the receiving end, resulting in ISI. ISI causes jitter in data and clock recovery circuits. ISI can be visualized by considering the following cases: If a series of ones (1s) is transmitted, followed by a zero (0), the transmission-line voltage has risen to a high value by the end of the string of ones. It takes longer for the signal to move toward the '0' state because the starting voltage on the line is so far from the zero crossing. Similarly, if a data pattern has a string of zeros followed by a one and then another zero, the one-to-zero transition starts from a voltage that is much closer to the zero crossing (V_Y - V_Z = 0) and it takes much less time for the signal to reach the zero crossing.

Preemphasis reduces ISI by boosting the differential signal amplitude at every transition edge, counteracting the high frequency attenuation of the cable. When the DI input changes from a logic low to a logic high, the differential output (V_Y - V_Z) is driven high to V_{ODP}. At the end of the preemphasis interval, the differential voltage returns to a lower level (V_{OD}). The preemphasis differential high voltage (V_{ODP}) is typically 1.37 times the V_{OD} voltage.

If DI switches back to a logic-low state before the preemphasis interval ends, the differential output switches directly from the 'strong' V_{ODP} high to a 'strong' low ($-V_{ODP}$).

Driver behavior is similar when the DI input changes from a logic-high to a logic-low. When this occurs, the differential output is pulled low to $-V_{ODP}$ until the end of the preemphasis interval, at which point V_Y - V_Z = $-V_{ODP}$.

Preemphasis Setting

Connect a resistor (R_{PSET}) between PSET and GND to set the preemphasis time interval on the MAX22502E. An optimum preemphasis interval ranges from 1 to 1.5 unit intervals (bit time). Use the following equation to calculate the resistance needed on PSET to achieve a 1.2 preemphasis interval:

$$R_{PSET} = 400x10^9/DR$$

where DR is the data rate and 1Mbps ≤ DR ≤ 100Mbps.

Preemphasis only minimally degrades the jitter on the eye diagram when using short cables, making it reasonable to permanently enable preemphasis on systems where cable lengths may vary or change. Figure 10 and Figure 11 are eye diagrams taken at 100Mbps over a 10m cat5e cable. Note that the eye varies only slightly as preemphasis is enabled or disabled.

Figure 12 and Figure 13 show the driver eye diagrams over a long cable length. The MAX22502E was used as the driver and the eye diagrams were taken at the receiver input after a length of 100m cat5e cable. Figure 12 shows the signal at the receiver when the driver preemphasis is disabled. Figure 13 shows the receiver signal when preemphasis is enabled.

Fail-Safe Functionality

The MAX22502E features fail-safe receiver inputs, guaranteeing a logic-high on the receiver output (RO) when the receiver inputs are shorted or open for longer than 10µs (typ). When the differential receiver input voltage is less than 50mV for more than 10µs (typ), RO is logic-high. For example, in the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination resistor, so (V_A - V_B = 0V) > -50mV and RO is guaranteed to be a logic-high after 10µs (typ).

Driver Single-Ended Operation

The Y and Z outputs on the MAX22502E can be used in the standard differential operating mode or as single-ended outputs. Because the driver outputs swing rail-to-rail, they can also be used as individual standard TTL logic outputs.

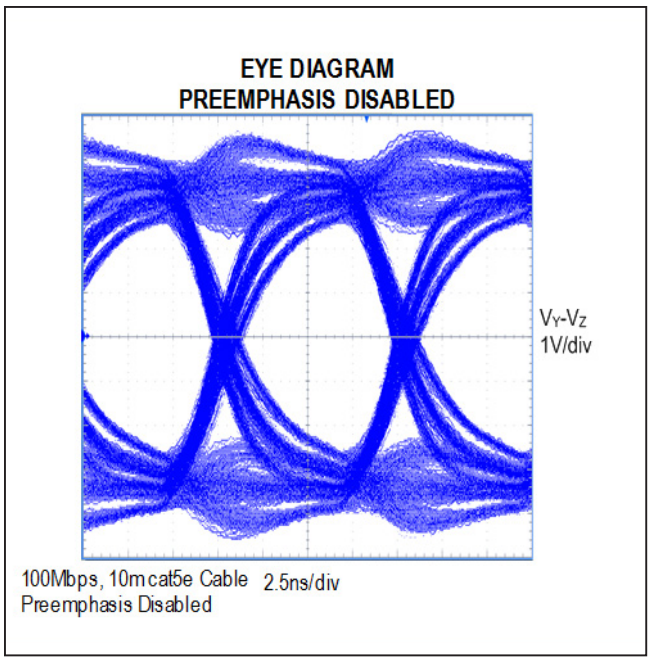


Figure 10. Eye Diagram, 100Mbps Over 10m Cat5e Cable, Preemphasis Disabled, V_{CC} = V_L = 5V

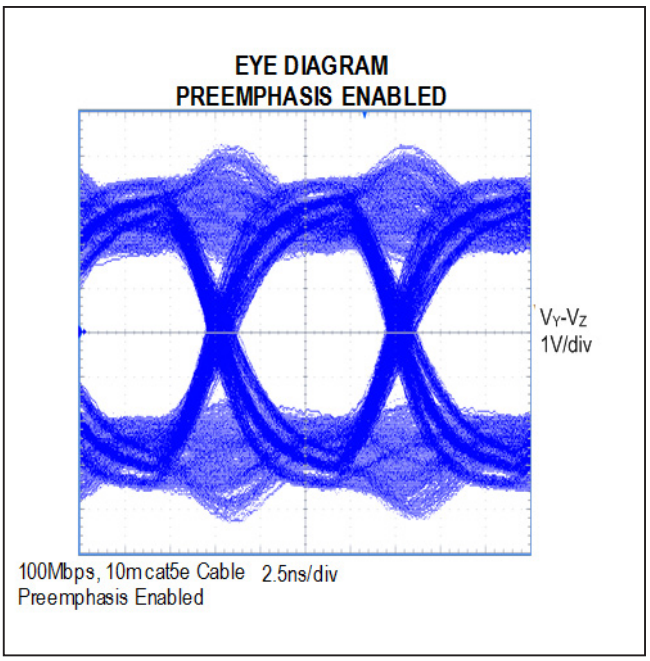


Figure 11. Eye Diagram, 100Mbps Over 10m Cat5e Cable, Preemphasis Enabled, V_{CC} = V_L = 5V

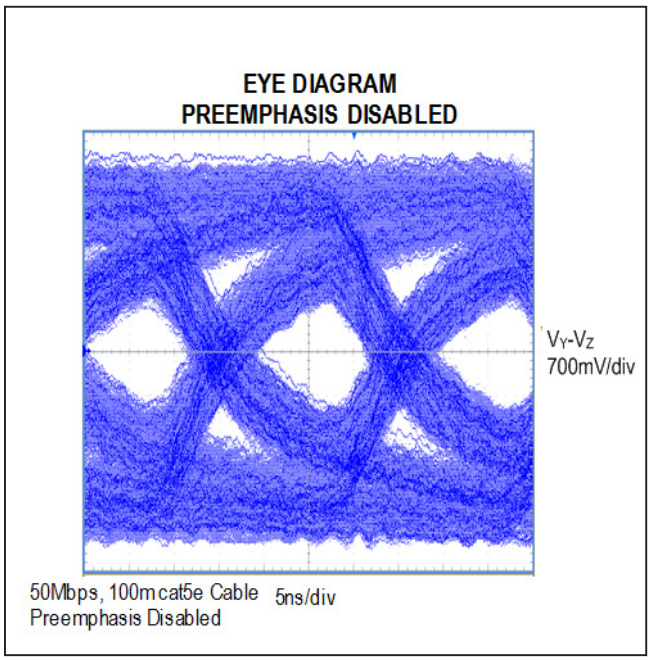


Figure 12. Eye Diagram, 50Mbps Over 100m Cat5e Cable, Preemphasis Disabled, V_{CC} = V_L = 5V

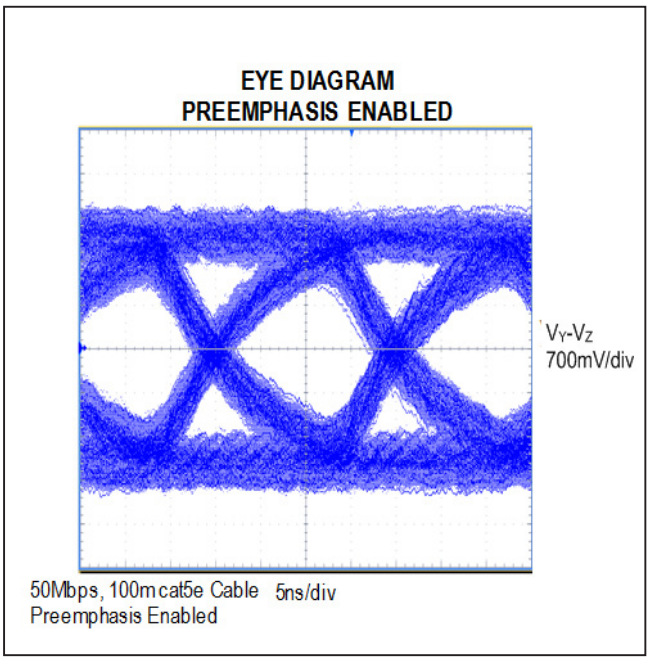


Figure 13. Eye Diagram, 50Mbps Over 100m Cat5e Cable, Preemphasis Enabled, V_{CC} = V_L = 5V

Hot-Swap Capability

The DE and $\overline{RE}$ enable inputs feature hot-swap functionality. At each input there are two NMOS devices, M1 and M2 (Figure 14). When V_{CC} ramps from zero, an internal 10ms timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 500µA current sink, and M1, a 100µA current sink, pull DE to GND through a 5kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

There is a complimentary circuit for $\overline{RE}$ that uses two PMOS devices to pull $\overline{RE}$ to V_{CC}.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Low-Power Shutdown Mode

The MAX22502E features low-power shutdown mode to reduce supply current when the transceiver is not needed. Pull the $\overline{RE}$ input high and the DE input low to put the device in low-power shutdown mode. If the inputs are in this state for at least 800ns, the part is guaranteed to enter shutdown. The MAX22502E draws 5µA (max) of supply current when the device is in shutdown.

The $\overline{RE}$ and DE inputs can be driven simultaneously. The MAX22502E is guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns.

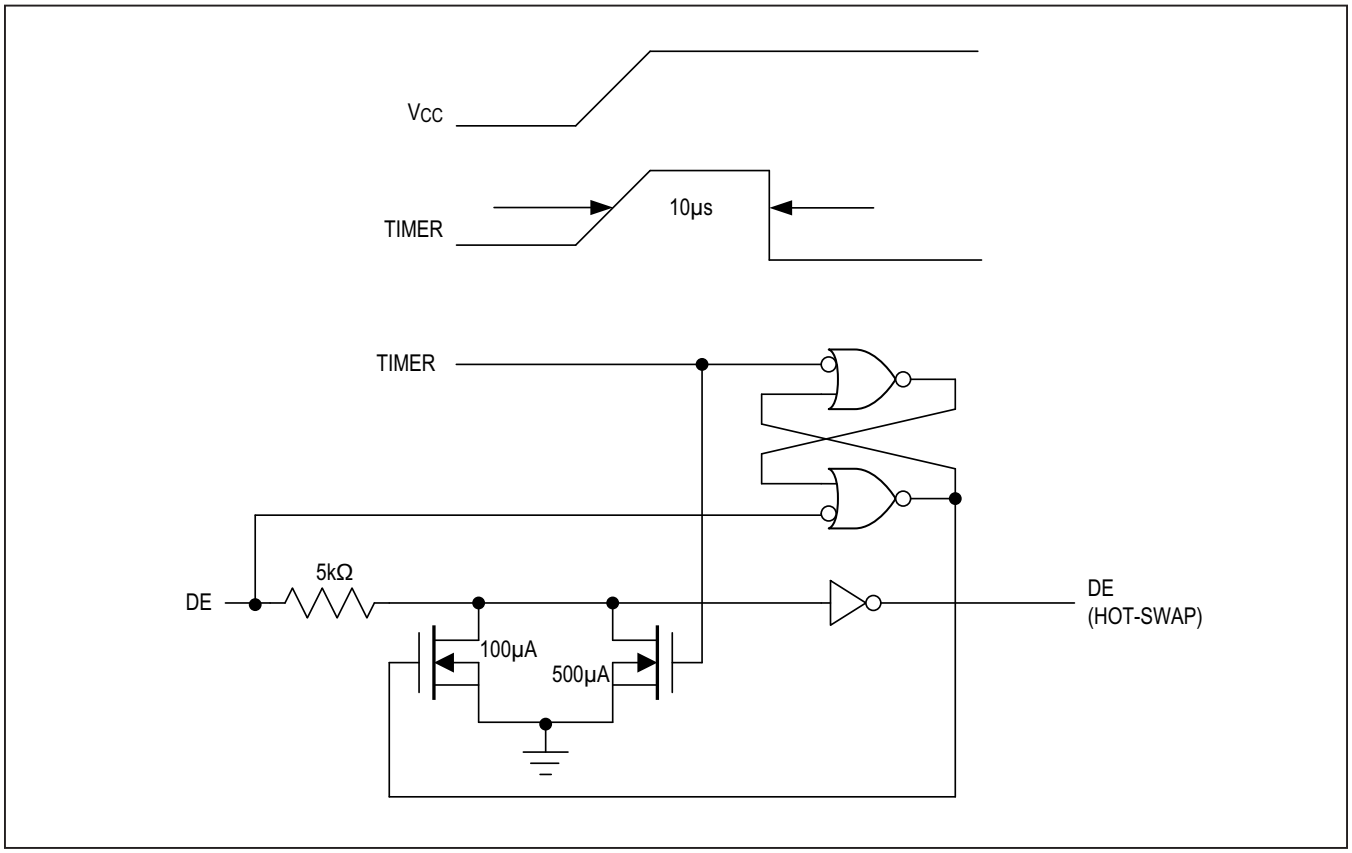


Figure 14. Simplified Structure of the Driver Enable (DE) Pin

Applications Information

Powering the MAX22502E

No particular power supply sequencing is required for the MAX22502 V_{CC} and V_L supplies during power-up. However, ensure that $V_L \leq V_{CC}$ for normal operation.

Layout Recommendations

Ensure that the preemphasis set resistor (R_{PSET}) is located close to the PSET and GND pins in order to minimize interference by other signals. Minimize the trace length to the PSET resistor. Additionally, place a ground plane under R_{PSET} and surround it with ground connections/ traces to minimize interference from the A and B switching signals. See Figure 15.

Network Topology

The MAX22502E transceiver is designed for high-speed bidirectional RS-485/RS-422 data communications. Multidrop networks can cause impedance discontinuities which affect signal integrity. Maxim recommends using a point-to-point network topology, instead of a multidrop topology, when communicating with high data rates. Terminate the transmission line at both ends with the cable's characteristic impedance to reduce reflections.

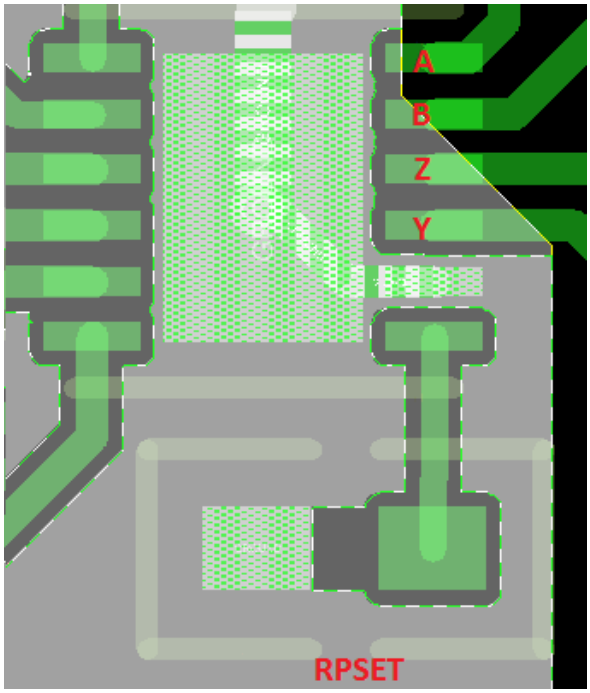


Figure 15. Sample PSET Resistor Placement

Ordering Information

PART	PREEMPHASIS	LOGIC SUPPLY	PIN-PACKAGE	PACKAGE CODE
MAX22502EATC+	Y	Y	TDFN12-EP*	TD1233+1C
MAX22502EATC+T	Y	Y	TDFN12-EP*	TD1233+1C

+Denotes a lead (Pb)-free/RoHS-compliant package.
**EP = Exposed Pad*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/17	Initial release	—
1	4/19	Corrected part references in the text	14, 17
.1		Corrected typo in Figure 8	8

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